SCAN928028 8 Channel 10:1 Serializer with IEEE 1149.1 and At-Speed BIST

Check for Samples: SCAN928028

FEATURES

- **IEEE 1149.1 (JTAG) Compliant and At-Speed BIST Test Mode.**
- **All 8 Channels Synchronous to One Parallel Clock Rate, from 18 to 66 MHz**
- **Duplicates Function of Multiple DS92LV1021 and '1023 10-Bit Serializer Devices**
- **Serializes from One to Eight 10-Bit Parallel Inputs into Data Streams with Embedded Clock**
- **Eight 5 mA Modified Bus LVDS Outputs that are Capable to Drive Double Terminations**
- **@Speed Test - PRBS Generation to Check LVDS Transmission Path to SCAN921224, SCAN921226, SCAN921260, or SCAN926260**
- **On Chip Filtering for PLL**
- **740mW Typ Power Dissipation (Loaded, PRBS, 66MHz, 3.3V)**
- **High Impedance Inputs and Outputs on Power off**
- **Single Power Supply at +3.3V (+/-10%)**
- **196-pin NFBGA Package**
- **Industrial Temperature Range Operation: -40 to +85°C**

DESCRIPTION

The SCAN928028 integrates eight serializer devices into a single chip. The SCAN928028 can simultaneously serialize up to eight 10-bit data streams. The 10-bit parallel inputs are LVTTL signal levels. The serialized outputs are LVDS signals with extra drive current for point-to-point and lightly loaded multidrop applications. Each serializer block in the SCAN928028 operates independently by using strobes from a single shared PLL.

The SCAN928028 uses a single +3.3V power supply with a typical power dissipation of 740mW (3.3V / PRBS / 66 MHz). Each serializer channel has a unique power down control to further conserve power consumption.

For high-speed LVDS serial data transmission, line quality is essential, thus the SCAN928028 includes an @SPEED TEST function. Each Serializer channel has the ability to internally generate a PRBS data pattern. This pattern is received by specific deserializers (SCAN921224) which have the complement PRBS verification circuit. The deserializer checks the data pattern for bit errors and reports any errors on the test verification pins on the deserializer.

For additional information - please see the Application Information section in this datasheet.

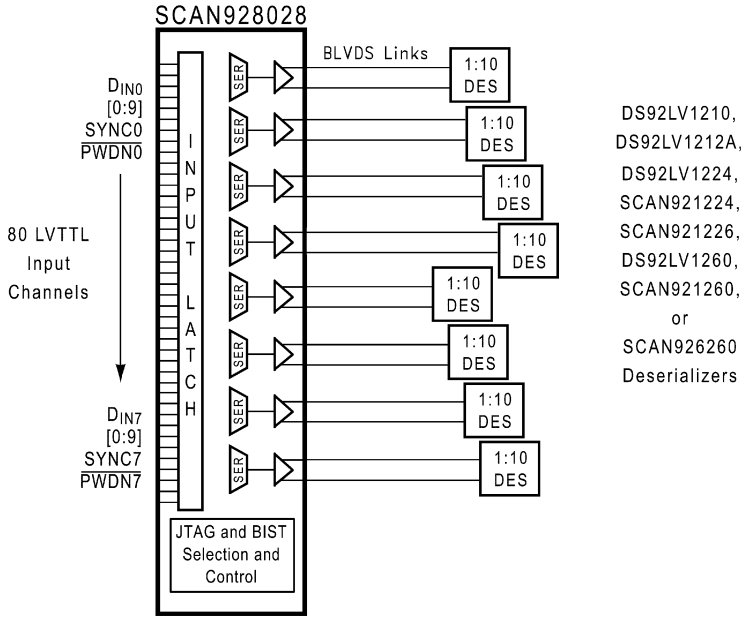
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Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (V_{CC})		−0.3V to +4V
LVCMOS/LVTTL Input Voltage		−0.3V to (V_{CC} +0.3V)
Bus LVDS Driver Output Voltage		−0.3V to +3.9V
Bus LVDS Output Short Circuit Duration		10ms
Package Thermal Resistance	θ_{JA} 196 NFBGA:	34°C/W
	θ_{JC} 196 NFBGA:	8°C/W
Storage Temperature		−65°C to +150°C
Junction Temperature		+125°C
Lead Temperature	(Soldering, 4 seconds)	+225°C
ESD Rating (HBM)		±1.5kV
Reliability Information	Transistor Count:	44.8k

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C
Clock Rate	18		66	MHz

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Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
LVCMOS/LVTTL DC Specifications							
V_{IH}	High Level Input Voltage		DINn[0-9], TCLK, PWDNn, SYNCn, DEN, BIST_ACT, TCK, TDI, TMS, TRST, BIST_SEL<0:3>	2.0		V_{CC}	V
			MS_PWDN	2.2		V_{CC}	V
V_{IL}	Low Level Input Voltage		DINn[0-9], TCLK, PWDNn, MS_PWDN, SYNCn, DEN, BIST_ACT, TCK, TDI, TMS, TRST, BIST_SEL<0:3>	GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.87	−1.5	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V	DINn[0-9], TCLK, PWDNn, MS_PWDN, SYNCn, TCK, DEN, BIST_ACT	−10	+/− 1	+10	µA
			TDI, TMS, TRST, BIST_SEL<0:3> (3)	−20		+10	µA
V_{OH}	High level Output Voltage	I_{OH} = -12mA	TDO	2.4			V
V_{OL}	Low level Output Voltage	I_{OL} = 12mA				0.5	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V			-95	-125	mA
I_{OZ}	Tri-state Output Current	V_{OUT} = 0V or 3.6V		−10		+10	uA
Bus LVDS DC Specifications Over recommended operating supply and temperature unless otherwise specified.							
V_{OD}	Output Differential Voltage (DO+) - (DO-)	RL = 100Ω, C_L = 10pF to GND	DOn+, DOn-	350	500		mV
ΔV_{OD}	Output Differential Voltage Unbalance				3	35	mV
V_{OS}	Offset Voltage			1.0	1.1	1.3	V
ΔV_{OS}	Offset Voltage Unbalance				2	35	mV
I_{OS}	Output Short Circuit Current	DO = 0V, Din = H, MS_PWDN and DEN = 2.4V			−50	-90	mA
I_{OZ}	Tri-state Output Current	MS_PWDN or DEN = 0.8V, DO = 0V OR VDD		-10	+/-1	10	µA
I_{OX}	Power-Off Output Current	VDD = 0V, DO = 0V or 3.6V		-10	+/− 1	10	µA
SER/DES SUPPLY CURRENT (apply to pins DVDD, PVDD and AVDD) Over recommended operating supply and temperature ranges unless otherwise specified.							
I_{CCD}	Supply Current (SYNC pattern)	V_{CC} = 3.6V, R_L = 100 Ω	f = 18MHz		145		mA
			f = 66MHz		175		mA
	Worst Case Supply Current (Checker-board pattern)	V_{CC} = 3.6V, R_L = 100 Ω Figure 1	f = 18 MHz		148	166	mA
			f = 66 MHz		263	350	mA
I_{CCXD} (Master)	Supply Current Powered Down	MS_PWDN = 0.1V, DEN = 0V			0.35	1.0	mA
I_{CCXD} (Ind. Ch)	Worst Cast Power Saving Per Channel Disabled	MS_PWDN = 3V, PWDNn = 0V	66 MHz		6		mA
			18 MHz		3.6		mA

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except VOD, and ΔVOD which are differential voltages.
(3) BIST_SEL have a weak internal pull-up. In a noisy operating environment, it is recommended that an external pull up be used to ensure that BIST_SEL is in the high state.

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Serializer Timing Requirements for TCLK

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{TCP}	Transmit Clock Period	See Figure 3	TCLK	15.15		55.5	ns
t_{TCIH}	Transmit Clock High Time			30	50	70	%
t_{TCIL}	Transmit Clock Low Time			30	50	70	%
t_{CLKT}	TCLK Input Transition Time				3	6	ns
t_{JIT}	TCLK Input Jitter					80	ps_{rms}

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except VOD, and ΔVOD which are differential voltages.

Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{LLHT}	Bus LVDS Low-to-High Transition Time	R_L = 100Ω C_L=10pF to GND (3) Figure 2	DOn+, DOn-	190	330	400	ps
t_{LHLT}	Bus LVDS High-to-Low Transition Time			190	330	400	ps
t_{DIS}	DIN (0-9) Setup to TCLK	R_L = 100Ω, C_L=10pF to GND Figure 4	DINn(0-9), TCLK	2.0			ns
t_{DIH}	DIN (0-9) Hold from TCLK			1.5			ns
t_{HZD}	DO ± HIGH to Tri-state Delay	R_L = 100Ω, C_L=10pF to GND Figure 5	DOn+, DOn-, DEN		5.7	12	ns
t_{LZD}	DO ± LOW to Tri-state Delay				6.9	12	ns
t_{ZHD}	DO ± Tri-state to HIGH Delay				6.2	12	ns
t_{ZLD}	DO ± Tri-state to LOW Delay				5.8	12	ns
t_{SPD}	SYNC Pattern Delay, Figure 9	R_L = 100Ω C_L=10pF to GND	TCLK, SYNCn, DOn+, DOn-, MS_PWDN	$4*t_{TCP}$		$5*t_{TCP}$	ns
t_{PLD}	Serializer PLL Lock Time, Figure 6			$510*t_{TCP}$		$513*t_{TCP}$	ns
t_{SD}	Serializer Delay	R_L = 100Ω C_L=10pF to GND Figure 8	DINn(0-9), TCLK, DOn+, DOn-	t_{TCP} + 1.0	t_{TCP} + 3.5	t_{TCP} + 5	ns
t_{ICR}	Individual Channel Power up Time	R_L = 100Ω, C_L=10pF to GND	TCLK, DOn+, DOn-, PWDNn Figure 7	$60*t_{TCP}$	$63*t_{TCP}$	$70*t_{TCP}$	ns
t_{MCR}	Master Power up Time		TCLK, DOn+, DOn-, MS_PWDN Figure 6	$510*t_{TCP}$		$513*t_{TCP}$	ns
t_{STE}	@Speed Test Enable Time	R_L = 100Ω	BIST_ACT, BIST_SEL (0:3), TCLK, DOn+, DOn-		$10*t_{TCP}$		ns
t_{STD}	@Speed Test Disable Time	R_L = 100Ω			$7*t_{TCP}$		ns
t_{SKEW}	Channel to Channel Skew	R_L = 100Ω, C_L=10pF to GND	18 MHz		130		ps
			66 MHz		80		ps

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except VOD, and ΔVOD which are differential voltages.
(3) t_{LLHT}, t_{LHLT}, t_{DJIT} and t_{RJIT} specifications are Ensured by Design using statistical analysis.

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Serializer Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{RJIT}	Random Jitter	R_L = 100Ω, C_L=10pF to GND(3)(4)	18MHz		39	45	ps (rms)
			66MHz		18	21	ps (rms)
t_{DJIT}	Deterministic Jitter, Figure 10	R_L = 100Ω, C_L=10pF to GND(3)(5)	18MHz	−225	20	257	ps (p-p)
			66MHz	−150	−55	68	ps (p-p)

(4) t_{RJIT} specification is the rms jitter measurement of the serializer output when the device is transmitting SYNC pattern.
(5) t_{DJIT} specification is measured with the serializer output transmitting checkerboard patterns. It is a measurement of the center distribution of 0V (differential) crossing in comparsion with the ideal bit position. See Figure 10.

SCAN Circuitry Timing Requirements

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{MAX}	Maximum TCK Clock Frequency	R_L = 500Ω, C_L = 35 pF	18			MHz
t_S	TDI to TCK, H or L		2.0			ns
t_H	TDI to TCK, H or L		1.0			ns
t_S	TMS to TCK, H or L		2.0			ns
t_H	TMS to TCK, H or L		1.0			ns
t_W	TCK Pulse Width, H or L		10.0			ns
t_W	$\overline{TRST}$ Pulse Width, L		2.5			ns
t_{REC}	Recovery Time, $\overline{TRST}$ to TCK		2.5			ns

AC Timing Diagrams and Test Circuits

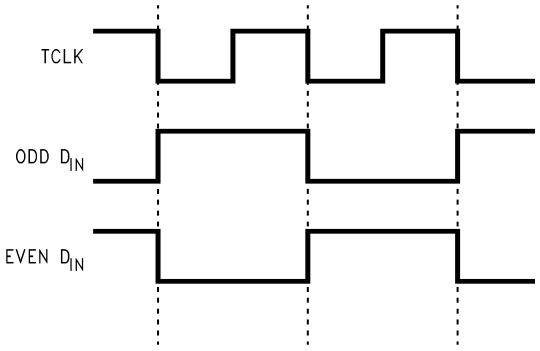


Figure 1. 'Worst Case Icc Test Pattern

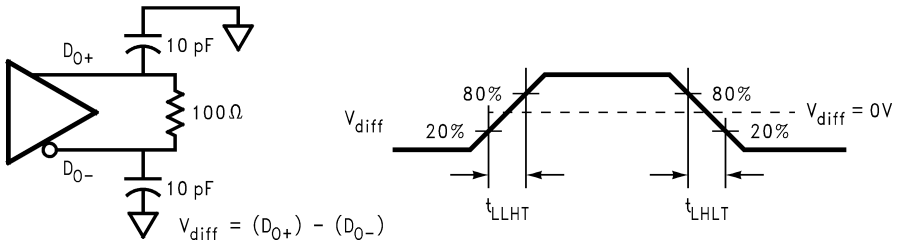


Figure 2. Serializer Bus LVDS Output Load and Transition Times

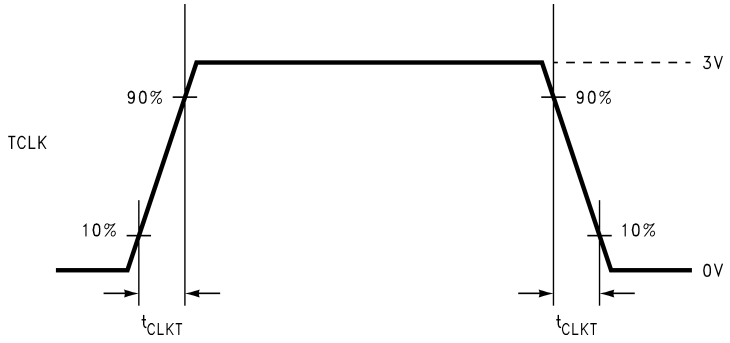


Figure 3. Serializer Input Clock Transition Time

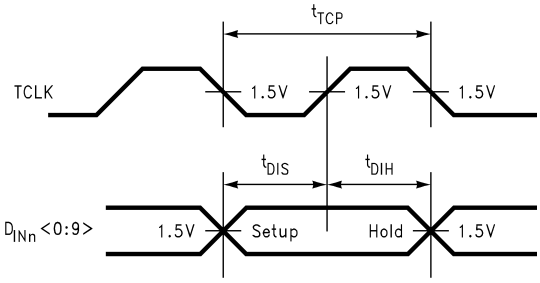


Figure 4. Serializer Setup/Hold Times

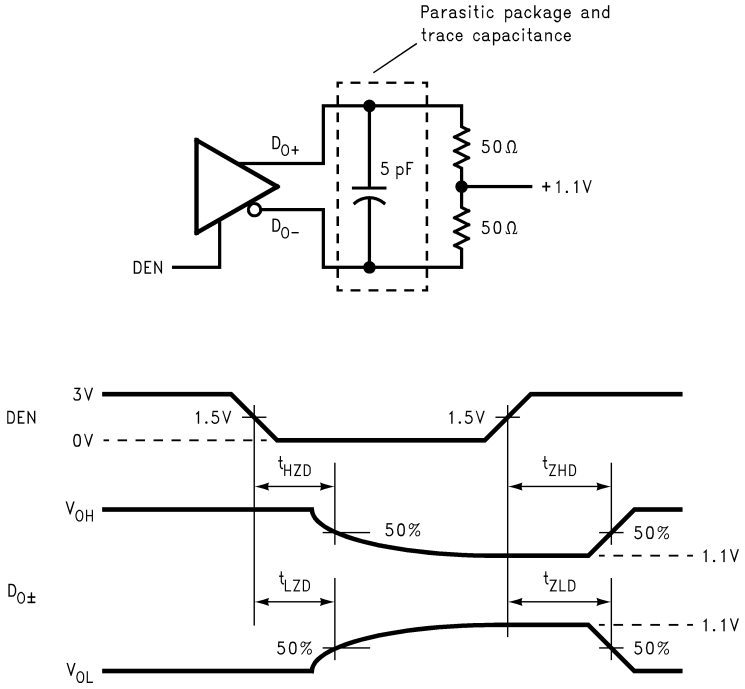


Figure 5. Serializer Input Clock Transition Time Tri-state Test Circuit and Timing

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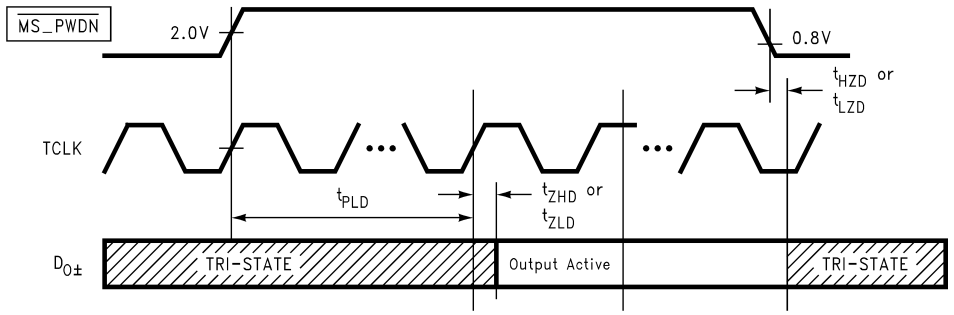


Figure 6. Serializer PLL lock Time and $\overline{\text{MS_PWDN}}$ Tri-state Delays

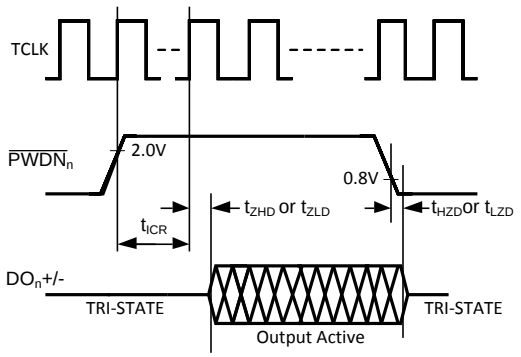


Figure 7. Individual Channel Power up Time, t_{ICR}

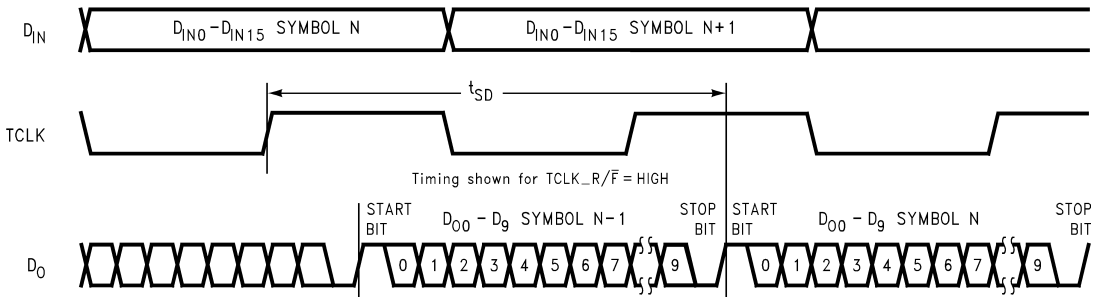


Figure 8. Serializer Delay

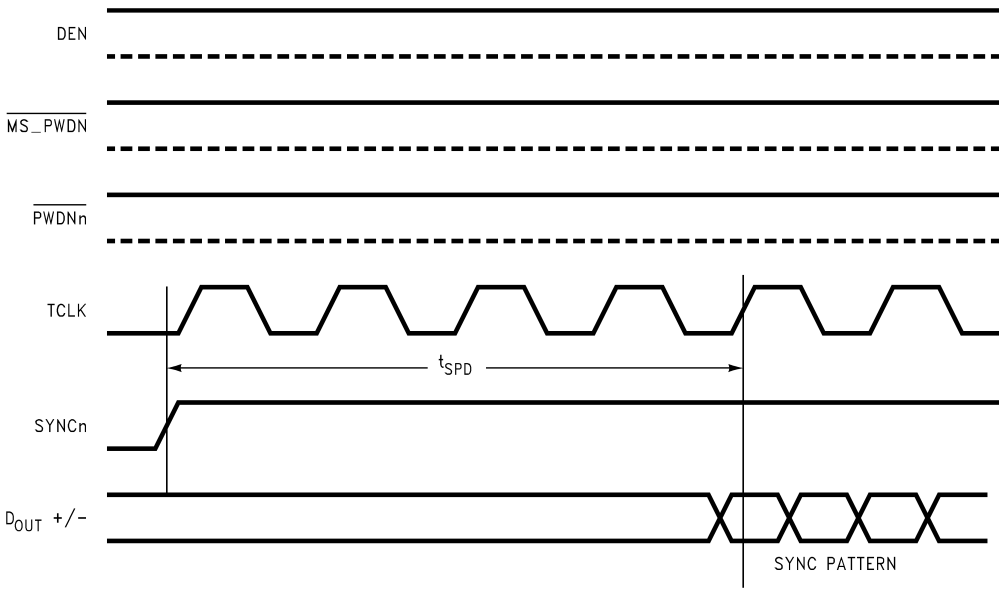


Figure 9. SYNC Timing Delays

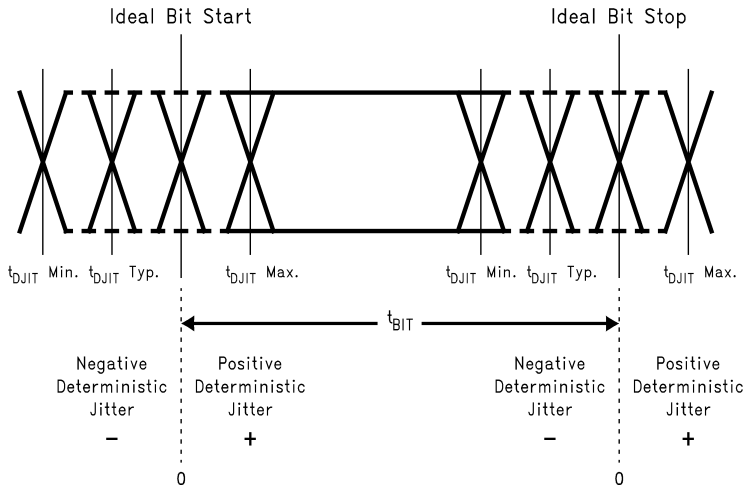


Figure 10. Deterministic Jitter and Ideal Bit Position

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Functional Description

The SCAN928028 combines eight 10:1 serializers into a single chip. Each of the eight serializers accepts 10 or less data bits. The serializers then multiplex the data into a serial stream with embedded clock bits and route to the LVDS output. The LVDS output is a 5 mA current loop driver. It provides enough drive for point-to-point and lightly loaded multidrop applications. The serialized data stream is compatible with the DS92LV1210, DS92LV1212A, DS92LV1224, DS92LV1260, SCAN921224, SCAN921226, SCAN921260, and SCAN926260 10-bit deserializers from Texas Instruments.

Each of the eight channels on the SCAN928028 has their own serializer function but share a single PLL. There is a single Transmit Clock (TCLK) for all eight channels. The data on all eight 10-bit interfaces is latched into the device with the rising edge of TCLK. Each of the serialized data streams is independent of the others and includes the embedded clock information. The skew between the serializer outputs is minimal.

There is a master power-down signal ($\overline{\text{MS_PWDN}}$) to put the entire device into a low power consumption state. In addition, there is a power-down control signal for each of the eight channels. This allows the device to efficiently operate as one to eight 10-bit serializers.

The @SPEED TEST signal initiates the sending of a random data pattern over the LVDS links. This allows for testing the links for bit error rates at the frequency they will be carrying data. In addition, JTAG can be used to verify the device interconnects and initiate/verify the at-speed BIST.

The SCAN928028 has four operating modes. They are the Initialization, Data Transfer, Resynchronization, @SPEED TEST states. There are also two passive states: Power-down and Tri-state. In addition to the active and passive states, there are test modes for JTAG access and at-speed BIST.

The following sections describe each operating mode, passive state, and the test modes.

INITIALIZATION

Before the '8028 serializes and transmits data, it and the receiving deserializer device(s) must initialize the link. Initialization refers to synchronizing the Serializer's and the Deserializer's PLLs to local clocks. The local clocks should be the same frequency, or within the specified range if from different sources. After all devices synchronize to local clocks, the Deserializers synchronize to the Serializers as the second and final initialization step.

Step 1: After applying power to the serializer, the outputs are held in tri-state and the on-chip power-sequencing circuitry disables the internal circuits. When Vcc reaches VccOK (2.1V), the PLL in the serializer begins locking to the local clock (TCLK). A local on-board data source or other source provides the specified clock input to the TCLK pin.

After locking to TCLK, the serializer is now ready to send data or SYNC patterns, depending on the level of the SYNC input or a data stream at the data inputs. The SYNC pattern sent by the serializer consists of six ones and six zeros switching at the input clock rate.

Step 2: The Deserializer PLL must synchronize to the Serializer to complete the initialization. (Refer to the deserializer data sheet for operation details during this step of the Initialization State.) The Deserializer identifies the rising clock edge in a synchronization pattern or non-repetitive data pattern. Depending on the data pattern that it is being transmitted, the Deserializer will synchronize to the data stream from the Serializer after some delay. At the point where the Deserializer's PLL locks to the embedded clock, the LOCK pin goes low and valid data appears on the output.

The user's application determines control of the SYNC signal input. One recommendation is a direct feedback loop from the LOCK pin on the deserializer. The serializer stops sending SYNC patterns when the SYNC input returns to a low state.

DATA TRANSFER

After initialization, the serializer accepts data from the inputs DINn0 to DINn9. The serializer uses the rising edge of the TCLK input to latch incoming data. If the SYNCn input is high for 4 TCLK cycles, the data on DINn0-DINn9 is ignored and SYNC pulses are transferred.

The serial data stream includes a start bit and stop bit appended by the serializer, which frame the ten data bits. The start bit is always high and the stop bit is always low. The start and stop bits also function as clock bits embedded in the serial stream.

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The Serializer transmits the data and clock bits (10+2 bits) at 12 times the TCLK frequency. For example, if TCLK is 40 MHz, the serial rate is 40 X 12 = 480 Mbps. Since only 10 bits are from input data, the serial 'payload' rate is 10 times the TCLK frequency. For instance, if TCLK = 40 MHz, the payload data rate is 40 X 10 = 400 Mbps. TCLK is provided by the data source and must be in the range 18 MHz to 66 MHz nominal.

The serializer outputs (DO0± – DO7±) can drive a point-to-point connection or lightly loaded multidrop connections. The outputs transmit data when the driver enable pin (DEN) is high, MS_PWDN and PWDNn are high, and SYNCn is low. When DEN is driven low, all the serializer output pins will enter tri-state.

When any one of eight attached Deserializer channels synchronizes to the input from the Serializer, it drives its LOCK pin low and synchronously delivers valid data on the output. The Deserializer locks to the embedded clock, uses it to generate multiple internal data strobes, and drives the embedded clock on the RCLK pin. The RCLK is synchronous to the data on the ROUT pins. While LOCK is low, data on ROUT is valid. Otherwise, ROUT is invalid.

RESYNCHRONIZATION

Whenever one of the connected DS92LV1212, '1212A, '1224, '1226, '1260, or '6260 deserializers loses lock, it will automatically try to resynchronize to the data stream from the serializer. If the data stream is not a repetitive pattern, then the deserializer will automatically lock.

For example, if the deserializer's received embedded clock edge is not detected two times in succession, the PLL loses lock and the LOCK pin is driven high. The '1212, '1212A, '1224, '1226, '1260, or '6260 deserializers will automatically begin searching for the embedded clock edge. If it is a random data pattern, the deserializer will lock to that stream. If the data pattern is repetitive, the deserializer's PLL will not lock in order to prevent the deserializer from locking to the data pattern rather than the clock. We refer to such patterns as repetitive-multiple-transition, RMT.

Therefore, if the data stream is not random data or the deserializer is the DS92LV1210, there needs to be a feedback path from the deserializer to the serializer. This feedback path can be as simple as connecting the deserializer's LOCK pin to the serializer's SYNC pin. This will automatically signal the serializers to send SYNC patterns whenever the deserializer loses lock.

The user has the choice of allowing the deserializer to resynchronize to the data stream, or to force synchronization by pulsing the Serializer SYNC pin. This scheme is left up to the user discretion.

POWER-DOWN

The Power-down state is a low power sleep mode that the Serializer and Deserializer typically occupy while waiting for initialization, or to reduce power when there are no pending data transfers. The SCAN928028 serializers enter Power-down when MS_PWDN is driven low. In Power-down, the PLL stops and the outputs go into tri-state. To exit Power-down, the system drives MS_PWDN high.

Each of the serializers in the '8028 also has an individual power down, $\overline{\text{PWDNn}}$ control pin. This control enables the deactivation of individual serializers while allowing others to operate normally. The benefit is that spare serializers can be allocated for backup operation, but not consuming power until employed for data transfers.

The Individual Power Down will NOT cause the PLL of the device to lose lock, but it will cause the specific serializer channel to go into a low power sleep mode and its output go into tri-state. Thus, the device will NOT go through the Initialization state when individual channels exit the Individual Power Down state, and the output of the specific channel will become available after a short delay, see Figure 7 and spec t_{ICR}

TRI-STATE

When the system drives DEN pin low, the serializer outputs enter tri-state. This will tri-state the output pins (DO0± to DO7±). When the system drives DEN high, the serializers will return to the previous state as long as all other control pins remain static (PWDNn, TCLK, SYNCn, and DINn[0:9]).

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TEST FEATURES

Since the high-speed LVDS serial data transmission line quality is essential to the chipset operation, a means of checking this signal integrity is built into the SCAN928028 serializer. Each Serializer channel has the ability to transfer an internally generated PRBS data pattern. This pattern traverses the transmission line to the deserializer. Specific deserializers (SCAN921224 for example) have the complement PRBS pattern verification circuit. The deserializer checks the data pattern for bit errors and reports any errors on the test verification pins on the deserializer.

The @SPEED feature uses 5 signal pins. The BIST_SEL[0:3] and BIST_ACT pins together determine the functions of the BIST mode. The BIST_ACT signal activates the test feature. The BIST_SEL[0:3] selects 1 of 8 channels as the output for the BIST pattern. All channels perform BIST when BIST_ACT = H and BIST_SEL<0:3>=08H.

JTAG TEST FEATURES

In addition to using IEEE 1149.1 test access to the digital TTL pins, the SCAN928028 has two instructions to test the LVDS interconnects. The first instruction is EXTEST. This is implemented at LVDS levels and is only intended as a go no-go test (e.g. missing cables). The second method is the RUNBIST instruction. It is an "at-system-speed" interconnect test. It is executed in approximately 33mS with a maximum system clock speed of 66MHz. There are two bits in the RX BIST data register for notification of PASS/FAIL and TEST_COMPLETE. Pass indicates that the BER (Bit-Error-Rate) is better than 10^{-7}.

An important detail is that once both devices have the RUNBIST instruction loaded into their respective instruction registers, both devices must move into the RTI (*Run-Test-Idle*) state within 4K system clocks (At a TCLK of 66Mhz and TCK of 1MHz this allows for 66 TCK cycles). This is not a concern when both devices are on the same scan chain or LSP, however, it can be a problem with some multi-drop devices. This test mode has been simulated and verified using TI's SCANSTA111.

If the user is unable to meet the constraint of moving both taps into RTI within 4K system clocks, the receiver must be moved into the RTI state first. The receiver can then stay in RTI indefinitely until the transmitter is moved into RTI and the BIST pattern begins. This is true for either SCAN initiated BIST or pin initiated BIST_ALONE or any combination of the two.

Truth Table (BIST mode)

No BIST function performed when BIST_SEL (0:3) are set from 9H to FH even when BIST_ACT is set at HIGH. See(1)(2)

BIST_ACT	BIST_SEL <3>	BIST_SEL <2>	BIST_SEL <1>	BIST_SEL <0>	MODE
H	L	L	L	L	BIST on channel 0
H	L	L	L	H	BIST on channel 1
H	L	L	H	L	BIST on channel 2
H	L	L	H	H	BIST on channel 3
H	L	H	L	L	BIST on channel 4
H	L	H	L	H	BIST on channel 5
H	L	H	H	L	BIST on channel 6
H	L	H	H	H	BIST on channel 7
H	H	L	L	L	BIST on ALL CHANNELS
L	X	X	X	X	NO BIST
L	H	H	H	H	Default - NO BIST

(1) BIST_SEL have a weak internal pull-up. In a noisy operating environment, it is recommended that an external pull up be used to ensure that BIST_SEL is in the high state.
(2) No BIST function performed when BIST_SEL (0:3) are set from 9H to FH even when BIST_ACT is set at HIGH.

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Functional Block Diagram

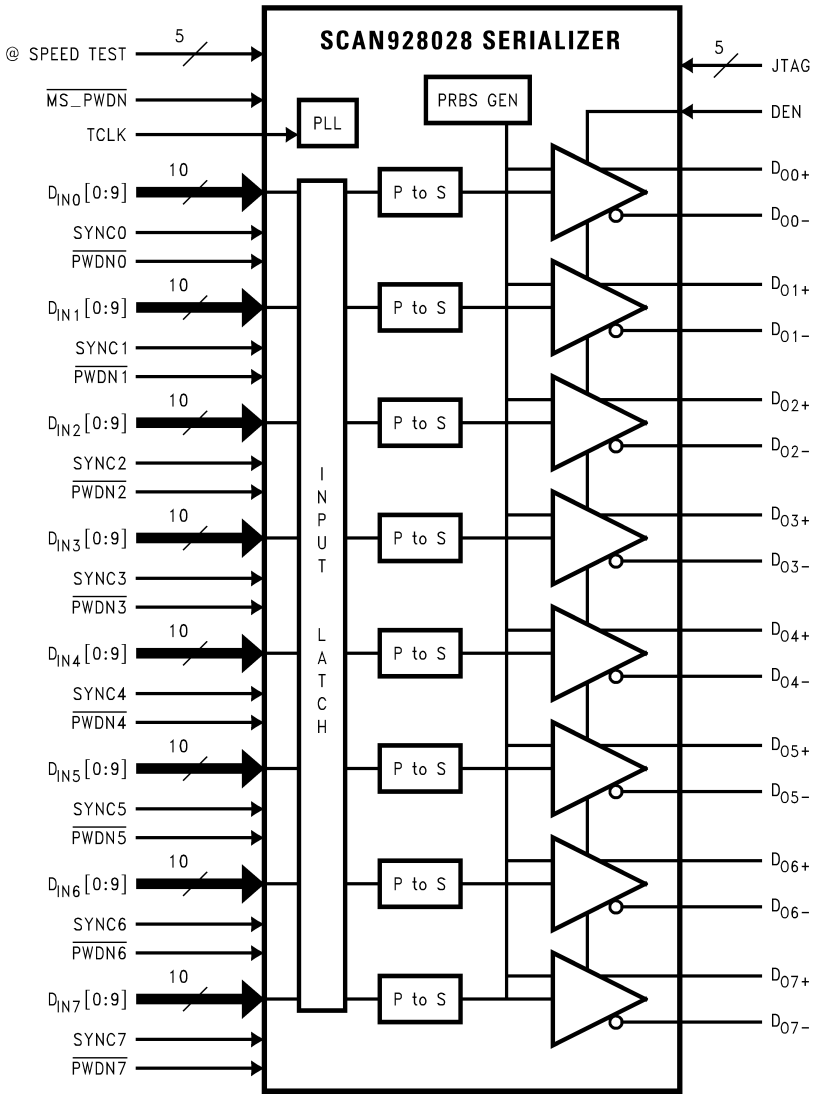


Figure 11. SCAN928028 Functional Block Diagram

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APPLICATION INFORMATION

USING THE SCAN928028

The SCAN928028 is an easy to use serializer that combines eight 10:1 serializers into a single chip with a maximum payload of 5.28Gbps. Each of the eight serializers accepts 10 or less data bits. The serializers then multiplex the data into a serial data stream with embedded clock bits and route to the LVDS output at up to 660Mbps per channels. The LVDS output is a 5 ma current loop driver that can be used for point-to-point and lightly loaded multidrop applications. Each of the eight channels has their own serializer function but share a single Transmit Clock (TCLK) with a single PLL for the entire chip. The data on all eight channels is latched into the device with the rising edge of TCLK and the data stream is compatible with the DS92LV1210, DS92LV1212A, DS92LV1224, DS92LV1260, SCAN921224, SCAN921226, SCAN921260, and SCAN926260 deserializers from Texas Instruments.

If using less than 10 bits of data, it is recommended to tie off adjacent bits to the embedded clock bits to prevent causing a RMT in the data payload. For example, if only using 8 bits, tie D0 High and D9 Low.

POWER CONSIDERATIONS

All CMOS design of the Serializer and Deserializer makes them inherently low power devices. Additionally, the constant current source nature of the LVDS outputs minimize the slope of the speed vs. I_{CC} curve of CMOS designs.

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the BLVDS devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high-frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitic, especially proven effective at high frequencies above approximately 50MHz, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

It is a recommended practice to use two vias at each power pin as well as at all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance by up to half, thereby reducing interconnect inductance and extending the effective frequency range of the bypass components. Locate RF capacitors as close as possible to the supply pins, and use wide low impedance traces (not 50 Ohm traces). Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins straight to the power and ground plane, with the bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting a power or ground pin to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. User must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30MHz range. To provide effective bypassing, very often, multiple capacitors are used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two via from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate CMOS (TTL) swings away from the LVDS lines to prevent coupling from the CMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely-coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. Also the tight coupled lines will radiate less.

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TRANSMISSION MEDIA

The SCAN928028 Serializers can be used in point-to-point configuration of a backplane across PCB traces or through cable interconnect. In point-to-point configurations the transmission media needs only to be terminated at the receiver end. The SCAN928028 may also be used with double terminations for a total load or 50 Ohms for use in certain limited multidrop applications. Termination impedances lower than 50 Ohms is not recommended.

TERMINATION

Termination of the LVDS interconnect is required. For point-to-point applications termination should be located at the load end. Nominal value is 100 Ohms to match the line's differential impedance. Place the resistor as close to the receiver inputs as possible to minimize the resulting stub between the termination resistor and receiver.

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the TI web site at: http://www.ti.com/ww/en/analog/interface/lvds.shtml

SCAN928028 BLVDS SERIALIZER BYPASS RECOMMENDATIONS

General device specific guidance is given below. Exact guidance can not be given as it is dictated by other board level /system level criteria. This includes the density of the board, power rails, power supply, and other integrated circuit power supply needs.

For a typical application circuit, please see Figure 12.

DVDD = DIGITAL SECTION POWER SUPPLY

These pins supply the digital portion of the device. A 0.1uF capacitor is sufficient for these pins.

PVDD = PLL SECTION POWER SUPPLY

The PVDD pin supplies the PLL circuit. The PLL(s) require clean power for the minimization of Jitter. A supply noise frequency in the 300kHZ to 1MHz range can cause increased output jitter. Certain power supplies may have switching frequencies or high harmonic content in this range. If this is the case, filtering of this noise spectrum may be required. A notch filter response is best to provide a stable VDD, suppression of the noise band, and good high-frequency response (clock fundamental). This may be accomplished with a pie filter (CRC or CLC). The pie filter should be located close to the PVDD power pin. Separate power planes for the PVDD pins is typically not required.

AVDD = LVDS SECTION POWER SUPPLY

The AVDD pin supplies the LVDS portion of the circuit. The SCAN928028 has nine AVDD pins. Due to the nature of the design, current draw is not excessive on these pins. A 0.1uF capacitor is sufficient for these pins. If space is available a 0.01uF may be used in parallel with the 0.1uF capacitor for additional high frequency filtering.

GROUNDS

The AGND pin should be connected to the signal common in the cable for the return path of any common-mode current. Most of the LVDS current will be odd-mode and return within the interconnect pair. A small amount of current may be even-mode due to coupled noise, and driver imbalances. This current should return via a low impedance known path.

A solid ground plane is recommended for DVDD, PVDD or AVDD. Using a split plane may have a potential problem of ground loops, or difference in ground potential at various ground pins of the device.

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Application Diagram

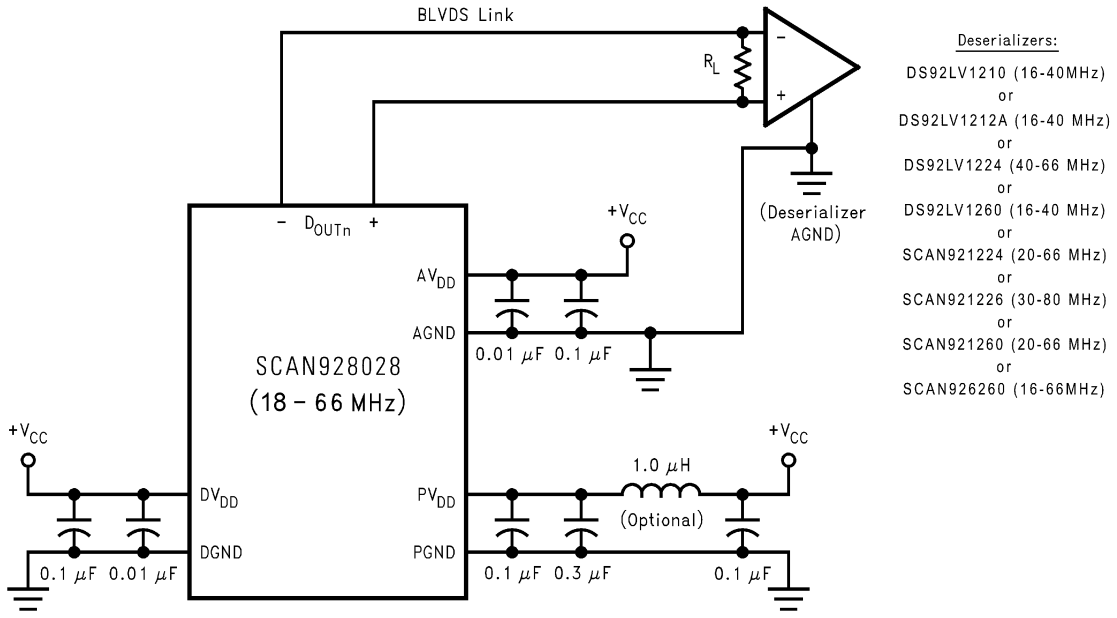


Figure 12. Typical Application Circuit

Pin Diagram

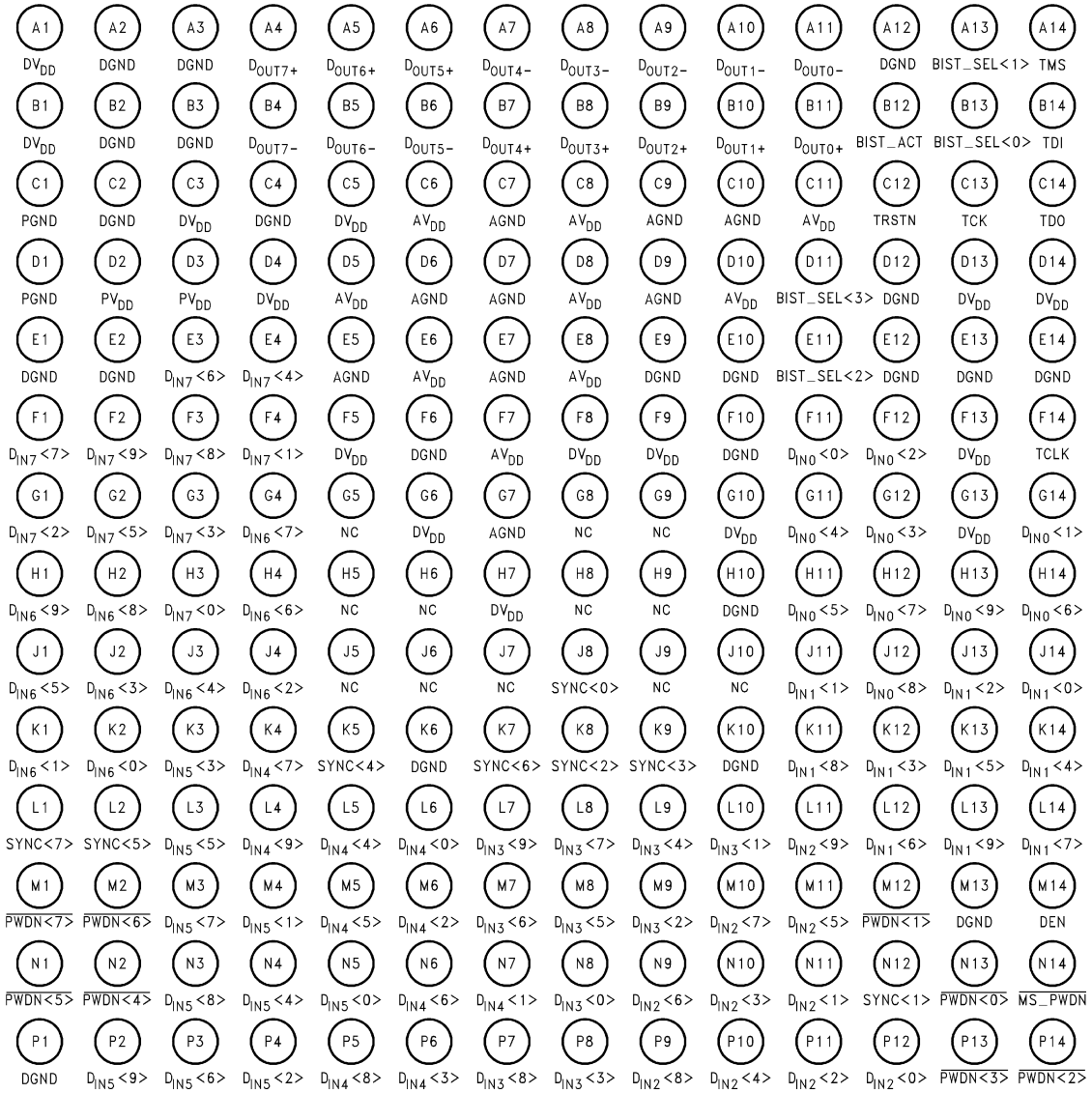


Figure 13. Top View of SCAN928028 (196-pin NFBGA)

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Pin Descriptions

Pin Number	Name	Type	Description
C7, C9, C10, D6, D7, D9, E5, E7, G7	AGND		Analog ground.
C6, C8, C11, D5, D8, D10, E6, E8, F7	AVDD		Analog power supply.
B12	BIST_ACT	3.3 V CMOS I	BIST Active. Control pin for BIST mode enable.When BIST_ACT = H and BIST_SEL (0:3) = 0H to 8H, device will go to BIST mode accordingly. See Truth Table (BIST mode) Default at Low
A13, B13, D11, E11	BIST_SEL (0:3)	3.3 V CMOS I	BIST select. Control pins for which serializer is set for BIST mode. See Truth Table (BIST mode) (1)
M14	DEN	3.3 V CMOS I	Serializer output data enable. Enable data output DOUTn (0:9). n = serializer number. When driven low, puts the Bus LVDS outputs in tri-state. Default at Low.
A2, A3, A12, B2, B3, C2, C4, D12, E1, E2, E9, E10, E12, E13, E14, F6, F10, H10, K6, K10, M13, P1	DGND		Digital Ground.
E3, E4, F1, F2, F3, F4, F11, F12, G1, G2, G3, G4, G11, G12, G14, H1, H2, H3, H4, H11, H12, H13, H14, J1, J2, J3, J4, J11, J12, J13, J14, K1, K2, K3, K4, K11, K12, K13, K14, L3, L4, L5, L6, L7, L8, L9, L10, L11, L12, L13, L14, M3, M4, M5, M6, M7, M8, M9, M10, M11, N3, N4, N5, N6, N7, N8, N9, N10, N11, P2, P3, P4, P5, P6, P7, P8, P9, P10 P11, P12	DINnx	3.3 V CMOS I	Data input. Inputs for the ten bit serializers. n = serializer number, x = bit number. Default at Low.
B11-A11, B10-A10, B9-A9, B8-A8, B7-A7, A6-B6, A5-B5, A4-B4	Doutn±	Bus LVDS O	Bus LVDS differential outputs. n = serializer number.
A1, B1, C3, C5, D4, D13, D14, F5, F8, F9, F13, G6, G10, G13, H7,	DVDD		Digital power supply.
N14	$\overline{\text{MS_PWDN}}$	3.3 V CMOS I	Master Powerdown. $\overline{\text{MS_PWDN}}$ driven low shuts down the PLL and tri-state all outputs, putting the device into a low power 'sleep' mode. Default at Low.
G5, G8, G9, H5, H6, H8, H9, J5, J6, J7, J9, J10	NC (1:12)		No connect.
C1, D1	PGND		PLL ground.
D2, D3	PVDD		PLL power supply.
N1, N2, N13, M1, M2, M12, P13, P14	$\overline{\text{PWDN (0:7)}}$	3.3 V CMOS I	Individual Powerdown. $\overline{\text{PWDN (0:7)}}$ driven low puts individual serializers into tri-state, low power 'sleep' mode. Default at Low.
J8, K5, K7, K8, K9, L1, L2, N12	SYNC (0:7)	3.3 V CMOS I	SYNC pattern enable. When driven high for a mininum of 4 cycles, SYNC patterns will be transmitted on the Bus LVDS serial output. The SYNC pattern sent by the serializer consists of six ones and six zeros switching at the input clock rate. SYNC pattern continues to be sent if SYNC continues at high. Default at Low. See Functional Description.
C13	TCK		Test Clock Input to support IEEE 1149.1
B14	TDI		Test Data Input to support IEEE 1149.1. There is an internal pullup resistor that defaults this input to high per IEEE 1149.1.
C14	TDO		Test Data Output to support IEEE 1149.1
A14	TMS		Test Mode Select Input to support IEEE 1149.1. There is an internal pullup resistor that defaults this input to high per IEEE 1149.1.
C12	TRSTN		Test Reset Input to support IEEE 1149.1. There is an internal pullup resistor that defaults this input to high per IEEE 1149.1.

(1) BIST_SEL have a weak internal pull-up. In a noisy operating environment, it is recommended that an external pull up be used to ensure that BIST_SEL is in the high state.

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Pin Descriptions (continued)

Pin Number	Name	Type	Description
F14	TCLK	3.3 V CMOS I	Transmit Clock. Input for 18 MHz - 66 MHz (nominal) system clock.

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REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	18

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SCAN928028TUF/NOPB	ACTIVE	NFBGA	NZH	196	119	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	SCAN928028T UF >B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

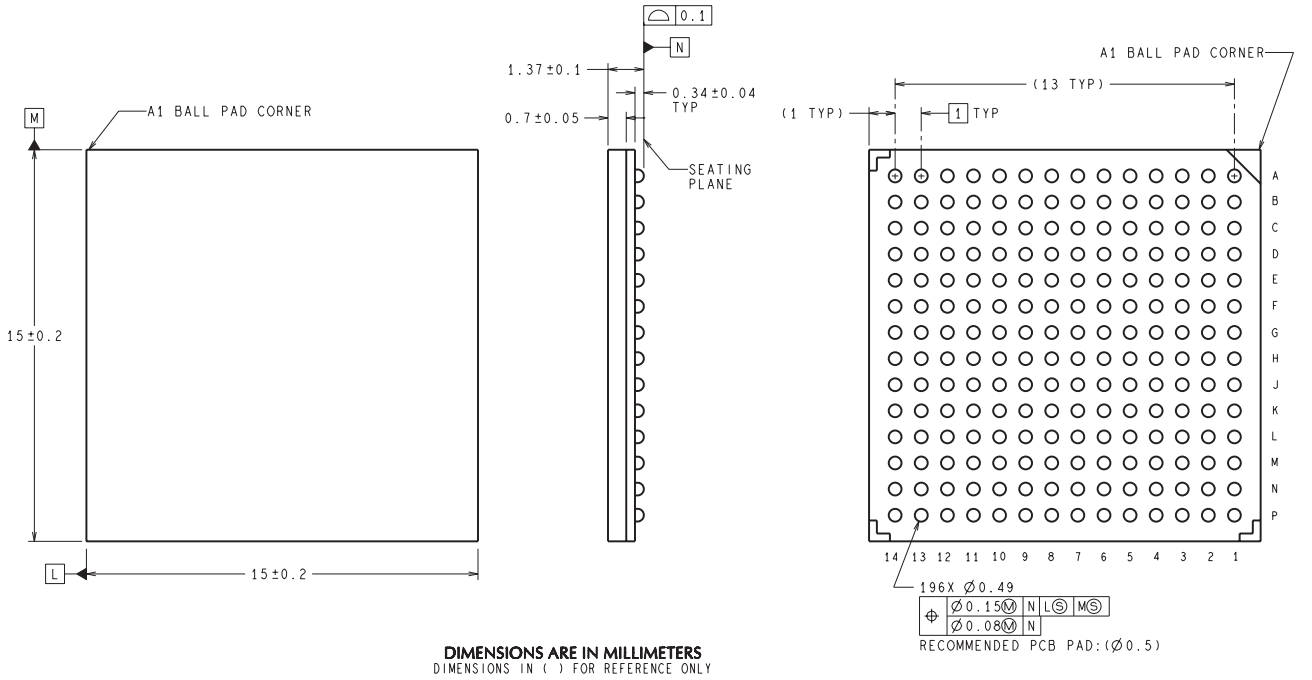
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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