

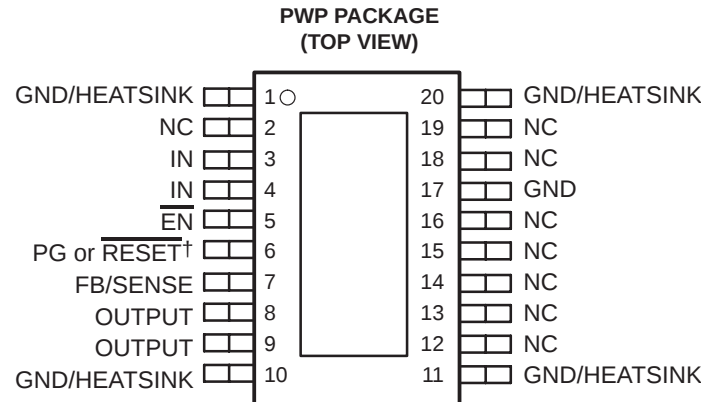
TPS75101-EP, '75115-EP, '75118-EP, '75125-EP, '75133-EP WITH POWER GOOD TPS75301-EP, TPS75315-EP, TPS75318-EP, TPS75325-EP, TPS75333-EP WITH RESET FAST-TRANSIENT-RESPONSE 1.5-A LOW-DROPOUT VOLTAGE REGULATORS

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- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree[†]**
- **1.5-A Low-Dropout Voltage Regulator**
- **Available in 1.5-V, 1.8-V, 2.5-V, 3.3-V, Fixed Output and Adjustable Versions**
- **Open Drain Power-Good (PG) Status Output (TPS751xxQ)**
- **Open Drain Power-On Reset With 100-ms Delay (TPS753xxQ)**
- **Dropout Voltage Typically 160 mV at 1.5 A (TPS75133Q)**

[†] Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **Ultralow 75 μ A Typical Quiescent Current**
- **Fast Transient Response**
- **2% Tolerance Over Specified Conditions For Fixed-Output Versions**
- **20-Pin TSSOP (PWP) PowerPAD™ Package**
- **Thermal Shutdown Protection**



NC – No internal connection

[†] PG is on the TPS751xx and RESET is on the TPS753xx

description

The TPS753xxQ and TPS751xxQ are low dropout regulators with integrated power-on reset and power-good (PG) functions respectively. These devices are capable of supplying 1.5 A of output current with a dropout of 160 mV (TPS75133Q, TPS75333Q). Quiescent current is 75 μ A at full load and drops down to 1 μ A when the device is disabled. TPS751xxQ and TPS753xxQ are designed to have fast transient response for larger load current changes.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 160 mV at an output current of 1.5 A for the TPS75x33Q) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 75 μ A over the full range of output current, 1 mA to 1.5 A). These two key specifications yield a significant improvement in operating life for battery-powered systems.

The device is enabled when $\overline{\text{EN}}$ is connected to a low level voltage. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to less than 1 μ A at $T_J = 25^\circ\text{C}$.

For the TPS751xxQ, the power-good terminal (PG) is an active high, open drain output, which can be used to implement a power-on reset or a low-battery indicator.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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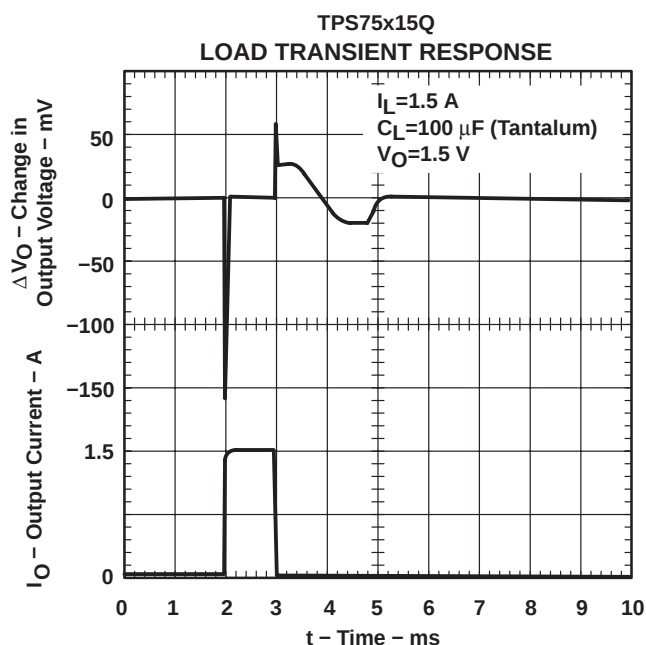
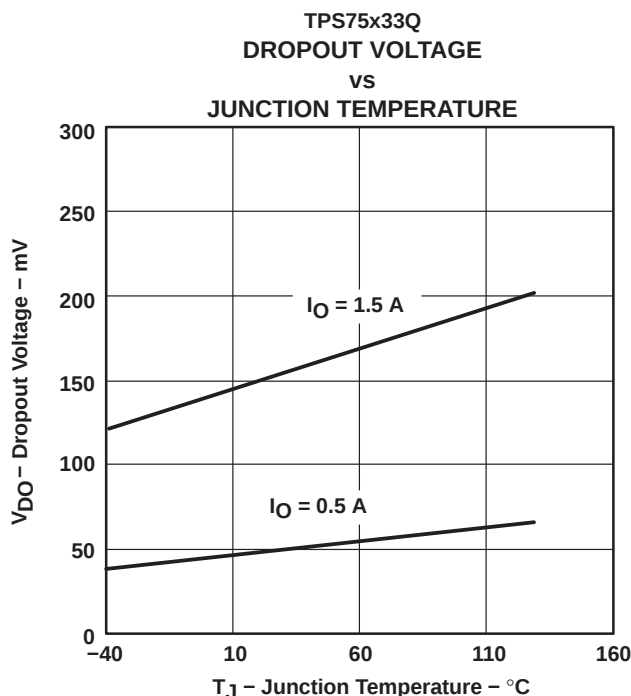
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description (continued)

The $\overline{\text{RESET}}$ (SVS, POR, or power on reset) output of the TPS753xxQ initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS753xxQ monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage. When the output reaches 95% of its regulated voltage, $\overline{\text{RESET}}$ goes to a high-impedance state after a 100-ms delay. $\overline{\text{RESET}}$ goes to a logic-low state when the regulated output voltage is pulled below 95% (i.e., over load condition) of its regulated voltage.

The TPS751xxQ or TPS753xxQ is offered in 1.5-V, 1.8-V, 2.5-V and 3.3-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS751xxQ and TPS753xxQ families are available in 20-pin TSSOP (PWP) packages.



AVAILABLE OPTIONS

T _J	OUTPUT VOLTAGE (TYP)	TSSOP (PWP)	
		PG	RESET
-40°C to 125°C	3.3 V	TPS75133QPWPREP [†]	TPS75333QPWPREP
	2.5 V	TPS75125QPWPREP [†]	TPS75325QPWPREP
	1.8 V	TPS75118QPWPREP [†]	TPS75318QPWPREP
	1.5 V	TPS75115QPWPREP [†]	TPS75315QPWPREP
	Adjustable 1.5 V to 5 V	TPS75101QPWPREP [†]	TPS75301QPWPREP

NOTE: The TPS75x01 is programmable using an external resistor divider (see application information). R suffix indicates tape and reel.

[†] Product preview

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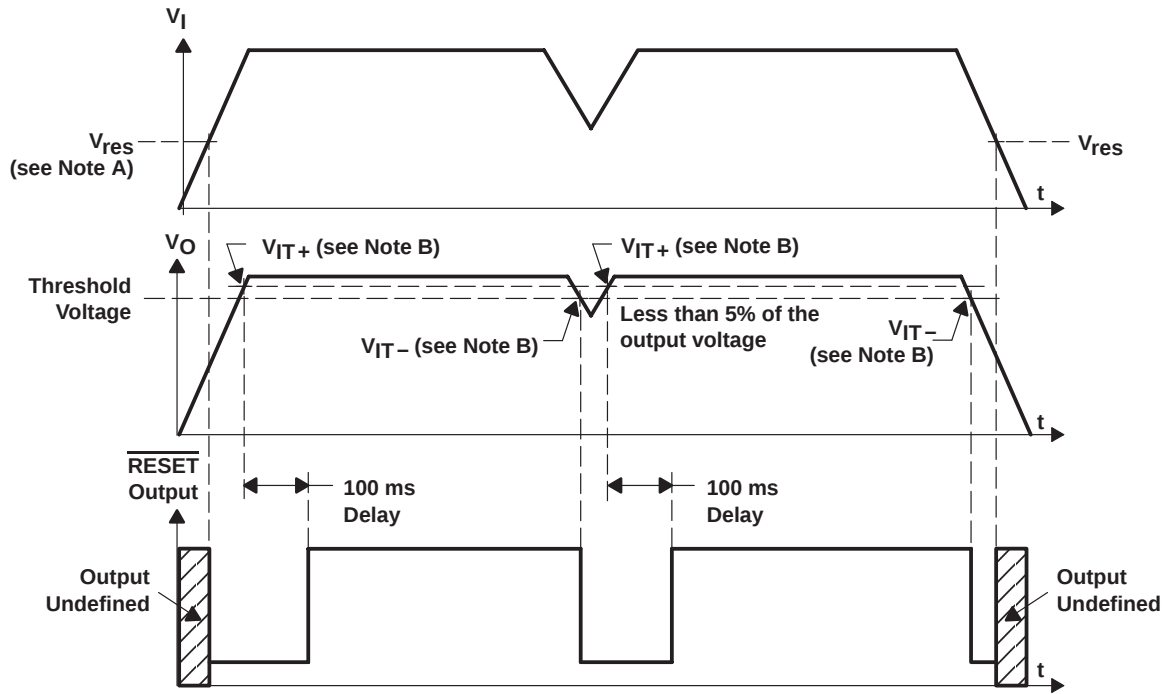
TERMINAL NAME	NO.	I/O	DESCRIPTION
EN	5	I	Enable Input
FB/SENSE	7	I	Feedback input voltage for adjustable device (sense input for fixed options)
GND	17		Regulator Ground
GND/HEATSINK	1, 10, 11, 20		Ground/heatsink
IN	3, 4	I	Input voltage
NC	2, 12, 13, 14, 15, 16, 18, 19		No connection
OUTPUT	8, 9	O	Regulated output voltage
PG	6	O	Power good output

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	5	I	Enable Input
FB/SENSE	7	I	Feedback input voltage for adjustable device (sense input for fixed options)
GND	17		Regulator Ground
GND/HEATSINK	1, 10, 11, 20		Ground/heatsink
IN	3, 4	I	Input voltage
NC	2, 12, 13, 14, 15, 16, 18, 19		No connection
OUTPUT	8, 9	O	Regulated output voltage
<u>RESET</u>	6	O	Reset output

**TPS75101-EP, '75115-EP, '75118-EP, '75125-EP, '75133-EP WITH POWER GOOD
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TPS753xxQ RESET timing diagram



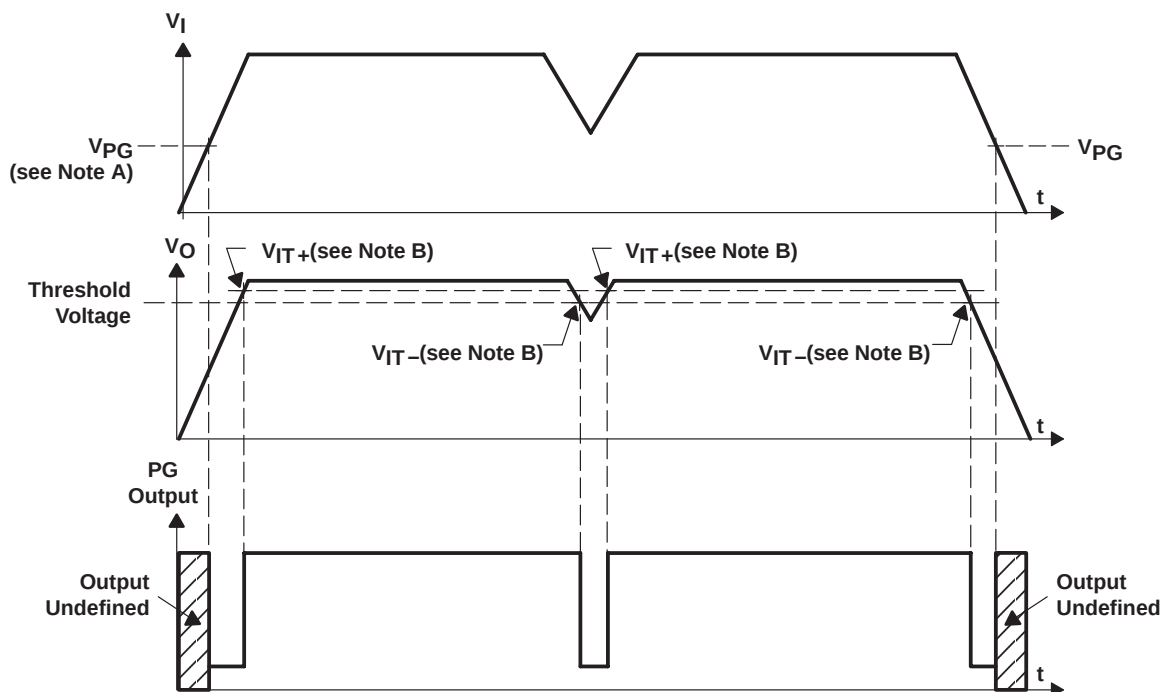
NOTES: A. V_{res} is the minimum input voltage for a valid RESET. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. V_{IT-} Trip voltage is typically 5% lower than the output voltage ($95\%V_O$) V_{IT-} to V_{IT+} is the hysteresis voltage.

**TPS75101-EP, '75115-EP, '75118-EP, '75125-EP, '75133-EP WITH POWER GOOD
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TPS751xxQ PG timing diagram



NOTES: A. V_{PG} is the minimum input voltage for a valid PG. The symbol V_{PG} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. V_{IT-} - Trip voltage is typically 17% lower than the output voltage ($83\%V_O$) V_{IT-} to V_{IT+} is the hysteresis voltage.

**TPS75101-EP, '75115-EP, '75118-EP, '75125-EP, '75133-EP WITH POWER GOOD
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FAST-TRANSIENT-RESPONSE 1.5-A LOW-DROPOUT VOLTAGE REGULATORS**

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absolute maximum ratings over operating junction temperature range (unless otherwise noted)[†]

Input voltage range [‡] , V_I	–0.3 V to 5.5 V
Voltage range at $\overline{EN}$	–0.3 V to 16.5 V
Maximum PG voltage (TPS751xxQ)	16.5 V
Maximum $\overline{RESET}$ voltage (TPS753xxQ)	16.5 V
Peak output current	Internally limited
Continuous total power dissipation	See dissipation rating tables
Output voltage, V_O (OUTPUT, FB)	5.5 V
Operating virtual junction temperature range, T_J	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
ESD rating, HBM	2 kV

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
PWP [§]	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP [¶]	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

[§] This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage (4 in²).

[¶] This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in²) and layers 3 and 6 at 100% coverage (6 in²). For more information, refer to TI technical brief SLMA002.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I [#]	2.7	5	V
Output voltage range, V_O	1.5	5	V
Output current, I_O	0	1.5	A
Operating virtual junction temperature, T_J	–40	125	°C

[#] To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$.



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electrical characteristics over recommended operating junction temperature range ($T_J = -40^{\circ}\text{C}$ to 125°C), $V_I = V_{O(\text{typ})} + 1\text{ V}$, $I_O = 1\text{ mA}$, $\overline{\text{EN}} = 0\text{ V}$, $C_O = 47\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage (see Notes 1 and 3)	Adjustable Voltage	1.5 V ≤ V _O ≤ 5 V, T _J = 25°C		V _O			V
		1.5 V ≤ V _O ≤ 5 V		0.98 V _O 1.02 V _O			
	1.5 V Output	T _J = 25°C, 2.7 V < V _{IN} < 5 V		1.5			
		2.7 V < V _{IN} < 5 V		1.470 1.530			
	1.8 V Output	T _J = 25°C, 2.8 V < V _{IN} < 5 V		1.8			
		2.8 V < V _{IN} < 5 V		1.764 1.836			
	2.5 V Output	T _J = 25°C, 3.5 V < V _{IN} < 5 V		2.5			
		3.5 V < V _{IN} < 5 V		2.450 2.550			
3.3 V Output	T _J = 25°C, 4.3 V < V _{IN} < 5 V		3.3				
	4.3 V < V _{IN} < 5 V		3.234 3.366				
Quiescent current (GND current) (see Note 2)		T _J = 25°C, See Note 3		75			μA
		See Note 3		125			
Output voltage line regulation (ΔV _O /V _O) (see Notes 1 and 2) Output voltage line regulation (ΔV _O /V _O) (see Notes 1 and 2)		V _O + 1 V < V _I ≤ 5 V, T _J = 25°C		0.01			%V
		V _O + 1 V < V _I < 5 V		0.1			
Load regulation (see Note 3)				1			mV
Output noise voltage		BW = 300 Hz to 50 kHz, V _O = 1.5 V C _O = 100 μF, T _J = 25°C		60			μVrms
Output current Limit		V _O = 0 V		3.3 4.5			A
Thermal shutdown junction temperature				150			°C
Standby current		EN = V _I , T _J = 25°C,		1			μA
		EN = V _I		10			μA
FB input current	TPS75x01Q	FB = 1.5 V		-1 1			μA
High level enable input voltage				2			V
Low level enable input voltage				0.7			V
Power supply ripple rejection (see Note 2)		f = 100 Hz, T _J = 25°C, C _O = 100 μF, See Note 1, I _O = 1.5 A		63			dB
PG (TPS751xxQ)	Minimum input voltage for valid PG	I _O (PG) = 300μA, V(PG) ≤ 0.8 V		1 1.3			V
	Trip threshold voltage	V _O decreasing		80 86			%V _O
	Hysteresis voltage	Measured at V _O		0.5			%V _O
	Output low voltage	V _I = 2.7 V, I _O (PG) = 1mA		0.15 0.4			V
	Leakage current	V(PG) = 5 V		1			μA

NOTES: 1. Minimum IN operating voltage is 2.7 V or $V_{O(\text{typ})} + 1\text{ V}$, whichever is greater. Maximum IN voltage 5 V .

2. If $V_O \leq 1.8\text{ V}$ then $V_{\text{imin}} = 2.7\text{ V}$, $V_{\text{imax}} = 5\text{ V}$:

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O(V_{\text{imax}} - 2.7\text{ V})}{100} \times 1000$$

If $V_O \geq 2.5\text{ V}$ then $V_{\text{imin}} = V_O + 1\text{ V}$, $V_{\text{imax}} = 5\text{ V}$:

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O(V_{\text{imax}} - (V_O + 1\text{ V}))}{100} \times 1000$$

3. $I_O = 1\text{ mA}$ to 1.5 A



**TPS75101-EP, '75115-EP, '75118-EP, '75125-EP, '75133-EP WITH POWER GOOD
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electrical characteristics over recommended operating junction temperature range ($T_J = -40^{\circ}\text{C}$ to 125°C), $V_I = V_{O(\text{typ})} + 1\text{ V}$, $I_O = 1\text{ mA}$, $\overline{\text{EN}} = 0\text{ V}$, $C_O = 47\text{ }\mu\text{F}$ (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reset (TPS753xxQ)	Minimum input voltage for valid $\overline{\text{RESET}}$	$I_{O(\text{RESET})} = 300\text{ }\mu\text{A}$, $V_{(\text{RESET})} \leq 0.8\text{ V}$		1.1	1.3	V
	Trip threshold voltage	V_O decreasing	92		98	% V_O
	Hysteresis voltage	Measured at V_O		0.5		% V_O
	Output low voltage	$I_{O(\text{RESET})} = 1\text{ mA}$		0.15	0.4	V
	Leakage current	$V_{(\text{RESET})} = 5.5\text{ V}$			1	μA
	RESET time-out delay			100		ms
Input current ($\overline{\text{EN}}$)		$\overline{\text{EN}} = V_I$	-1		1	μA
		$\overline{\text{EN}} = 0\text{ V}$	-1	0	1	μA
High level $\overline{\text{EN}}$ input voltage			2			V
Low level $\overline{\text{EN}}$ input voltage					0.7	V
Dropout voltage, (3.3 V output) (see Note 4)		$I_O = 1.5\text{ A}$, $T_J = 25^{\circ}\text{C}$		160		mV
		$I_O = 1.5\text{ A}$, $V_I = 3.2\text{ V}$			300	

NOTE 4: V_{IN} voltage equals $V_{O(\text{Typ})} - 100\text{ mV}$; TPS75x15Q, TPS75x18Q and TPS75x25Q dropout voltage limited by input voltage range limitations (i.e., TPS75x33Q input voltage needs to drop to 3.2 V for purpose of this test).

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	2, 3
		vs Junction temperature	4, 5
	Ground current	vs Junction temperature	6
	Power supply ripple rejection	vs Frequency	7
	Output spectral noise density	vs Frequency	8
Z_O	Output impedance	vs Frequency	9
V_{DO}	Dropout voltage	vs Input voltage	10
		vs Junction temperature	11
	Input voltage (min)	vs Output voltage	12
	Line transient response		13, 15
	Load transient response		14, 16
V_O	Output voltage	vs Time	17
	Equivalent series resistance (ESR)	vs Output current	19, 20

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TYPICAL CHARACTERISTICS

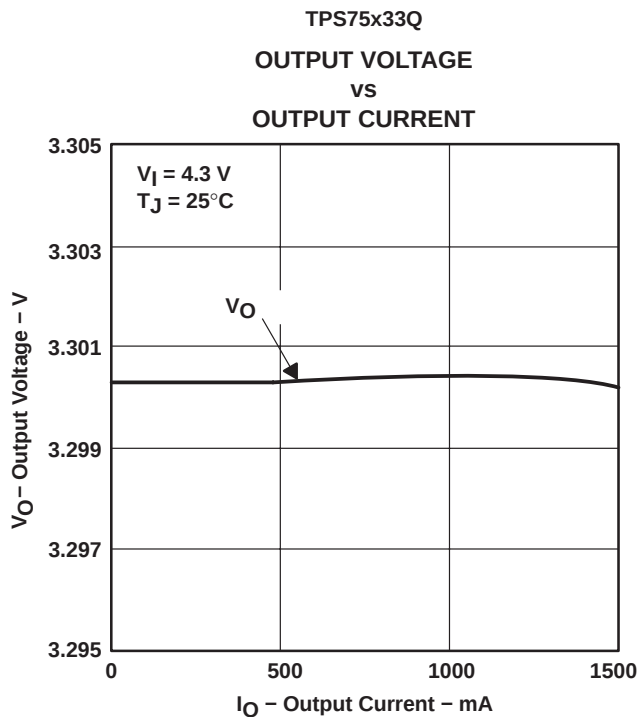


Figure 2

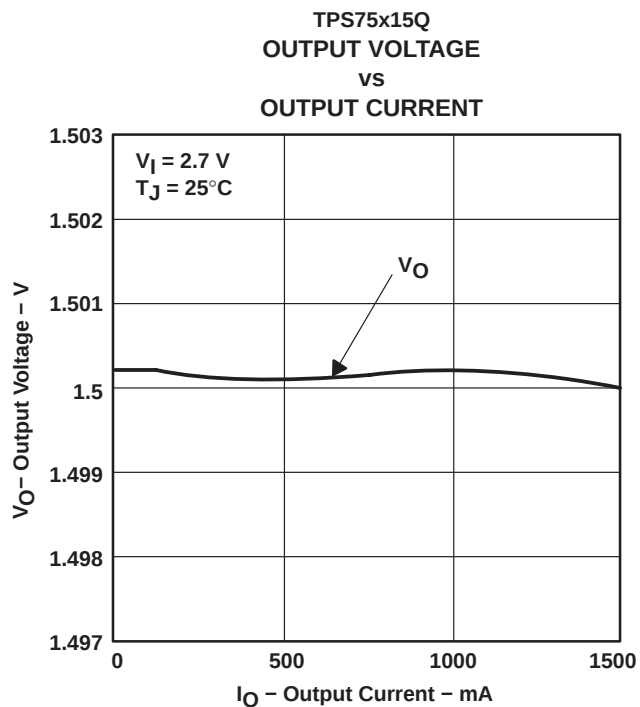


Figure 3

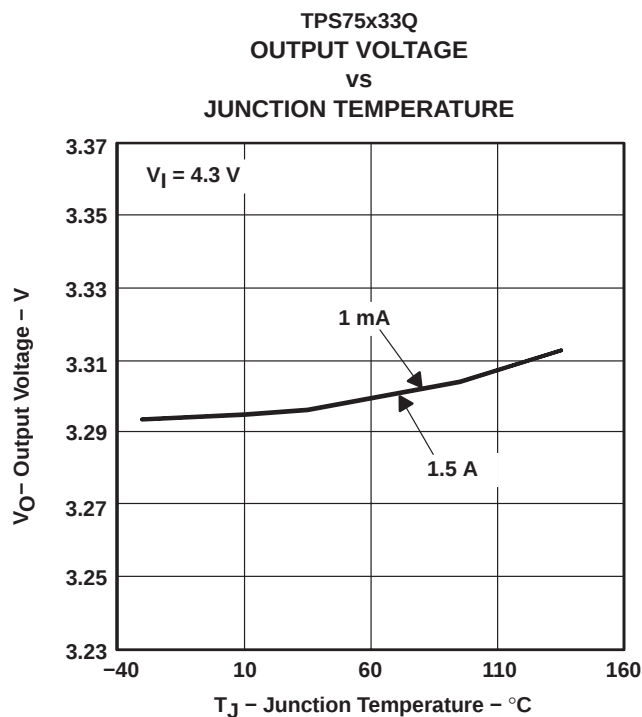


Figure 4

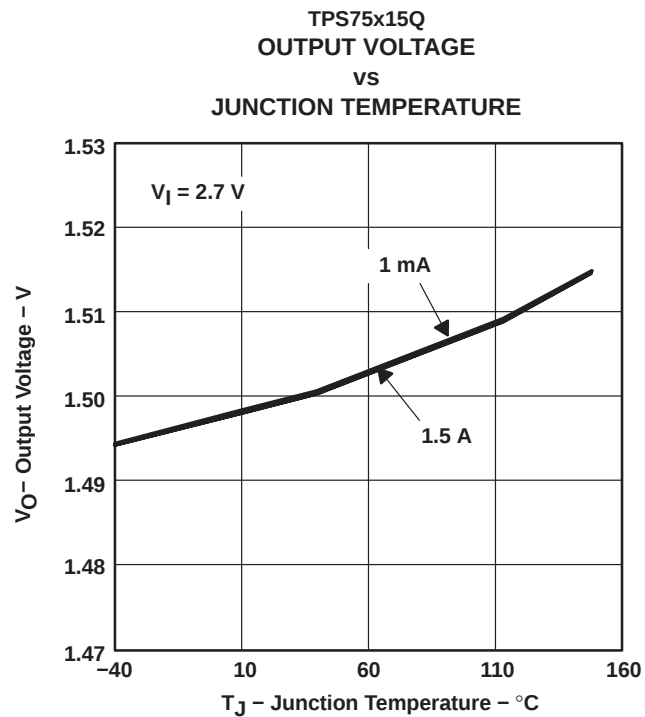


Figure 5

TYPICAL CHARACTERISTICS

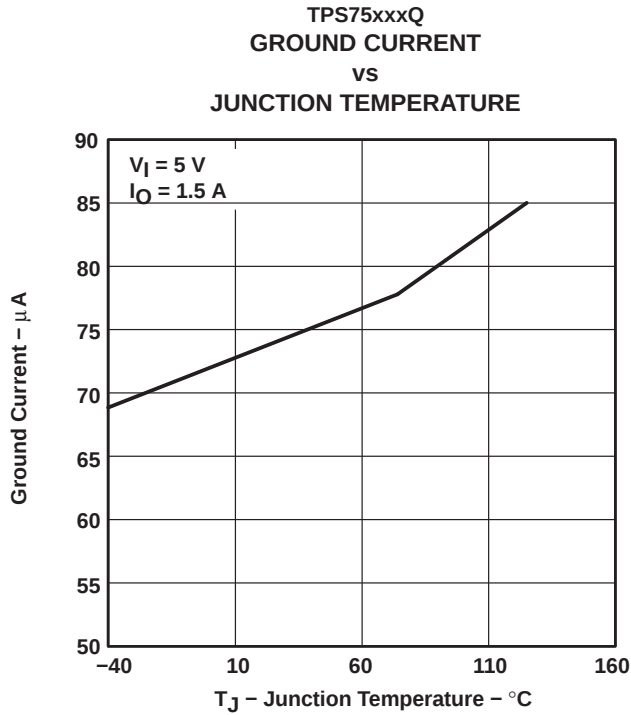


Figure 6

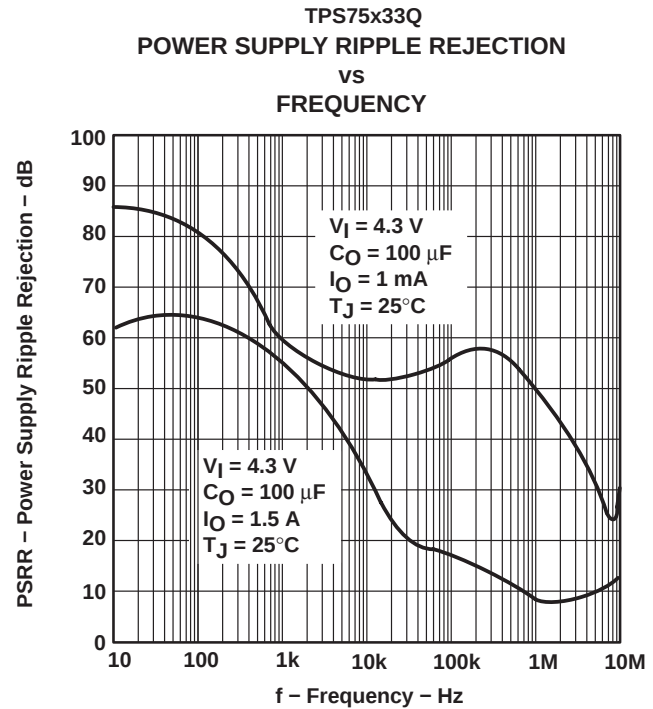


Figure 7

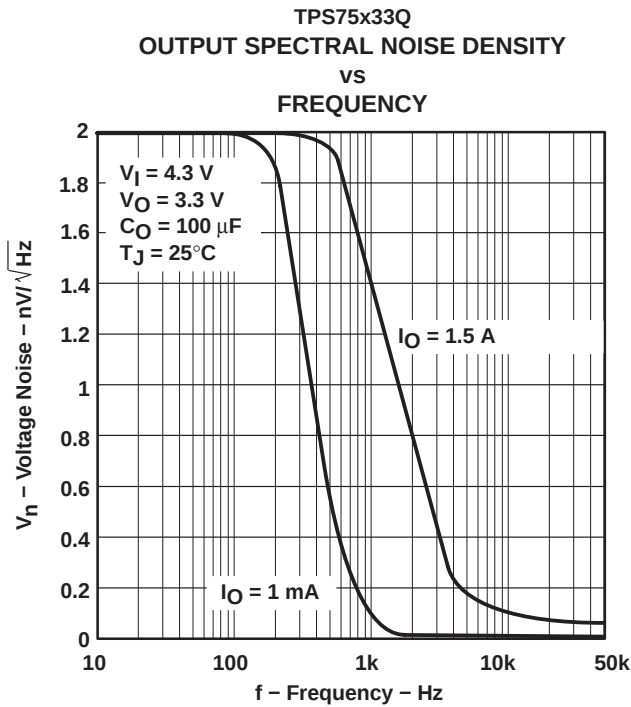


Figure 8

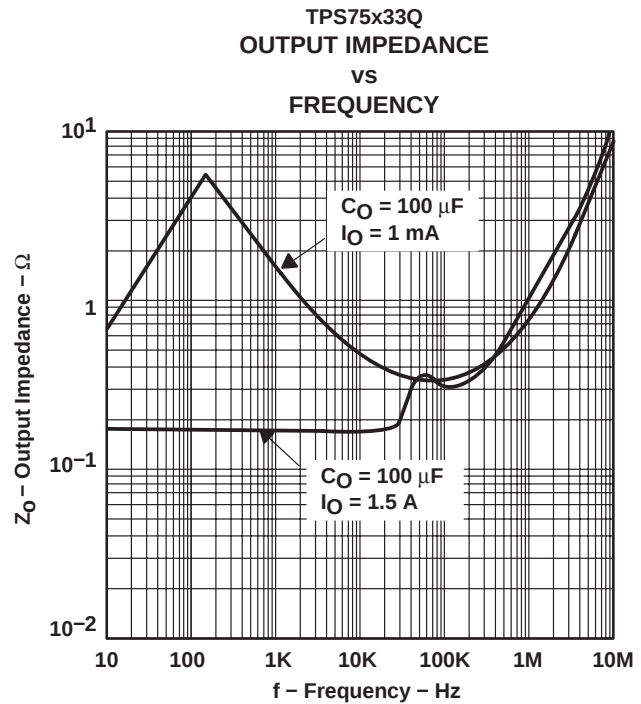


Figure 9

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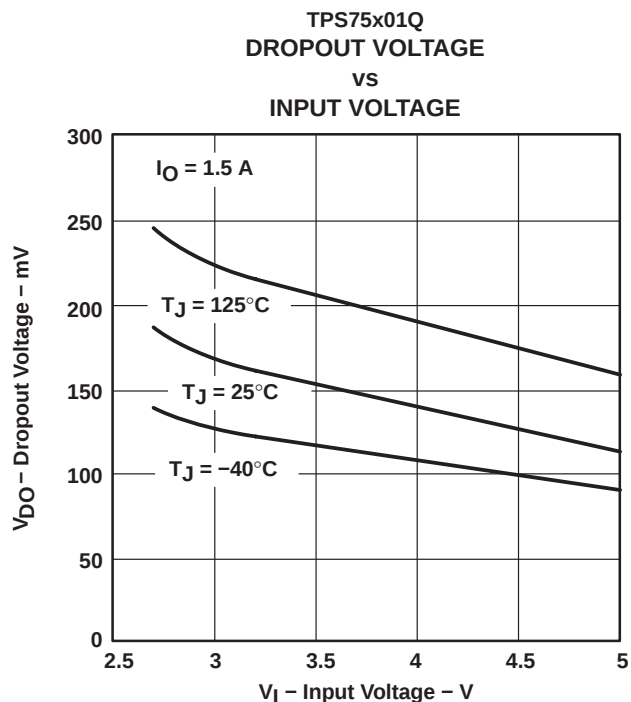


Figure 10

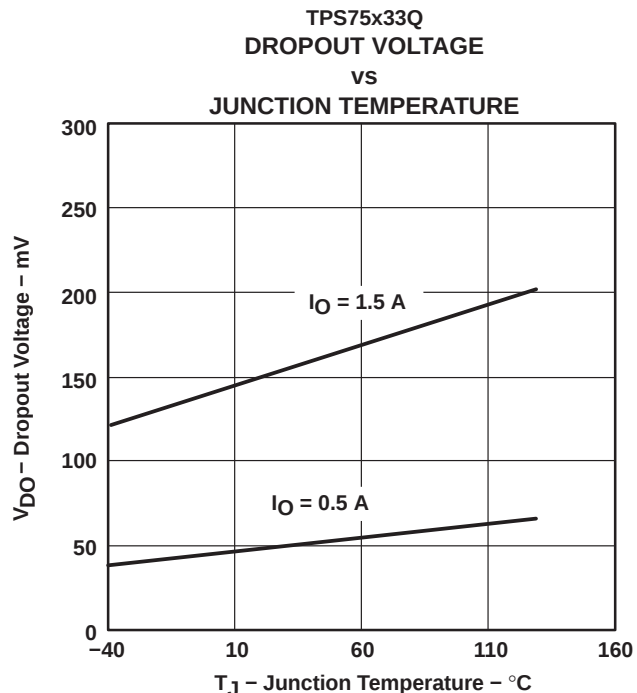


Figure 11

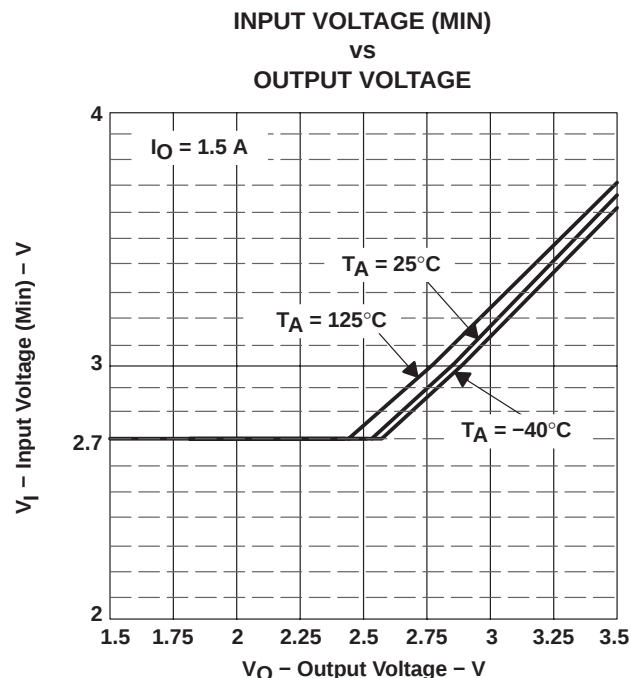


Figure 12

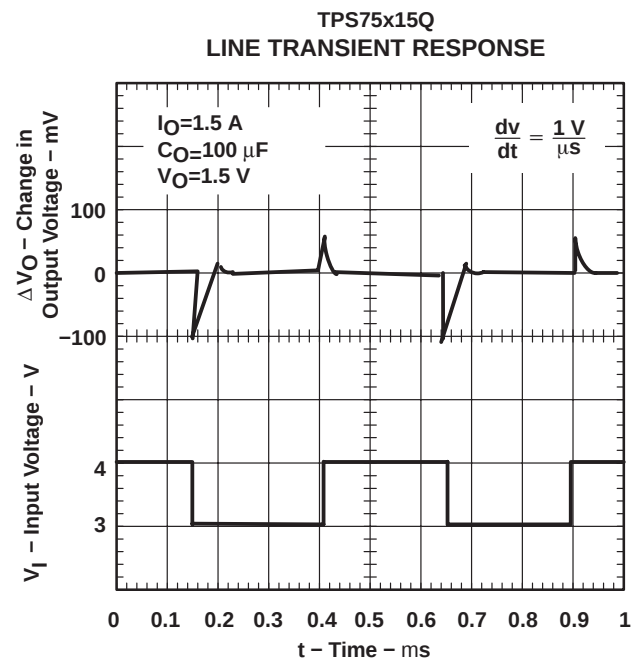


Figure 13

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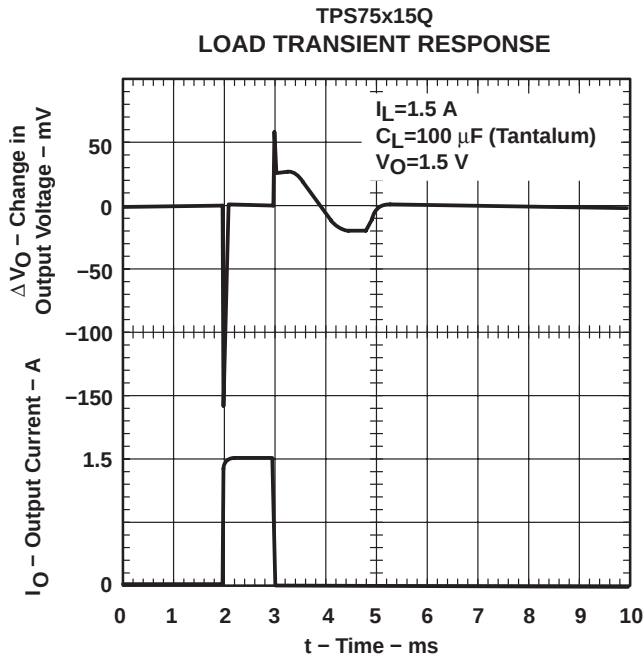


Figure 14

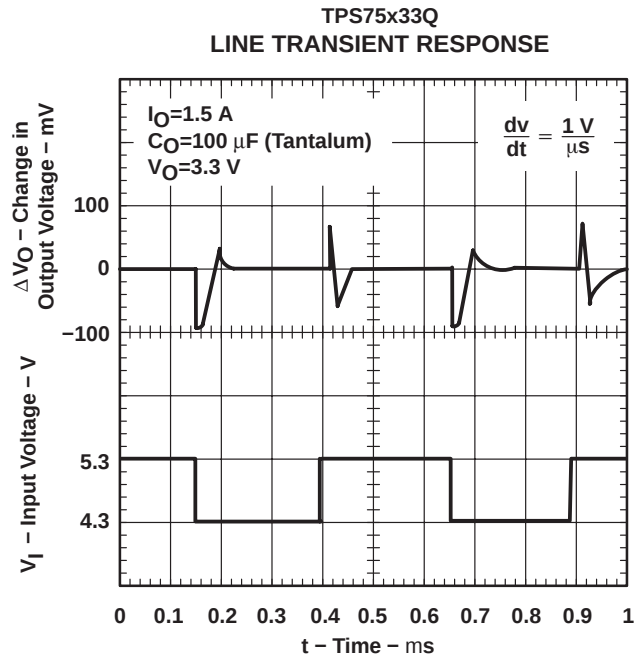


Figure 15

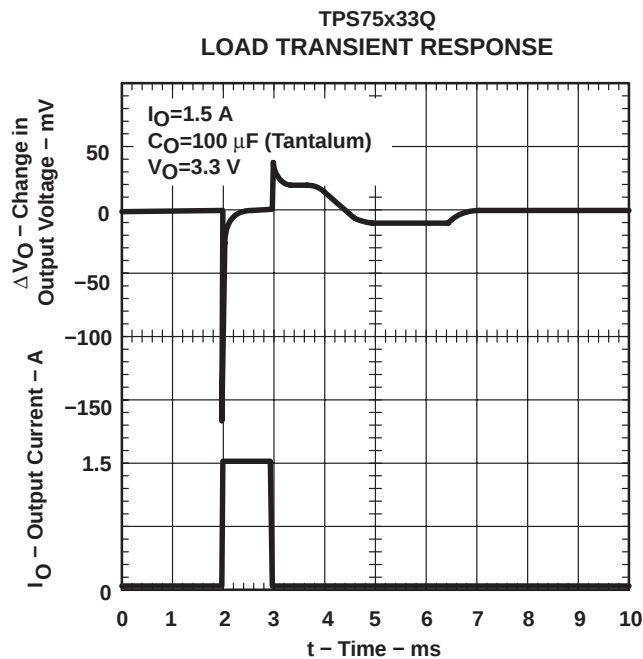


Figure 16

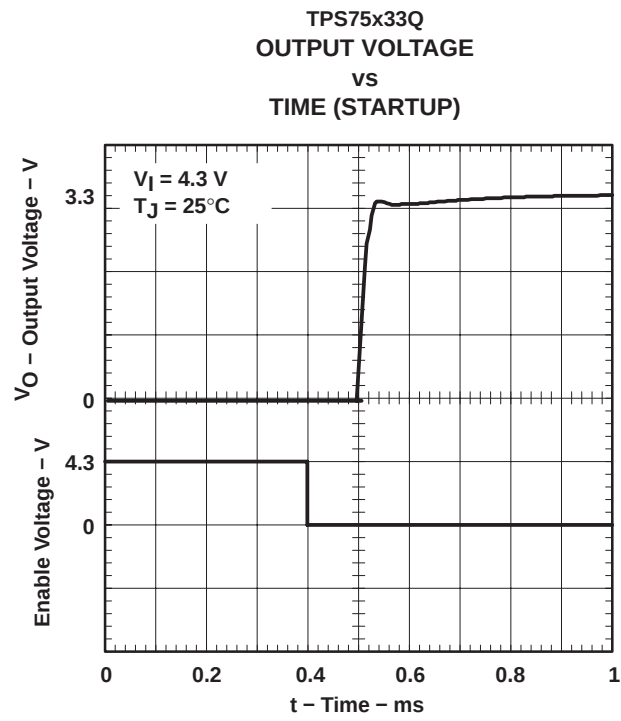


Figure 17

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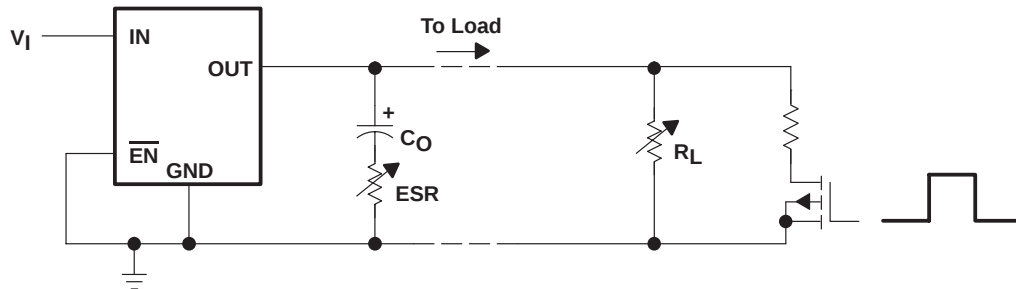


Figure 18. Test Circuit for Typical Regions of Stability (Figures 19 and 20) (Fixed Output Options)

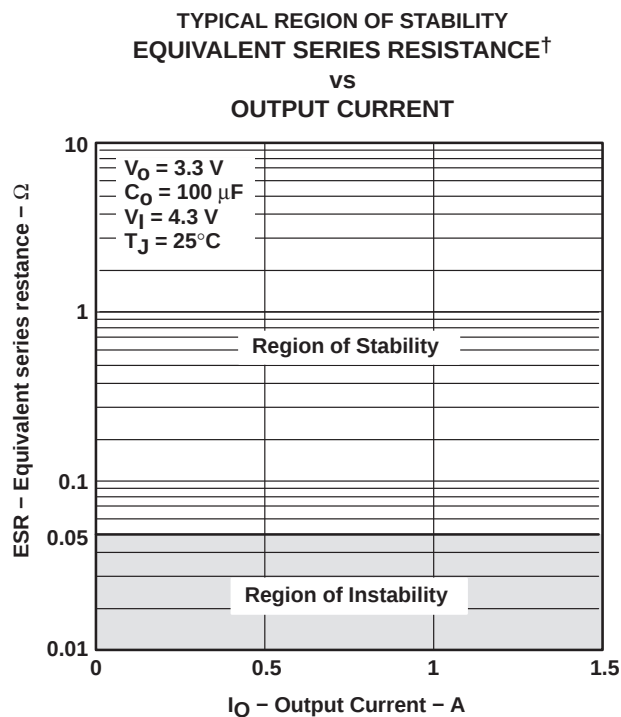


Figure 19

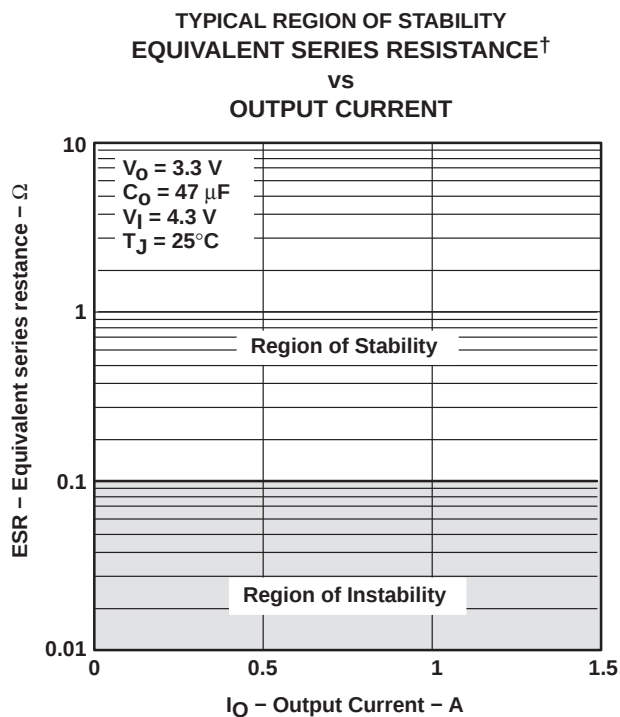


Figure 20

[†] Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

APPLICATION INFORMATION

The TPS751xxQ or TPS753xxQ family includes four fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V and 3.3 V), and an adjustable regulator, the TPS75x01Q (adjustable from 1.5 V to 5 V).

minimum load requirements

The TPS751xxQ and TPS753xxQ families are stable even at no load; no minimum load is required for operation.

pin functions

enable ($\overline{\text{EN}}$)

The $\overline{\text{EN}}$ terminal is an input which enables or shuts down the device. If $\overline{\text{EN}}$ is a logic high, the device will be in shutdown mode. When $\overline{\text{EN}}$ goes to logic low, then the device will be enabled.

power-good (PG) (TPS751xxQ)

The PG terminal is an open drain, active high output that indicates the status of V_O (output of the LDO). When V_O reaches 83% of the regulated voltage, PG will go to a high impedance state. It will go to a low-impedance state when V_O falls below 83% (i.e. over load condition) of the regulated voltage. The open drain output of the PG terminal requires a pullup resistor.

sense (SENSE)

The SENSE terminal of the fixed-output options must be connected to the regulator output, and the connection should be as short as possible. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. It is essential to route the SENSE connection in such a way to minimize/avoid noise pickup. Adding RC networks between the SENSE terminal and V_O to filter noise is not recommended because it may cause the regulator to oscillate.

feedback (FB)

FB is an input terminal used for the adjustable-output options and must be connected to an external feedback resistor divider. The FB connection should be as short as possible. It is essential to route it in such a way to minimize/avoid noise pickup. Adding RC networks between FB terminal and V_O to filter noise is not recommended because it may cause the regulator to oscillate.

reset ($\overline{\text{RESET}}$) (TPS753xxQ)

The $\overline{\text{RESET}}$ terminal is an open drain, active low output that indicates the status of V_O . When V_O reaches 95% of the regulated voltage, $\overline{\text{RESET}}$ will go to a low-impedance state after a 100-ms delay. $\overline{\text{RESET}}$ will go to a high-impedance state when V_O is below 95% of the regulated voltage. The open-drain output of the $\overline{\text{RESET}}$ terminal requires a pullup resistor.

GND/HEATSINK

All GND/HEATSINK terminals are connected directly to the mount pad for thermal-enhanced operation. These terminals could be connected to GND or left floating.

input capacitor

For a typical application, an input bypass capacitor (0.22 μF – 1 μF) is recommended for device stability. This capacitor should be as close to the input pins as possible. For fast transient condition where droop at the input of the LDO may occur due to high inrush current, it is recommended to place a larger capacitor at the input as well. The size of this capacitor is dependant on the output current and response time of the main power supply, as well as the distance to the load (LDO).

TPS75101-EP, '75115-EP, '75118-EP, '75125-EP, '75133-EP WITH POWER GOOD TPS75301-EP, TPS75315-EP, TPS75318-EP, TPS75325-EP, TPS75333-EP WITH RESET FAST-TRANSIENT-RESPONSE 1.5-A LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

output capacitor

As with most LDO regulators, the TPS751xxQ and TPS753xxQ require an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 47 μF and the ESR (equivalent series resistance) must be between 100 m Ω and 10 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described in this section. Larger capacitors provide a wider range of stability and better load transient response.

This information, along with the ESR graphs, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet these guidelines.

ESR and transient response

LDOs typically require an external output capacitor for stability. In fast transient response applications, capacitors are used to support the load current while LDO amplifier is responding. In most applications, one capacitor is used to support both functions.

Besides its capacitance, every capacitor also contains parasitic impedances. These parasitic impedances are resistive as well as inductive. The resistive impedance is called equivalent series resistance (ESR), and the inductive impedance is called equivalent series inductance (ESL). The equivalent schematic diagram of any capacitor can therefore be drawn as shown in Figure 21.



Figure 21. – ESR and ESL

APPLICATION INFORMATION

In most cases one can neglect the effect of inductive impedance ESL. Therefore, the following application focuses mainly on the parasitic resistance ESR.

Figure 22 shows the output capacitor and its parasitic impedances in a typical LDO output stage.

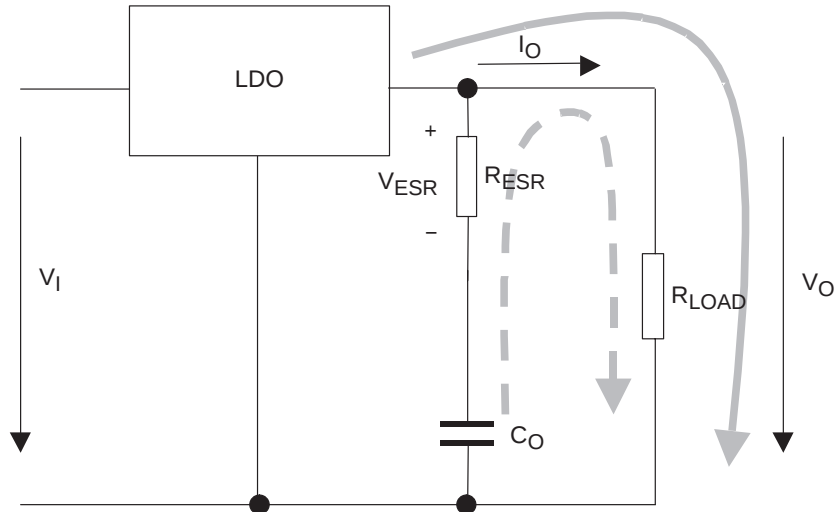


Figure 22. LDO Output Stage With Parasitic Resistances ESR and ESL

In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage ($V(C_O) = V_O$). This means no current is flowing into the C_O branch. If I_O suddenly increases (transient condition), the following occurs:

- The LDO is not able to supply the sudden current need due to its response time (t_1 in Figure 23). Therefore, capacitor C_O provides the current for the new load condition (dashed arrow). C_O now acts like a battery with an internal resistance, ESR. Depending on the current demand at the output, a voltage drop will occur at R_{ESR} . This voltage is shown as V_{ESR} in Figure 22.
- When C_O is conducting current to the load, initial voltage at the load will be $V_O = V(C_O) - V_{ESR}$. Due to the discharge of C_O , the output voltage V_O will drop continuously until the response time t_1 of the LDO is reached and the LDO will resume supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as t_2 in Figure 23.

Figure 23 also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs where number 1 displays the lowest and number 3 displays the highest ESR.

From above, the following conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the bigger the voltage droop during the LDO response period.

APPLICATION INFORMATION

conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output voltage requirement.

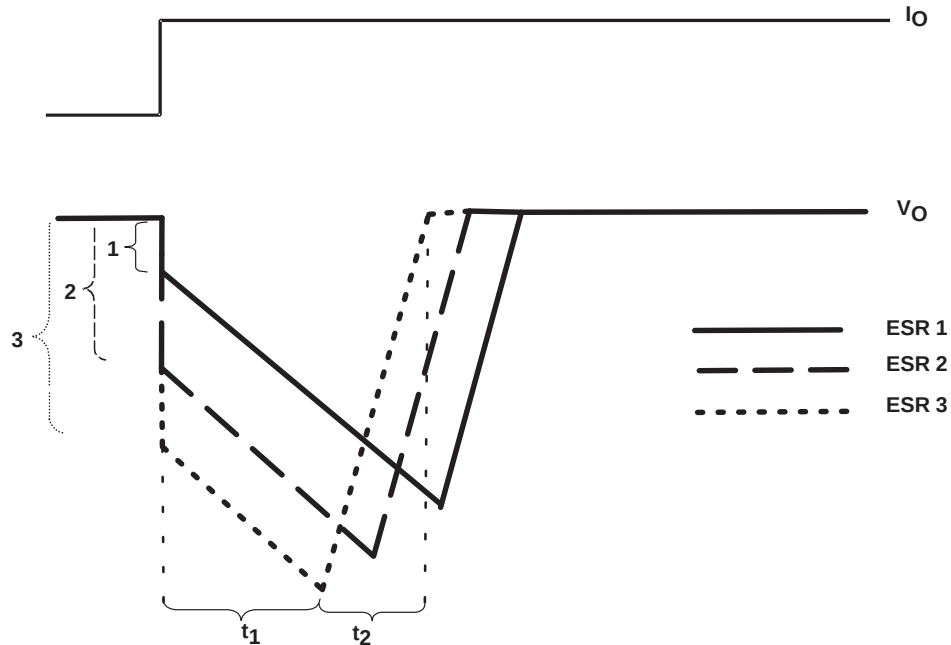


Figure 23. Correlation of Different ESRs and Their Influence to the Regulation of V_O at a Load Step From Low-to-High Output Current

APPLICATION INFORMATION

programming the TPS75x01Q adjustable LDO regulator

The output voltage of the TPS75x01Q adjustable regulator is programmed using an external resistor divider as shown in Figure 24. The output voltage is calculated using:

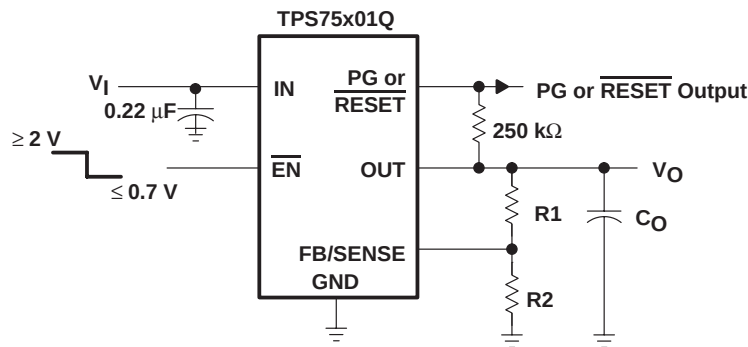
$$V_O = V_{\text{ref}} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Where:

$V_{\text{ref}} = 1.1834 \text{ V typ}$ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 40- μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose $R_2 = 30.1 \text{ k}\Omega$ to set the divider current at 40 μA and then calculate R1 using:

$$R_1 = \left(\frac{V_O}{V_{\text{ref}}} - 1\right) \times R_2 \quad (2)$$



OUTPUT VOLTAGE
PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	33.2	30.1	k Ω
3.3 V	53.6	30.1	k Ω
3.6 V	61.9	30.1	k Ω

NOTE: To reduce noise and prevent oscillation, R1 and R2 need to be as close as possible to the FB/SENSE terminal.

Figure 24. TPS75x01Q Adjustable LDO Regulator Programming

**TPS75101-EP, '75115-EP, '75118-EP, '75125-EP, '75133-EP WITH POWER GOOD
TPS75301-EP, TPS75315-EP, TPS75318-EP, TPS75325-EP, TPS75333-EP WITH RESET
FAST-TRANSIENT-RESPONSE 1.5-A LOW-DROPOUT VOLTAGE REGULATORS**

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APPLICATION INFORMATION

regulator protection

The TPS751xxQ or TPS753xxQ PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS751xxQ or TPS753xxQ also features internal current limiting and thermal protection. During normal operation, the TPS751xxQ or TPS753xxQ limits output current to approximately 3.3 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}} \quad (3)$$

Where:

T_{Jmax} is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 34.6°C/W for the 20-terminal PWP with no airflow (see Table 1).

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O \quad (4)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

THERMAL INFORMATION

thermally enhanced TSSOP-20 (PWP – PowerPad™)

The thermally enhanced PWP package is based on the 20-pin TSSOP, but includes a thermal pad [see Figure 25(c)] to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

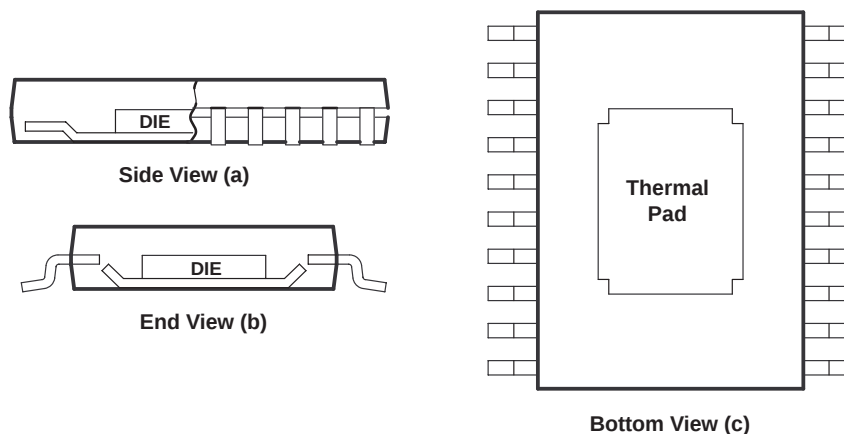


Figure 25. Views of Thermally Enhanced PWP Package

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heat-sink surface), which is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air (reference Figure 27(a), 8 cm² of copper heat sink and natural convection). Increasing the heat-sink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly (see Figures 26 and 27). The line drawn at 0.3 cm² in Figures 26 and 27 indicates performance at the minimum recommended heat-sink size, illustrated in Figure 29.

**TPS75101-EP, '75115-EP, '75118-EP, '75125-EP, '75133-EP WITH POWER GOOD
TPS75301-EP, TPS75315-EP, TPS75318-EP, TPS75325-EP, TPS75333-EP WITH RESET
FAST-TRANSIENT-RESPONSE 1.5-A LOW-DROPOUT VOLTAGE REGULATORS**

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THERMAL INFORMATION

thermally enhanced TSSOP-20 (PWP – PowerPad™) (continued)

The thermal pad is directly connected to the substrate of the IC, which for the TPS751xxQPWP and TPS753XXQPWP series is a secondary electrical connection to device ground. The heat-sink surface that is added to the PWP can be a ground plane or left electrically isolated. In TO220-type surface-mount packages, the thermal connection is also the primary electrical connection for a given terminal which is not always ground. The PWP package provides up to 16 independent leads that can be used as inputs and outputs (Note: leads 1, 10, 11, and 20 are internally connected to the thermal pad and the IC substrate).

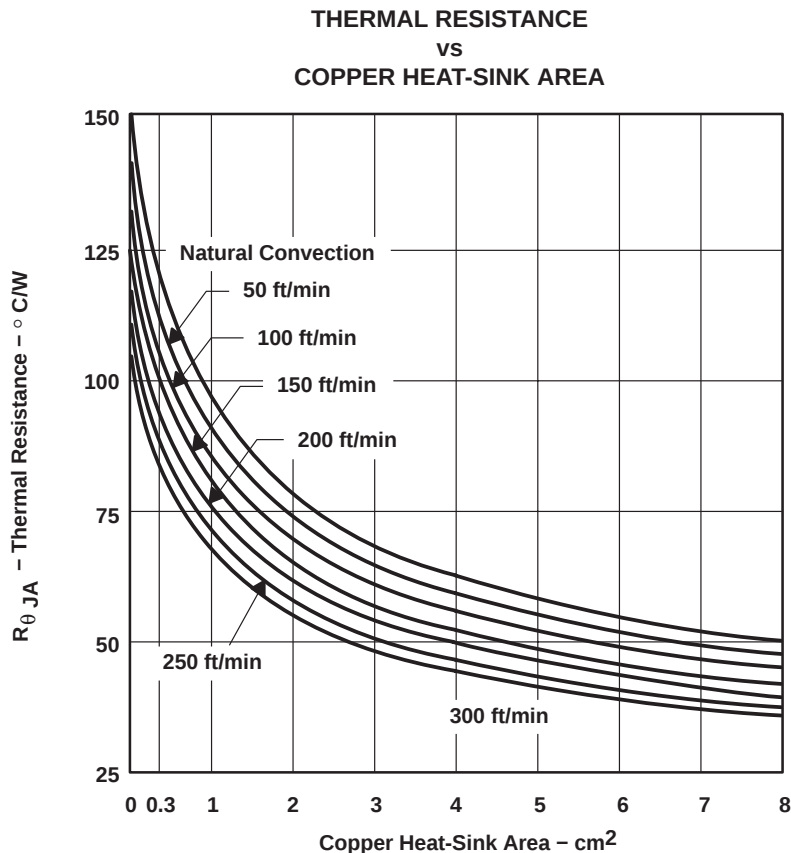


Figure 26

THERMAL INFORMATION

thermally enhanced TSSOP-20 (PWP – PowerPad™) (continued)

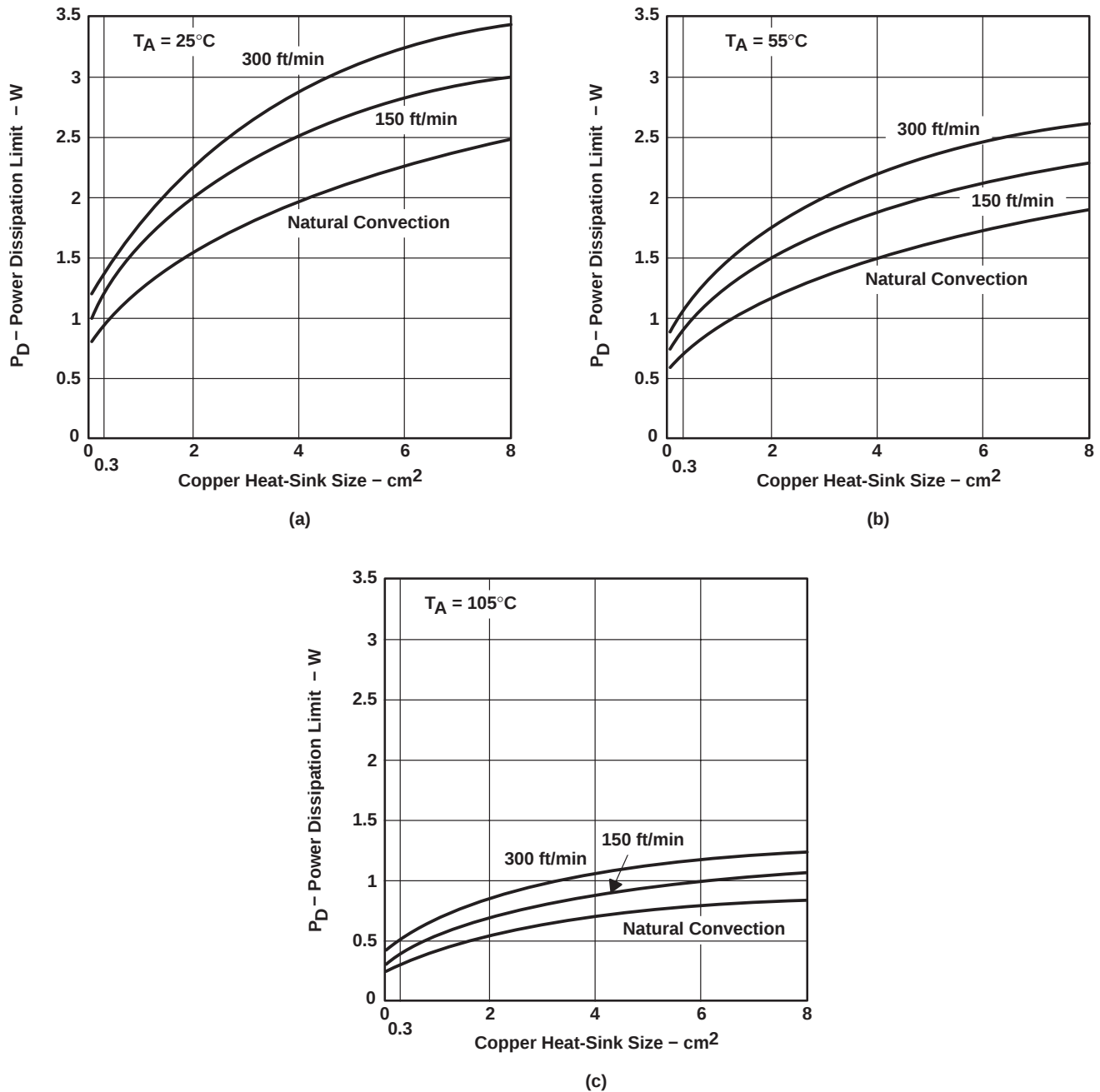


Figure 27. Power Ratings of the PWP Package at Ambient Temperatures of 25°C , 55°C , and 105°C

THERMAL INFORMATION

thermally enhanced TSSOP-20 (PWP – PowerPad™) (continued)

Figure 28 is an example of a thermally enhanced PWB layout for use with the new PWP package. This board configuration was used in the thermal experiments that generated the power ratings shown in Figure 26 and Figure 27. As discussed earlier, copper has been added on the PWB to conduct heat away from the device. $R_{\theta JA}$ for this assembly is illustrated in Figure 26 as a function of heat-sink area. A family of curves is included to illustrate the effect of airflow introduced into the system.

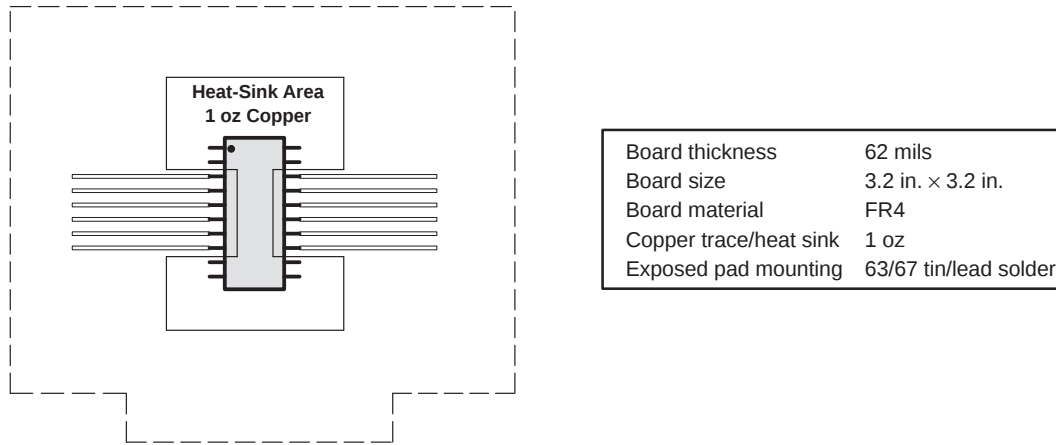


Figure 28. PWB Layout (Including Copper Heatsink Area) for Thermally Enhanced PWP Package

From Figure 26, $R_{\theta JA}$ for a PWB assembly can be determined and used to calculate the maximum power-dissipation limit for the component/PWB assembly, with the equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA(system)}} \quad (5)$$

Where:

T_{Jmax} is the maximum specified junction temperature (150°C absolute maximum limit, 125°C recommended operating limit) and T_A is the ambient temperature.

$P_{D(max)}$ should then be applied to the internal power dissipated by the TPS75133QPWP regulator. The equation for calculating total internal power dissipation of the TPS75133QPWP is:

$$P_{D(total)} = (V_I - V_O) \times I_O + V_I \times I_Q \quad (6)$$

Since the quiescent current of the TPS75133QPWP is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = (V_I - V_O) \times I_O \quad (7)$$

For the case where $T_A = 55^\circ\text{C}$, airflow = 200 ft/min, copper heat-sink area = 4 cm², the maximum power-dissipation limit can be calculated. First, from Figure 26, we find the system $R_{\theta JA}$ is 50°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA(system)}} = \frac{125^\circ\text{C} - 55^\circ\text{C}}{50^\circ\text{C/W}} = 1.4 \text{ W} \quad (8)$$

THERMAL INFORMATION

thermally enhanced TSSOP-20 (PWP – PowerPad™) (continued)

If the system implements a TPS75133QPWP regulator, where $V_I = 5\text{ V}$ and $I_O = 800\text{ mA}$, the internal power dissipation is:

$$P_{D(\text{total})} = (V_I - V_O) \times I_O = (5 - 3.3) \times 0.8 = 1.36\text{ W} \quad (9)$$

Comparing $P_{D(\text{total})}$ with $P_{D(\text{max})}$ reveals that the power dissipation in this example does not exceed the calculated limit. When it does, one of two corrective actions should be made: raising the power-dissipation limit by increasing the airflow or the heat-sink area, or lowering the internal power dissipation of the regulator by reducing the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

mounting information

The primary requirement is to complete the thermal contact between the thermal pad and the PWB metal. The thermal pad is a solderable surface and is fully intended to be soldered at the time the component is mounted. Although voiding in the thermal-pad solder-connection is not desirable, up to 50% voiding is acceptable. The data included in Figures 26 and 27 is for soldered connections with voiding between 20% and 50%. The thermal analysis shows no significant difference resulting from the variation in voiding percentage.

Figure 29 shows the solder-mask land pattern for the PWP package. The minimum recommended heat-sink area is also illustrated. This is simply a copper plane under the body extent of the package, including metal routed under terminals 1, 10, 11, and 20.

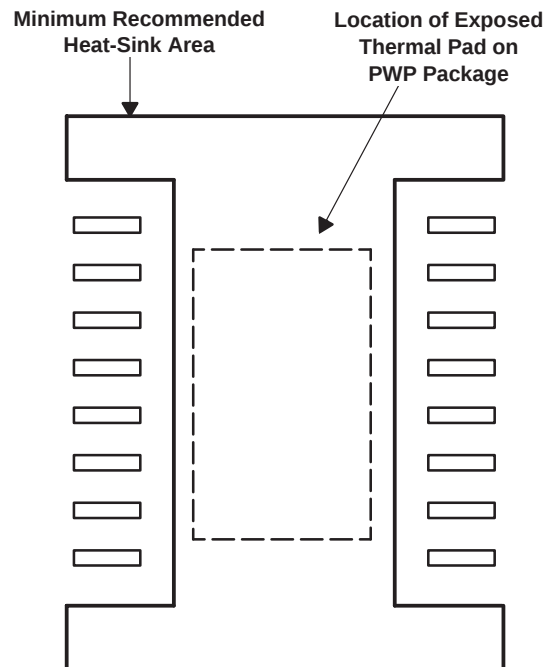


Figure 29. PWP Package Land Pattern

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS75125MPWPREP	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	75125MEP	Samples
TPS75301QPWPREP	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	75301EP	Samples
TPS75318QPWPREP	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	75318EP	Samples
TPS75325QPWPREP	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	75325EP	Samples
TPS75333QPWPREP	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	75333EP	Samples
V62/03636-06XE	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	75301EP	Samples
V62/03636-08XE	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	75318EP	Samples
V62/03636-09XE	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	75325EP	Samples
V62/03636-10XE	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	75333EP	Samples
V62/03636-14XE	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	75125MEP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- ⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- ⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- ⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS75125MPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS75301QPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS75318QPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS75325QPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS75333QPWPREP	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS75125MPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS75301QPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS75318QPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS75325QPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS75333QPWPREP	HTSSOP	PWP	20	2000	350.0	350.0	43.0

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-4/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

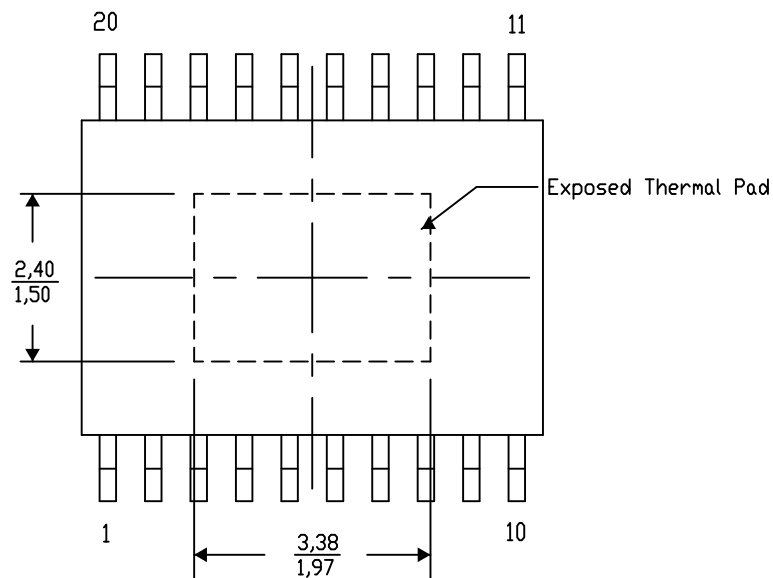
PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

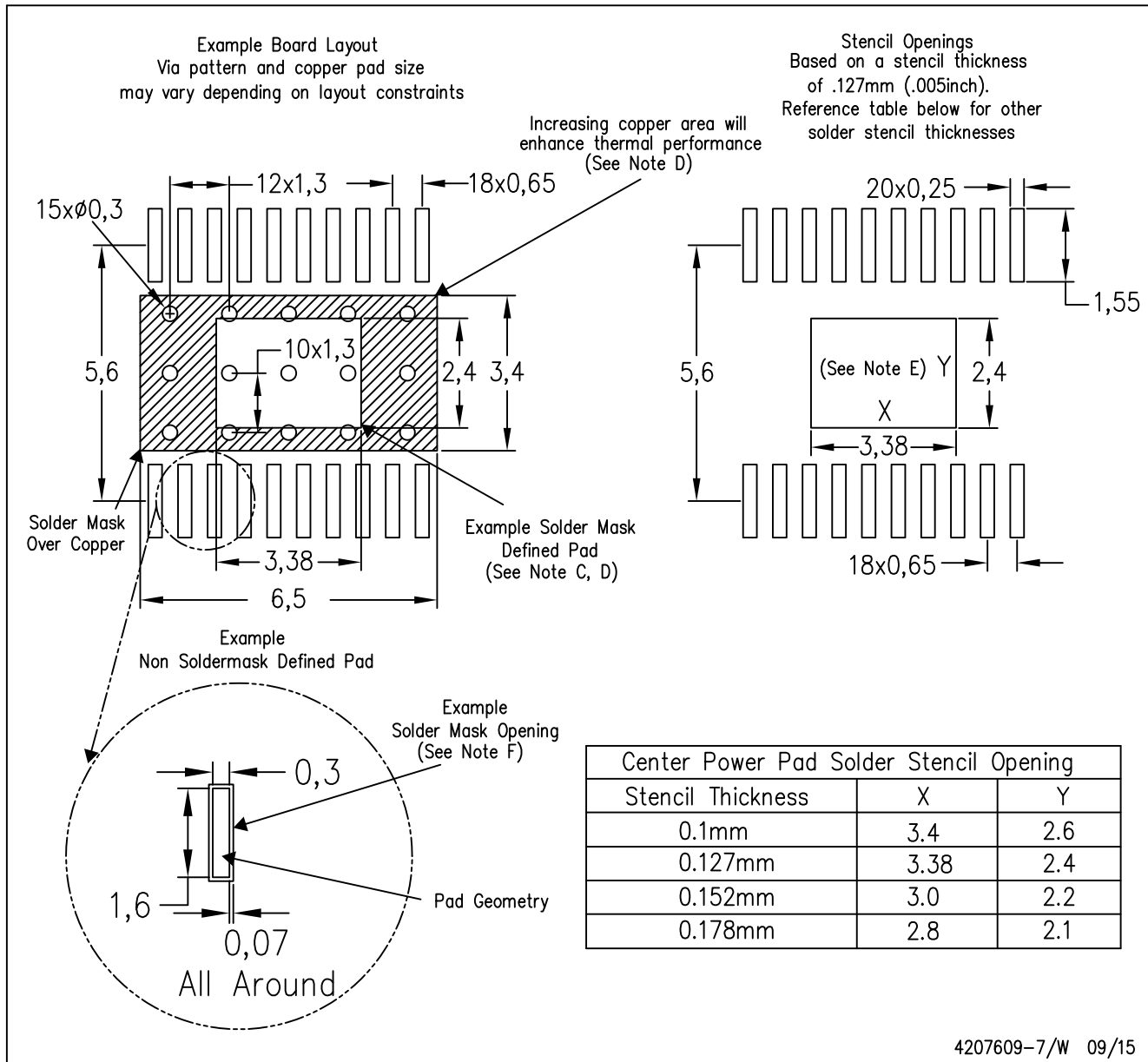


4206332-19/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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