LMK00338EVM

User's Guide

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LMK00338EVM User Guide

This user guide describes how to set up and operate the LMK00338 evaluation module (EVM). The LMK00338 is a 400 MHz, 8-output HCSL clock buffer intended for high frequency, low additive jitter clock distribution and level translation. The EVM allows the user to verify the functionality and performance specifications of the device. Refer to the LMK00338 datasheet for the functional description and specifications.

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1 General Description

2 Features

- Low-noise clock fan-out via two banks of four HCSL outputs and one LVCMOS output
- 3:1 input multiplexer with two universal input buffers and one crystal oscillator interface
- DIP switch control of device configuration
- 3.3 V core and 3 independent 3.3 V/2.5 V output supplies (one per output bank) using external supply inputs or optional LP3878-ADJ LDO or LMZ10500 switching regulator on board
- AC- or DC-coupled input & output interface with low-skew, controlled-impedance traces and edge SMA connectors

3 Quick Setup

To quickly set up and operate the board with basic equipment, refer to the setup procedure below and test setup shown in Figure 1.

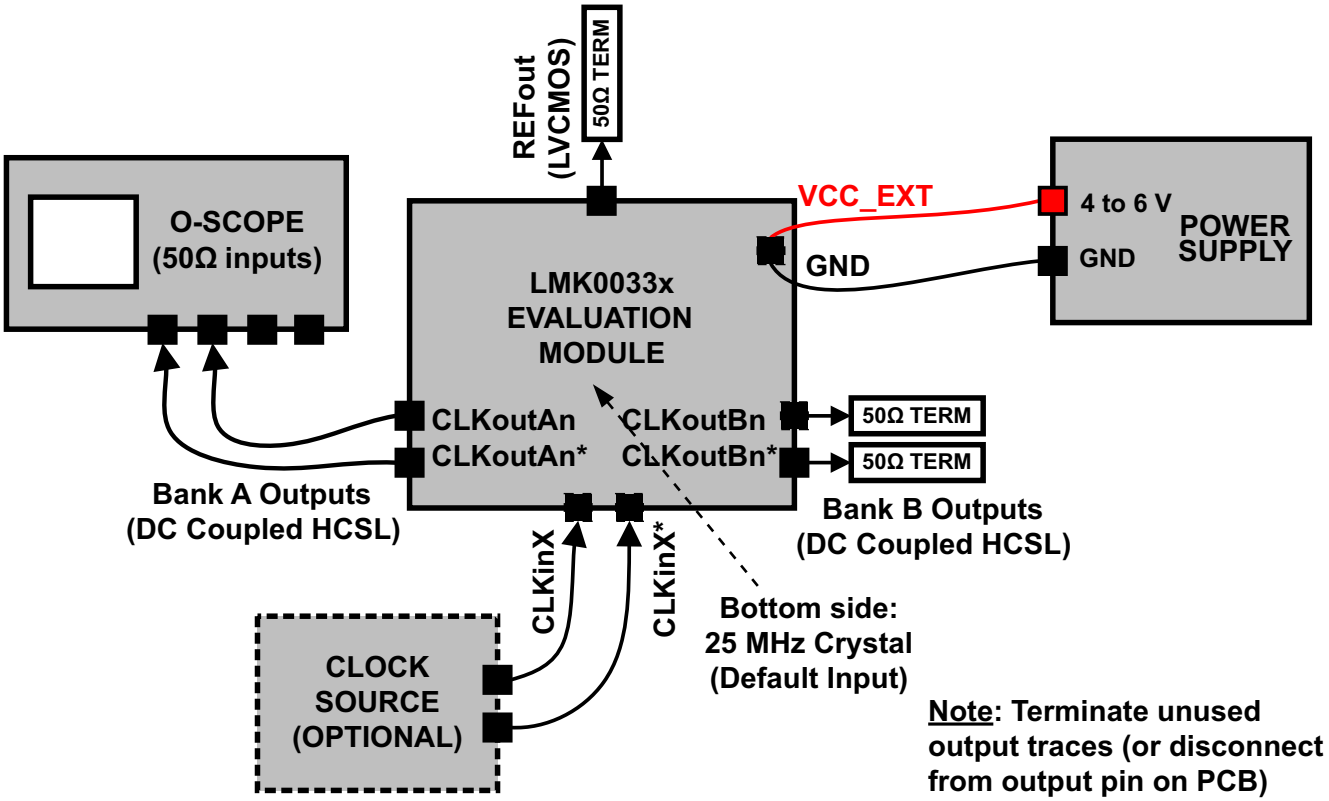


Figure 1. LMK00338 Evaluation Board Quick Start Setup

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Setup Procedure:

1. Verify the output mode control switches, S1[1:5], match the states shown in Table 1 to reflect the default output clock interfaces configured on the EVM.

Table 1. Default Clock Output Modes

SW Position/Name	SW State	Default Clock Output Modes
S1[2] / CLKoutB_A_EN	OFF	Bank A outputs enabled
S1[4] / CLKoutB_B_EN	OFF	Bank B outputs enabled
S1[5] / REFout_EN	ON	REFout (CMOS) enabled

2. Connect a 4 to 6 V power supply to VCC_EXT and GND terminals of the power block labeled J2. This powers the on-board LDO regulator to supply 3.3 V to the VCC and VCCO rails of the IC. Both VCC & VCCO status LEDs should be lit green when ON.
3. Set the desired clock input using the input selection control switches, S1[6:7], as seen in Table 2. The onboard 25 MHz crystal (Y1) can be selected, so an external clock source is not required. A differential clock source can be connected to SMAs labeled CLKin0/0* or CLKin1/1*. By default, these differential inputs are AC coupled and terminated near the device with 100 Ω differential. To configure the EVM for a single-ended input, refer to the Clock Inputs section.

Table 2. Input Selection

Selected Input	Default Input Mode	S1[6] CLKin_Sel1 State	S1[7] CLKin_Sel0 State
CLKin0/0*	Differential clock	OFF	OFF
CLKin1/1*	Differential clock	OFF	ON
OSCin	25 MHz XTAL onboard	ON	Don't care

4. Connect and measure any clock output SMA labeled CLKoutA#/A#*, CLKoutB#/B#*, or REFout to an oscilloscope or other test instrument using SMA cable(s). The output clock will be a level-translated/buffered copy of the selected clock input or crystal oscillator. Note: All output clocks are DC-coupled to the SMA connectors.

   Note: Any active output trace(s) without proper load termination can cause signal reflections on the board, which can couple onto nearby outputs and degrade signal quality and measurement accuracy. To minimize these effects, be sure to properly terminate any unused output trace with a 50 Ω SMA load, or else disconnect any unused output trace from the device output pin by removing the series 0 Ω resistor. An unused output or output bank may also be disabled using the output mode control switch.

4 Signal Path and Control Switches

The LMK00338 supports single-ended or differential clocks on CLKin0 and CLKin1. A third input, OSCin, has an integrated crystal oscillator interface that supports a fundamental mode, AT-cut crystal or an external single-ended clock. To achieve the maximum operating frequency and lowest additive jitter, it is recommended to use a differential input clock with high slew rate (>3 V/ns) on either CLKin0 or CLKin1 port.

The device provides up to 8 HCSL outputs with pin-selectable output enable (HCSL, or Hi-Z). An additional output, REFout, has a fixed LVCMOS buffer with output enable input.

All control pins are configured with the control DIP switch, S1. The input selection logic is shown in Table 2. The output enable selection logic for Bank A and Bank B are shown in Table 1. The REFout enable logic is shown in Table 3.

Table 3. REF out Enable Selection

REFout Enable Mode	S1[5] REFout_EN State
Disabled/Hi-Z	OFF
Enabled	ON

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5 Power Supplies

The power supply section on the EVM provides flexibility to power the device using the onboard regulator(s) or direct supply input(s). A combination of 0 Ω resistor options allows the user to modify the EVM power supply configuration, if desired.

By default, 3.3 V is supplied to both VCC and VCCO rails by the onboard LDO regulator, U3. To power the regulator, connect a 4 V to 6 V input voltage and ground from an external power source to the terminal block, J2, or SMA input labeled VCC_EXT.

To modify the EVM with a different power supply configuration, populate the resistor options as shown in Table 4. Then, apply the appropriate voltage(s) to the EVM power input(s).

If the EVM is configured for dual direct supplies, connect the 3.3 V supply and ground to VCC_EXT and the 2.5 V supply and ground to the SMA input labeled VCCO_EXT.

Decoupling capacitors and 0 Ω resistor footprints, which can accommodate ferrite beads, can be used to isolate the EVM power input(s) from the device power pins.

Table 4. EVM Power Supply Configuration Options

	LP3878 LDO Regulator (U3) 3.3 V (DEFAULT)	LMZ10500 Switcher (U2) 3.3 V	Single Direct Supply 3.3 V	Dual Direct Supplies 3.3 V & 2.5 V
VCC_EXT port (J2 or SMA)	Apply 4 V to 6 V	Apply 4 V to 5.5 V	Apply 3.3 V ± 5%	Apply 3.3 V ± 5%
VCCO_EXT port (SMA)	Not used	Not used	Not used	Apply 2.5 V ± 5%
U2 Vout	Not used	3.3 V (VCC & VCCO)	Not used	Not used
U3 Vout	3.3 V (VCC & VCCO)	Not used	Not used	Not used
R131	OPEN	OPEN	OPEN	0
R132	0	0	0	0
R134	OPEN	0	OPEN	OPEN
R145	OPEN	0	OPEN	OPEN
R153	OPEN	OPEN	0	0
R155	0	OPEN	OPEN	OPEN
R156	0	OPEN	OPEN	OPEN

5.1 Independent Output Supply Voltages

On the bottom side of the EVM, resistor options provide flexibility to power each of the three individual output supply pins (VCCOA, VCCOB, and VCCOC) from either VCC or VCCO rail. This is useful when 3.3 V and 2.5 V are both needed for separate output supplies.

The EVM power supply needs to be modified to get 2.5 V on the VCCO rail, either using the VCCO_EXT input or LMZ10500 switcher, as seen in Table 4. To configure LMZ10500 with 2.5 V output, set R138 to 150k and R139 to 118k.

Note: When the LMZ10500 switcher is used to power the DUT and an ultra-low-noise clock source is used, the higher output noise voltage of the switcher (compared to the LP3878-ADJ) can cause an slight increase in the output phase noise floor at low offset frequencies as well as low-level spurs. The high PSRR of the device helps to minimize supply-induced jitter.

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6 Clock Inputs

The SMA inputs labeled CLKin0 & CLKin0* and CLKin1 & CLKin1* can be configured to receive a differential clock or single-ended clock. Best performance is achieved with a differential input clock, which is the default configuration for both CLKin ports.

Both CLKin0 and CLKin1 paths include footprint options to provide the user with flexibility in configuring the termination, biasing, and coupling for the device inputs.

6.1 Configuring CLKinX+ for a Single Ended Input

To configure an AC-coupled or DC-coupled single-ended clock input on CLKin0, follow the steps below. CLKin1 can be modified similarly.

1. Remove R24 (100 Ω differential termination).
2. Terminate CLKin0 (driven input) by installing 51 Ω on R30.
3. Install 0.1 uF on C10 as a bypass capacitor.
4. Modify for AC or DC coupled input:
   (a) AC-coupled input: Install 0 Ω on R23, so CLKin0* input pin is AC coupled to ground via C17.
   (b) DC-coupled input:
      (i) Replace R22 and R28 with 0 Ω to DC couple the input path.
      (ii) Bias CLKin0*(non-driven input) with a reference voltage near the common-mode voltage of the DC-coupled input signal (on CLKin0) using R21 and R23 to form a voltage divider from VCC.

For example, if CLKin0 will be driven by a single-ended, DC-coupled LVCMOS signal with a common-mode voltage of 1.65 V, then 1 kΩ resistors can be installed on R21 and R23 to bias CLKin0* to VCC/2.

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7 Crystal Oscillator Interface

The LMK00338 has an integrated crystal oscillator interface (OSCin/OSCout) that supports a fundamental mode, AT-cut crystal. If the crystal input is selected, the onboard XTAL on either footprint Y1 or Y2 will start- up and the oscillator clock can be measured on any enabled output.

By default, a 25.000 MHz XTAL is populated on Y1, which uses a HC49 footprint on the bottom side of the PCB. Alternatively, a 3.2 x 2.5 mm XTAL or 3.3 V XO (3.3 V CMOS or clipped sinewave) can be populated on Y2, located on the top side. Only one XTAL footprint should be used at a time.

When using a XTAL, the external load capacitor values of C18 and C22 (C_{EXT}) depend on the specified load capacitance (C_L) for the crystal, as well as the device's OSCin input capacitance (C_{IN} = 1 pF typical) and the PCB stray capacitance (C_{STRAY} ~ 1 pF). The selected 25 MHz crystal is specified for C_L of 18 pF. Assuming equal external load capacitor values for optimum symmetry, C_{EXT} can be calculated as follows:

- $C_{EXT} = (C_L - C_{IN} - C_{STRAY}) \times 2$
- $C_{EXT} = (18\ pF - 1\ pF - 1\ pF) \times 2$
- C_{EXT} ~ 33 pF (nearest standard value)

To limit crystal power dissipation, a 1 kΩ resistor is placed between the OSCout pin and the crystal.

7.1 Configuring OSCin for a Single Ended Input

To configure a single-ended clock input on OSCin, remove R34 and R37 to disconnect the crystal. Install 0.1 uF on C24 to provide an AC-coupled path from the SMA input labeled OSCin to the device input, which has internal biasing. Note that the OSCin path includes a 51Ω termination on R42.

8 Clock Outputs

By default, Bank A and B are configured as enabled HCSL outputs, source-terminated with 50 Ω resistors, and DC coupled to the SMA connectors labeled CLKoutA#+ / CLKoutA#, or CLKoutB#+ / CLKoutB#–.

REFout is a LVCMOS output and is AC coupled to its SMA connector.

As noted before, active output traces should be properly terminated; otherwise any unused output pin can be disconnected from the output trace by removing the 0 Ω series resistor.

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9 Schematics

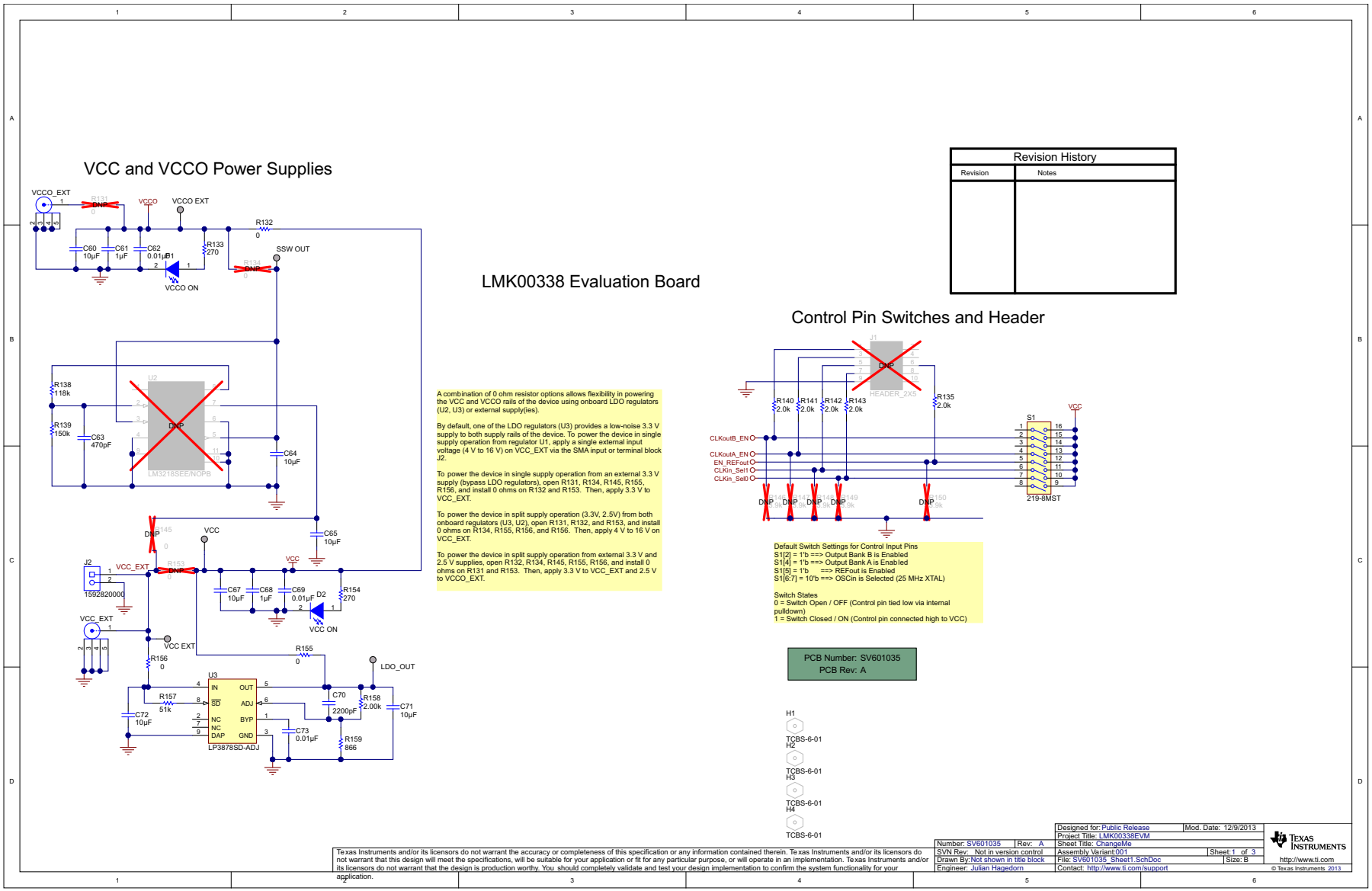


Figure 2. Schematic Sheet #1

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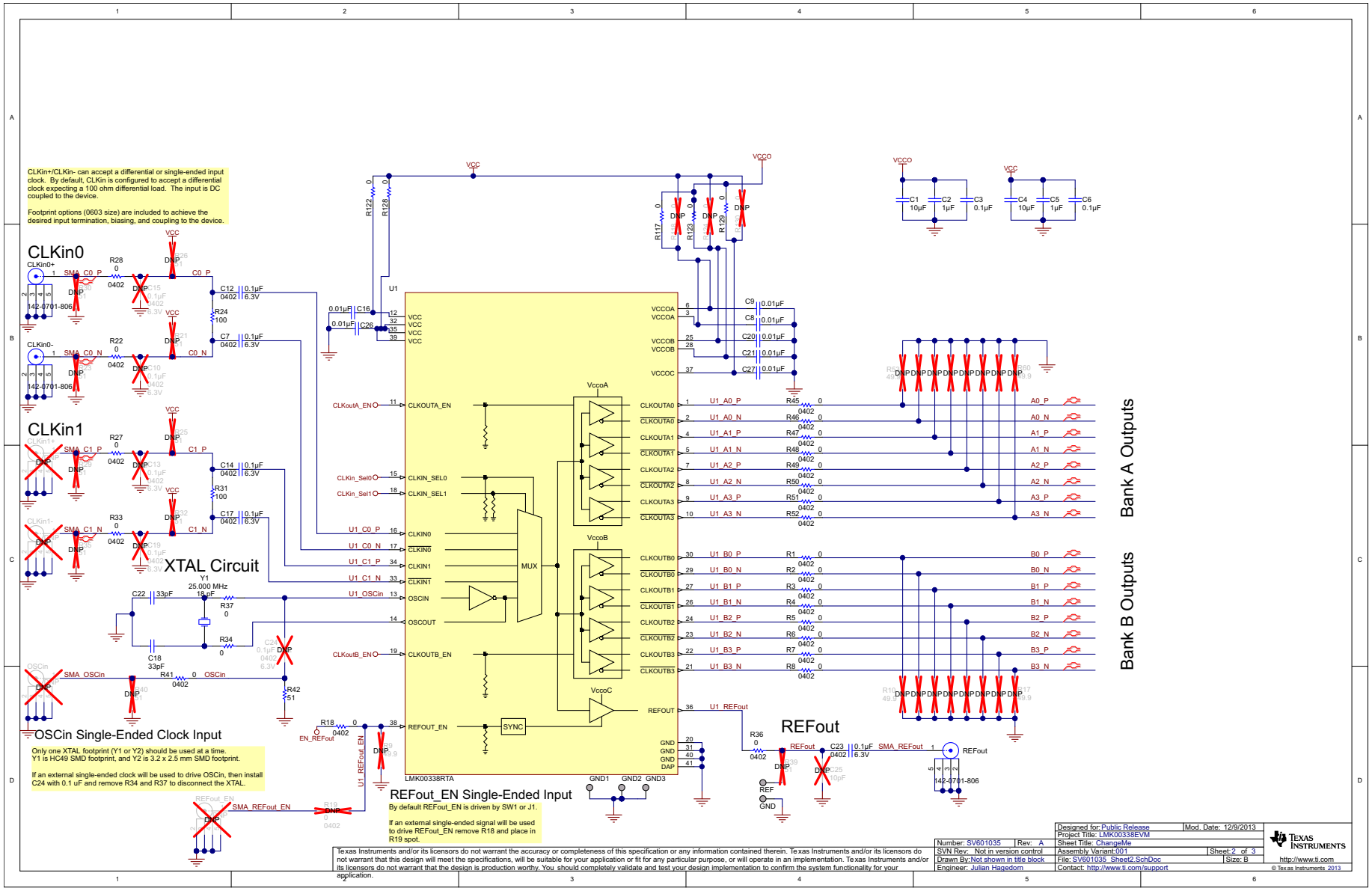


Figure 3. Schematic Sheet #2

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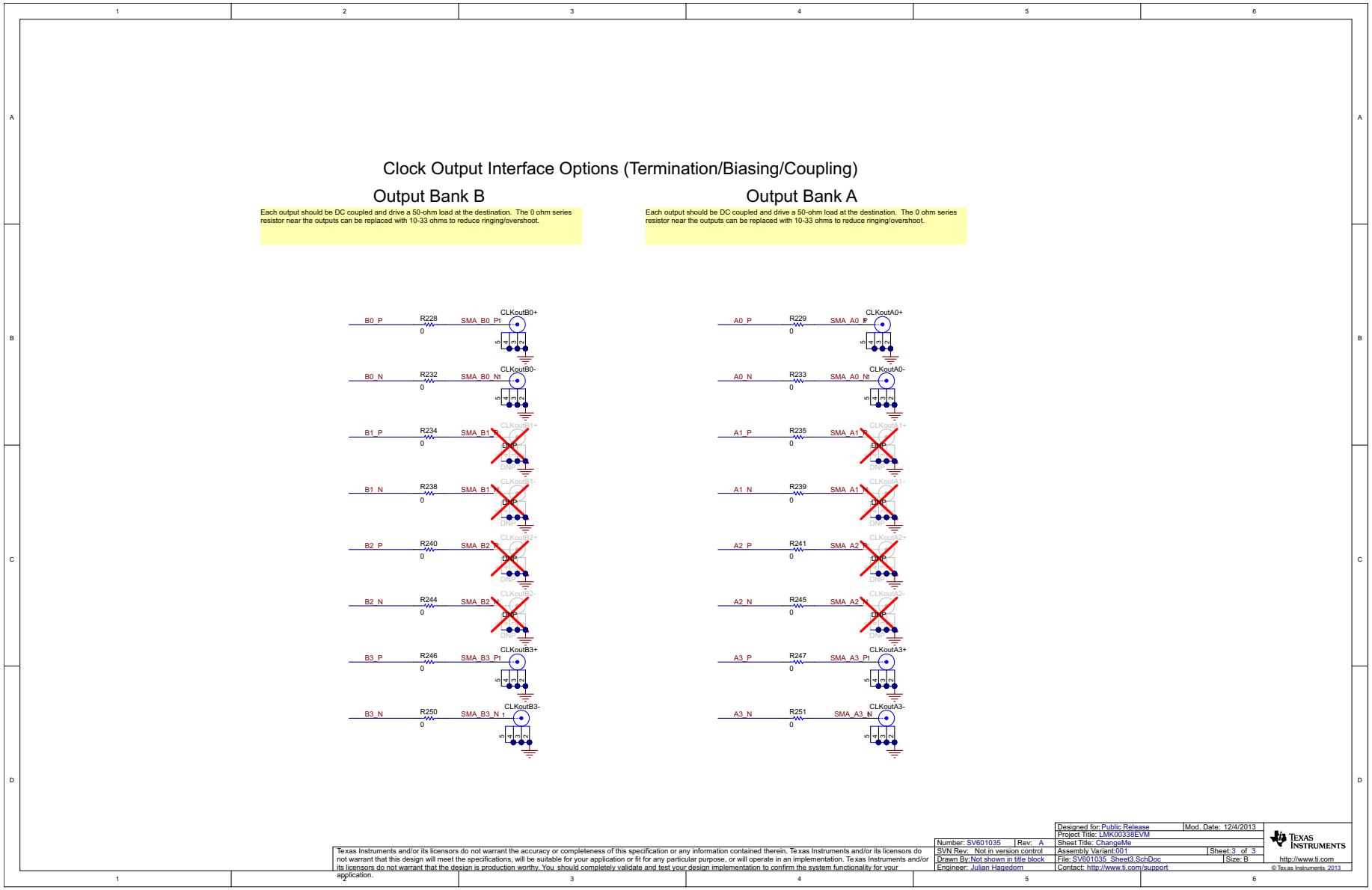


Figure 4. Schematic Sheet #3

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10 Board Layout

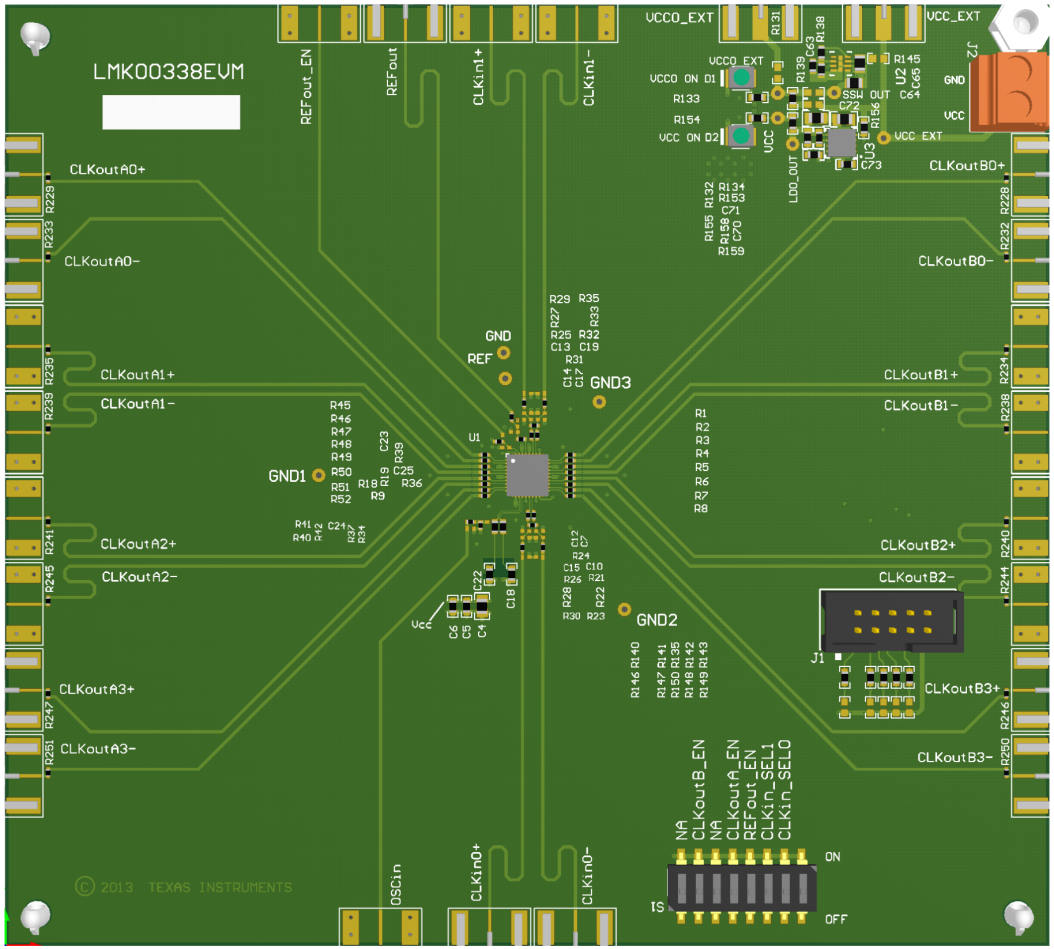


Figure 5. 3D PCB Print – Top (Not to Scale)

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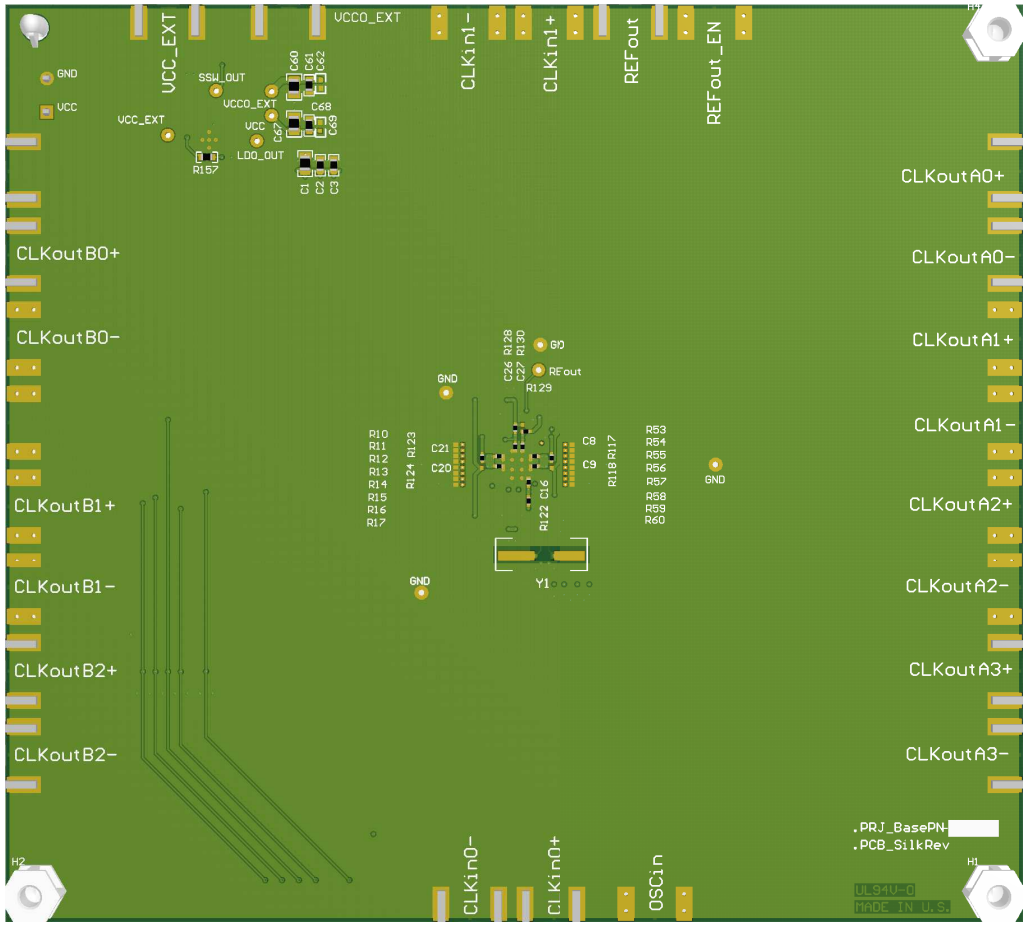


Figure 6. 3D PCB Print – Bottom (Not to Scale)

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11 Bill of Materials

Table 5. LMK00338EVM Bill of Materials

Designator	Description	Manufacturer	Part Number	Quantity
!PCB	Printed Circuit Board	Any	SV601035	1
C1, C4, C60, C64, C65, C67, C71, C72	CAP, CERM, 10uF, 10 V, ±10%, X5R, 0805	MuRata	GRM21BR61A106KE19L	8
C2, C5, C61, C68	CAP, CERM, 1uF, 16 V, ±10%, X7R, 0603	TDK	C1608X7R1C105K	4
C3, C6	CAP, CERM, 0.1uF, 16 V, ±10%, X7R, 0603	TDK	C1608X7R1C104K	2
C7, C12, C14, C17, C23	CAP, CERM, 0.1uF, 6.3 V, ±10%, X5R, 0402	TDK	C1005X5R0J104K	5
C8, C9, C16, C20, C21, C26, C27, C62, C69	CAP, CERM, 0.01uF, 16 V, ±10%, X7R, 0402	TDK	C1005X7R1C103K	9
C18, C22	CAP, CERM, 33pF, 50 V, ±5%, C0G/NP0, 0603	Kemet	C0603C330J5GACTU	2
C63	CAP, CERM, 470pF, 50 V, ±10%, X7R, 0603	TDK	C1608X7R1H471K	1
C70	CAP, CERM, 2200pF, 100 V, ±5%, X7R, 0603	AVX	06031C222JAT2A	1
C73	CAP, CERM, 0.01uF, 25 V, ±5%, C0G/NP0, 0603	TDK	C1608C0G1E103J	1
CLKin0+, CLKin0-, CLKoutA0+, CLKoutA0-, CLKoutA3+, CLKoutA3-, CLKoutB0+, CLKoutB0-, CLKoutB3+, CLKoutB3-, REFout, VCC_EXT, VCCO_EXT	Connector, SMT, End launch SMA 50 ohm	Emerson Network Power	142-0701-806	13
D1, D2	LED, Green, SMD	Lumex	SML-LX2832GC-TR	2
H1, H2, H3, H4	HEX STANDOFF SPACER, 9.53 mm	Richco Plastics	TCBS-6-01	4
J2	Terminal Block, 10.76x17x11 mm, 2POS, 26-12AWG, TH	Weidmuller	1592820000	1
R1, R2, R3, R4, R5, R6, R7, R8, R18, R22, R27, R28, R33, R36, R41, R45, R46, R47, R48, R49, R50, R51, R52, R117, R122, R123, R128, R129, R228, R229, R232, R233, R234, R235, R238, R239, R240, R241, R244, R245, R246, R247, R250, R251	RES, 0 Ω, 5%, 0.063W, 0402	Panasonic	ERJ-2GE0R00X	44
R24, R31	RES, 100 Ω, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402100RFKED	2
R34, R37, R132, R155, R156	RES, 0 Ω, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	5
R42	RES, 51 Ω, 5%, 0.063 W, B0402	Vishay-Dale	CRCW040251R0JNED	1
R133, R154	RES, 270 Ω, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603270RJNEA	2
R135, R140, R141, R142, R143	RES, 2.0k Ω, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06032K00JNEA	5
R138	RES, 118k Ω, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603118KFKEA	1
R139	RES, 150k Ω, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603150KFKEA	1

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Table 5. LMK00338EVM Bill of Materials (continued)

Designator	Description	Manufacturer	Part Number	Quantity
R157	RES, 51k Ω, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060351K0JNEA	1
R158	RES, 2.00k Ω, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06032K00FKEA	1
R159	RES, 866 Ω, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603866RFKEA	1
S1	Switch, Slide, SPST 8 poles, SMT	CTS Electrocomponents	219-8MST	1
U1	LMK00338 3-GHz 8-Output Differential Clock Buffer/Level Translator, RTA0040A	Texas Instruments	LMK00338RTA	1
U3	Micropower 800 mA Low Noise 'Ceramic Stable' Adjustable Voltage Regulator for 1V to 5V Applications, 8-pin LLP	National Semiconductor	LP3878SD-ADJ	1
Y1	CRYSTAL 25.000 MHZ 18PF SMD	Abracon Corporation	ABLS-25.000MHZ-B4-F-T	1

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3 *Regulatory Notices:*

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      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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