ANALOG DEVICES

EVAL-ADG5243FEBZ User Guide
UG-894

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluation Board for the ADG5243F, Overvoltage Protected Triple SPDT Switch

FEATURES

- Supply voltages
  - Dual supply: ±5 V to ±22 V
  - Single supply: 8 V to 44 V
- Protected against overvoltage on source pins
  - Signal voltages up to −55 V and +55 V
- LED for visual overvoltage indication
- Parallel interface compatible with 3 V logic
- On-board LDO regulator for digital supply and control, if required

EVALUATION KIT CONTENTS

EVAL-ADG5243FEBZ evaluation board

DOCUMENTS NEEDED

ADG5243F data sheet
EVAL-ADG5243FEBZ user guide

EQUIPMENT NEEDED

- DC voltage source
  - ±22 V for dual supply
  - 44 V for single supply
- Optional digital voltage source: 3 V to 5 V
- Analog signal source
- Method to measure voltage, such as a digital multimeter (DMM)

GENERAL DESCRIPTION

The EVAL-ADG5243FEBZ is the evaluation board for the ADG5243F, which features three independently controlled single-pole/double-throw (SPDT) switches. The ADG5243F has overvoltage detection and protection circuitry on the source pins and is protected against signals up to −55 V and +55 V in both the powered and unpowered states.

Figure 1 shows the EVAL-ADG5243FEBZ in a typical evaluation setup. The ADG5243F is soldered to the center of the evaluation board, and screw terminals are provided to connect to each of the source and drain pins. Three screw terminals power the device, and a fourth terminal provides a user defined digital voltage, if required. Alternatively, a low dropout (LDO) regulator is provided for 5 V digital voltage control and to supply the LED, which is mounted to provide visual indication of the fault status of the switch.

Full specifications on the ADG5243F are available in the product data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.

EVALUATION BOARD CONNECTION DIAGRAM

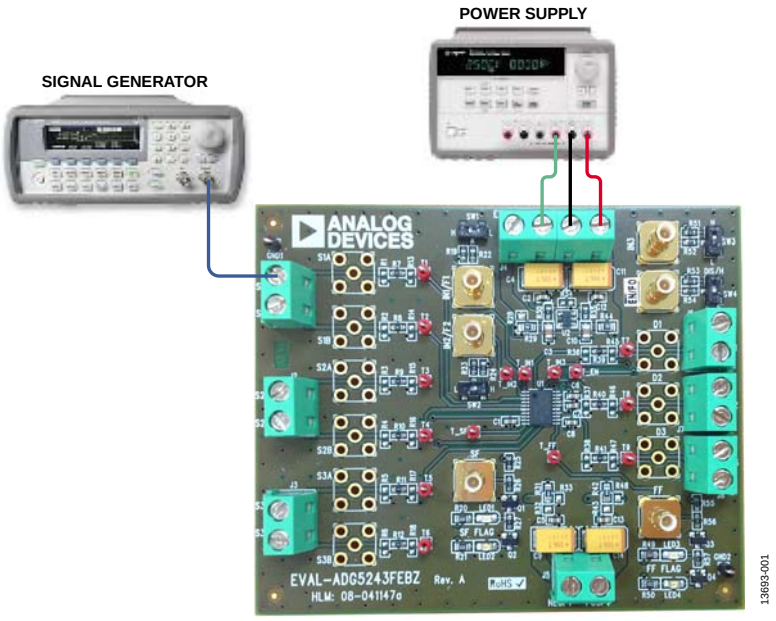

Figure 1. EVAL-ADG5243FEBZ, Power Supply, and Signal Generator

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REVISION HISTORY

10/15—Revision 0: Initial Version

GETTING STARTED

EVALUATION BOARD SETUP PROCEDURE

The EVAL-ADG5243FEBZ board operates independently and does not require any additional evaluation boards or software. An on-board LDO regulator is provided for digital control and supply voltage.

Supply the evaluation board with a dual-supply power source of up to ±22 V or a single-supply power source of up to 44 V. For single-supply operation, connect VSS to GND using Connector J4.

Set up a simple functionality test as follows:

1. Connect a power supply to J4. If a single supply is required, connect VSS and GND together.
2. Ensure that a 0 Ω resistor is inserted in R44 to use the on-board LDO regulator, and that a 0 Ω resistor is inserted into R29. SW1 to SW4 control the digital signals for each switch on the ADG5243F.
3. LED1 and LED3 illuminate green to indicate that the multiplexer is operating normally.

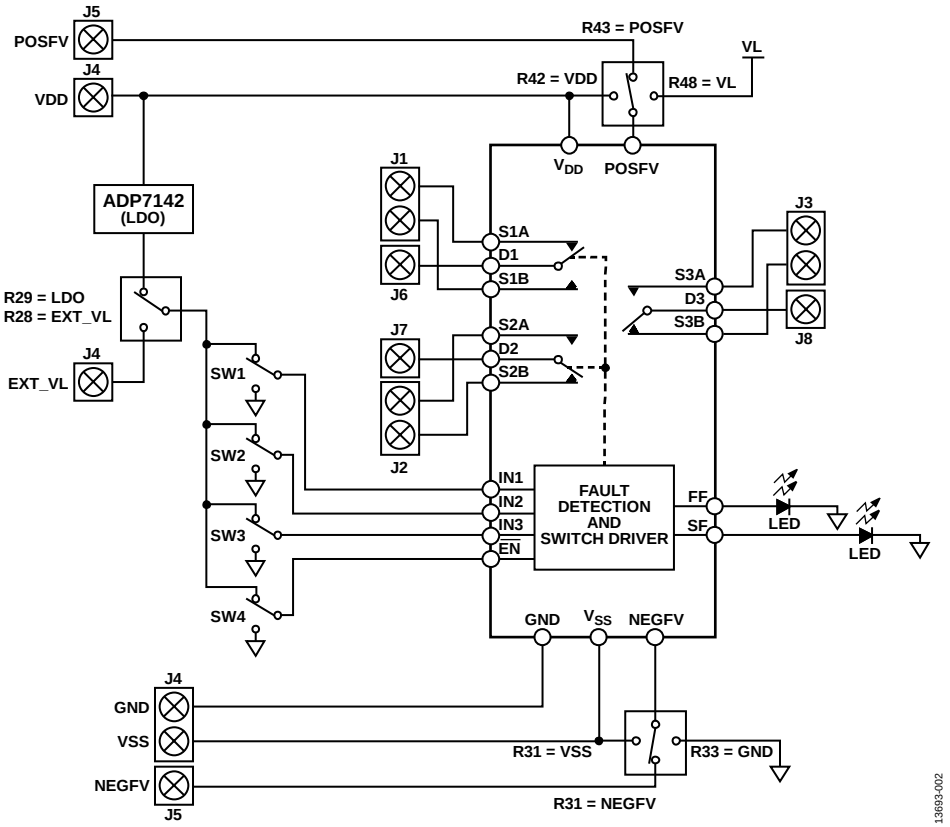

Figure 2. EVAL-ADG5243FEBZ Block Diagram

EVALUATION BOARD HARDWARE

Evaluate the operation of the ADG5243F using the EVAL-ADG5243FEBZ. Figure 1 shows a typical evaluation setup where only power supply and signal generator are required. Figure 2 shows a block diagram of the main components of the evaluation board.

Using the evaluation board, the ADG5243F passes signals from either the source or the drain connectors. The source pins have fault detection circuitry that reacts to an overvoltage. During an overvoltage event, the channel where the fault occurs turns off, and the FF pin pulls low. The SF pin pulls low when the $\overline{EN}$/F0, IN1/F1, or IN2/F2 pins select the source where the overvoltage occurs. See the ADG5243F data sheet for further details.

POWER SUPPLY

Connector J4 provides access to the supply pins of the ADG5243F. VDD, GND, and VSS link to the appropriate pins of the ADG5243F. For dual supply voltages, power the evaluation board from ±5 V to ±22 V. For single supply voltages, connect the GND and VSS terminals and power the evaluation board with 8 V to 44 V. Additionally, an on-board LDO regulator is provided for digital control voltage. If necessary, connect a secondary voltage source to EXT_VL and use it as the digital control voltage. To use EXT_VL, move the 0 Ω resistor from R29 to R28. Do not expose the on-board LDO regulator to voltages greater than 28 V; remove R44 and supply an alternative digital voltage via EXT_VL, if required.

INPUT SIGNALS

Six screw connectors are provided to connect both the source and drain pins of the ADG5243F. Additional subminiature Version B (SMB) connector pads are provided if extra connections are required. The ADG5243F is overvoltage protected on the source side, and each source terminal (SxA to SxB) can be presented with a voltage of up to +55 V or −55 V. See the ADG5243F data sheet for more details.

Each trace on the source and drain side includes two sets of 0603 pads, which can be used to place a load on the signal path to ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user defined value. Use the resistor combined with the 0603 pads to create a simple resistor/capacitor (RC) filter.

The ADG5243F uses a parallel interface to control the operation of the switches. The switch operation can be manually controlled using SW1 to SW4, or an external controller can be interfaced directly to the control pins by using the SMB connectors ($\overline{EN}$/F0, IN1/F1, IN2/F2, and IN3) and remove the 0 Ω resistors: R54, R22, R23, and R52.

OUTPUT SIGNALS

There are two outputs on the ADG5243F. The FF pin indicates when the device is operating normally or whether there is an overvoltage fault on one of the source pins. The SF pin also indicates when an overvoltage fault occurs on one of the source pins and transitions low only when an overvoltage occurs on the channels selected by the $\overline{EN}$/F0, IN1/F1 and IN2/F2 inputs.

For visual indication, an LED is mounted on the evaluation board. When the device is operating normally, the FF and SF pins remain high, and LED1 and LED3 illuminate green. If an overvoltage occurs at any of the source pins, the FF pin pulls low and LED4 illuminates red. If an overvoltage occurs at the source pin selected by $\overline{EN}$/F0, IN1/F1, and IN2/F2, the SF pin pulls low and LED2 illuminates red.

SMB connectors are provided to interface the evaluation board with external controllers.

JUMPER SETTINGS

LINK HEADERS

The switches on the evaluation board control the ADG5243F manually, and 0 Ω resistors are used to configure the VL supply voltage, the voltage present on POSFV and NEGFV, and to isolate the LEDs from the remainder of the system. Table 2 shows a summary of the uses of the switches and 0 Ω resistors on the evaluation board.

Use SW1 to SW4 to control the switches of the ADG5243F. Position L is tied to GND and sets the logic low. Position H is tied to VL and sets the logic high.

Use SW1 to enable or disable the device. Position DIS is tied to VL and disables the device. Position $\overline{EN}$ is tied to GND and enables the device.

Table 1. ADG5243F Truth Table[1]

SW1 ($\overline{EN}$/F0)	SW2 (IN1/F1)	SW2 (IN2/F2)	SW4 (IN3)	Connected Sx
DIS	X	X	X	All switches off
$\overline{EN}$	L	X	X	S1B
$\overline{EN}$	H	X	X	S1A
$\overline{EN}$	X	L	X	S2B
$\overline{EN}$	X	H	X	S2A
$\overline{EN}$	X	X	L	S3B
$\overline{EN}$	X	X	H	S3A

[1] X means don't care.

R44 connects the on-board LDO regular to the VDD supply. Remove this resistor to isolate the LDO regulator from the input screw terminals. Change the 0 Ω resistor from position R29 to R28 to use an alternative digital supply voltage from EXT_VL screw terminal.

The R49, R50, R20, and R21 resistors connect the LEDs to the digital power supply. R56 and R26 connect the FF and SF pins of the ADG5243F to the LED controls.

The R42, R43, and R48 resistors configure POSFV to either VDD, the voltage present on POSFV on J5, or VL. The R31, R32, and R33 resistors configure NEGFV to either VSS, the voltage present on NEGFV on J5, or GND.

SMB CONNECTORS

The SW1 to SW4 switches allow the user to manually control the parallel interface of the ADG5243F. Alternatively, the SMB connectors ($\overline{EN}$/F0, IN1/F1, IN2/F2, F3) can be populated to allow control via external control signals. To use the SMB connectors, remove the 0 Ω resistors: R54, R22, R23, and R53. The FF/SF SMB connectors to access the FF/SF digital outputs from the ADG5243F.

Table 2. Switch and 0 Ω Resistor Descriptions

Label	Position	Description
SW1	$\overline{EN}$	Logic 0 on $\overline{EN}$/F0 pin
	DIS	Logic 1 on $\overline{EN}$/F0 pin
SW2	L	Logic 0 on IN1/F1 pin
	H	Logic 1 on IN1/F1 pin
SW3	L	Logic 0 on IN2/F2 pin
	H	Logic 1 on IN2/F2 pin
SW4	L	Logic 0 on IN3 pin
	H	Logic 1 on IN3 pin
R42, R43, R48	R42	POSFV set to VDD
	R43	POSFV set to voltage on J5 POSFV screw terminal
	R48	POSFV set to VL
R31, R32, R33	R31	NEGFV set to VSS
	R32	NEGFV set to voltage on J5 NEGFV screw terminal
	R33	NEGFV set to GND
R29, R28	R29	On-board LDO regulator digital voltage
	R28	EXT_VL digital voltage
R44	Inserted	LDO regulator powered up
	Removed	LDO regulator unpowered
R56, R26	Inserted	FF and SF pins connected to LED
	Removed	FF and SF pins disconnected from LED
R49, R50, R20, R21	Inserted	LED connected to digital supply
	Removed	LED isolated

EVALUATION BOARD SCHEMATICS AND ARTWORK

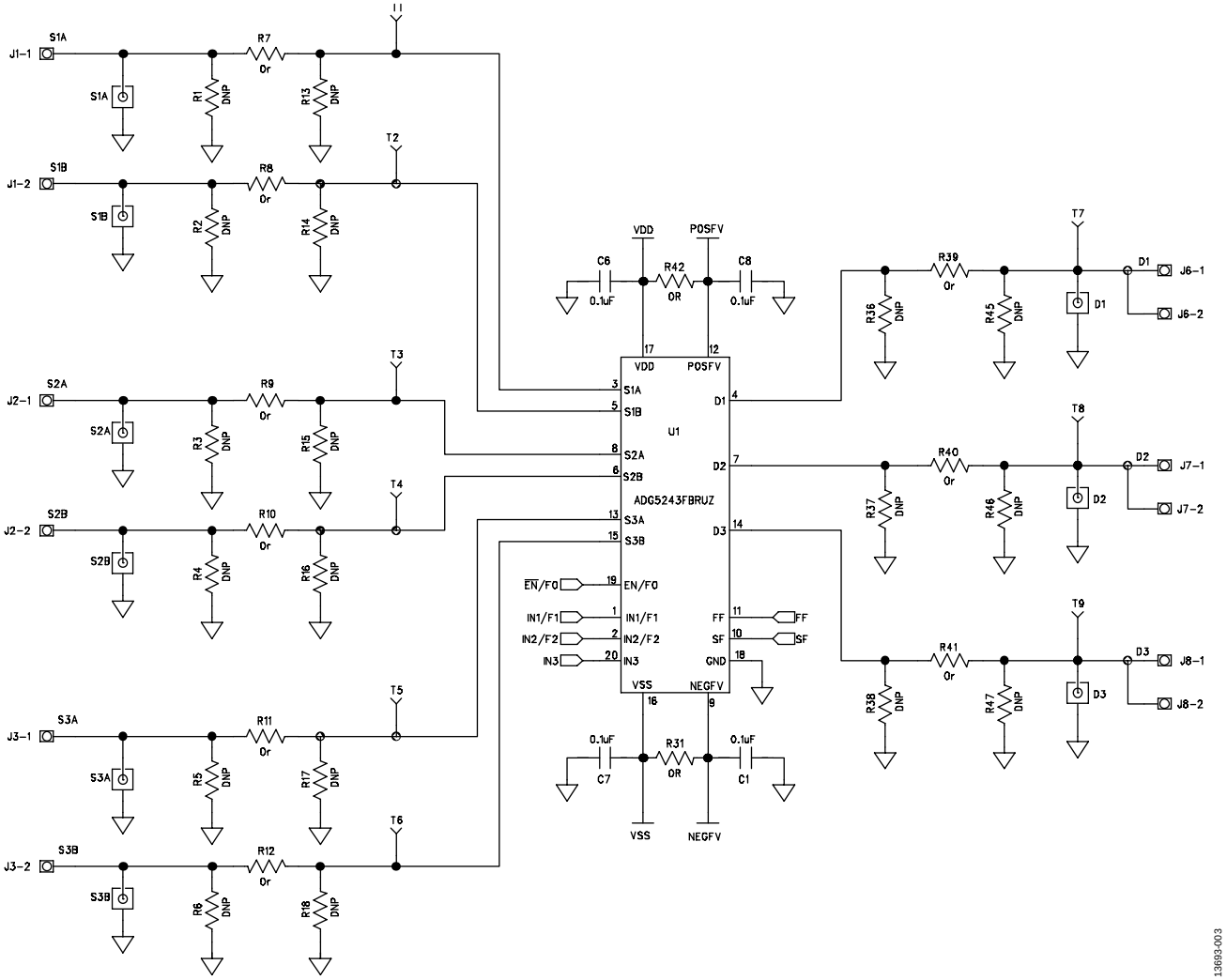

Figure 3. ADG5243F Evaluation Board Schematic (Part 1)

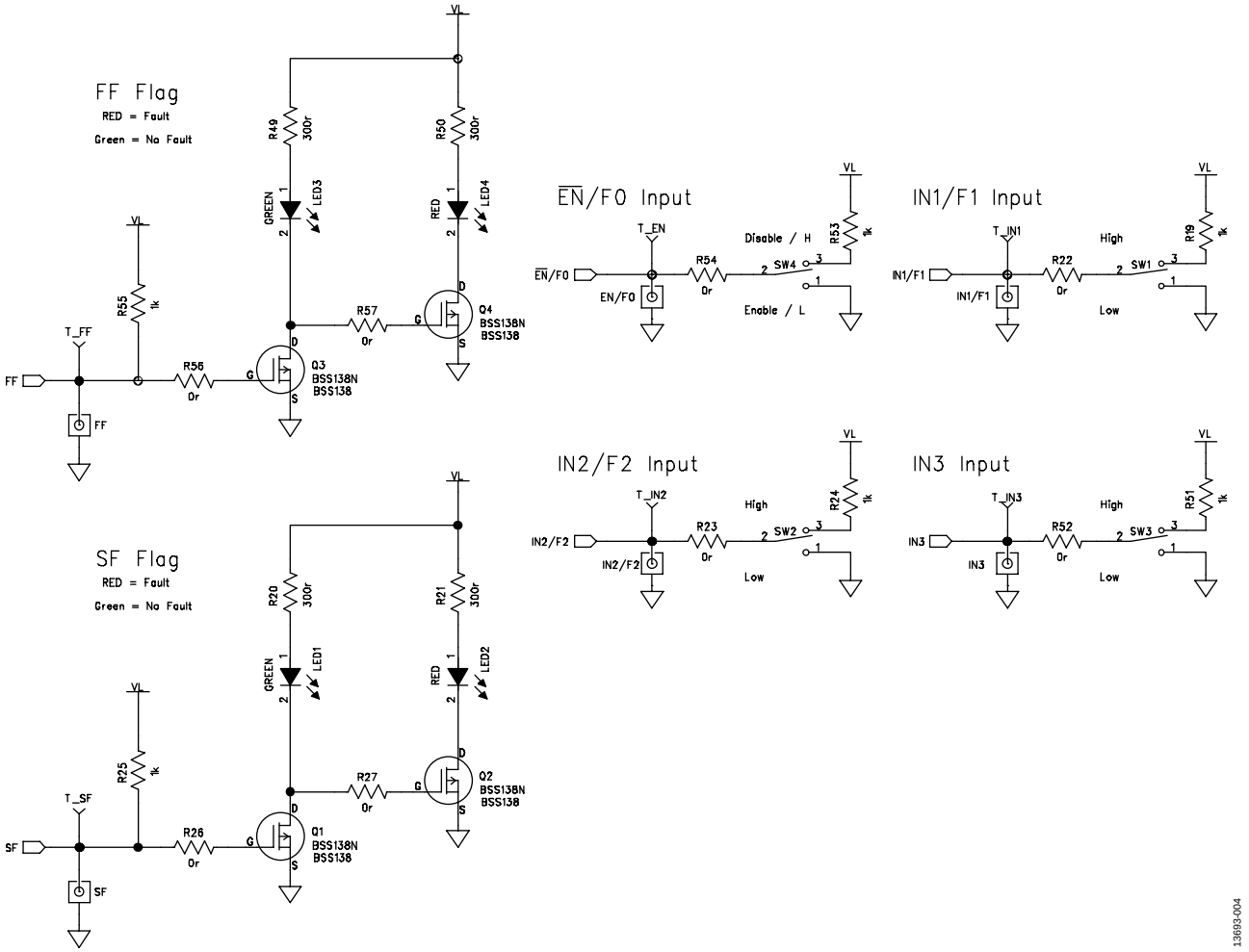

Figure 4. ADG5243F Evaluation Board Schematic (Part 2)

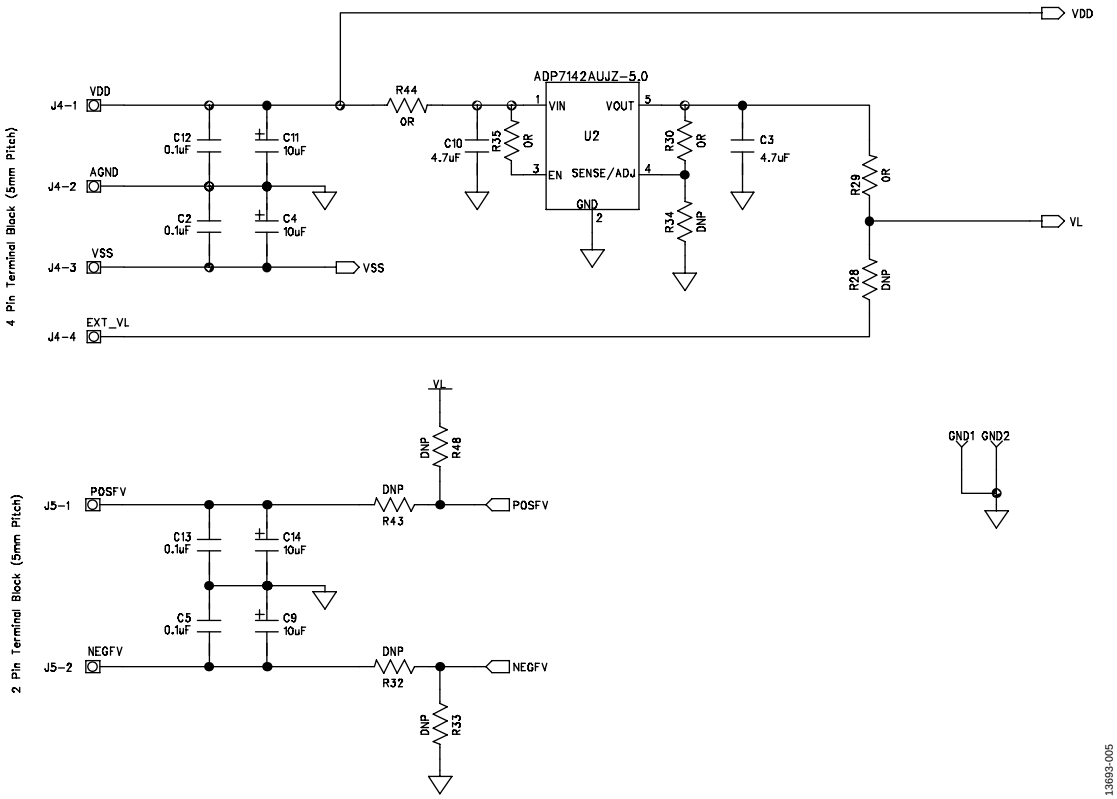

Figure 5. ADG5243F Evaluation Board Schematic (Part 3)

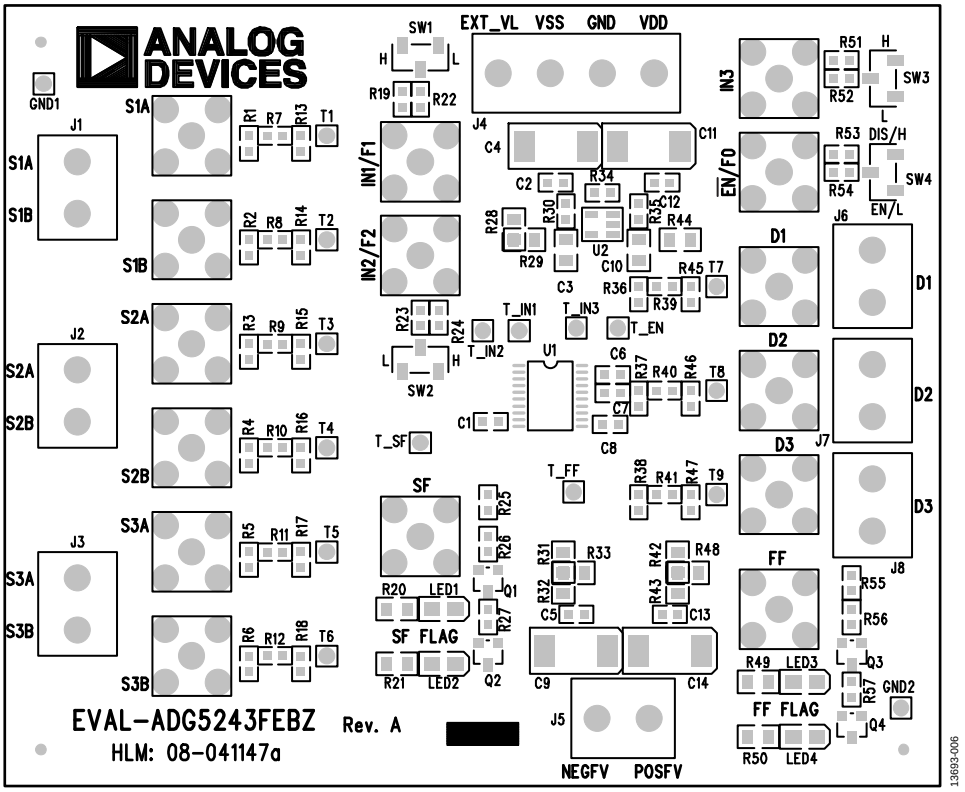

Figure 6. EVAL-ADG5243FEBZ Silk Screen

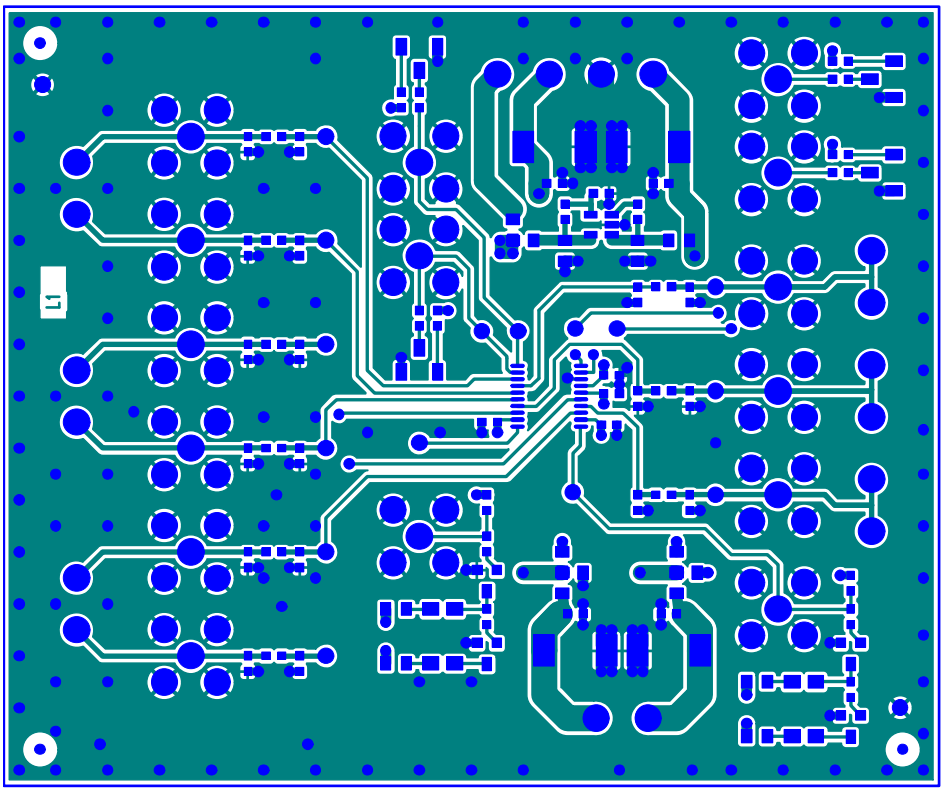

Figure 7. EVAL-ADG5243FEBZ Top Layer

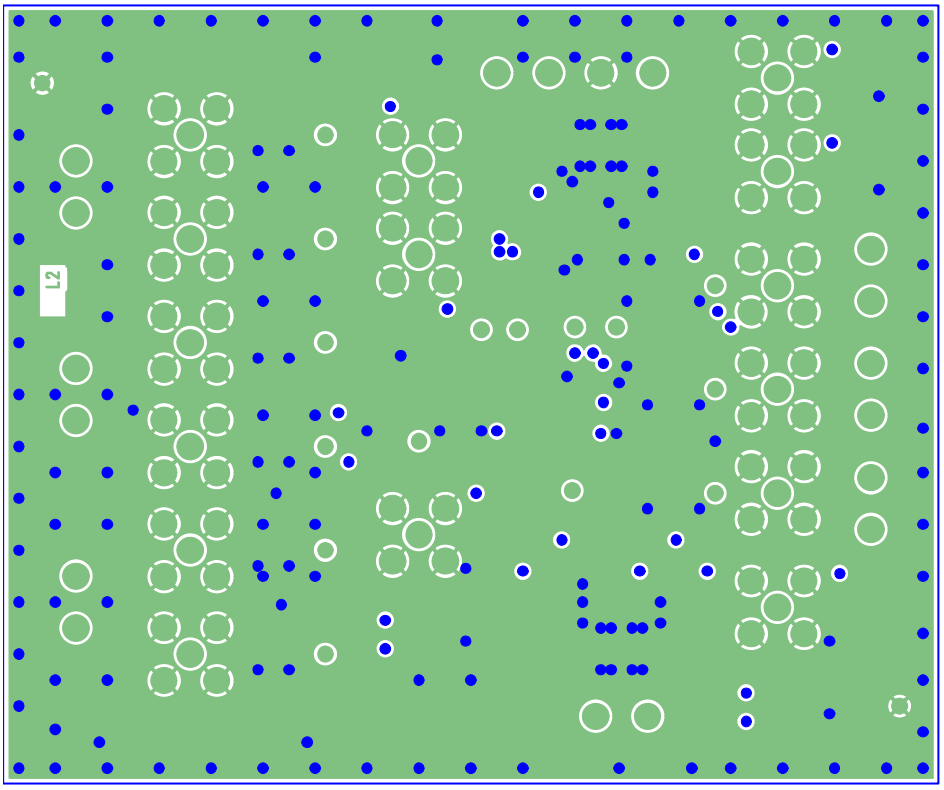

Figure 8. EVAL-ADG5243FEBZ Layer 2

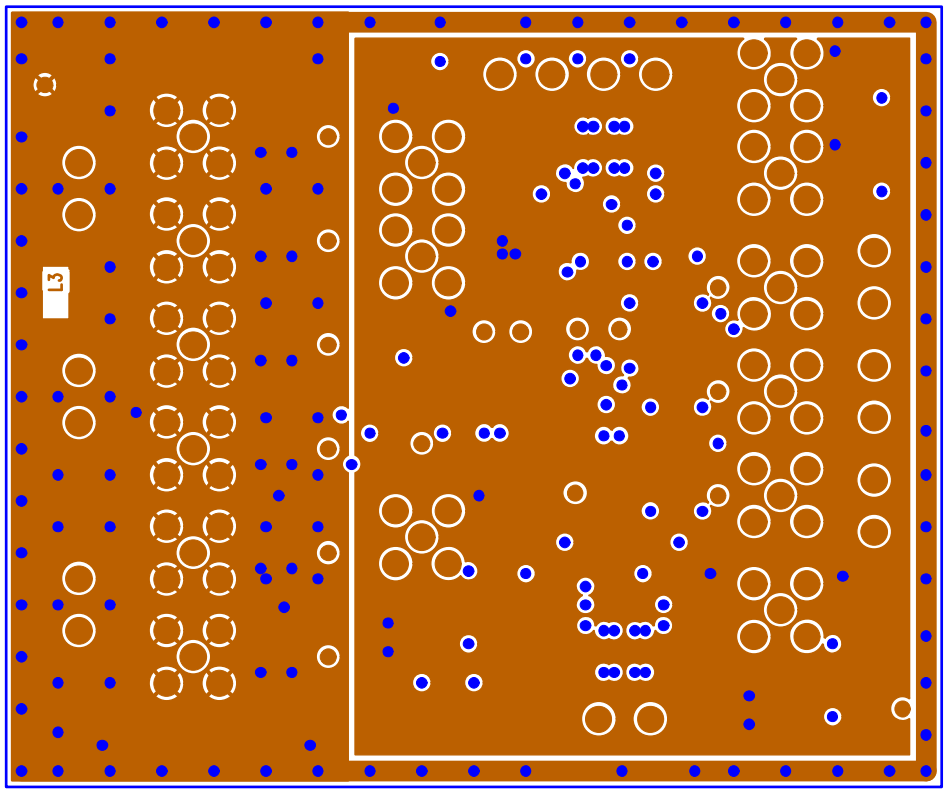

Figure 9. EVAL-ADG5243FEBZ Layer 3

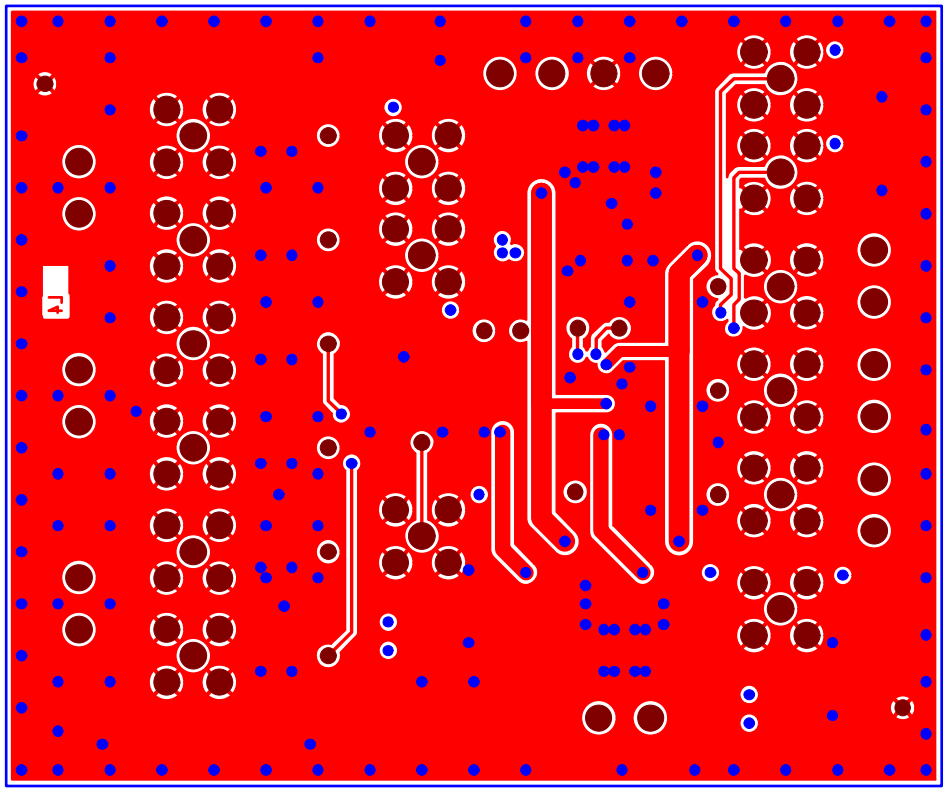

Figure 10. EVAL-ADG5243FEBZ Bottom Layer

BILL OF MATERIALS

Table 3.

Reference Designator	Description	Part Number	Stock Code
C1, C2, C5 to C8, C12, C13	50 V, X7R, multilayer, ceramic capacitor, 0603 size, 0.1 µF	GRM188R71H104KA93D	FEC 882-0023
C3, C10	Ceramic, multilayer capacitor, 4.7 µF	C2012X5R1H475K125AB	FEC 2346932
C4, C9, C11, C14	50 V, tantalum capacitor, D size, 10 µF	TAJD106K050RNJ	FEC 143-2387
D1 to D3, S1A, S1B, S2A, S2B, S3A, S3B	50 Ω, SMB socket	SMB1251B1-3GT30G-50	Do not insert
$\overline{EN}$/F0, FF, IN1/F1, IN2/F2, IN3, SF	50 Ω, straight SMB jack	SMB1251B1-3GT30G-50	FEC 1111349
GND1, GND2	Black test point	20-2137	FEC 873-1128
J1 to J8	2-pin terminal block (5 mm pitch)	CTB5000/2	FEC 151789
LED1, LED3	LED, SMD, green, 0805	KP-2012SGC	FEC 1318243
LED2, LED4	LED, SMD, red, 0805	KP-2012SRC-PRV	FEC 1318244
Q1 to Q4	Transistor, N-MOSFET, 60 V, 0.23 A, SOT-23	BSS138N	FEC 115-6434
R1 to R6, R13 to R18, R34, R36 to R38, R45 to R47	SMD, resistor, 0603	Not applicable	Do not place
R7 to R12, R22, R23, R26, R27, R30, R35, R39 to R41, R52, R54, R56, R57	Resistor, 0603, 1%, 0 Ω	MC0063W06030R	FEC 9331662
R19, R24, R25, R51, R53, R55	Resistor, 1 kΩ, 0.063 W, 1%, 0603	MC0063W060311K	FEC 9330380
R20, R21, R49, R50	Resistor, 300 Ω, 0.1 W, 1%, 0805	MC01W08051300R	FEC 9332987
R28, R32, R33, R43, R48	SMD, resistor, 0805	Not applicable	Do not place
R29, R31, R42, R44	Resistor, 0805, 1%, 0 Ω	MC01W08050R	FEC 9333681
SW1 to SW4	SPDT, SMT, slide switch	CAS-120TA	Digi-Key CAS120JCT-ND
T1 to T9, T_EN, T_FF, T_IN1, T_IN2, T_IN3, T_SF	Red test point	20-313137	FEC 873-1144
U1	Fault protection and detection, 1 pC, QINJ, triple SPDT	ADG5243FBRUZ	ADG5243FBRUZ-RL7
U2	Linear regulator, 5.0 V, LDO	ADP7142AUJZ-5.0	ADP7142AUJZ-5.0-R7

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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