DEMO MANUAL DC045
Micropower A/D Demo Board

LTC1298 Micropower 12-Bit A/D Converter Demo Board

DESCRIPTION

The LTC®1298 is a micropower, 11.1ksps, two-channel sampling 12-bit A/D converter that draws only 1.25mW from a single 5V supply. The LTC1298 demo board provides the user with a stable and consistent platform on which to evaluate the LTC1298 A/D converter. In addition, the LTC1298 demo board illustrates the layout and bypassing techniques required to obtain optimum performance from this part. The LTC1298 demo board is designed to be easy to use and requires only a 7V to 15V supply, a clock signal, and an analog input signal. As shown in the Board Photo, the LTC1298 is a very space efficient solution for A/D users. By combining a micropower 12-bit A/D, sample-and-hold, two-channel multiplexer, serial port, and auto shutdown circuit into a single 8-pin SOIC package, all the data acquisition circuitry including the bypass caps occupy an area of only 0.1 square inch.

This manual shows how to use the demo board. It includes timing diagrams, power supply requirements, and analog input range information. Additionally, a schematic, parts list, drawings, and dimensions of all the PC board layers are included. Finally, an explanation of the layout and bypass strategies used in this board allows anyone designing a PC board to achieve maximum performance from the device.

FEATURES

- Proven µPower 12-Bit ADC Surface Mount Layout
- On-Chip Two-Channel Mulitplexer
- Actual ADC Footprint Only 0.1 Inch^2 Including Bypass Capacitors
- 71dB SINAD, 84dB THD and ±0.25LSB DNL
- Gerber Files for This Circuit Board Are Available. Call the LTC Factory.

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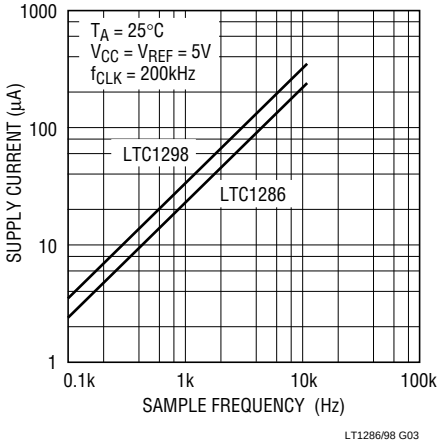
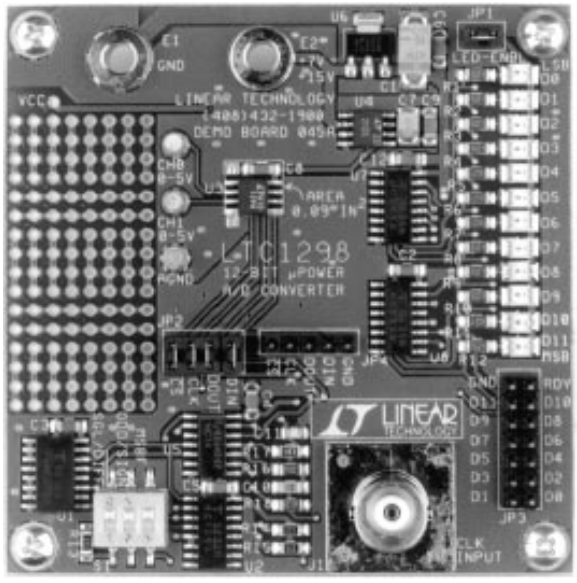
TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

Supply Current vs Sample Rate



LT1286/98 G03



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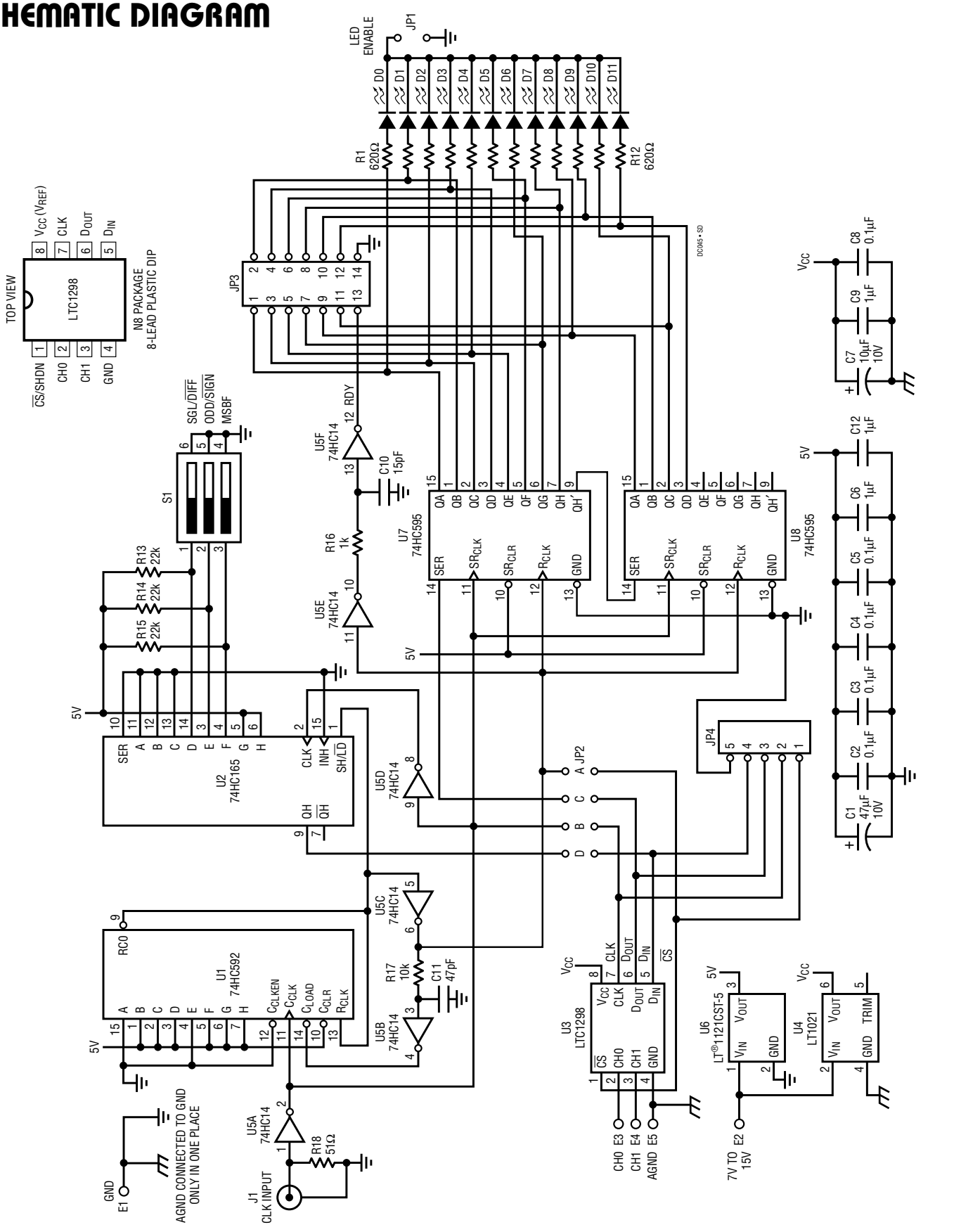
SCHEMATIC DIAGRAM



PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C1	1	TAJD476M010	47µF 10V 20%, Tantalum Capacitor	AVX	(207) 282-5111
C2 to C5, C8	5	GRM42-6X7R104K050AD	0.1µF 50V 10%, X7R Chip Capacitor	Murata Erie	(814) 237-1431
C6, C9, C12	3	12063G105ZATMA	1µF 25V +80%/–20%, Y5V Chip Capacitor	AVX	(803) 448-9411
C7	1	TAJB106M010	10µF 10V 20%, Tantalum Capacitor	AVX	(207) 282-5111
C10	1	12062R150K9BB2	15pF 50V 10% NPO Chip Capacitor	Philips	(407) 744-4200
C11	1	08055A470GATBA	47pF 50V 2% NPO Chip Capacitor	AVX	(803) 448-9411
D0 to D11	12	SF1-BR	Red LED	Data Display	(800) 421-6815
E1, E2	2	575-4	Banana Jack	Keystone	(718) 956-8900
E3 to E5	3	1502-2	Turret	Keystone	(718) 956-8900
JP1	1	TSW-101-07-G-D	Header	Samtec	(800) 726-8329
JP2	1	TSW-104-07-G-D	Header	Samtec	(800) 726-8329
JP3	1	TSW-107-06-G-D	Header	Samtec	(800) 726-8329
JP4	1	TSW-105-07-G-SN	Header	Samtec	(800) 726-8329
J1	1	227699-3	BNC Connector	AMP	(717) 564-0100
R1 to R12	12	CR32-621J-T	620Ω 1/8W 5% 1206 Chip Resistor	AVX	(803) 448-9411
R13 to R15	3	CT32-223J-T	22k 1/8W 5% 1206 Chip Resistor	AVX	(803) 448-9411
R16	1	CT32-102J-T	1k 1/8W 5% 1206 Chip Resistor	AVX	(803) 448-9411
R17	1	CT32-103J-T	10k 1/8W 5% 1206 Chip Resistor	AVX	(803) 448-9411
R18	1	CT32-5101J-T	51Ω 1/8W 5% 1206 Chip Resistor	AVX	(803) 448-9411
S1	1	90HBW03S	DIP Switch	Grayhill	(708) 354-1040
U1	1	74HC592	IC	Toshiba	(408) 737-9844
U2	1	74HC165	IC	Toshiba	(408) 737-9844
U3	1	LTC1298CS8	IC	LTC	(408) 432-1900
U4	1	LTC1021DCS8-5	IC	LTC	(408) 432-1900
U5	1	74HC14	IC	Texas Instruments	(800) 336-5236
U6	1	LT1121CST-5	IC	LTC	(408) 432-1900
U7, U8	2	74HC595	IC	Toshiba	(408) 737-9844
	4	HTSP-3	Plastic Stand.	Micro Plastic	(501) 453-8861
	5	SNT-100-BK-5	Shunt	Samtec	(800) 726-8329
	4	4/40 × 3/8	Steel Screw		

OPERATION

OPERATING THE BOARD

Powering the Board

To use the demo board, apply a 7V to 15V power source capable of supplying ≥100mA to the banana jacks (E1 and E2). Be careful to observe the correct polarity. On-board regulators provide 5V to the LTC1298's V_{CC} pin. LT1121-5 and LT1021 regulators generate 5V for the digital circuitry and ADC, respectively.

Applying the Analog Input

Analog input signals are applied to the LTC1298's two-channel (CH0 and CH1) input multiplexer through the demonstration board's turret terminals E3 (CH0) and E4 (CH1). The input signals' ground reference is applied to turret terminal E5. The analog signal input range is 0V to 5V. Optimum performance is achieved using a signal source that has low output impedance, is low noise, and

OPERATION

has low distortion. Signal generators such as the B & K Type 1051 sine generator give excellent results.

Applying the Clock Signal

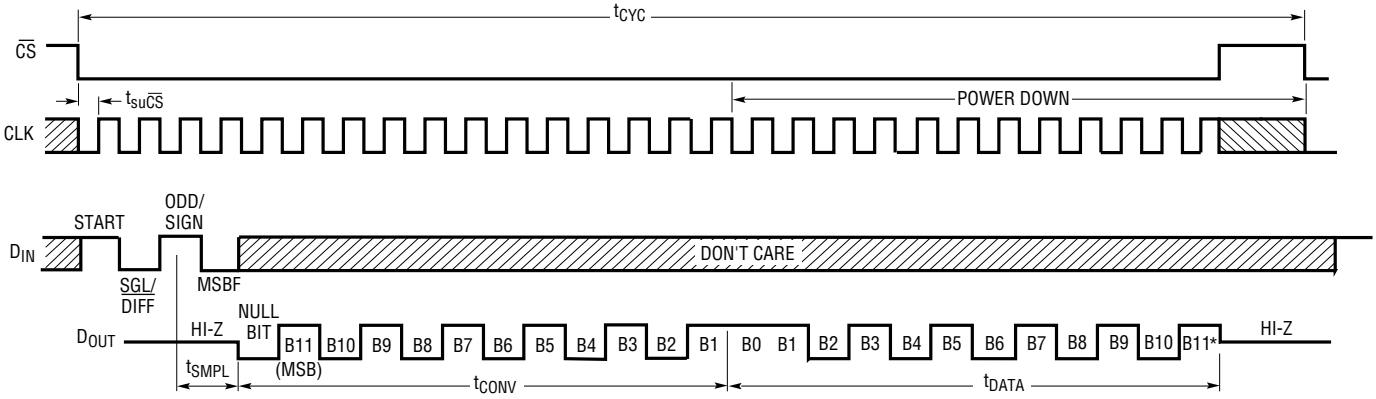
The clock signal is applied to BNC connector J1 and the $\overline{CS}$ signal is generated on the board. The clock input uses TTL or CMOS levels. The maximum clock frequency is 200kHz. While the clock signal is active, a high-to-low logic level transition is generated on the LTC1298's $\overline{CS}$ input which initiates a conversion. The data transfer is shown in the timing diagrams (Figure 1).

Reading the Output Data

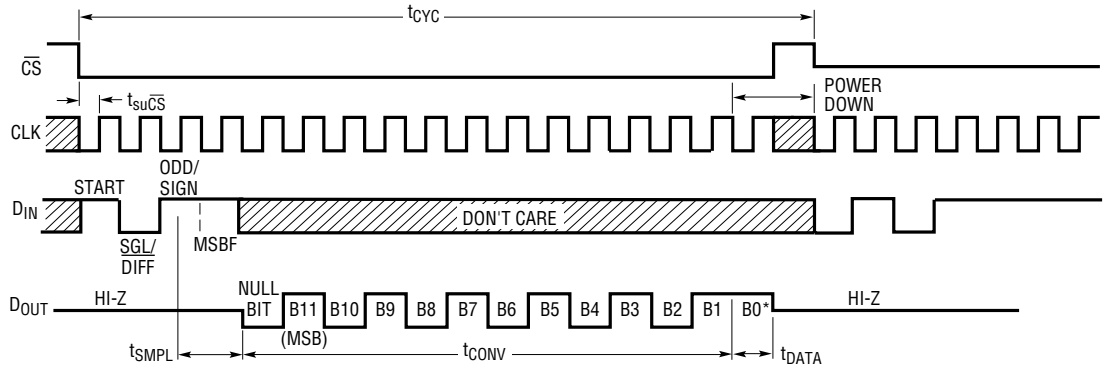
The LTC1298 serial data outputs are buffered by the two 74HC595 latches and are available as a parallel output on connector JP3. The latches are used to drive the LEDs D0 to D11. (Refer to the LTC1298 data sheet for details on different digital interface modes.)

The LTC1298 output data is in unipolar format. A Data Ready line, RDY, (JP3 pin 13) is provided to latch the data. Data is valid on the rising edge of RDY. Connector JP3 has one ground pin (JP3 pin 14). Connect this pin to the data receiving system's digital ground.

MSB-First Data (MSBF = 0)



MSB-First Data (MSBF = 1)



*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY.

t_{DATA}: DURING THIS TIME, THE BIAS CIRCUIT AND THE COMPARATOR POWER DOWN AND THE REFERENCE INPUT BECOMES A HIGH IMPEDANCE NODE. WITH $\overline{CS}$ LOW AND THE CLOCK ACTIVE, THE OUTPUT ON D_{OUT} IS EITHER LSB-FIRST DATA (MSBF = 0) OR ZEROS (MSBF = 1).

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Figure 1. Timing Diagram

OPERATION

The LTC1298's data word can be acquired with a logic analyzer. By using a logic analyzer that has a PC-compatible floppy drive, (such as an HP1663A), conversion data can be stored on a disk and easily transferred to a PC. Once the data is transfered to a PC, programs such as Mathcad or Excel can be used to calculate FFTs. The FFTs can be used to obtain LTC1298 AC specifications such as signal-to-noise ratio and total harmonic distortion.

LEDs D0 to D11 provide a visual display of the LTC1298's digital output word. D0 is the LSB and D11 is the MSB. Jumper JP1 can be removed to disable the LEDs, reducing supply consumption by up to 56mA.

Driving $\overline{CS}$, D_{IN}, and CLK

Jumpers for $\overline{CS}$, CLK, D_{IN}, and D_{OUT} (JP2) are shorted for normal operation. The jumpers can be removed and $\overline{CS}$, D_{IN}, and CLK lines can be externally driven if desired. See the LTC1298 data sheet for details on driving these lines.

LAYOUT

The use of separate analog and digital ground planes is a good practice for a well designed LTC1298 PC board. The proper way to make the analog and digital ground planes can be seen by examining the solder side of the PCB layout. The two ground planes are completely isolated except for one connection at the power supply ground input, E1. The two ground planes follow the same path on the component and solder sides of the board to reduce coupling between the ground planes. Also ensure that the analog ground plane's solder side has a limited number of plane-breaking traces within it. Any trace that opens a portion of the ground plane may reduce the ground plane's efficiency. Further, the analog and digital traces do not cross each other (whether on the board's top or bottom side) or run adjacent to each other.

BYPASSING

It is important to place the supply/reference bypass capacitor as close as possible to the LTC1298's supply/reference pin. The ground side of the capacitor should have a very short path to analog ground. The V_{CC}/V_{REF} pins should be bypassed with high quality ceramic capacitors of at least 0.1µF.

Table 1.

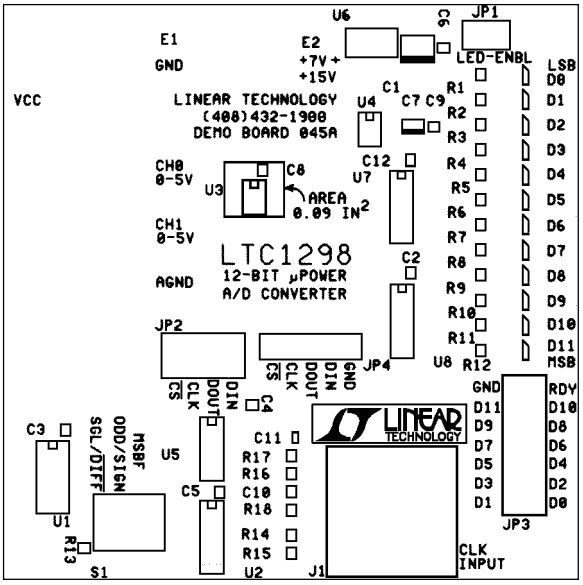
JUMPER	JUMPER NAME	JUMPER CONNECTION
JP1	LED Enable	Shorted to enable LEDs. Open to disable the LEDs.
JP2A	$\overline{CS}$	Shorted for normal operation. If open, the $\overline{CS}$ line can be driven externally to select or deselect the LTC1286.
JP2B	CLK	Shorted for normal operation. If open, the CLK line can be driven externally to clock the LTC1286.
JP2C	D_{OUT}	Shorted for normal operation. If open, the D_{OUT} line can drive a scope probe.
JP2D	D_{IN}	Shorted for normal operation. If open, the D_{IN} line can be driven externally to configure the input multiplexer.

OPERATION

Table 2.

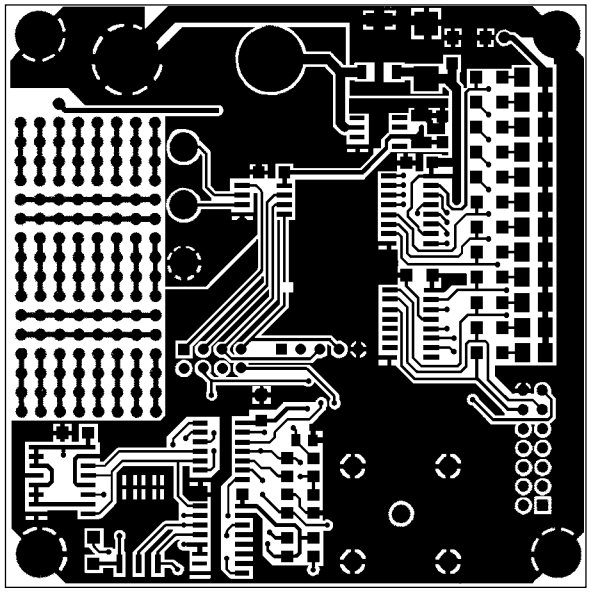
INPUT/OUTPUT PIN	FUNCTION
J1	Clock Input
E1	Ground
E2	7V to 15V at ≥100mA
CH0	Multiplexer Input Channel 0
CH1	Mulitplexer Input Channel 1
AGND	Input signals' ground reference
JP3-1	D0 (LSB)
JP3-2	D1
JP3-3	D2
JP3-4	D3
JP3-5	D4
JP3-6	D5
JP3-7	D6
JP3-8	D7
JP3-9	D8
JP3-10	D9
JP3-11	D10
JP3-12	D11 (MSB)
JP3-13	RDY. Can be used by an external system to latch the ADC's output. Latch data on the rising edge.
JP3-14	Ground. Connect to the digital ground of a data receiving system.

PCB LAYOUT AND FILM

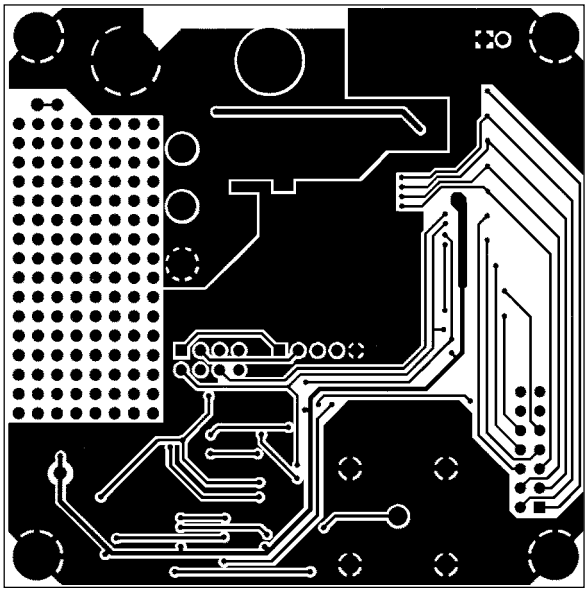


Component Side Silkscreen

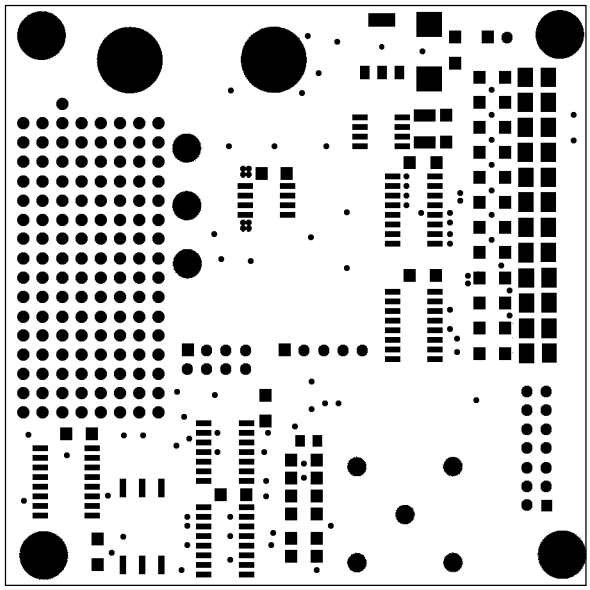
PCB LAYOUT AND FILM



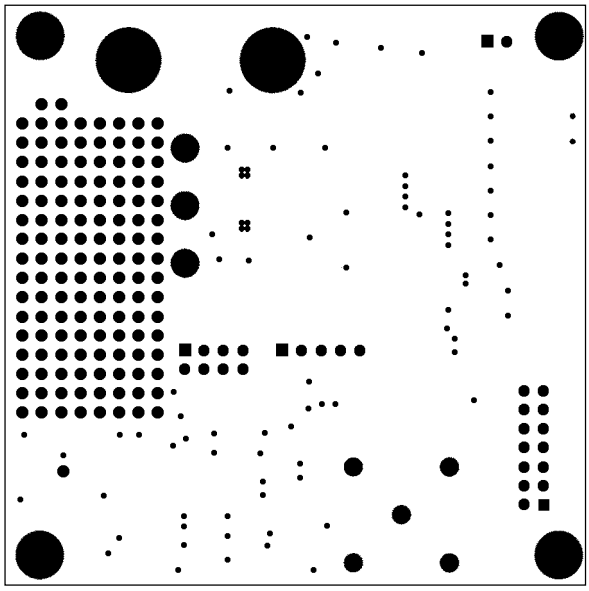
Circuit: Component Side



Circuit: Solder Side



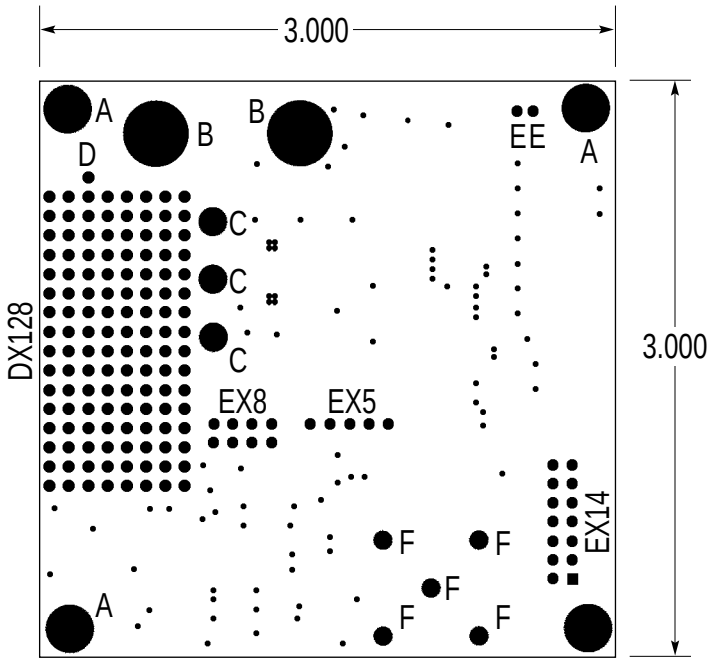
Component Side Solder Mask



Solder Side Solder Mask

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

PC FAB DRAWING



NOTES:
1. MATERIAL IS FR4, 0.062″ THICK WITH 2 OUNCE COPPER.
2. PCB WILL BE DOUBLE-SIDED WITH PLATED THROUGH-HOLES.
3. HOLE SIZES ARE AFTER PLATING. PLATED THROUGH-HOLE WALL THICKNESS MINIMUM 0.0014″ (1OZ.).
4. USE PADMASTER PROCESS.
5. SOLDER MASK BOTH SIDES WITH PC401 USING FILM PROVIDED.
6. SILKSCREEN COMPONENT SIDE USING FILM PROVIDED. USE WHITE, NON-CONDUCTIVE INK.
7. ALL DIMENSIONS ARE IN INCHES.

SYMBOL	DIAMETER	# OF HOLES
A	0.125	4
B	0.210	2
C	0.094	3
D	0.035	129
E	0.040	29
F	0.045	5
UNMARKED	0.018	97
	TOTAL HOLES	269

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