Monaural Power Amplifier

Monolithic Linear IC

LA4815VH

Overview

The LA4815VH incorporates a 1−channel power amplifier with a wide operating supply voltage range built into a surface−mounted package. This IC also has a mute function and requires only a few external components, making it suitable for low−cost set design.

Features

- Built−in 1−channel Power Amplifier
  - Output Power 1 = 1.84 W typ. (V_{CC} = 12 V, R_L = 8 Ω, THD = 10%)
  - Output Power 2 = 1.55 W Typ. (V_{CC} = 9 V, R_L = 4 Ω, THD = 10%)
  - Output Power 3 = 0.36 W Typ. (V_{CC} = 6 V, R_L = 8 Ω, THD = 10%)
  - Output Power 4 = 0.23 W Typ. (V_{CC} = 5 V, R_L = 8 Ω, THD = 10%)
- Mute Function
- Selectable Voltage Gain: 2 Types
  - 26 dB/40 dB
    *Gain values between 26 and 40 dB can also be set by adding external components (two resistors).
- Only a few External Components
  - 4 Components/Total
- Wide Supply Voltage Range
  - 4 to 16 V
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Intercoms, Door Phones, Transceivers, Radios, Toys, Home Appliances with Voice Guidance, etc.

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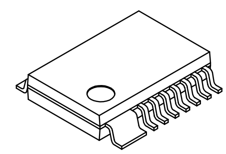
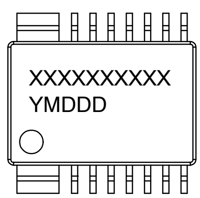


HSSOP14
CASE 944AA

MARKING DIAGRAM



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

ORDERING INFORMATION

Device	Package	Shipping†
LA4815VH−TLM−H	HSSOP14 (Pb−Free/ Halide Free)	2,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

SPECIFICATIONS

MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Power Supply Voltage	V_{CC} max		18	V
Allowable Power Dissipation	P_d max	*Mounted on the board	1.5	W
Operating Temperature	T_{opr}		−30 to +75	°C
Storage Temperature	T_{stg}		−40 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Mounted on Our evaluation board: Double−sided board with dimensions of 50 mm × 50 mm × 1.6 mm (glass epoxy).

OPERATING CONDITIONS (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Recommended Power Supply Voltage	V_{CC}		12	V
Recommended Load Resistance	R_L		4 to 32	Ω
Allowable Operating Supply Voltage Range	V_{CC} op		4 to 16	V

*The supply voltage level to be used must be determined with due consideration given to the allowable power dissipation of the IC.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω, f_{in} = 1 kHz)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Quiescent Current Drain − 1	I_{CCOP}1	No signal	–	5.3	9.5	mA
Quiescent Current Drain − 2	I_{CCOP}2	No signal, pin 3 = LOW	–	2.4	–	mA
Maximum Output Power − 1	POMAX1	THD = 10%	1.2	1.84	–	W
Maximum Output Power − 2	POMAX2	THD = 10%, V_{CC} = 9 V, R_L = 4 Ω	–	1.55	–	W
Voltage Gain − 1	VG1	V_{IN} = −30 dB	23.9	25.9	27.9	dB
Voltage Gain − 2	VG2	V_{IN} = −40 dB, pin 4/pin 11 = GND	37	39.5	42	dB
Total Harmonic Distortion	THD	V_{IN} = −30 dB	–	0.125	0.7	%
Mute Attenuation	MT	V_{IN} = −10 dB, pin 3 = LOW	−90	−115	–	dBV
Output Noise Voltage	V_NOUT	R_g = 620 Ω, 20 to 20 kHz	–	40	100	μVrms
Ripple Rejection Ratio	SVRR	R_g = 620 Ω, f_r = 100 Hz, V_r = −20 dBV	–	44	–	dB
Mute Control Voltage − Low	V3cntL	Mute mode	–	–	0.3	V
Mute Control Voltage − HIGH1	V3cntH1	Mute released, V_{CC} = 6.5 V or lower	1.8	–	–	V
Mute Control Voltage − HIGH2	V3cntH2	Mute released, V_{CC} = 6.5 V or higher	2.4	–	–	V
Input Resistance	R_i		–	100	–	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

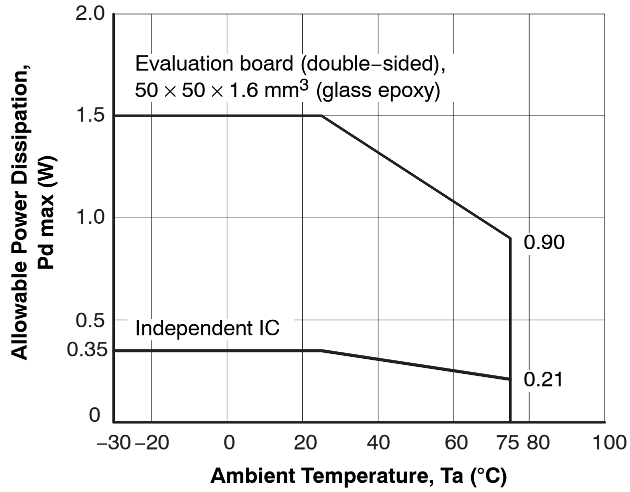
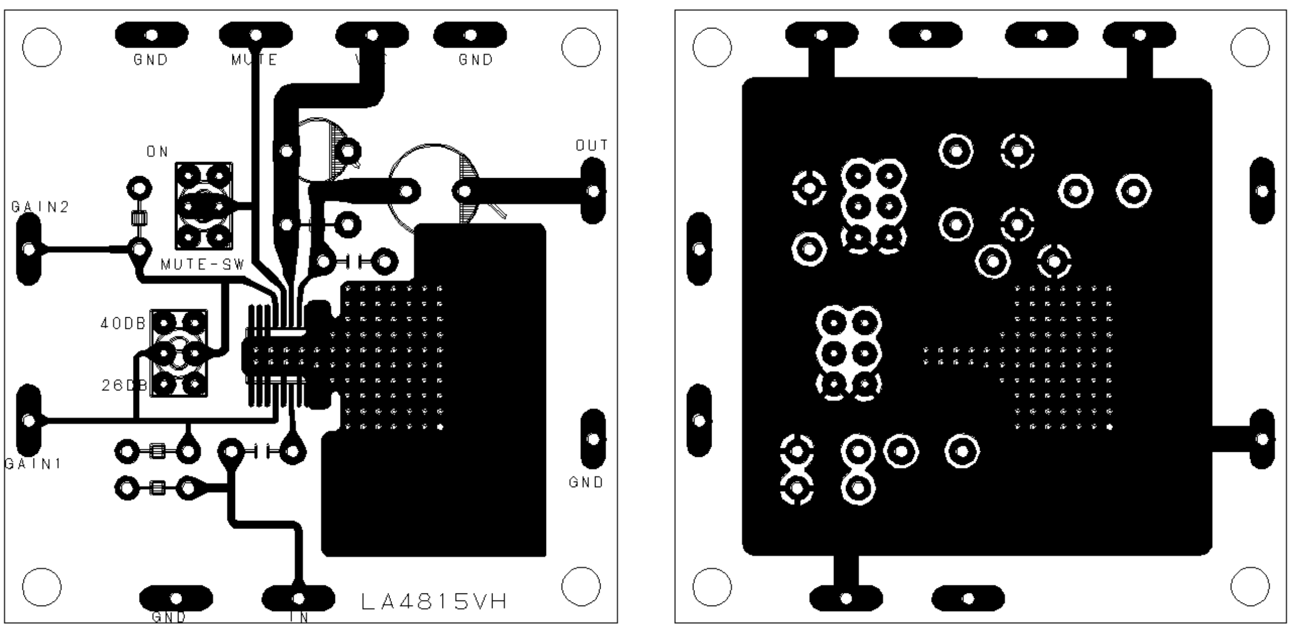


Figure 1. P_d max – T_a

EVALUATION BOARD



Top Layer (Top View)

Bottom Layer (Top View)

Figure 2. Double−sided Circuit Board (Dimensions: 50 mm × 50 mm × 1.6 mm)

BLOCK DIAGRAM AND SAMPLE APPLICATION CIRCUIT

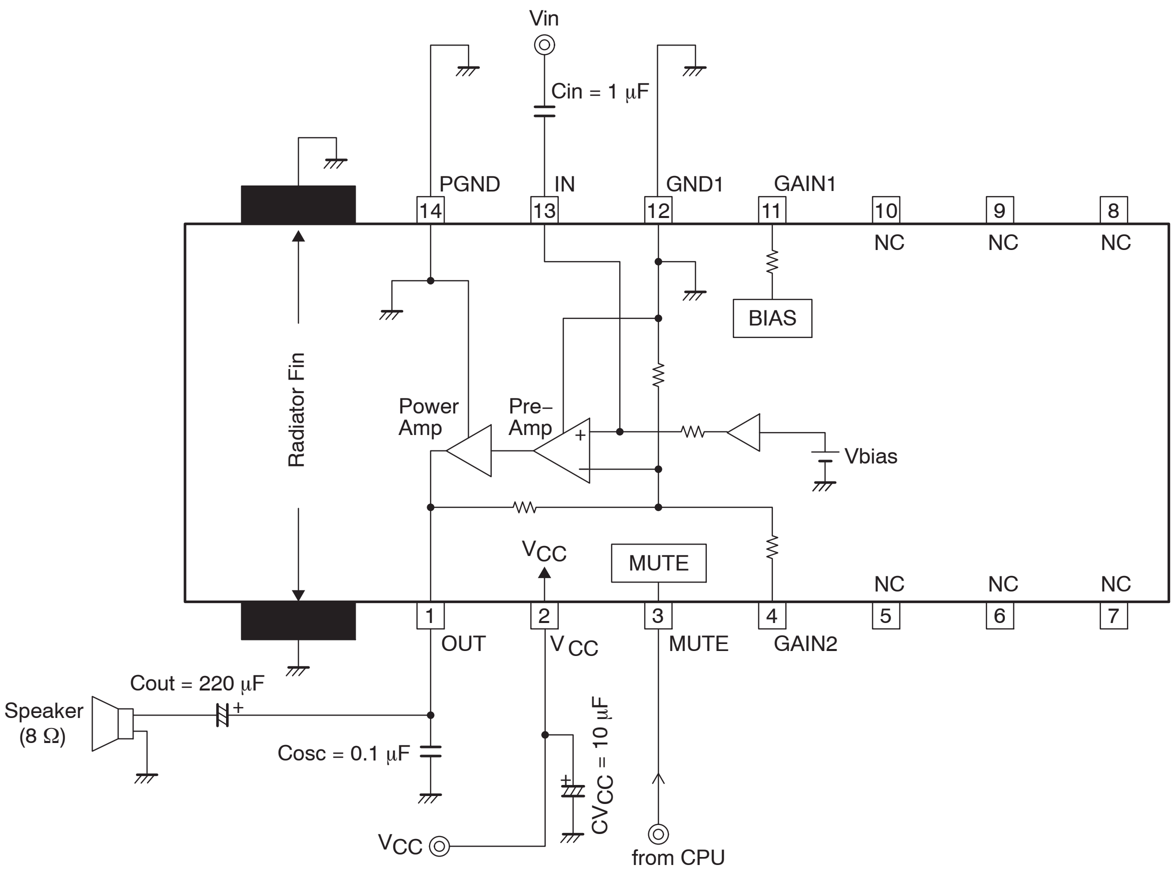


Figure 3. Block Diagram and Sample Application Circuit

TEST CIRCUIT

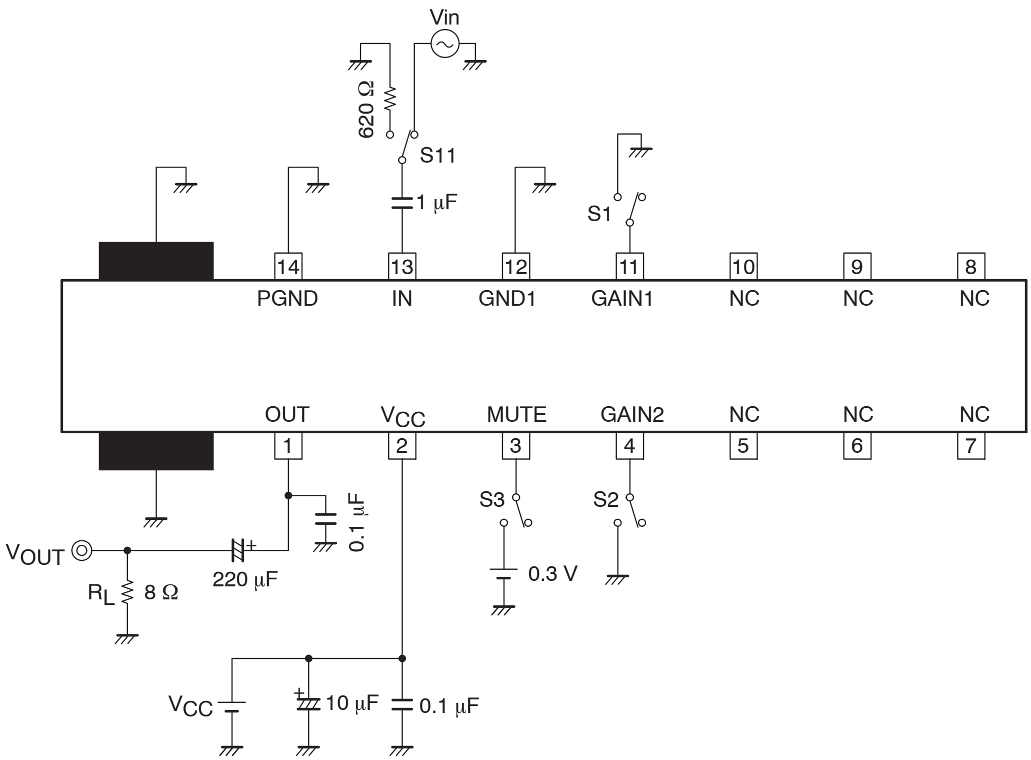
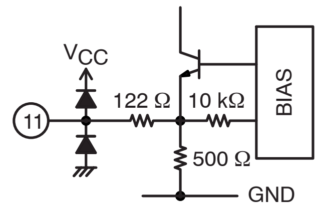
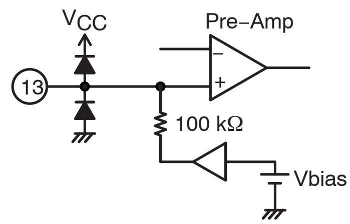
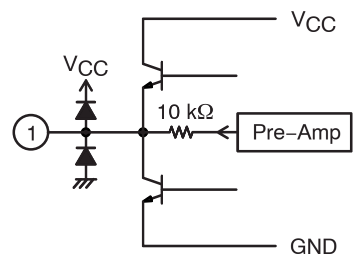
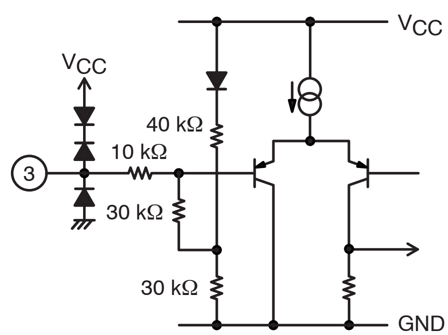
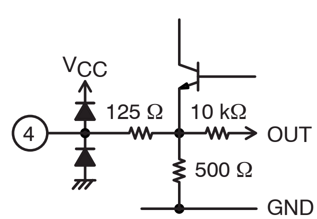


Figure 4. Test Circuit

PIN FUNCTIONS

PIN FUNCTIONS

Pin No.	Pin Name	Pin Voltage (V_{CC} = 12 V)	Description	Equivalent Circuit
11	GAIN1	0.35	Gain switching pin • 26 dB mode when left open • 40 dB mode when connected to ground (Both pins 11 and 4 must be reconfigured at the same time)	
12	GND1	0	Preamplifier system ground pin	
13	IN	1.7	Input pin	
14	PGND	0	Power amplifier ground pin	
1	OUT	5.9	Power amplifier output pin	
2	V_{CC}	12	Power supply pin	
3	MUTE	4.9	Mute control pin • Mute ON ⇒ Low • Mute OFF ⇒ High	
4	GAIN2	0.35	Gain switching pin • 26 dB mode when left open • 40 dB mode when connected to ground (Both pins 11 and 4 must be reconfigured at the same time)	

Notes on Using IC

1. Voltage Gain Settings (Pins 4 and 11)

The voltage gain of the power amplifier is fixed by the internal resistors.

- Pins 4 and 11 be left open: Approximately 26 dB
- Pins 4 and 11 connected to GND: Approximately 39.5 dB

Note that the voltage gain can be changed using two resistors. (See Figure 5)

- Voltage gain setting: According to the resistor connected between Pin 4 and Pin 12 (GND1)

$$\text{Voltage gain} = 20\log\left(20 \times \frac{625 + Rvg1}{125 + Rvg1}\right)$$

- Output DC voltage setting: According to the resistor connected between Pin 11 and Pin 12 (GND1)
  - Rvg1 = Rvg2 must be satisfied.

In addition, the voltage gain can also be lowered to approximately 20 dB (when using 5 V or 6 V power supply) by an application such as shown in Figure 6 below.

- Voltage gain setting: According to the resistor connected between Pin 4 and Pin 1 (OUT)

$$\text{Voltage gain} = 20\log\left(20 \times \frac{125 + Rvg3}{10{,}125 + Rvg3}\right)$$

- Output DC voltage setting: According to the resistor connected between Pin 11 and Pin 2 (V_{CC}).
  - Set the resistor values so that the Pin 5 (OUT) DC voltage is approximately half the supply voltage.
    Example:
    When Rvg3 = 10 kΩ, Rvg4 = 22 kΩ
    (when V_{CC} = 6 V)

However, note that using this method to greatly lower the voltage gain deteriorates the characteristics, so the voltage gain should be lowered only to approximately 20 dB. In addition, when using a high supply voltage (7 V or more), the clipped waveform may invert, so this voltage gain reduction method must not be used in these cases.

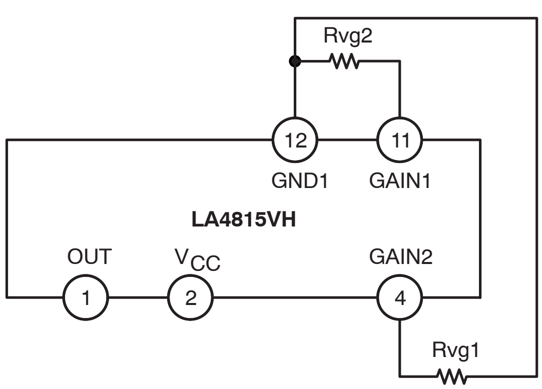


Figure 5.

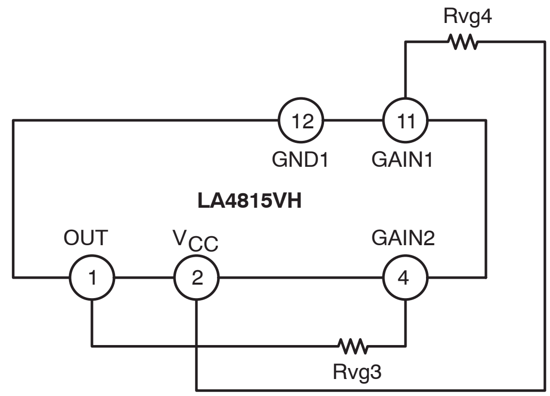


Figure 6.

2. Signal Source Impedance: rg

Since the input coupling capacitor Cin affects the ripple rejection ratio, the signal source impedance value rg, which is associated with this capacitor, also affects the ripple rejection ratio, so rg should be as small as possible. Therefore, when attenuating the signal at the Cin front end as shown in Figure 8, the constants should be set in consideration of these characteristics. Using the smallest resistor Rg1 value possible is recommended.

In addition, when setting the signal level, the voltage gain should be set on the LA4815VH side and the input front−end should be configured using only the input coupling capacitor, Cin, as shown in Figure 9 in order to maximize the ripple rejection ratio.

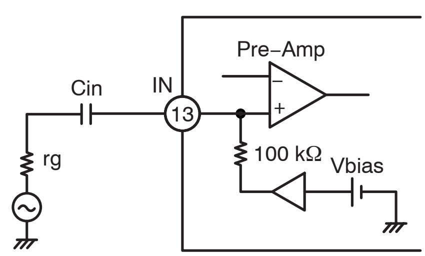


Figure 7.

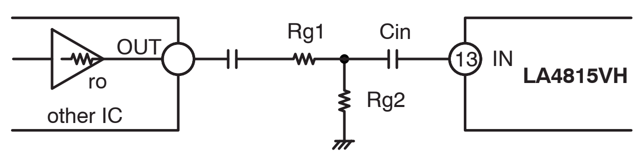


Figure 8.

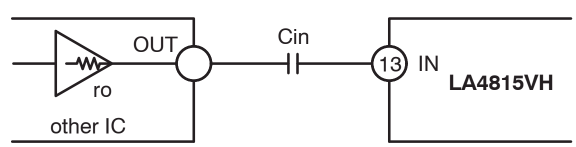


Figure 9.

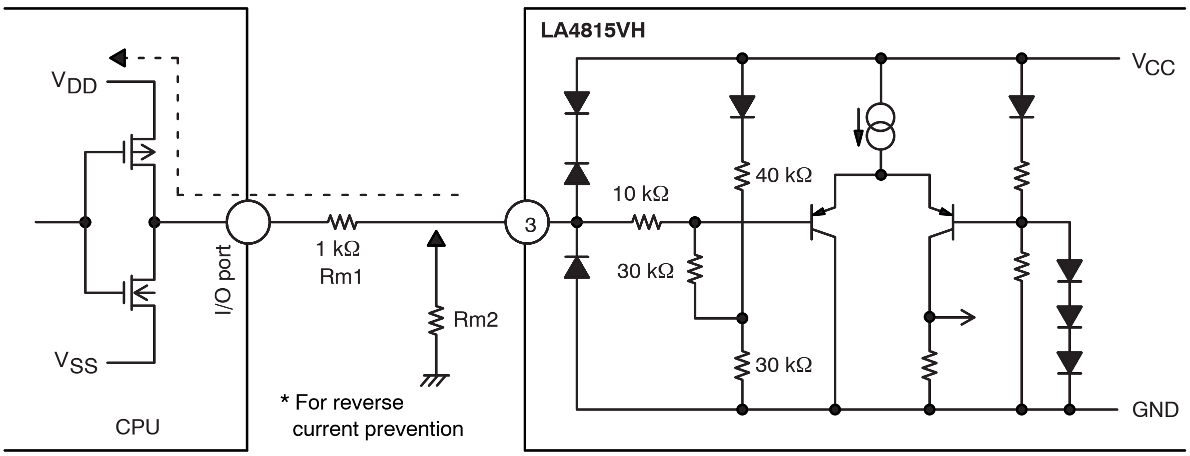
3. Mute Control Pin (Pin 3)

The internal power amplifier circuit can be disabled and audio mute is turned on by controlling the voltage applied to Pin 3. Control can be performed directly using the CPU output port, but digital noise from the CPU may worsen the LA4815VH noise floor. Therefore, inserting a series resistor, Rm1 (1 to 2.2 kΩ) as shown in Figure 10, is recommended.

- Mute ON: Low
- Mute OFF: High or open

In addition, the Pin 3 DC voltage is dependent on the supply voltage, so a reverse current flows to the CPU power supply line when the Pin 3 voltage is higher than the CPU supply voltage. In these cases, connect a resistor, Rm2 (see Figure 11) between Pin 3 and GND to lower the Pin 3 DC voltage as shown in Figure 10.

Note that when not using the mute function, Pin 3 must be left open.



Reverse current prevention resistor value: Rm2 (reference value) ← When V3 is set to approximately 2.5 V

Figure 10.

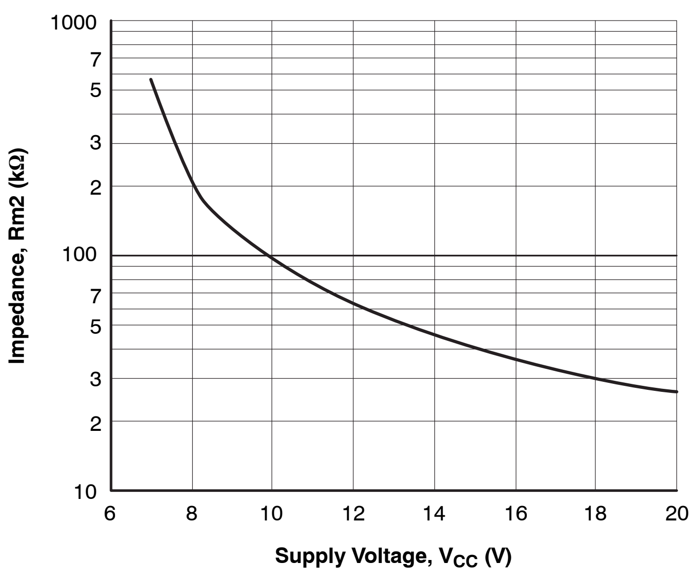


Figure 11. Rm2 – V_{CC}

4. Mute Control Timing

When performing mute control, exercise control at the timing shown in Figure 12.

- During power−on: Twu = 0 to 50 ms
  - Pins 2 and 3 can also rise simultaneously.
- During power−off: Twd = 100 to 200 ms

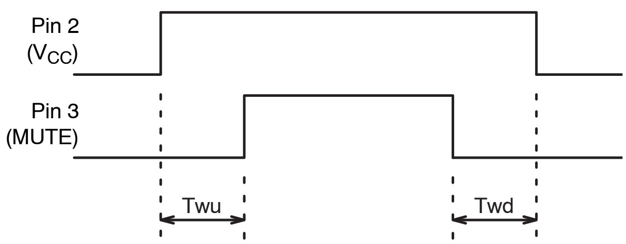


Figure 12.

5. Popping Noise Reduction During Power−Off

The power supply line can be directly controlled ON and OFF without using the mute function. However, when using a high supply voltage, the shock noise and after sound during power−off tends to worsen. One method of coping with this is to connect a capacitor between Pin 2 (V_{CC}) and Pin 3 (MUTE) so that the auto mute function operates during power−off.

Recommended value = 1 μF.

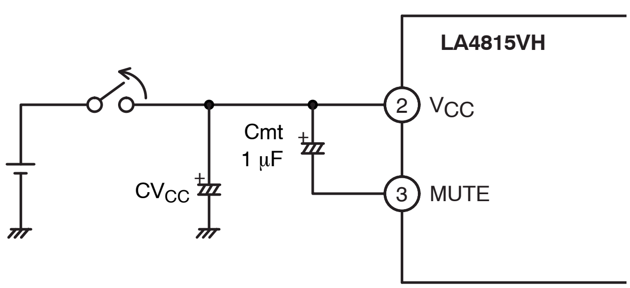


Figure 13.

6. Input Coupling Capacitor (Cin)

Cin is an input coupling capacitor, and is used for DC cutting. However, this capacitor is also used to improve the ripple rejection ratio, which changes according to the capacitance value (recommended value = 1 μF). In addition, this capacitor also affects the transient response characteristics during power−on and when mute is canceled, so the constant should be set in consideration of these characteristics.

Design reference value = approximately 0.33 to 3.3 μF

- Ripple Rejection Ratio: Increasing the capacitance value increases the rate, and reducing the value reduces the rate.
- Rise Response Speed: Increasing the capacitance value reduces the speed, and reducing the value increases the speed.
- Popping Noise: Increasing the capacitance value reduces the noise, and reducing the value increases the noise.

7. Output Coupling Capacitor (Cout)

Cout is an output coupling capacitor used for DC cutting. However, this capacitor, Cout, in combination with load impedance RL forms a high−pass filter and attenuates the low frequency signals. Take into account the cutoff frequency when determining the capacitance value. In addition, normally a chemical capacitor is used for this capacitor, but the capacitance value of chemical capacitors decreases at low temperatures, so the value should be set in accordance with this characteristic.

The cutoff frequency is expressed by the following formula.

$$f_c = \frac{1}{2\pi \times R_L \times C_{out}}$$

8. Output Phase Compensation Capacitor (Cosc)

The Cosc capacitor is used to prevent output oscillation. Use a ceramic capacitor (recommended value = 0.1 μF) with good high frequency characteristics, and locate this capacitor as close to the IC as possible.

9. Power Supply Capacitor (CV_{CC})

The CV_{CC} capacitor is used to suppress the ripple component of the power supply line. Normally a chemical capacitor (recommended value = 10 μF) is used for this capacitor. However, chemical capacitors have poor high frequency characteristics, so when using a CPU, DSP or other IC that generates digital noise in the set, it is recommended that a power supply bypass capacitor (ceramic capacitor, recommended value = approximately 0.1 μF) be added to reject high−frequency components. Locate this bypass capacitor as close to the IC as possible.

10. NC Pin Treatment

Since the NC pins (pins 5 to 10) are connected to nothing internally, they may be left open. To increase the heat dissipation efficiency, however, it is recommended that the NC pins should be connected to the GND line.

11. Signal Mixing Methods

The following methods can be used to mix a beep, key tone or other signal into the audio signal. Note that when input to Pin 4 is selected, amplification of signals input from Pin 4 changes according to impedance Z4 connected to Pin 13.

A) Mixing method using resistors in the Pin 13 input front end:

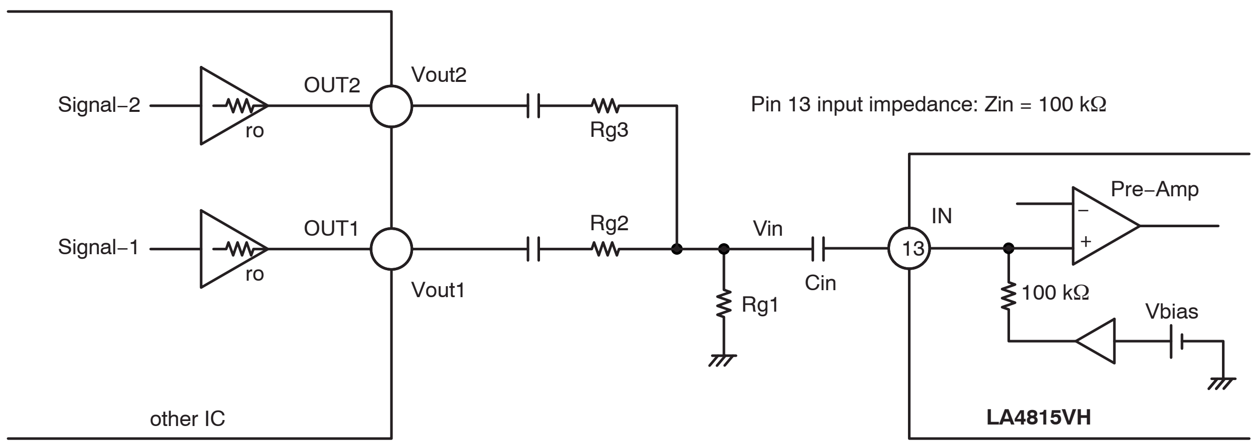


Figure 14.

B) Method using input to Pin 4:

- First signal system (Signal−1) voltage gain: Vg1

$$Vg1 = 20\log\left(\frac{Vout}{Vin1}\right) = 20\log\left[\frac{4 \times (125 + Z4) \times \left(500 + \left(125 \times \frac{Z4}{125+Z4}\right)\right)}{25 \times Z4}\right]$$

$*Z4 = R1 + ro$

- Second signal system (Signal−2) voltage gain: Vg2

$$Vg2 = 20\log\left(\frac{Vout}{Vin2}\right) = 20\log\left(\frac{10000}{125 + R1}\right)$$

$$*fc2 = \frac{1}{2\pi \times Cin2 \times (R1 + 125)}$$

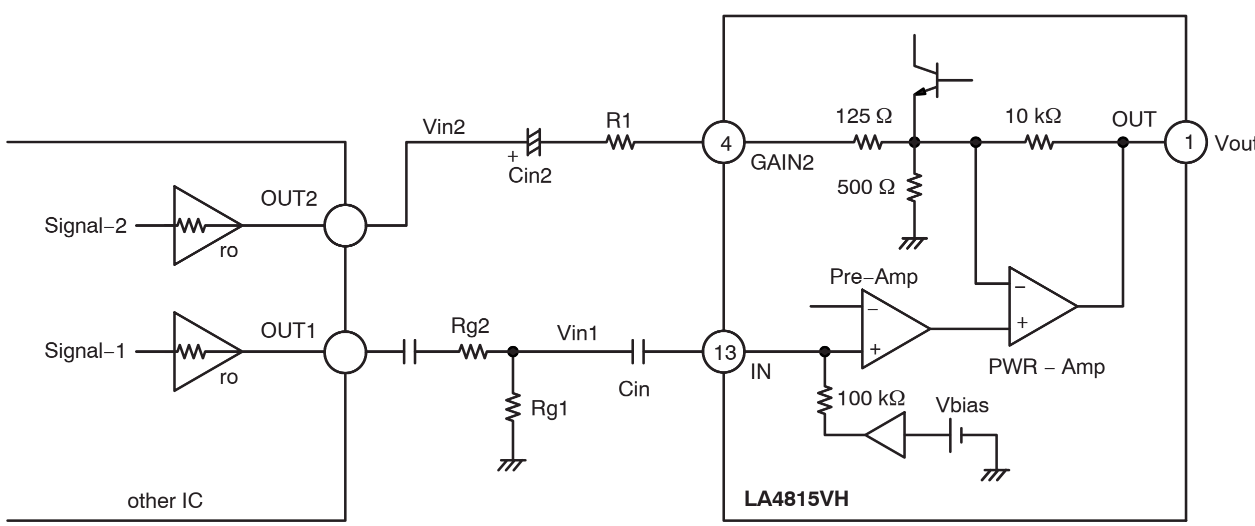


Figure 15.

12. Short−circuit between Pins

Turning on the power supply with some pins short−circuited may cause deterioration or breakdown. Therefore, when mounting the IC on a board, check to make sure that no short−circuit is formed between pins by solder or other foreign substances before turning on the power supply.

13. Load Short Circuit

Leaving the IC for a long time in the condition with a load short circuit may cause deterioration or breakdown. Therefore, never short−circuit the load.

14. Maximum Ratings

When used under conditions near the maximum ratings, even a slight fluctuation in the conditions may cause the maximum ratings to be exceeded, possibly resulting in a breakdown or other accidents. Therefore, always provide enough margin for fluctuations in the supply voltage and other conditions, and use within a range not exceeding the maximum ratings.

GENERAL CHARACTERISTICS

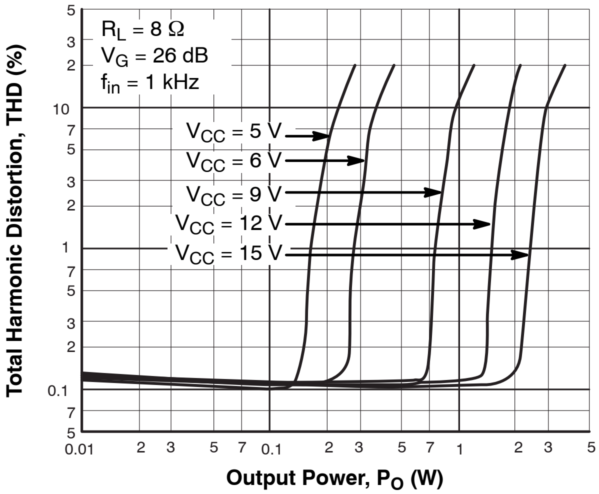


Figure 16. THD – P_O

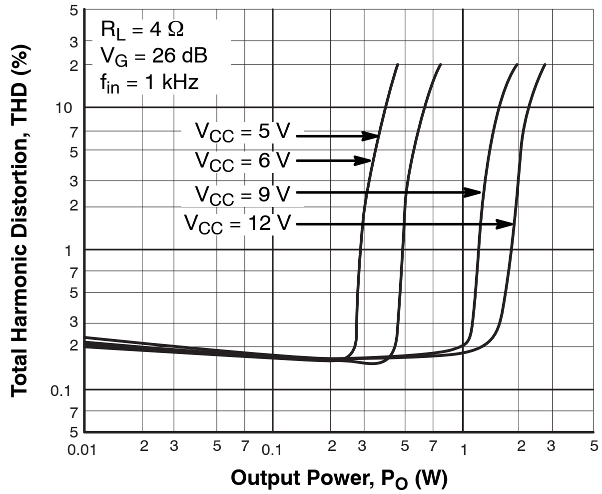


Figure 17. THD – P_O

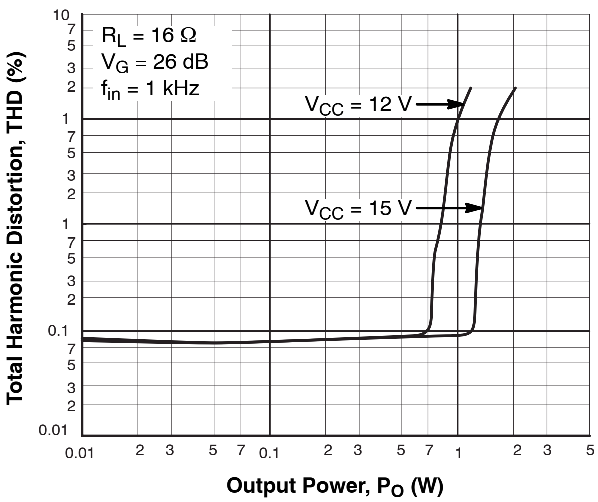


Figure 18. THD – P_O

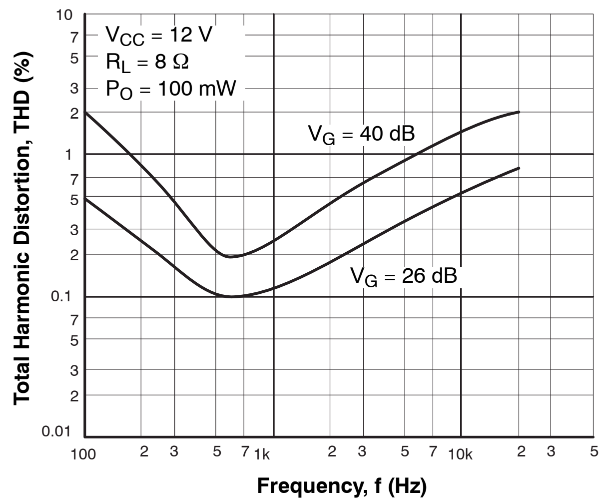


Figure 19. THD – f

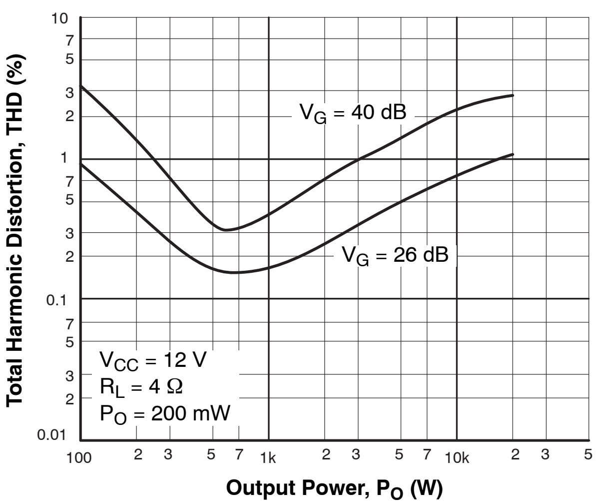


Figure 20. THD – f

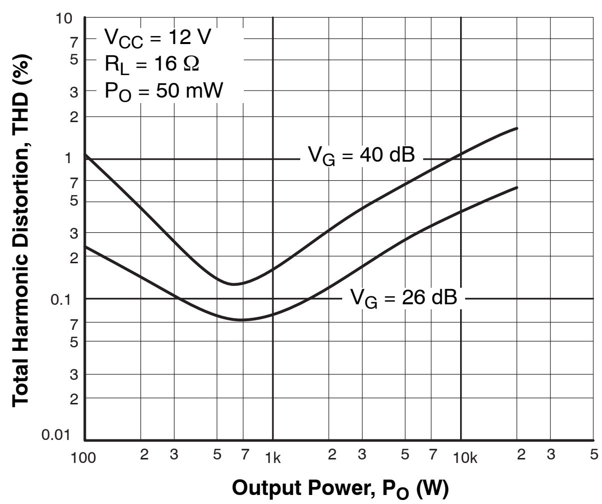


Figure 21. THD – f

GENERAL CHARACTERISTICS (Continued)

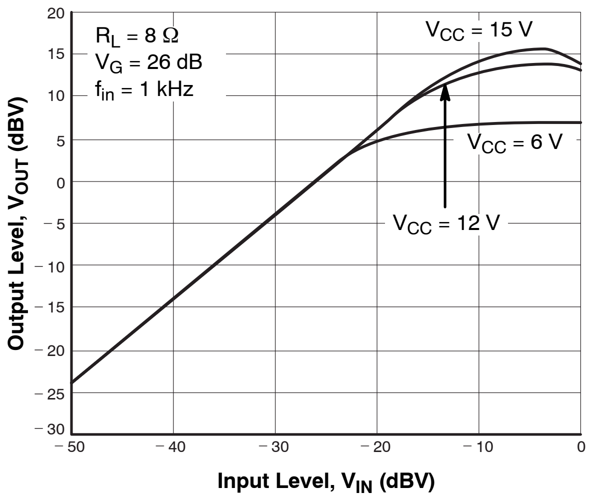


Figure 22. V_{OUT} – V_{IN}

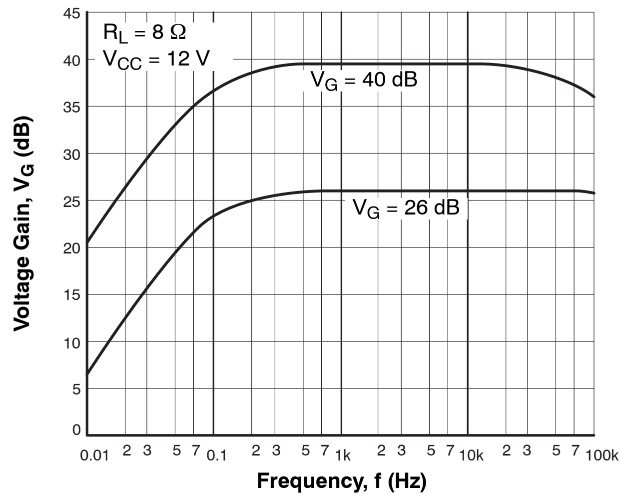


Figure 23. V_G – f

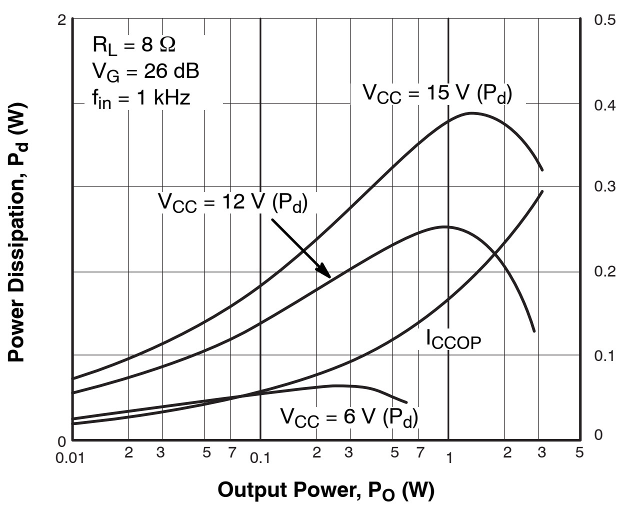


Figure 24. P_d – P_O

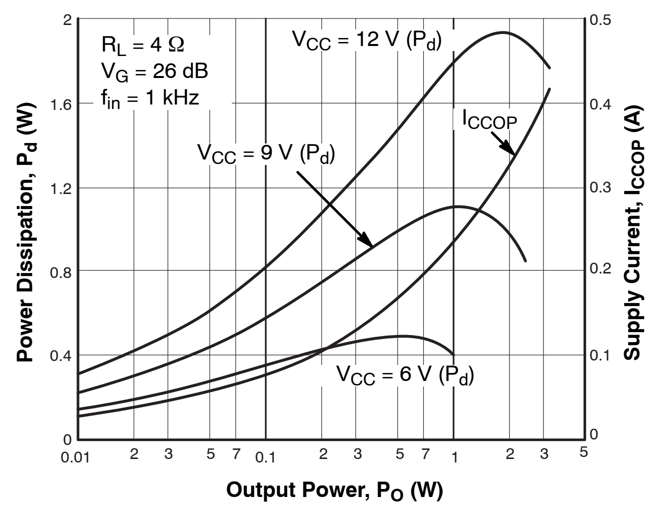


Figure 25. P_d – P_O

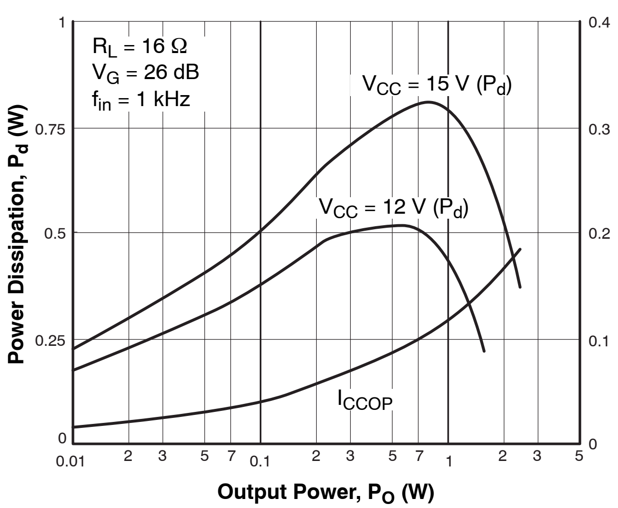


Figure 26. P_d – P_O

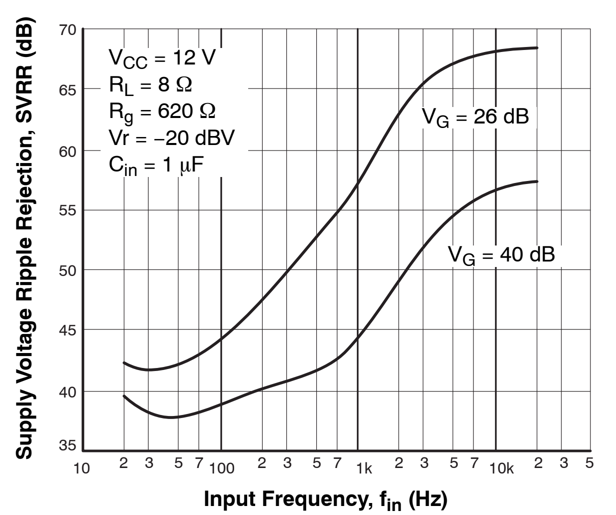


Figure 27. SVRR – f_{in}

GENERAL CHARACTERISTICS (Continued)

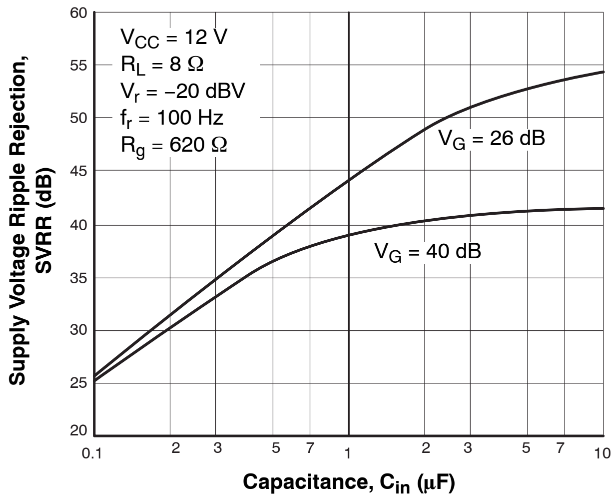


Figure 28. SVRR – C_{in}

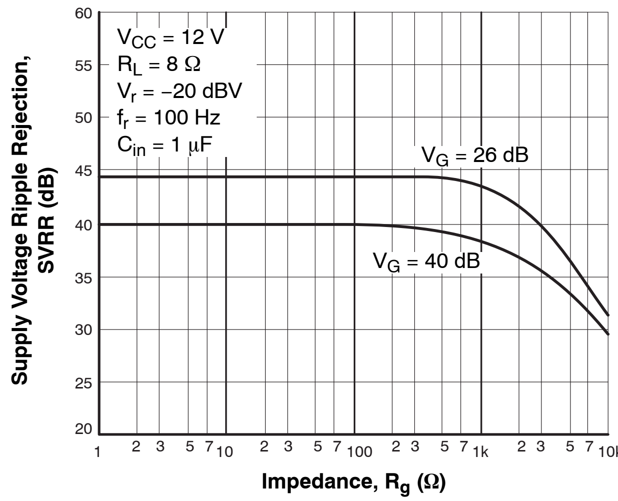


Figure 29. SVRR – R_g

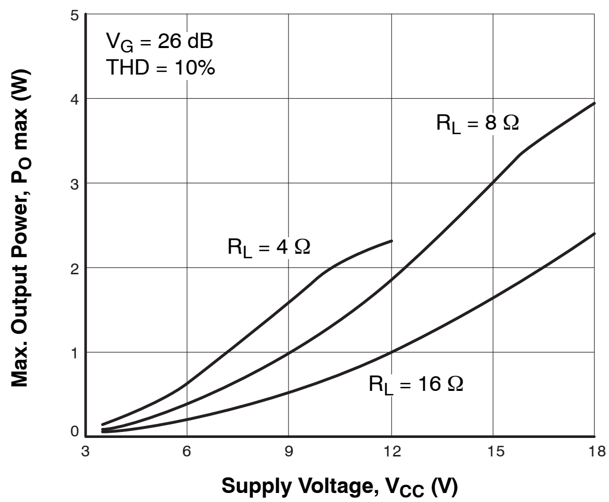


Figure 30. P_O max – V_{CC}

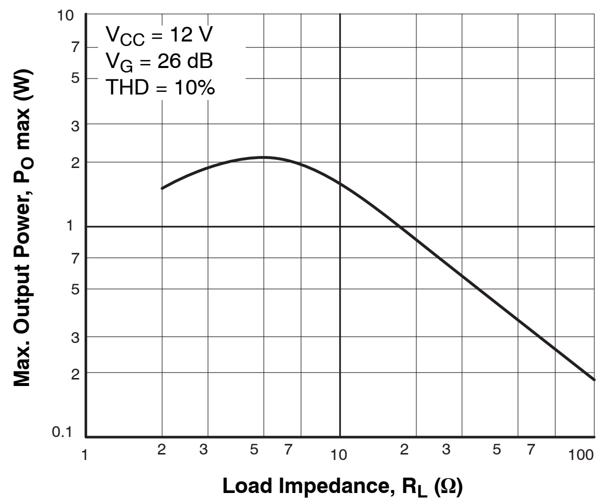


Figure 31. P_O max – R_L

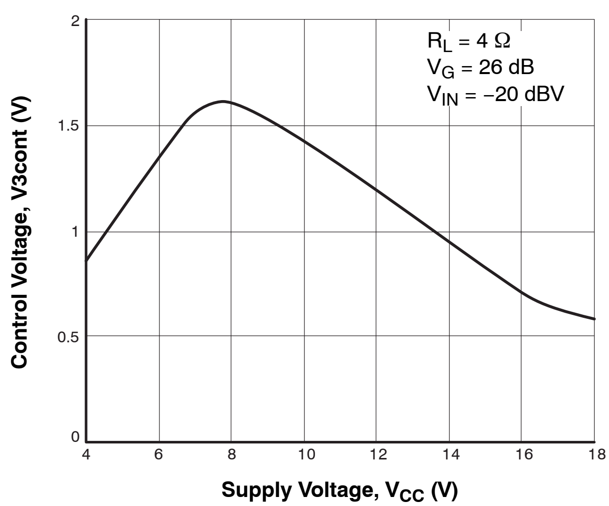


Figure 32. V3cont – V_{CC}

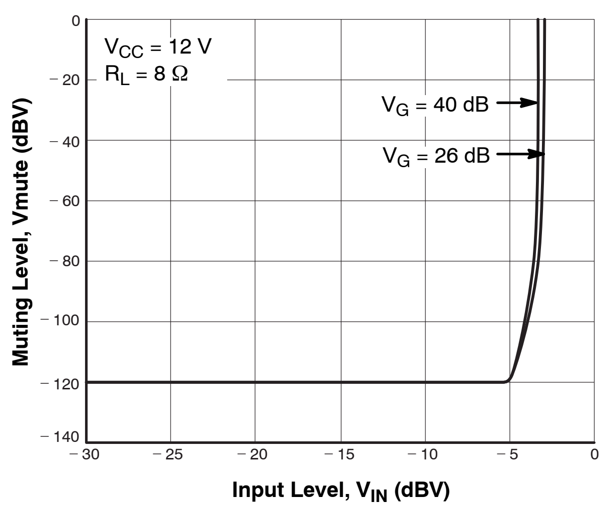


Figure 33. Vmute – V_{IN}

GENERAL CHARACTERISTICS (Continued)

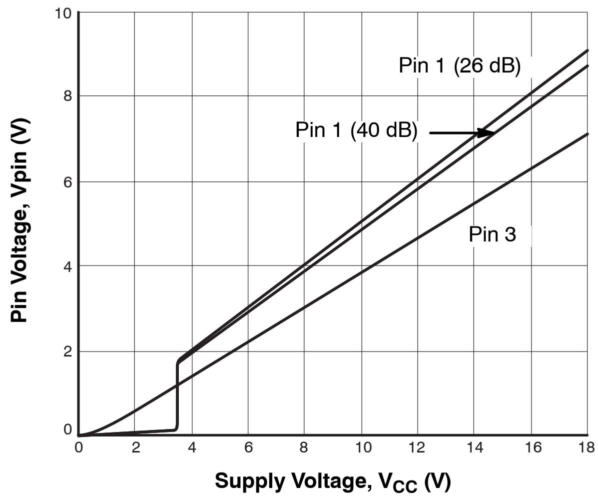


Figure 34. Vpin – V_{CC}

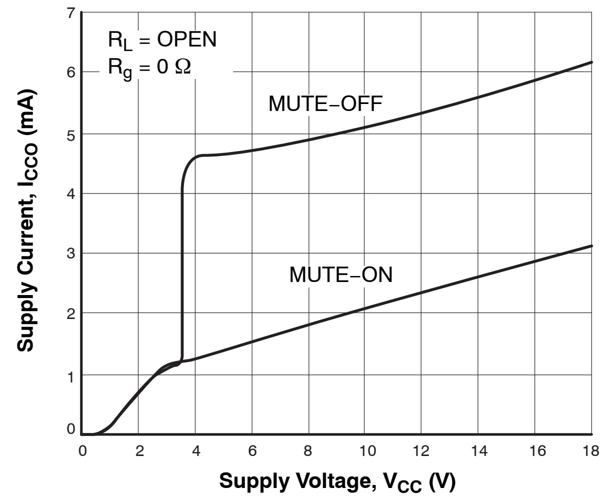


Figure 35. I_{CCO} – V_{CC}

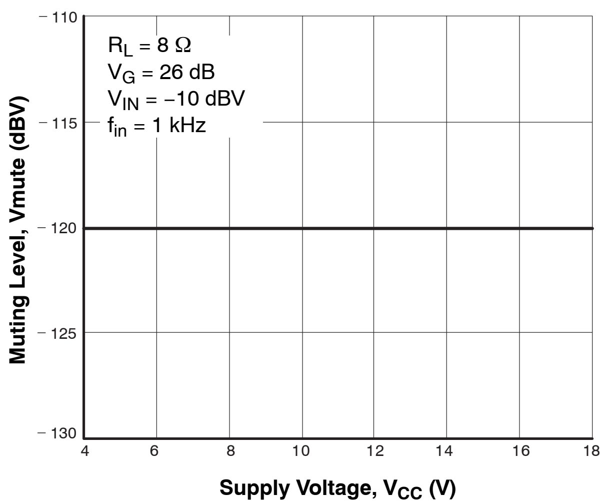


Figure 36. Vmute – V_{CC}

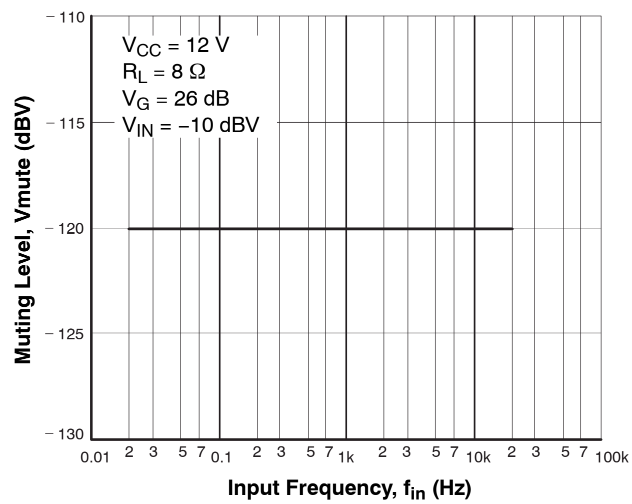


Figure 37. Vmute – f_{in}

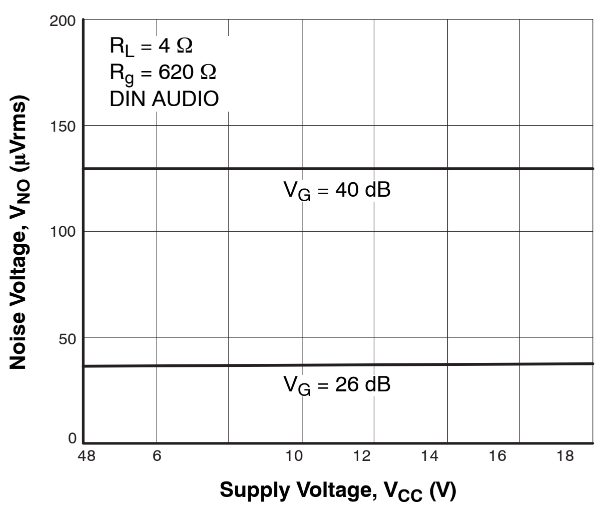


Figure 38. V_{NO} – V_{CC}

TEMPERATURE CHARACTERISTICS

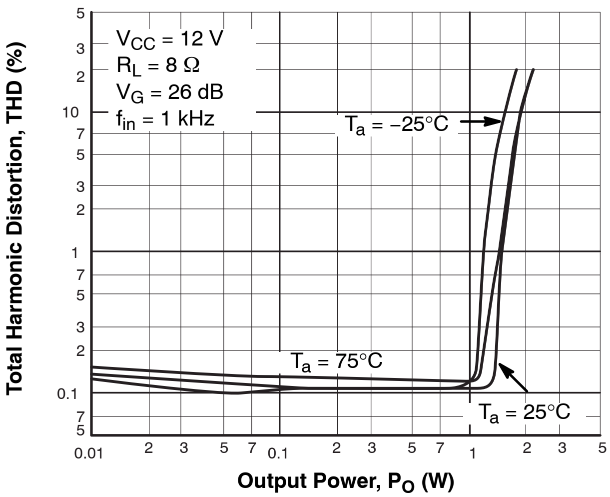


Figure 39. THD – P_O

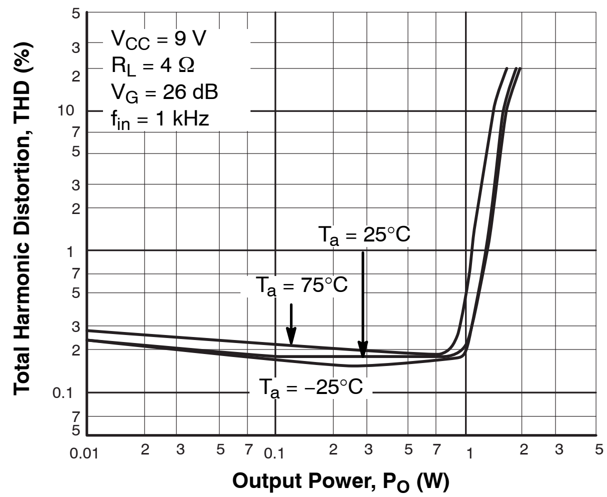


Figure 40. THD – P_O

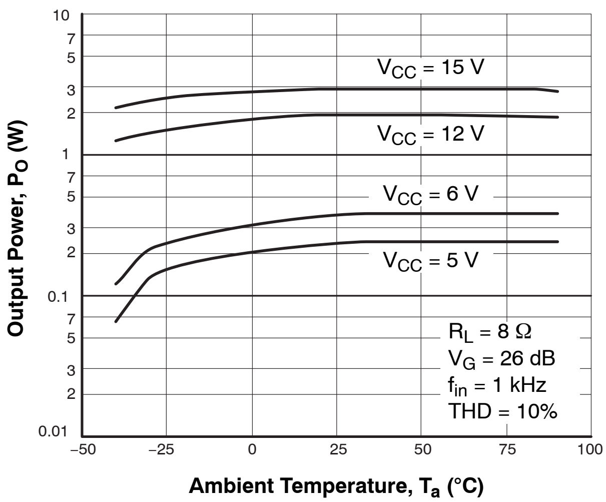


Figure 41. P_O – T_a

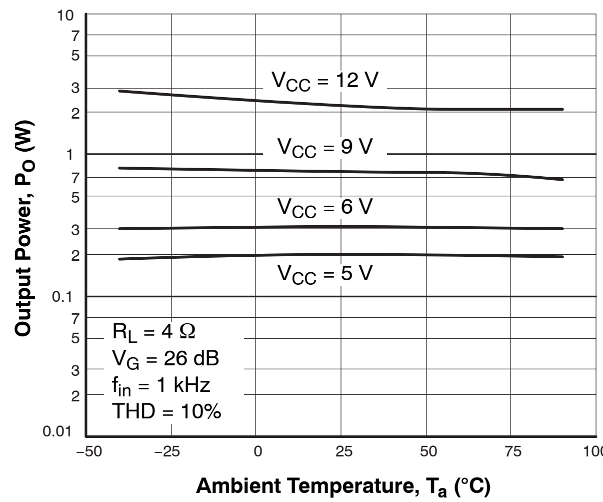


Figure 42. P_O – T_a

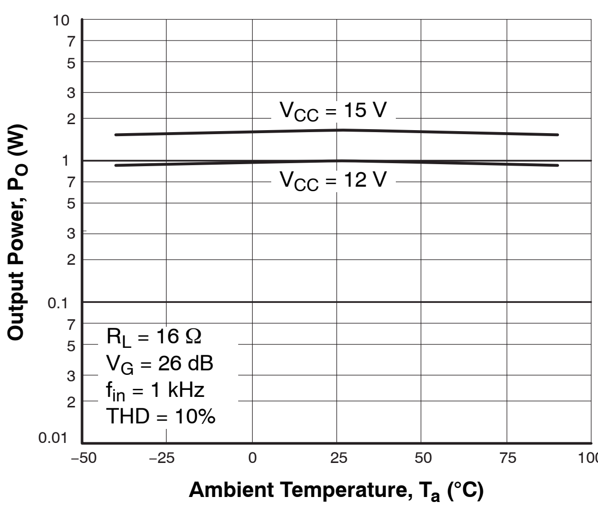


Figure 43. P_O – T_a

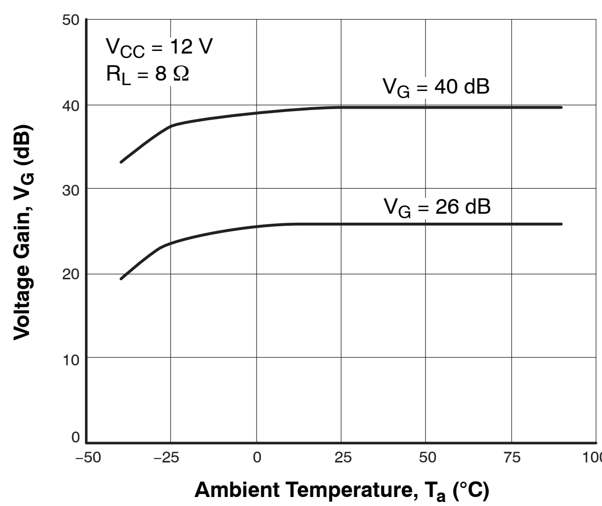


Figure 44. V_G – T_a

TEMPERATURE CHARACTERISTICS (Continued)

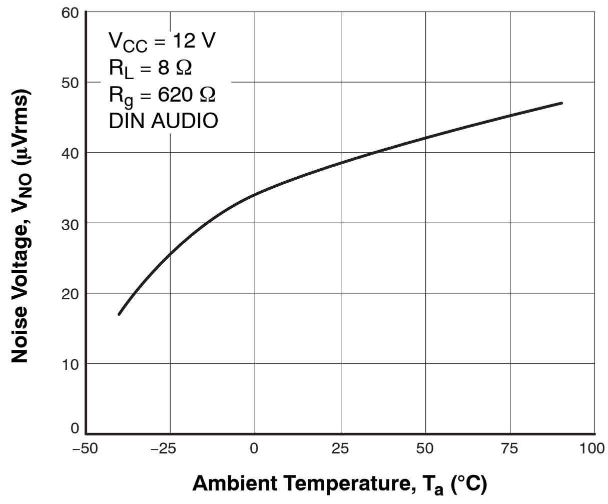


Figure 45. V_{NO} − T_a

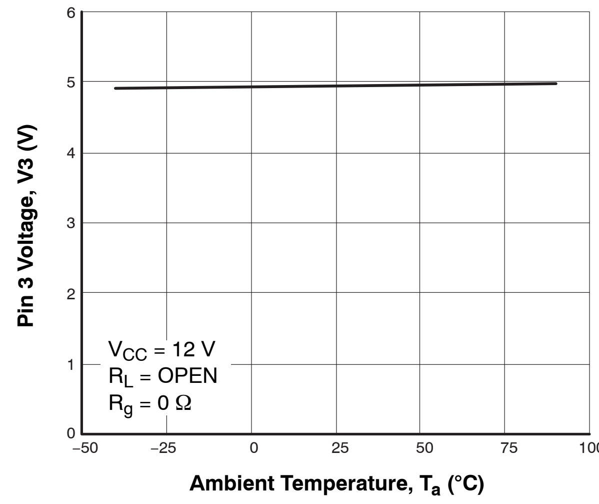


Figure 46. V3 − T_a

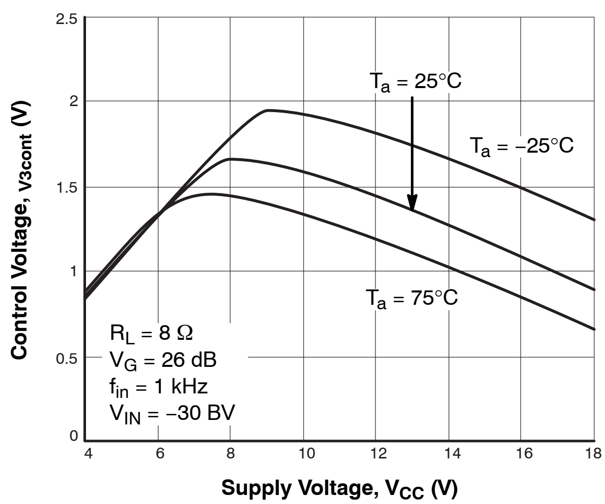


Figure 47. V3cont − V_{CC}

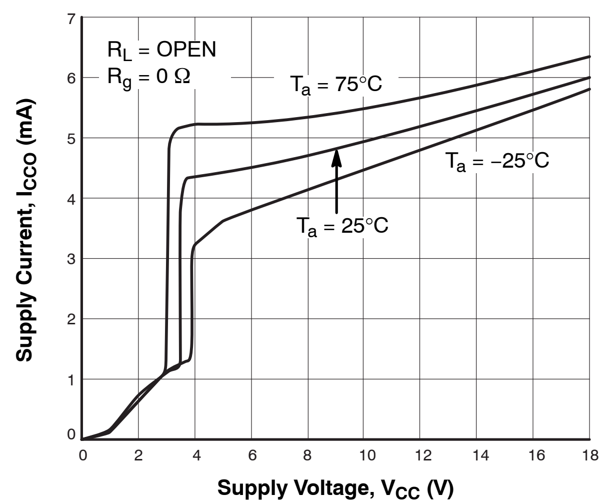
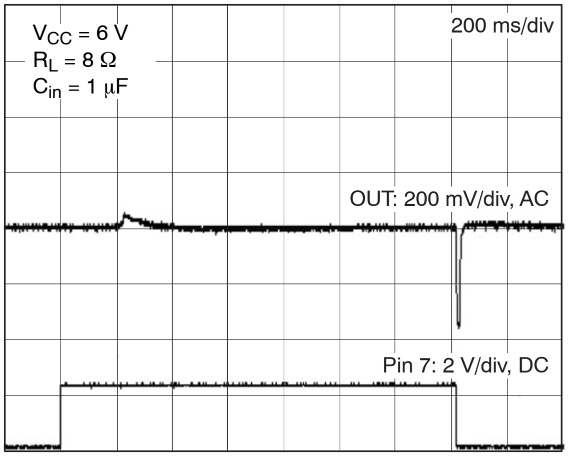


Figure 48. I_{CCO} − V_{CC}

MUTING ON AND OFF TRANSIENT CHARACTERISTICS



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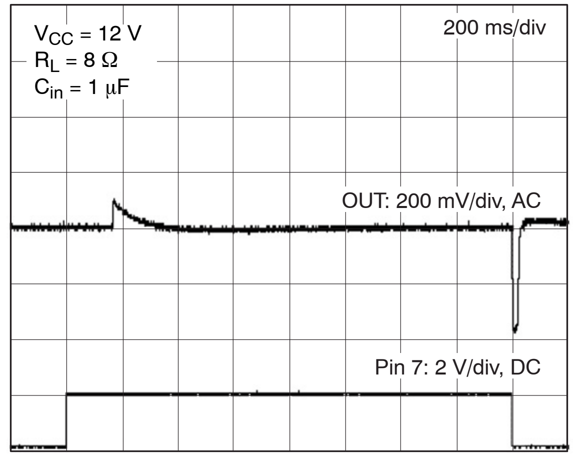


Figure 50.

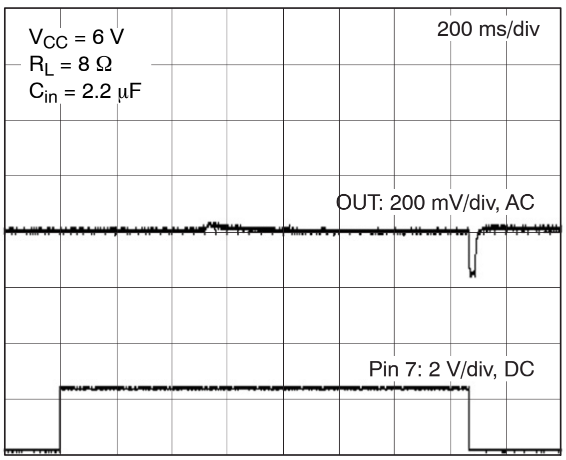


Figure 51.

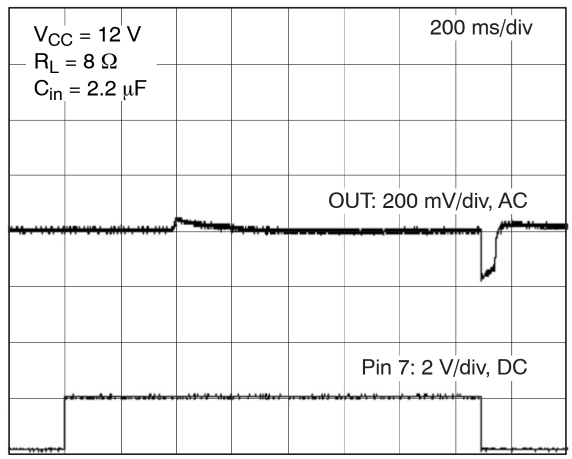
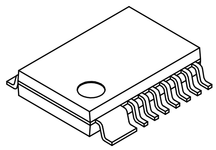
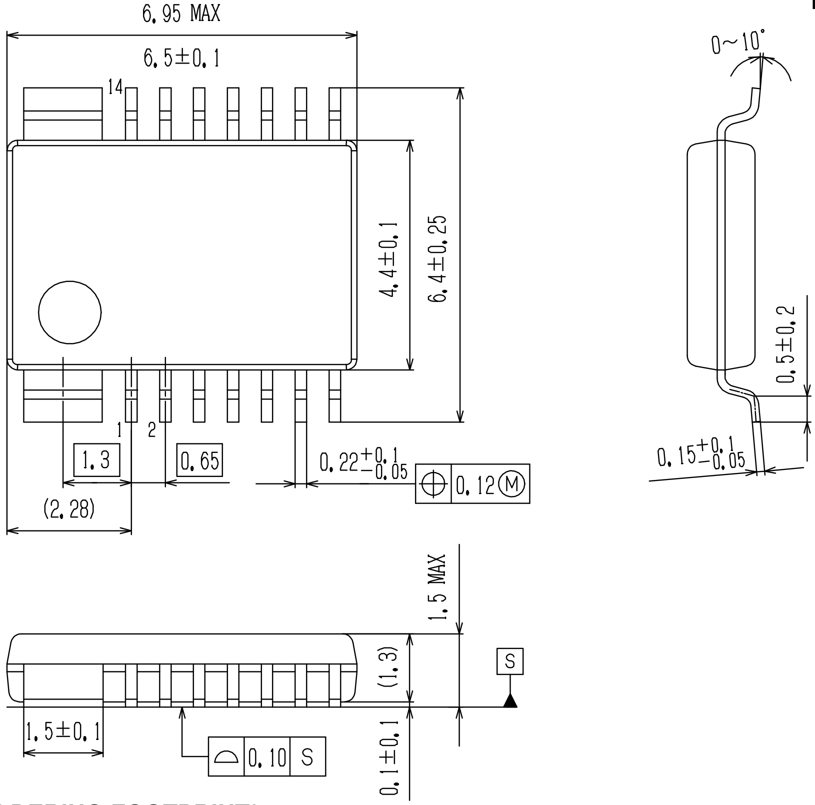


Figure 52.

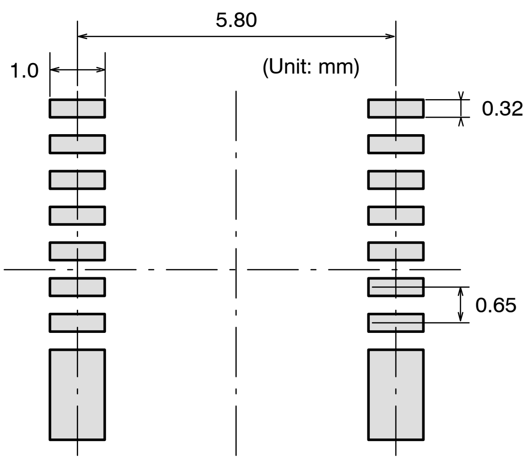


HSSOP14 (225mil)
CASE 944AA
ISSUE A

DATE 23 OCT 2013



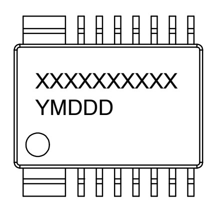
SOLDERING FOOTPRINT*



NOTES: 1. The measurements are not to guarantee but for reference only.
2. Land pattern design in Fin area to be altered in response to customer’s individual application.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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