

# EZRadioPRO<sup>®</sup> Family Rev B1B/B1C Device Errata

This document describes the errata for the following EZRadioPRO<sup>®</sup> devices:

- Si4060-B1B
- Si4460-B1B
- Si4461-B1B
- Si4063-B1B
- Si4463-B1B
- Si4362-B1B
- Si4438-B1C
- Si4464-B1B

To verify the revision of a chip, the ROMID replay field of the PART\_INFO API command can be used. All the revisions above correspond to ROMID = 3.

For a detailed description of the APIs referenced in this document, see the EZRadioPRO API Documentation available on the Silicon Labs website.

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## 1. Errata Summary

### Table 1.1. Errata Status Summary

Errata	Title/Problem	Workaround Available	Si4x60-B1B	Si4464-B1B				
Number			Si4461-B1B					
			Si4x63-B1B					
			Si4362-B1B					
			Si4438-B1C					
1.	If configured to skip sync and preamble on transmit, the TX data from the FIFO is corrupted.	Yes	+	+				
2.	When the CAL timer and Wakeup timer fire at the same time, the Wakeup timer function is skipped.	Yes	+	+				
3.	CHANGE_STATE to TX from TX is an invalid state transition.	Yes	+	+				
4.	TX packet abort does not reset the packet handler.	Yes	+	+				
5.	Packet re-transmit does not function as expected.	Yes	+	+				
6.	SPI active to Ready state without any SPI activity is not supported.	Yes	+	+				
7.	Non-zero BER in Low-Power mode at strong signal levels.	FW patch	+	+				
8.	RSSI jump interrupt API not supported	No	+	+				
9.	RSSI status is not reset upon START_RX.	Yes	+	+				
10.	Variable packet length cannot be zero.	Yes	+	+				
11.	Ramp waveform of external PA ramp signal on TXRAMP pin is not correct.	Yes	+	+				
12.	Preamble detect signal for nonstandard preambles is incorrect on the GPIO.	No	+	+				
13.	For non-standard preambles, the modem can get stuck in Low-Gear mode if gear switch is set to pre- amble detection and sync word detection fails.	Yes	+	+				
14.	If a received packet has a CRC error, subsequent packets will report a spurious command error.	Yes	+	+				
15.	Use of TCXO with low VDD supply may cause a CTS failure.	FW patch	+	+				
16.	FIFO_INFO command does not update TX_FIFO_ALMOST_EMPTY status properly.	Yes	+	+				
17.	FIFO threshold setting limitations	Yes	+	+				
18.	479-639 MHz center frequency band is not suppor- ted.	No	-	+				
19.	Transmission gets stuck in CW if it is started after IRCAL and RX state.	Yes	+	+				
Note: - means not affected, + means affected								

### 2. Detailed Errata Descriptions

#### 2.1 If Configured to Skip Sync and Preamble on Transmit, the TX Data from the FIFO is Corrupted

#### Description of Errata

If preamble and sync word are excluded from the transmitted data (PREMABLE\_TX\_LENGTH = 0 and SYNC\_CONFIG: SKIP\_TX = 1), data from the FIFO is not transmitted correctly.

#### Affected Conditions / Impacts

Some number of missed bytes will occur at the beginning of the packet and some number of repeated bytes at the end of the packet.

#### Workaround

Set PKT\_FIELD\_1\_CRC\_CONFIG: CRC\_START to 1. This will trigger the packet handler and result in transmitting the correct data, while still not sending a CRC unless enabled in a FIELD configuration. A fix has been identified and will be included in a future release.

#### 2.2 When the CAL Timer and Wakeup Timer Fire at the Same Time, the Wakeup Timer Function is Skipped

#### Description of Errata

If the Wakeup timer and calibration timer intervals are chosen such that they will occur at the same time, the Wakeup timer function will not occur.

#### Affected Conditions / Impacts

When the Wakeup timer and calibration timer intervals exactly coincide, the Wakeup timer function will not occur. This will impact functionality that relies on the Wakeup timer under these specific conditions.

#### Workaround

Configure the Wakeup timer and CAL timer to separate intervals. The CAL timer will first expire at half its programmed interval and at every programmed interval afterwards. The Wakeup timer always expires on its programmed interval after it is enabled. These intervals should be configured such that they never align. Alternatively, the RC calibration can be performed on Wakeup timer intervals as configured using GLOBAL\_WUT\_CAL API. A fix has been identified and will be included in a future release.

#### 2.3 CHANGE\_STATE to TX from TX is an Invalid State Transition

#### Description of Errata

This is an invalid state change for the device. However, if the chip is currently in TX state and a CHANGE\_STATE to TX or START\_TX command is issued, the chip will stop responding. (CTS will remain low until the chip is reset).

#### Affected Conditions / Impacts

If attempting the invalid state transition, the host will not be able to issue subsequent commands to the device without resetting the device first. The device can be reset via the shutdown pin or by power cycling the VDD supply to the device.

#### Workaround

Avoid going from TX state to TX state directly. If the chip is in TX state, exit to some other state before starting TX again.

#### 2.4 TX Packet Abort does not Reset the Packet Handler

#### Description of Errata

When a packet is aborted before it has completed transmitting, by issuing a CHANGE\_STATE out of TX state, the next transmission will continue where the previous packet stopped. For example, if START\_TX is issued with TX\_LEN = 700, the packet is aborted after 300 bytes have been sent, the next TX will not send preamble and sync and will attempt to send 400 bytes.

#### Affected Conditions / Impacts

The second packet will have invalid information if the first packet is aborted during transmission with a change state out of TX state. This does not impact direct mode operation of the device.

#### Workaround

To abort TX, always use CHANGE\_STATE to SLEEP mode. Once in sleep mode, the device can change state to any other state properly. A fix has been identified and will be included in a future release.

#### 2.5 Packet Re-Transmit does not Function as Expected

#### Description of Errata

The RETRANSMIT bit affects the next transmission, not the current transmission.

#### Affected Conditions / Impacts

If the first transmission has the RETRANSMIT bit set to 0, re-transmission will not occur.

#### Workaround

For packet re-transmission, users have to set the RETRANSMIT bit of START\_TX to 1 for the very first packet transmitted. In the last re-transmission, users should set the bit to 0. A fix has been identified and will be included in a future release.

#### 2.6 SPI Active to Ready State without SPI Activity is not Supported

#### Description of Errata

If the chip transitions from SPI active state to ready state, there must be some SPI activity when leaving the SPI active state. This is not a common condition but can occur where the user sets the device to SPI active state and the Wakeup timer to TX or RX a packet on timer expiry. This could also occur if the user goes from SPI active to ready state and polls CTS on a GPIO instead of the SPI interface.

#### Affected Conditions / Impacts

The device cannot go from SPI active to ready state without SPI activity.

#### Workaround

Ensure there is SPI activity when going from SPI active to ready state. A fix has been identified and will be included in a future release.

#### 2.7 Non-Zero BER in Low-Power Mode at Strong Signal Levels

#### Description of Errata

If the transceiver is in low-power mode (default is high-performance mode), there is a chance of non-zero BER at very strong signal levels (e.g., 1% BER at > -12 dBm).

#### Affected Conditions / Impacts

High-performance mode, which is the default setting is not impacted. Non-zero BER (~1%) will be seen at strong signal levels.

#### Workaround

None. A firmware patch is available on request and a fix has been identified and will be included in a future release.

#### 2.8 RSSI Jump Interrupt API not Supported

#### Description of Errata

The RSSI jump interrupt indicates a sudden change in RSSI. This feature is not supported.

#### Affected Conditions / Impacts

RSSI jump interrupt functionality is not supported in this revision.

#### Workaround

None. A fix has been identified and will be included in a future release.

#### 2.9 RSSI Status is not Reset upon START\_RX

#### Description of Errata

Transitioning out of RX state and then going back to RX will not result in automatically resetting the RSSI status bit. 'RSSI status' indicates whether the current RSSI is above the threshold, while 'RSSI pending' indicates whether sometime during RX the current RSSI ever went above the threshold.

#### Affected Conditions / Impacts

This issue occurs when there is a constant radio signal, which is above the RSSI threshold, in between START\_RX calls. Because the radio does not reset the RSSI status bit, it will stay TRUE and won't set the RSSI pending bit. As a result, the chip will not be able to generate an RSSI interrupt more than once per reset.

#### Workaround

Clear the RSSI pending bit manually with a GET\_INT\_STATUS command, strictly outside of RX state. As a side effect, it will clear the RSSI status bit also. A fix has been identified and will be included in a future release.

#### 2.10 Variable Packet Length cannot be Zero

#### Description of Errata

If the variable packet length field of the received packet is zero (e.g., detected in noise), the device will never finish packet reception. Instead, it will stay in RX state and preamble and sync-detect signals will remain high.

#### Affected Conditions / Impacts

The variable packet length of zero will cause the device to remain in RX state.

#### Workaround

Error state can be detected by setting up a timeout of packet reception in the host MCU. Then, issue a CHANGE\_STATE to stand by and a START\_RX to re-start reception. A fix has been identified and will be included in a future release.

#### 2.11 Ramp Waveform of External PA Ramp Signal on TXRAMP Pin is not Smooth

#### Description of Errata

The TXRAMP pin is intended to ramp external PAs for higher TX power. The waveform is not smooth and could cause transient spectral splatter that impacts certain regulatory requirements.

#### Affected Conditions / Impacts

Potentially impacts certain regulatory requirements due to transient spectral splatter.

#### Workaround

Add RC filtering on the board to smoothe the TXRAMP signal. A fix has been identified and will be included in a future release.

#### 2.12 Preamble Detect Signal for Non-Standard Preambles is Incorrect on the GPIO

#### Description of Errata

Preamble detection for non-standard (non 1010) patterns is not indicated correctly on GPIOs.

#### Affected Conditions / Impacts

The host can't use the GPIO to indicate detection of a non-standard preamble.

#### Workaround

None. A fix has been identified and will be included in a future release.

## 2.13 For Non-Standard Preambles, the Modem may Remain in Low-Gear Mode if Gear Switch is Set to Preamble Detection and Sync Word Detection Fails

#### Description of Errata

The modem can switch gears (signal acquisition speed) based on preamble detection. If the sync word is not detected after preamble detection, the modem will remain in Low-Gear mode. This is only observed when using non-standard preambles.

#### Affected Conditions / Impacts

This can have severe implications on receive performance if the modem gets stuck in Low-Gear mode where the AFC algorithm may not be running, the reception will not have any frequency error tolerance.

#### Workaround

Always set the gear switch condition to sync word detection instead of preamble detection, if non-standard preamble is used. For configuring the gear switching event manually, see property "MODEM\_AFC\_MISC" in the API documentation. A fix has been identified and will be included in a future release.

#### 2.14 If a Received Packet has CRC Error, Subsequent Packets will Report a Command Error

#### Description of Errata

If a received packet has a CRC error, the next received packet may raise a CMD\_ERR interrupt during the reception of the packet.

#### Affected Conditions / Impacts

The device is still functional but a spurious CMD\_ERR interrupt will occur.

#### Workaround

After a packet with a CRC error is received, go to sleep state before going back to receive state. A fix has been identified and will be included in a future release.

#### 2.15 Use of TCXO with Low VDD Supply may Cause a CTS Failure

#### Description of Errata

In high-performance mode, use of TCXO as clock source with a supply voltage of less than 2.3 V may cause CTS failures if there are state transitions. This occurs at specific temperatures within the operating temperature range and varies chip-to-chip.

#### Affected Conditions / Impacts

Without a CTS response, the host MCU will be unable to send further commands to the transceiver.

#### Workaround

A firmware patch is available on request and a fix has been identified, which will be included in a future release. Workarounds include increasing supply voltage above 2.3 V when using a TCXO, switching to a XTAL clock source, or using the device in low-power (LP) mode.

#### 2.16 FIFO\_INFO Command does not Update TX\_FIFO\_ALMOST\_EMPTY Status Properly

#### Description of Errata

If the TX FIFO is reset by the FIFO\_INFO command, the chip does not update the TX\_FIFO\_ALMOST\_EMPTY status bit correctly. It gets updated only by the next TX FIFO fill that causes the TX\_FIFO\_ALMOST\_EMPTY interrupt to occur later than expected.

#### Affected Conditions / Impacts

TX\_FIFO\_ALMOST\_EMPTY interrupt occurs later than expected.

#### Workaround

Write one dummy byte into the TX\_FIFO to fire the TX\_FIFO\_ALMOST\_EMPTY interrupt and reset the TX\_FIFO again. A fix has been identified and will be included in the next revision of the device.

#### 2.17 FIFO Threshold Limitations

#### Description of Errata

Threshold of TX\_FIFO\_ALMOST\_EMPTY interrupt can only be set as high as 58 bytes for reliable interrupt generation when the threshold is reached. If the payload length of the transmitted packet is less than 7 bytes, the user can rely on the PACKET\_SENT interrupt which indicates the end of packet transmission. Threshold of RX\_FIFO\_ALMOST\_FULL interrupt can only be set as low as 12 bytes for reliable interrupt generation when the threshold is reached. If the payload length of the received packet is less than 12 bytes, the user can rely on the PACKET\_RX interrupt which indicates the end of packet.

#### Affected Conditions / Impacts

Users should not rely on FIFO threshold interrupts for greater than 58 bytes on the TX side and less than 12 bytes on the RX side.

#### Workaround

Rely on PACKET\_SENT and PACKET\_RX interrupts for very small payload lengths as described above. A fix has been identified and will be included in the next revision of the device.

#### 2.18 479-639 MHz Center Frequency Band is not Supported

#### **Description of Errata**

Using the radio at a center frequency in the 470-639 MHz band requires the use of the divide by 6 output divider (DIV6) of the synthesizer. The divider is selected by setting the BAND field of the MODEM\_CLKGEN\_BAND property to 1.

Depending on runtime conditions, such as supply voltage, DIV6 can go into a failure state and stay there until it is reset by restarting RX state.

#### Affected Conditions / Impacts

In the failure state the receiver can't receive. Restarting the receive state (by using START\_RX API command) can recover the receiver, but it can get halted again after running for some time. As a result, the 470-639 MHz band can't be used. This affects only the Si4464-B1B.

#### Workaround

For the 470-479MHz band, the DIV8 divider can be used alternatively. (For details see the frequency control section in the data sheet.)

No workaround exists for the 479-639 MHz band.

#### 2.19 Transmission is Stuck in CW if Started after IRCAL and RX State

#### Description of Errata

If IR calibration is performed, the receiver is started and then transmission is started, transmission will get stuck in Continuous Wave transmission. If no IR calibration is performed, the issue does not occur.

#### Affected Conditions / Impacts

In this failure state the transmitter cannot transmit modulated signal.

#### Workaround

A state transition to READY state before starting transmission solves the problem.



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Silicon Laboratories Inc. 400 West Cesar Chavez Austin, TX 78701 USA

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