ESD5384

ESD Protection Diode

5−Line HDMI Control Line ESD Protection

Functional Description

The ESD5384 chip is a low capacitance ESD protection for HDMI control pins. It also integrates pull−up resistor for I^2C bus and pull−down resistor for hot plug detect and pull−up resistor for CEC line.

The ESD protection circuitry prevents damage to the protected device when subjected to ESD surges up to 15 kV.

The ESD5384 is available in 9 bump CSP package.

Features

- Line Capacitance: 12 pF max
- IEC 61000−4−2 Level 4
  - ♦ ±15 kV (air discharge)
  - ♦ ±8 kV (contact discharge)
- This is a Pb−Free Device

Applications

- HDMI Control Line Interfaces
  - ♦ Smart Phones
  - ♦ Tablets
  - ♦ Consumer Electronics

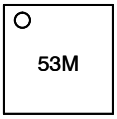
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MARKING DIAGRAM

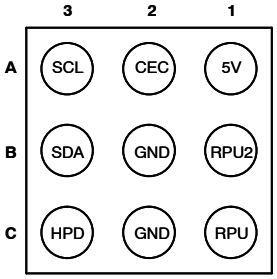


WLCSP9
CASE 567CX



53 = Specific Device Code
M = Date Code

PINOUT



(Bump Side)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

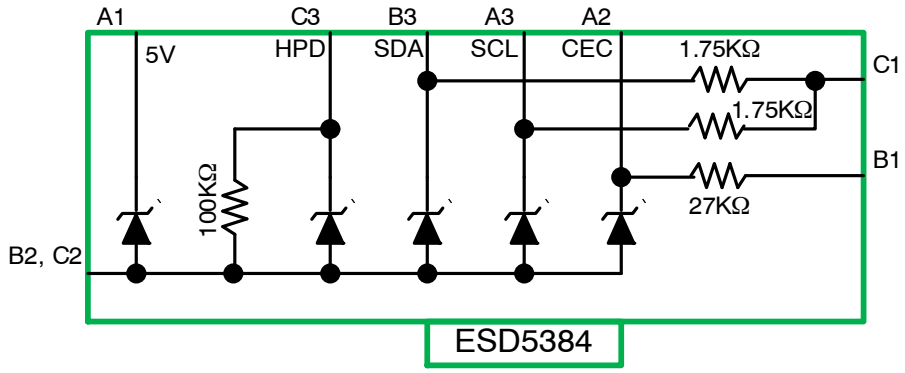


Figure 1. Electrical Schematic

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{PP}	External pins (A1, A2, A3, B3 and C3): ESD IEC 61000−4−2, level 4 − air discharge ESD IEC 61000−4−2, level 4 − contact discharge Internal pins (B1, C1): ESD IEC 61000−4−2, level 1 − air discharge ESD IEC 61000−4−2, level 1 − contact discharge	 ± 15 ± 8 ± 2 ± 2	kV
T_{op}	Operating Temperature Range	−30 to +85	°C
T_{stg}	Storage Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (Note 1)

Symbol	Test Condition	Min	Typ	Max	Unit
V_{BR}	Breakdown Voltage (I_r = 1mA)	6		20	V
I_{RM}	Leakage Current @ V_{rm} (V_{rm} = 3 V per line), excluding HPD line		50	200	nA
I_{RM}	Leakage Current @ V_{rm} (V_{rm} = 3 V per line), HPD line			32	μA
R1, R2	Resistance	1575	1750	1925	Ω
R3	Pull−up Resistance	80	100	120	kΩ
R4	Pull−up Resistance	22	27	32	kΩ
C_{line}	V_{line} = 0 V, V_{osc} = 30 mV, F = 1 MHz, A2 with B1 not connected		14	17	pF
	V_{line} = 0 V, V_{osc} = 30 mV, F = 1 MHz, A3, B3 with C1 not connected.		24	29	
	V_{line} = 0 V, V_{osc} = 30 mV, F = 1 MHz, A2, A3, B3 with C1 and B1 grounded		10	12	

1. All parameters specified at T_A = 25°C unless otherwise noted.

TYPICAL CHARACTERISTICS

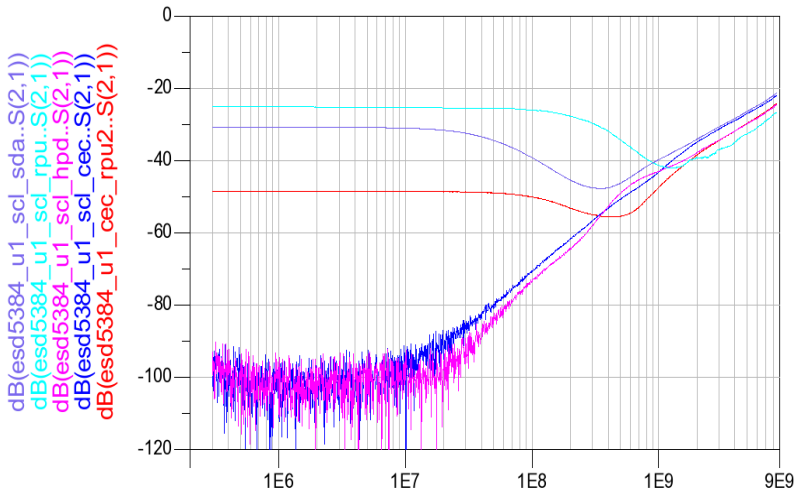


Figure 2. Crosstalk Measurements

TYPICAL CHARACTERISTICS

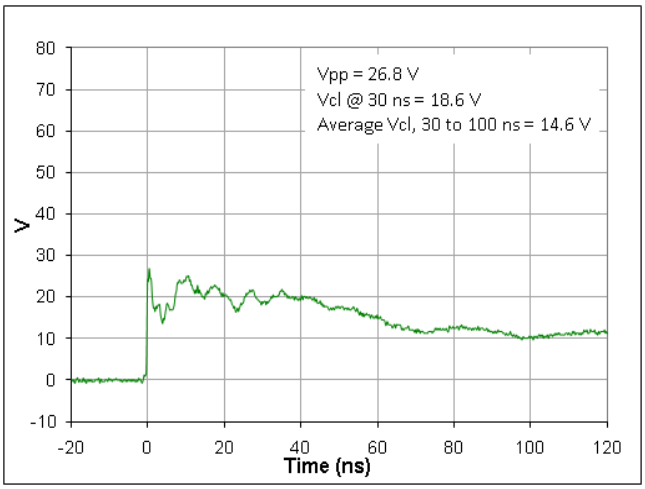


Figure 3. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2, CEC line

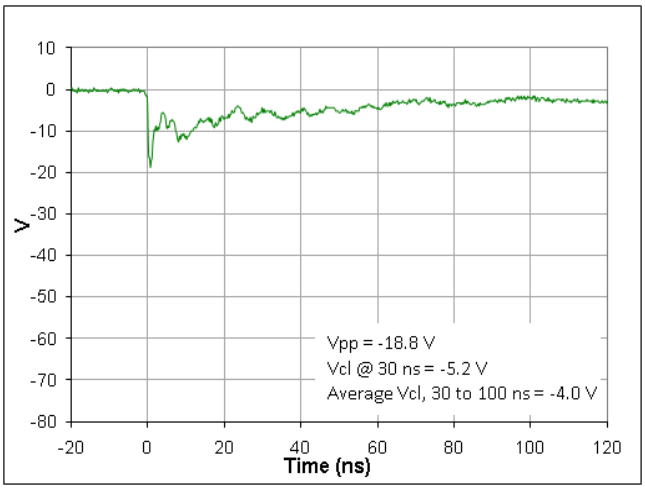


Figure 4. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2, CEC line

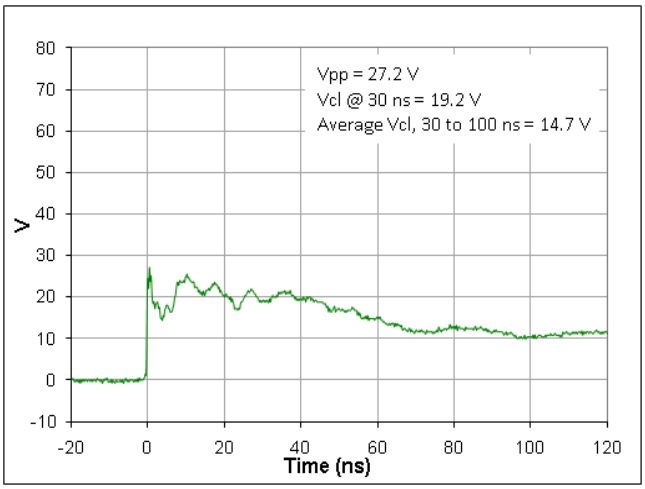


Figure 5. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2, SCL line

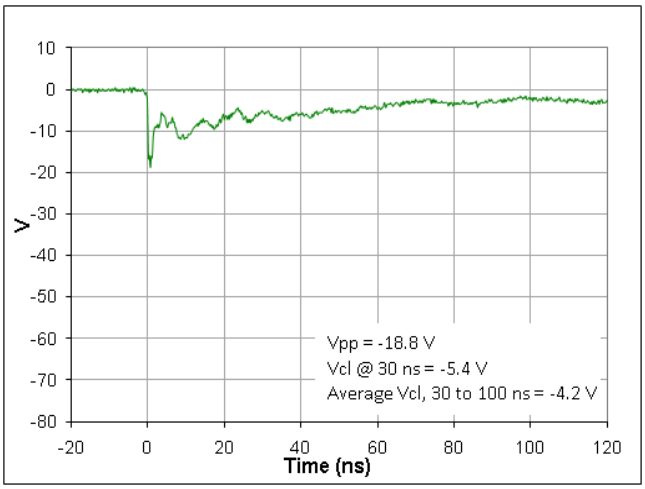


Figure 6. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2, SCL line

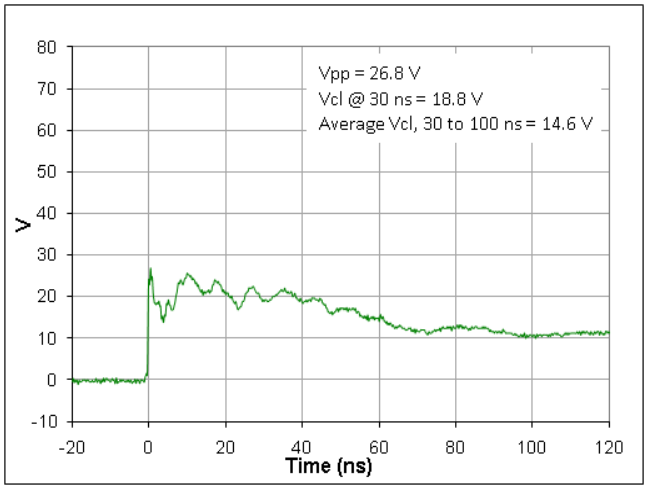


Figure 7. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2, SDA line

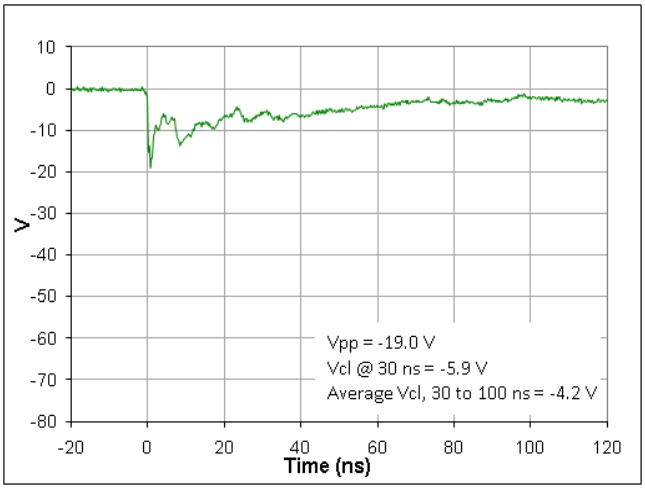


Figure 8. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2, SDA line

TYPICAL CHARACTERISTICS

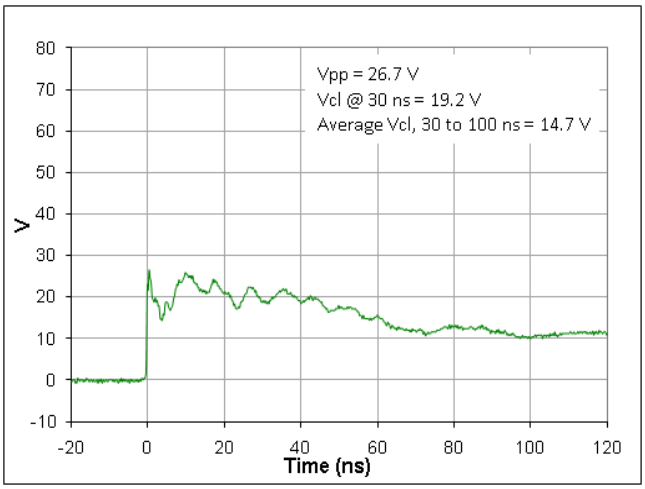


Figure 9. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2, HPD line

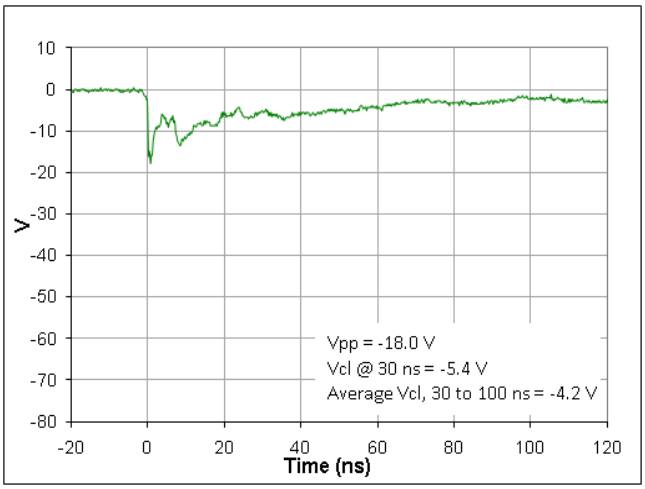


Figure 10. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2, HPD line

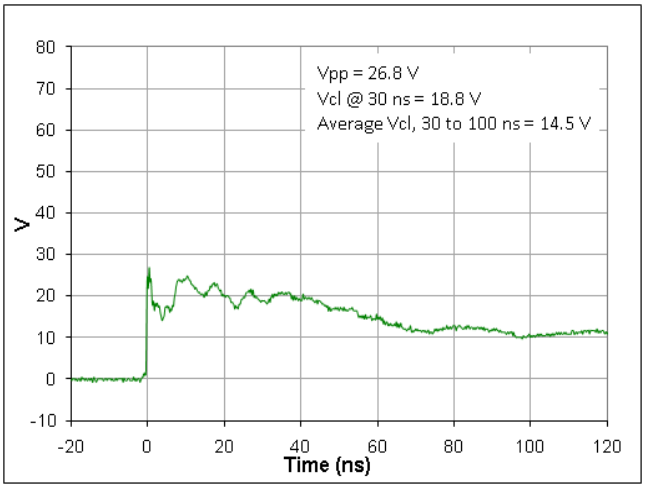


Figure 11. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2, 5 V line

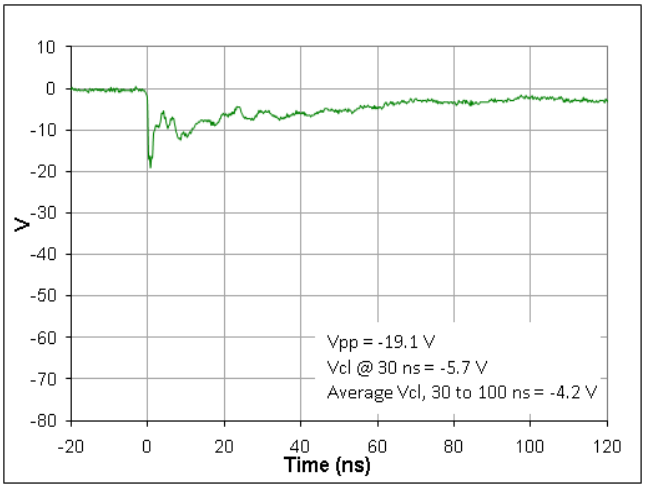


Figure 12. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2, 5 V line

IEC61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

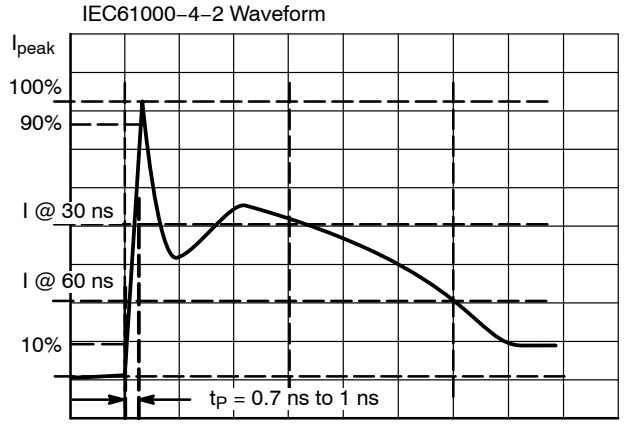


Figure 13. IEC61000−4−2 Spec

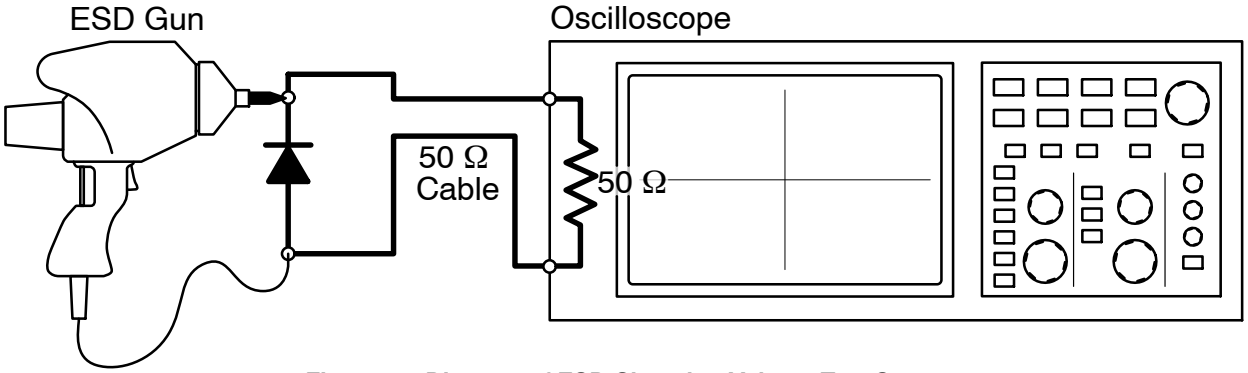


Figure 14. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

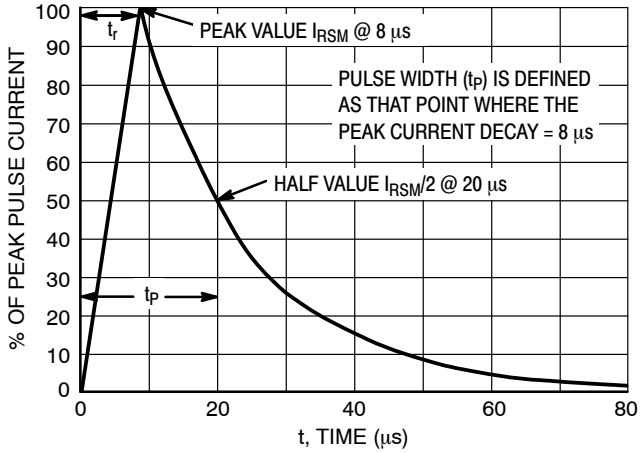


Figure 15. 8 x 20 μs Pulse Waveform

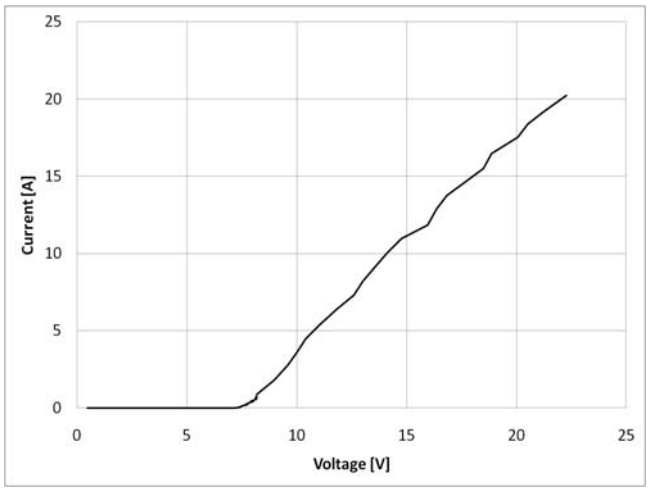


Figure 16. Positive TLP I−V Curve

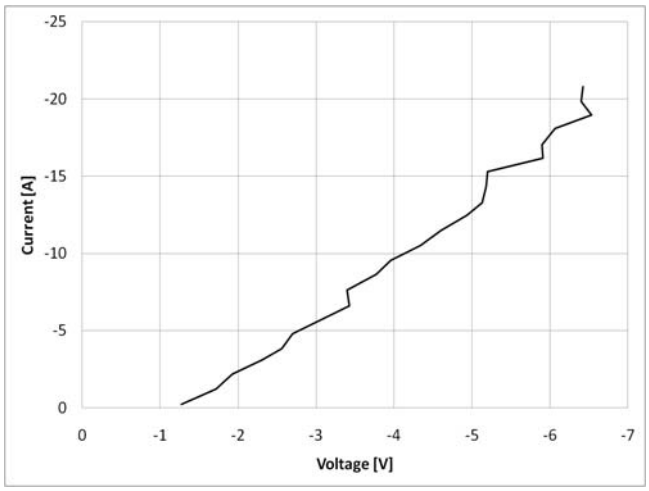


Figure 17. Negative TLP I−V Curve

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 18. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 19 where an 8 kV IEC61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. A typical TLP I−V curve for the ESD7383 is shown in Figures 16 and 17.

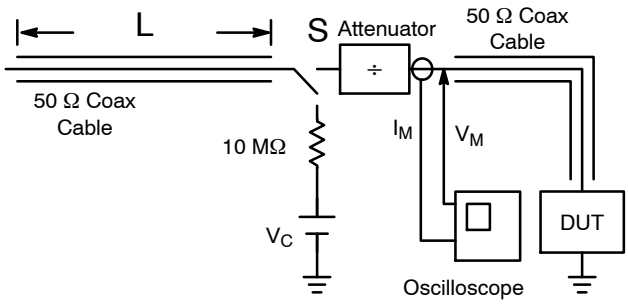


Figure 18. Simplified Schematic of a Typical TLP System

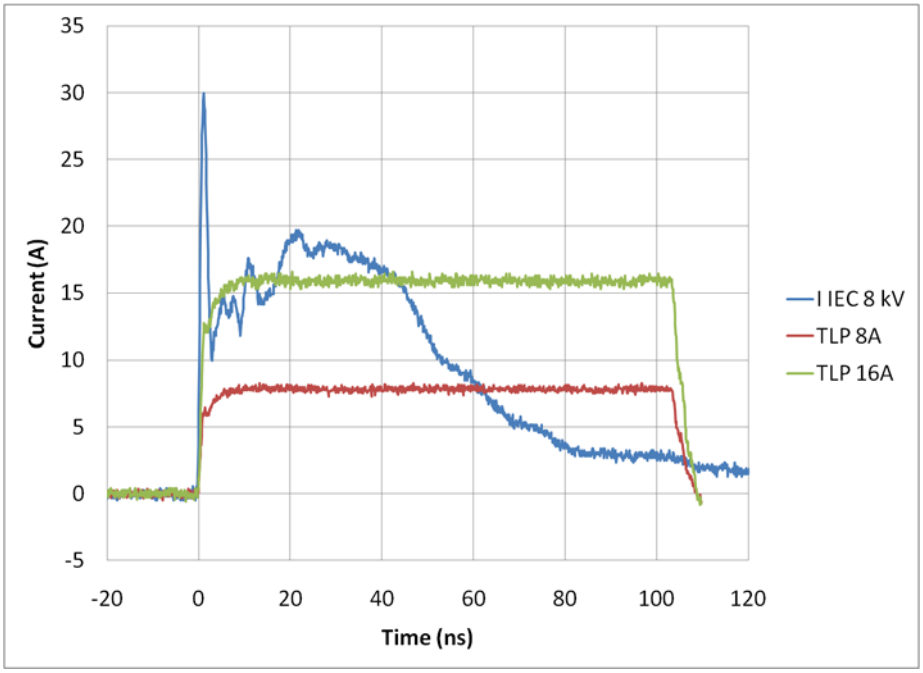


Figure 19. Comparison Between 8 kV IEC61000−4−2 and 8 A and 16 A TLP Waveforms

TYPICAL APPLICATION SCHEMATIC

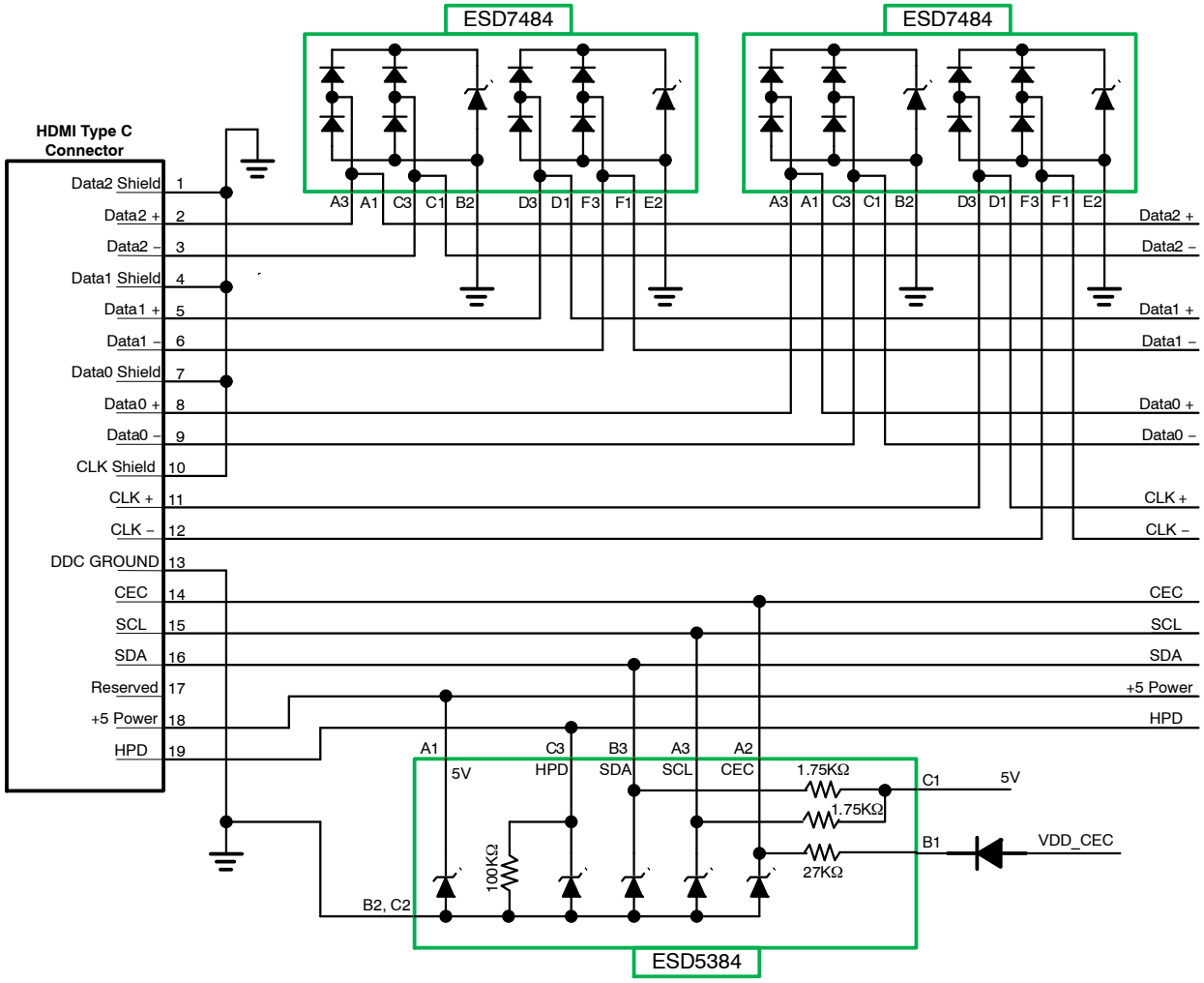


Figure 20. Typical Application Schematic

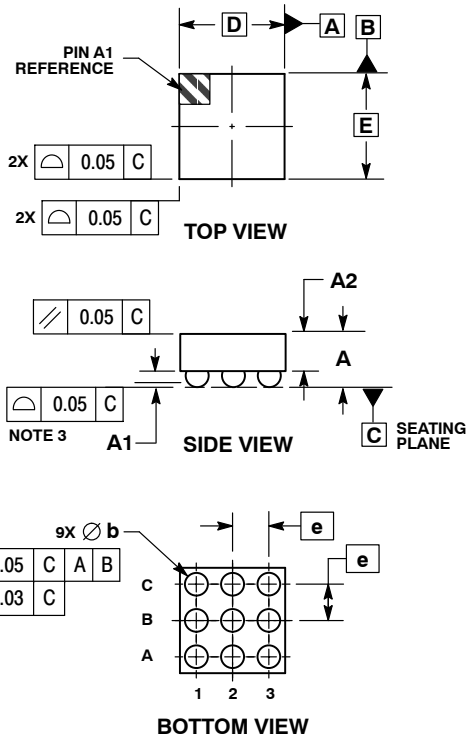
ORDERING INFORMATION

Part Number	Chip Size (mm)	Package	Shipping†
ESD5384	1.14 x 1.14 x 0.605	WLCSP9 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

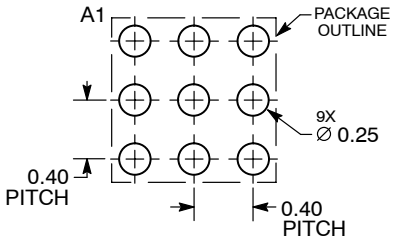
WLCSP9, 1.14x1.14
CASE 567CX−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.57	0.63
A1	0.17	0.24
A2	0.41 REF	
b	0.24	0.29
D	1.14 BSC	
E	1.14 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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