TEXAS INSTRUMENTS

DLPC3436 Display Controller

1 Features

- DLP230NP (.23 1080p) DMD display controller
  - Supports input resolutions up to 1080p
  - Low-power DMD interface with interface training
- Input frame rates up to 240 Hz (60 Hz at 1080p resolution)
- 24-Bit, input pixel interface support:
  - Parallel interface protocol
  - Pixel clock up to 150 MHz
  - Multiple input pixel data format options
- Pixel data processing including:
  - IntelliBright™ suite of image processing algorithms
    - Content adaptive illumination control
    - Local area brightness boost
  - Color coordinate adjustment
  - Active power management processing
- External flash support
- Embedded frame memory (eDRAM)
- System features:
  - I^2C control of device configuration
  - Programmable LED current control
  - One frame latency

2 Applications

- DLP signage
- Mobile projector
- Mobile smart TV
- Smart speaker
- Virtual or augmented reality headsets and glasses
- Mobile accessory
- Smart home displays
- Pico projectors

3 Description

The DLPC3436 digital controller, a component of the DLP230NP (.23 1080p) chipset, supports reliable operation of the DLP230NP digital micromirror device (DMD). The DLP230NP chipset enables small form factor, low power, and high resolution 1080p displays.

Visit the *Getting Started with TI DLP® Pico™ Display Technology* page to learn more about the DLP230NP chipset.

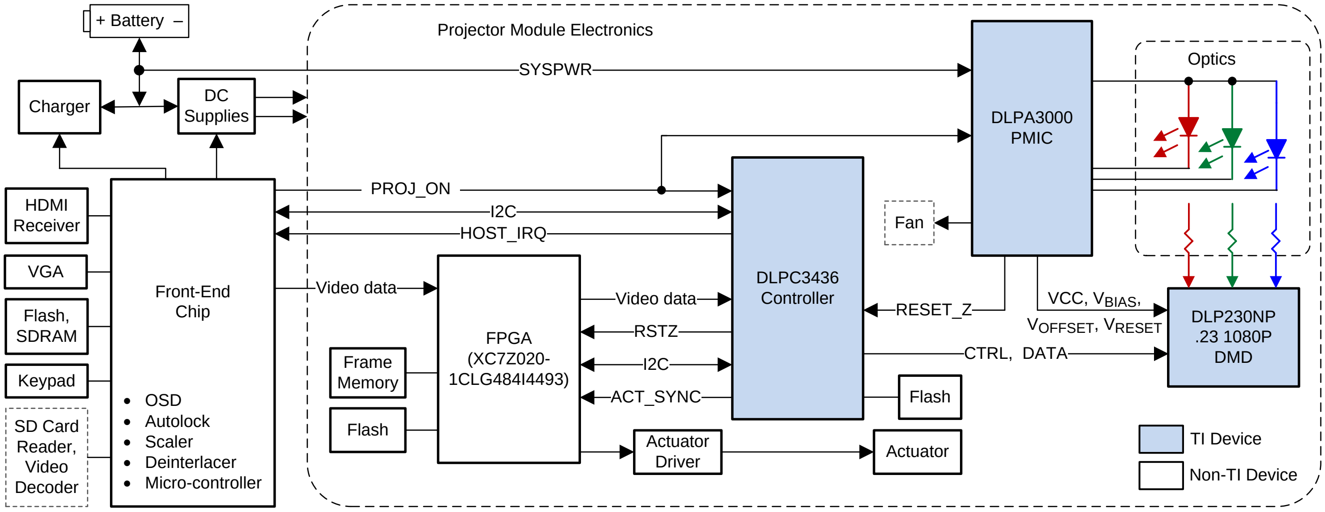
The DLP230NP chipset includes established resources to help the user accelerate the design cycle, which include production ready optical modules, optical modules manufactures, and design houses.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLPC3436	NFBGA (176)	7.00 × 7.00 mm^2

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application



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4 Revision History

Changes from Revision A (April 2019) to Revision B — Page

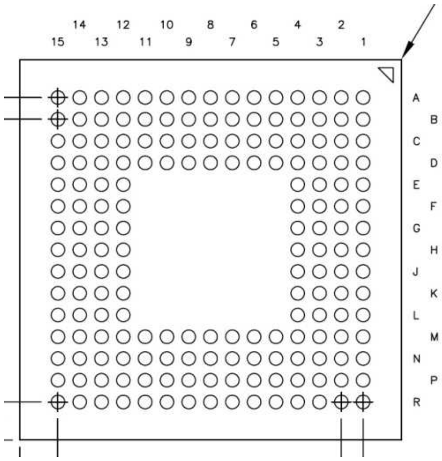
- Added missing revision A notes 1
- Changed normal park time from 500 µs to 20 ms 4

Changes from Original (January 2019) to Revision A — Page

- Removed 3.3-V reference from $I_{(VCC\_INTF)}$ in *Electrical Characteristics over Recommended Operating Conditions* 14
- Updated Figure 8 24
- Updated Figure 9 24
- Timing values added in Figure 20 41
- Updated Running Normal DMD Park and Power Shut-Down times in Figure 21 43
- Updated Running Fast DMD Park Sequence and Power Shut-Down times in Figure 22 43
- Corrected *Device Markings* image and updated table 51

5 Pin Configuration and Functions

ZVB Package
176-Pin NFBGA
Bottom View



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	DMD_LS_CLK	DMD_LS_WDATA	DMD_HS_WDATAH_P	DMD_HS_WDATAG_P	DMD_HS_WDATAF_P	DMD_HS_WDATAE_P	DMD_HS_CLK_P	DMD_HS_WDATAD_P	DMD_HS_WDATAC_P	DMD_HS_WDATAB_P	DMD_HS_WDATAA_P	CMP_OUT	SPI0_CLK	SPI0_CSZ0	CMP_PWM
B	DMD_DEN_ARSTZ	DMD_LS_RDATA	DMD_HS_WDATAH_N	DMD_HS_WDATAG_N	DMD_HS_WDATAF_N	DMD_HS_WDATAE_N	DMD_HS_CLK_N	DMD_HS_WDATAD_N	DMD_HS_WDATAC_N	DMD_HS_WDATAB_N	DMD_HS_WDATAA_N	SPI0_DIN	SPI0_DOUT	LED_SEL_1	LED_SEL_0
C	DD3P	DD3N	VDDLP12	VSS	VDD	VSS	VCC	VSS	VCC	HWTEST_EN	RESETZ	SPI0_CSZ1	PARKZ	GPIO_00	GPIO_01
D	DD2P	DD2N	VDD	VCC	VDD	VSS	VDD	VSS	VDD	VSS	VCC_FLSH	VDD	VDD	GPIO_02	GPIO_03
E	DCLKP	DCLKN	VDD	VSS								VCC	VSS	GPIO_04	GPIO_05
F	DD1P	DD1N	RREF	VSS								VCC	VDD	GPIO_06	GPIO_07
G	DD0P	DD0N	VSS_PLLM	VSS								VSS	VSS	GPIO_08	GPIO_09
H	PLL_REFCLK_I	VDD_PLLM	VSS_PLLD	VSS								VSS	VDD	GPIO_10	GPIO_11
J	PLL_REFCLK_O	VDD_PLLD	VSS	VDD								VDD	VSS	GPIO_12	GPIO_13
K	PDATA_1	PDATA_0	VDD	VSS								VSS	VCC	GPIO_14	GPIO_15
L	PDATA_3	PDATA_2	VSS	VDD								VDD	VDD	GPIO_16	GPIO_17
M	PDATA_5	PDATA_4	VCC_INTF	VSS	VSS	VDD	VCC_INTF	VSS	VDD	VDD	VCC	VSS	JTAGTMS1	GPIO_18	GPIO_19
N	PDATA_7	PDATA_6	VCC_INTF	PDM_CVS_TE	HSYNC_CS	3DR	VCC_INTF	HOST_IRQ	IIC0_SDA	IIC0_SCL	JTAGTMS2	JTAGTDO2	JTAGTDO1	TSTPT_6	TSTPT_7
P	VSYNC_WE	DATEN_CMD	PCLK	PDATA_11	PDATA_13	PDATA_15	PDATA_17	PDATA_19	PDATA_21	PDATA_23	JTAGTRSTZ	JTAGTCK	JTAGTDI	TSTPT_4	TSTPT_5
R	PDATA_8	PDATA_9	PDATA_10	PDATA_12	PDATA_14	PDATA_16	PDATA_18	PDATA_20	PDATA_22	IIC1_SDA	IIC1_SCL	TSTPT_0	TSTPT_1	TSTPT_2	TSTPT_3

Pin Functions – Board Level Test, Debug, and Initialization

PIN		I/O	DESCRIPTION
NAME	NUMBER		
HWTEST_EN	C10	I_6	Manufacturing test enable signal. This signal should be connected directly to ground on the PCB for normal operation.
PARKZ	C13	I_6	DMD fast PARK control (active low input) (hysteresis buffer). PARKZ must be set high to enable normal operation. PARKZ should be set high prior to releasing RESETZ (that is, prior to the low-to-high transition on the RESETZ input). PARKZ should be set low for a minimum of 32 µs before any power is removed from the DLPC3436 such that the fast DMD PARK operation can be completed. Note for PARKZ, fast PARK control should only be used when loss of power is eminent and beyond the control of the host processor (for example, when the external power source has been disconnected or the battery has dropped below a minimum level). The longest lifetime of the DMD may not be achieved with the fast PARK operation. The longest lifetime is achieved with a normal PARK operation. Because of this, PARKZ is typically used in conjunction with a normal PARK request control input through GPIO_08. The difference being that when the host sets PROJ_ON low, which connects to both GPIO_08 and the DLPAxxxx PMIC chip, the DLPC3436 takes much longer than 32 µs to park the mirrors. The DLPAxxxx holds on all power supplies, and keep RESETZ high, until the longer mirror parking has completed. This longer mirror parking time, of up to 20 ms, ensures the longest DMD lifetime and reliability. The DLPAxxxx monitors power to the DLPC3436 and detects an eminent power loss condition and drives the PARKZ signal accordingly.
Reserved	P12	I_6	TI internal use. Should be left unconnected.
Reserved	P13	I_6	TI internal use. Should be left unconnected.
Reserved	N13 (1)	O_1	TI internal use. Should be left unconnected.
Reserved	N12 (1)	O_1	TI internal use. Should be left unconnected.
Reserved	M13	I_6	TI internal use. Should be left unconnected.
Reserved	N11	I_6	TI internal use. Should be left unconnected.
Reserved	P11	I_6	TI internal use This pin must be tied to ground, through an external 8-kΩ, or less, resistor for normal operation. Failure to tie this pin low during normal operation causes startup and initialization problems.
RESETZ	C11	I_6	DLPC3436 power-on reset (active low input) (hysteresis buffer). Self-configuration starts when a low-to-high transition is detected on RESETZ. All ASIC power and clocks must be stable before this reset is de-asserted. Note that the controller tri-states the following signals while RESETZ is asserted: SPI0_CLK, SPI0_DOUT, SPI0_CSZ0, SPI0_CSZ1, and GPIO(19:00) External pullups or downs (as appropriate) should be added to all tri-stated output signals listed (including bidirectional signals to be configured as outputs) to avoid floating ASIC outputs during reset if connected to devices on the PCB that can malfunction. For SPI, at a minimum, any chip selects connected to the devices should have a pullup. Unused bidirectional signals can be functionally configured as outputs to avoid floating ASIC inputs after RESETZ is set high. The following signals are forced to a logic low state while RESETZ is asserted and corresponding I/O power is applied: LED_SEL_0, LED_SEL_1 and DMD_DEN_ARSTZ No signals are in an active state while RESETZ is asserted. Note that no I^2C activity is permitted for a minimum of 500 ms after RESETZ (and PARKZ) are set high.
TSTPT_0	R12	B_1	Reserved for test output. Should be left open for normal use.
TSTPT_1	R13	B_1	Reserved for test output. Should be left open for normal use.
TSTPT_2	R14	B_1	Reserved for test output. Should be left open for normal use.
TSTPT_3	R15	B_1	Reserved for for test output. Should be left open for normal use.
TSTPT_4	P14	B_1	Reserved for for test output. Should be left open for normal use.
TSTPT_5	P15	B_1	Reserved for test output. Should be left open for normal use.
TSTPT_6	N14	B_1	Reserved for test output. Should be left open for normal use.
TSTPT_7	N15	B_1	Reserved for test output. Should be left open for normal use.

(1) If operation does not call for an external pullup and there is no external logic that might overcome the weak internal pulldown resistor, then this I/O can be left open or unconnected for normal operation. If operation does not call for an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown resistor is recommended to ensure a logic low.

Pin Functions – Parallel Port Input Data and Control(1)(2)

PIN		I/O	DESCRIPTION	
NAME	**NUMBER**		**PARALLEL RGB MODE**	
PCLK	P3	I_{11}	Pixel clock(3)	
PDM_CVS_TE	N4	B_5	Parallel data mask(4)	
VSYNC_WE	P1	I_{11}	Vsync(5)	
HSYNC_CS	N5	I_{11}	Hsync(5)	
DATAEN_CMD	P2	I_{11}	Data valid(5)	
PDATA_0 PDATA_1 PDATA_2 PDATA_3 PDATA_4 PDATA_5 PDATA_6 PDATA_7	K2 K1 L2 L1 M2 M1 N2 N1	I_{11}	**(TYPICAL RGB 888)** Blue (bit weight 1) Blue (bit weight 2) Blue (bit weight 4) Blue (bit weight 8) Blue (bit weight 16) Blue (bit weight 32) Blue (bit weight 64) Blue (bit weight 128)	
PDATA_8 PDATA_9 PDATA_10 PDATA_11 PDATA_12 PDATA_13 PDATA_14 PDATA_15	R1 R2 R3 P4 R4 P5 R5 P6	I_{11}	**(TYPICAL RGB 888)** Green (bit weight 1) Green (bit weight 2) Green (bit weight 4) Green (bit weight 8) Green (bit weight 16) Green (bit weight 32) Green (bit weight 64) Green (bit weight 128)	
PDATA_16 PDATA_17 PDATA_18 PDATA_19 PDATA_20 PDATA_21 PDATA_22 PDATA_23	R6 P7 R7 P8 R8 P9 R9 P10	I_{11}	**(TYPICAL RGB 888)** Red (bit weight 1) Red (bit weight 2) Red (bit weight 4) Red (bit weight 8) Red (bit weight 16) Red (bit weight 32) Red (bit weight 64) Red (bit weight 128)	
3DR	N6	I_{11}	3D reference • For 3D applications: Left or right 3D reference (left = 1, right = 0). To be provided by the host when a 3D command is not provided. Must transition in the middle of each frame (no closer than 1 ms to the active edge of VSYNC) • If a 3D application is not used, then this input should be pulled low through an external resistor.	

(1) PDATA(23:0) bus mapping is pixel format and source mode dependent. See later sections for details.
(2) PDM_CVS_TE is optional for parallel interface operation. If unused, inputs should be grounded or pulled down to ground through an external resistor (8 kΩ or less).
(3) Pixel clock capture edge is software programmable.
(4) The parallel data mask signal input is optional for parallel interface operations. If unused, inputs must be grounded or pulled down to ground through an external resistor (8 kΩ or less).
(5) VSYNC, HSYNC, and DATAEN polarity is software programmable.

Pin Functions – DMD Reset and Bias Control

PIN		I/O	DESCRIPTION
NAME	**NUMBER**		
DMD_DEN_ARSTZ	B1	O_2	DMD driver enable (active high) or DMD reset (active low). Assuming the corresponding I/O power is supplied, the controler drives this signal low after the DMD is parked and before power is removed from the DMD. If the 1.8-V power to the DLPC3436 is independent of the 1.8-V power to the DMD, then TI recommends a weak, external pulldown resistor to hold the signal low in the event the DLPC3436 power is inactive while the DMD power is applied.
DMD_LS_CLK	A1	O_3	DMD, low speed interface clock
DMD_LS_WDATA	A2	O_3	DMD, low speed serial write data
DMD_LS_RDATA	B2	I_6	DMD, low speed serial read data

Pin Functions – DMD Sub-LVDS Interface

PIN		I/O	DESCRIPTION
NAME	**NUMBER**		
DMD_HS_CLK_P DMD_HS_CLK_N	A7 B7	O_4	DMD high speed interface
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	A3 B3 A4 B4 A5 B5 A6 B6 A8 B8 A9 B9 A10 B10 A11 B11	O_4	DMD high speed interface lanes, write data bits: The true numbering and application of the DMD_HS_DATA pins are software configuration dependent

Pin Functions – Peripheral Interface(1)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
CMP_OUT	A12	I_6	Reserved. Pull-down to ground.
CMP_PWM	A15	O_1	Reserved. Leave unconnected.
HOST_IRQ(2)	N8	O_9	Host interrupt (output) HOST_IRQ indicates when the DLPC3436 auto-initialization is in progress and most importantly when it completes. The DLPC3436 tri-states this output during reset and requires that an external pullup is in place to drive this signal to its inactive state.
IIC0_SCL	N10	B_7	I^{2}C slave (port 0) SCL (bidirectional, open-drain signal with input hysteresis): An external pullup is required. The slave I^{2}C I/Os are 3.6-V tolerant (high-volt-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I^{2}C pullups must be connected to a host supply with an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage would not likely satisfy the V_{IH} specification of the slave I^{2}C input buffers).
IIC1_SCL	R11	B_8	I^{2}C master (port 1) SCL (bidirectional, open-drain signal with input hysteresis): An external pullup is required. The slave I^{2}C I/Os are 3.6-V tolerant (high-volt-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I^{2}C pullups must be connected to a host supply with an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage would not likely satisfy the V_{IH} specification of the slave I^{2}C input buffers).
IIC0_SDA	N9	B_7	I^{2}C slave (port 0) SDA. (bidirectional, open-drain signal with input hysteresis): An external pullup is required. The slave I^{2}C port is the control port of ASIC. The slave I^{2}C I/Os are 3.6-V tolerant (high-volt-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I^{2}C pullups must be connected to a host supply with an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage would not likely satisfy the V_{IH} specification of the slave I^{2}C input buffers).
IIC1_SDA	R10	B_8	I^{2}C master (port 1) SDA. (bidirectional, open-drain signal with input hysteresis): An external pullup is required. The slave I^{2}C port is the control port of ASIC. The slave I^{2}C I/Os are 3.6-V tolerant (high-volt-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I^{2}C pullups must be connected to a host supply with an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage would not likely satisfy the V_{IH} specification of the slave I^{2}C input buffers).
LED_SEL_0	B15	O_1	LED enable select. Controlled by programmable DMD sequence Timing / Enabled LED LED_SEL(1:0) / DLPAxxxx application 00 / None 01 / Red 10 / Green 11 / Blue The controller drives these signals low when RESETZ is asserted and the corresponding I/O power is supplied. The controller continues to drive these signals low throughout the auto-initialization process. A weak, external pulldown resistor is still recommended to ensure that the LEDs are disabled when I/O power is not applied.
LED_SEL_1	B14	O_1	
SPI0_CLK	A13	O_{13}	Synchronous serial port 0, clock
SPI0_CSZ0	A14	O_{13}	SPI port 1, chip select 0 (active low output) TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during ASIC reset assertion.
SPI0_CSZ1	C12	O_{13}	SPI port 1, chip select 1 (active low output) TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during ASIC reset assertion.
SPI0_DIN	B12	I_{12}	Synchronous serial port 0, receive data in
SPI0_DOUT	B13	O_{13}	Synchronous serial port 0, transmit data out

(1) External pullup resistor must be 8 kΩ or less.
(2) For more information about usage, see *HOST_IRQ Usage Model*.

Pin Functions – GPIO Peripheral Interface

PIN		I/O	DESCRIPTION
NAME	NUMBER		
GPIO_19	M15	B_1	General purpose I/O 19 (hysteresis buffer). Reserved
GPIO_18	M14	B_1	General purpose I/O 18 (hysteresis buffer). FPGA_RESET (output): Logic reset for the chipset FPGA.

Pin Functions – GPIO Peripheral Interface (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
GPIO_17	L15	B_1	General purpose I/O 17 (hysteresis buffer). ACT_SYNC (output): Output to FPGA, used for synchronizing the actuator position with the ASIC data processing
GPIO_16	L14	B_1	General purpose I/O 16 (hysteresis buffer). SUB_FRAME_2 (input): Input from FPGA, signaling sub-frames
GPIO_15	K15	B_1	General purpose I/O 15 (hysteresis buffer). SUB_FRAME_1 (input): Input from FPGA, signaling sub-frames
GPIO_14	K14	B_1	General purpose I/O 14 (hysteresis buffer). FPGA_RDY (input): Input from FPGA, indicating when the FPGA initialization process is complete.
GPIO_13	J15	B_1	General purpose I/O 13 (hysteresis buffer). CAL_PWR (output): Intended to feed the calibration control of the successive approximation ADC light sensor.
GPIO_12	J14	B_1	General purpose I/O 12 (hysteresis buffer). ADC Light Sensor Power 2 (output): Power enable control for LABB light sensor.
GPIO_11	H15	B_1	General purpose I/O 11 (hysteresis buffer). Thermistor power enable (output)
GPIO_10	H14	B_1	General purpose I/O 10 (hysteresis buffer). RC_CHARGE (output): Intended to feed the RC charge circuit of the successive approximation ADC used to control the light sensor comparator.
GPIO_09	G15	B_1	General purpose I/O 09 (hysteresis buffer). LS_PWR (active high output): Intended to feed the power control signal of the successive approximation ADC light sensor.
GPIO_08	G14	B_1	General purpose I/O 08 (hysteresis buffer). Normal mirror parking request (active low): To be driven by the PROJ_ON output of the host. A logic low on this signal causes the DLPC3436 to PARK the DMD, but it does not power down the DMD (the DLPAxxxx does that instead). The minimum high time is 200 ms. The minimum low time is also 200 ms.
GPIO_07	F15	B_1	General purpose I/O 07 (hysteresis buffer). LABB_SAMPLE (output): LABB output sample and hold sensor control signal.
GPIO_06	F14	B_1	General purpose I/O 06 (hysteresis buffer). Reserved.
GPIO_05	E15	B_1	General purpose I/O 05 (hysteresis buffer). Reserved.
GPIO_04	E14	B_1	General purpose I/O 04 (hysteresis buffer). 3D glasses control (output): Intended to be used to control the shutters on 3D glasses (Left = 1, Right = 0).
GPIO_03	D15	B_1	General purpose I/O 03 (hysteresis buffer). SPI1_CSZ0 (active low output): Optional SPI1 chip select 0 signal. An external pullup resistor is required to deactivate this signal during reset and auto-initialization processes.

Pin Functions – GPIO Peripheral Interface (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
GPIO_02	D14	B_1	General purpose I/O 02 (hysteresis buffer). SPI1_DOUT (output): Optional SPI1 data output signal.
GPIO_01	C15	B_1	General purpose I/O 01 (hysteresis buffer). SPI1_CLK (output): Optional SPI1 clock signal.
GPIO_00	C14	B_1	General purpose I/O 00 (hysteresis buffer). SPI1_DIN (input): Optional SPI1 data input signal.

Pin Functions – Clock and PLL Support

PIN		I/O	DESCRIPTION
NAME	NUMBER		
PLL_REFCLK_I	H1	I_{11}	Reference clock crystal input. If an external oscillator is used in place of a crystal, then this pin should be used as the oscillator input.
PLL_REFCLK_O	J1	O_5	Reference clock crystal return. If an external oscillator is used in place of a crystal, then this pin should be left unconnected (that is floating with no added capacitive load).

Pin Functions – Power and Ground(1)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{DD}	C5, D5, D7, D12, J4, J12, K3, L4, L12, M6, M9, D9, D13, F13, H13, L13, M10, D3, E3	PWR	Core power 1.1 V (main 1.1 V)
V_{DDLP12}	C3	PWR	Core power 1.1 V
V_{SS}	Common to all package types C4, D6, D8, D10, E4, E13, F4, G4, G12, H4, H12, J3, J13, K4, K12, L3, M4, M5, M8, M12, G13, C6, C8	GND	Core ground (eDRAM, I/O ground, thermal ground)
V_{CC18}	C7, C9, D4, E12, F12, K13, M11	PWR	All 1.8-V I/O power: (1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ LED_SEL, CMP, GPIO, IIC1, TSTPT, and JTAG pins)
V_{CC_INTF}	M3, M7, N3, N7	PWR	Host or parallel interface I/O power: 1.8 to 3.3 V (Includes IIC0, PDATA, video syncs, and HOST_IRQ pins)
V_{CC_FLSH}	D11	PWR	Flash interface I/O power: 1.8 to 3.3 V (Dedicated SPI0 power pin)
V_{DD_PLLM}	H2	PWR	MCG PLL 1.1-V power
V_{SS_PLLM}	G3	RTN	MCG PLL return
V_{DD_PLLD}	J2	PWR	DCG PLL 1.1-V power
V_{SS_PLLD}	H3	RTN	DCG PLL return

(1) The only power sequencing restrictions are:
  (a) The VDD supply should ramp up with a 1-ms maximum rise time.
  (b) The reverse is needed at power down.

Table 1. I/O Type Subscript Definition

I/O		SUPPLY REFERENCE	ESD STRUCTURE
SUBSCRIPT	DESCRIPTION		
1	1.8-V LVCMOS I/O buffer with 8-mA drive	V_{CC18}	ESD diode to GND and supply rail
2	1.8-V LVCMOS I/O buffer with 4-mA drive	V_{CC18}	ESD diode to GND and supply rail
3	1.8-V LVCMOS I/O buffer with 24-mA drive	V_{CC18}	ESD diode to GND and supply rail
4	1.8-V sub-LVDS output with 4-mA drive	V_{CC18}	ESD diode to GND and supply rail
5	1.8-, 2.5-, 3.3-V LVCMOS with 4-mA drive	V_{CC_INTF}	ESD diode to GND and supply rail
6	1.8-V LVCMOS input	V_{CC18}	ESD diode to GND and supply rail
7	1.8-, 2.5-, 3.3-V I^2C with 3-mA drive	V_{CC_INTF}	ESD diode to GND and supply rail
8	1.8-V I^2C with 3-mA drive	V_{CC18}	ESD diode to GND and supply rail
9	1.8-, 2.5-, 3.3-V LVCMOS with 8-mA drive	V_{CC_INTF}	ESD diode to GND and supply rail
11	1.8-, 2.5-, 3.3-V LVCMOS input	V_{CC_INTF}	ESD diode to GND and supply rail
12	1.8-, 2.5-, 3.3-V LVCMOS input	V_{CC_FLSH}	ESD diode to GND and supply rail
13	1.8-, 2.5-, 3.3-V LVCMOS with 8-mA drive	V_{CC_FLSH}	ESD diode to GND and supply rail

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
SUPPLY VOLTAGE(2)(3)				
$V_{(VDD)}$ (core)		–0.3	1.21	V
$V_{(VDDLP12)}$ (core)		–0.3	1.32	V
$V_{(VCC18)}$ (All 1.8-V Power + sub-LVDS)		–0.3	1.96	V
$V_{(VCC\_INTF)}$	Host I/O power	–0.3	3.60	V
	If 1.8-V power used	–0.3	1.99	
	If 2.5-V power used	–0.3	2.75	
	If 3.3-V power used	–0.3	3.60	
$V_{(VCC\_FLSH)}$	Flash I/O power	–0.3	3.60	V
	If 1.8-V power used	–0.3	1.96	
	If 2.5-V power used	–0.3	2.72	
	If 3.3-V power used	–0.3	3.58	
$V_{(VDD\_PLLM)}$ (MCG PLL)		–0.3	1.21	V
$V_{(VDD\_PLLD)}$ (1DCG PLL)		–0.3	1.21	V
GENERAL				
T_J	Operating junction temperature	–30	125	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Overlap currents, if allowed to continue flowing unchecked, not only increase total power dissipation in a circuit, but degrade the circuit reliability, thus shortening its usual operating life.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(VDD)}$	Core power 1.1 V (main 1.1 V)	±5% tolerance	1.045	1.1	1.155	V
$V_{(VDDLP12)}$	Core power 1.1 V (supplemental 1.1 V)	±5% tolerance	1.045	1.1	1.155	V
$V_{(VCC18)}$	All 1.8-V I/O power: (1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ LED_SEL, CMP, GPIO, IIC1, TSTPT, and JTAG pins.)	±8.5% tolerance	1.64	1.8	1.96	V
$V_{(VCC\_INTF)}$	Host or parallel interface I/O power: 1.8 to 3.3 V (includes IIC0, PDATA, video syncs, and HOST_IRQ pins)	±8.5% tolerance See (1)	1.64	1.8	1.96	V
			2.28	2.5	2.72	
			3.02	3.3	3.58	
$V_{(VCC\_FLSH)}$	Flash interface I/O power: 1.8 to 3.3 V	±8.5% tolerance See (1)	1.64	1.8	1.96	V
			2.28	2.5	2.72	
			3.02	3.3	3.58	
$V_{(VDD\_PLLM)}$	MCG PLL 1.1-V power	±9.1% tolerance See (2)	1.025	1.1	1.155	V
$V_{(VDD\_PLLD)}$	DCG PLL 1.1-V power	±9.1% tolerance See (2)	1.025	1.1	1.155	V
T_A	Operating ambient temperature(3)		–30		85	°C
T_J	Operating junction temperature		–30		105	°C

(1) These supplies have multiple valid ranges.
(2) These I/O supply ranges are wider to facilitate additional filtering.
(3) The operating ambient temperature range assumes 0 forced air flow, a JEDEC JESD51 junction-to-ambient thermal resistance value at 0 forced air flow ($R_{\theta JA}$ at 0 m/s), a JEDEC JESD51 standard test card and environment, along with minimum and maximum estimated power dissipation across process, voltage, and temperature. Thermal conditions vary by application, which impacts $R_{\theta JA}$. Thus, maximum operating ambient temperature varies by application.
   (a) $T_{a\_min} = T_{j\_min} – (P_{d\_min} \times R_{\theta JA}) = –30°C – (0.0\ W \times 30.3°C/W) = –30°C$
   (b) $T_{a\_max} = T_{j\_max} – (P_{d\_max} \times R_{\theta JA}) = 105°C – (0.348\ W \times 30.3°C/W) = 94.4°C$

6.4 Thermal Information

THERMAL METRIC(1)			DLPC3436	UNIT
			ZVB (NFBGA)	
			176 PINS	
$R_{\theta JC}$	Junction-to-case thermal resistance		11.2	°C/W
$R_{\theta JA}$	Junction-to-air thermal resistance	at 0 m/s of forced airflow(2)	30.3	°C/W
		at 1 m/s of forced airflow(2)	27.4	
		at 2 m/s of forced airflow(2)	26.6	
ψ_{JT}	Temperature variance from junction to package top center temperature, per unit power dissipation(3)		0.27	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal coefficients abide by JEDEC Standard 51. $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC3436 PCB and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance.
(3) Example: (0.5 W) × (0.2°C/W) ≈ 0.1°C temperature rise.

6.5 Electrical Characteristics over Recommended Operating Conditions

see (1)(2)(3)

PARAMETER		TEST CONDITIONS(4)(5)	MIN	TYP(6)	MAX(7)	UNIT
$I_{(VDD)}$	Core current 1.1 V (main 1.1 V)	IDLE disabled, 1920 x 1080, 60 Hz			TBE	mA
$I_{(VDD\_PLLM)}$	MCG PLL 1.1-V current	IDLE disabled, 1920 x 1080, 60 Hz			TBD	mA
$I_{(VDD\_PLLD)}$	DCG PLL 1.1-V current	IDLE disabled, 1920 x 1080, 60 Hz			TBD	mA
$I_{(VDD)}$ + $I_{(VDD\_PLLM)}$ + $I_{(VDD\_PLLD)}$	Core Current 1.1 V + MCG PLL 1.1-V current + DCG PLL 1.1-V current	IDLE disabled, 1920 x 1080, 60 Hz		TBD	TBD	mA
$I_{(VCC18)}$	Main 1.8-V I/O current: 1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface. This includes sub-LVDS DMD I/O , RESETZ, PARKZ, LED_SEL, CMP, GPIO, IIC1, TSTPT and JTAG pins	IDLE disabled, 1920 x 1080, 60 Hz			TBD	mA
$I_{(VCC\_INTF)}$	Host or parallel interface I/O current: 1.8 V (includes IIC0, PDATA, video syncs, and HOST_IRQ pins)	IDLE disabled, 1920 x 1080, 60 Hz			TBD	mA
$I_{(VCC\_FLSH)}$	Flash Interface I/O current: 1.8 V to 3.3 V	IDLE disabled, 1920 x 1080, 60 Hz			TBD	mA
$I_{(VCC18)}$ + $I_{(VCC\_INTF)}$ + $I_{(VCC\_FLSH)}$	Main 1.8 V I/O current + V_{CC_INTF} current + V_{CC_FLSH} current	IDLE disabled, 1920 x 1080, 60 Hz		TBD	TBD	mA

(1) Programmable host and flash I/O are at minimum voltage (that is 1.8 V) for this typical scenario.
(2) Max currents column use typical motion video as the input. The typical currents column uses SMPTE color bars as the input.
(3) Some applications may be forced to use 1-oz. copper to manage ASIC package heat.
(4) Chipset input image is 1924 x 1080 24-bits on the FPGA parallel interface at the frame rate shown with a 0.23-inch 1080p DMD.
(5) In normal operation while displaying an image with CAIC enabled. "IDLE" is a low-power mode that is disabled in normal operation.
(6) Assumes typical case power PVT condition = nominal process, typical voltage, typical temperature (55°C junction), a 0.23-inch 1080p DMD.
(7) Assumes worse case power PVT condition = corner process, high voltage, high temperature (105°C junction), a 0.23-inch 1080p DMD.

6.6 Electrical Characteristics(1)(2)

over operating free-air temperature range (unless otherwise noted)

PARAMETER(3)			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input threshold voltage	I^2C buffer (I/O type 7)		0.7 × V_{CC_INTF}		(1)	V
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		1.17		3.6	
		1.8-V LVTTL (I/O type 1, 6) identified below: (2) CMP_OUT; PARKZ; RESETZ; GPIO 0 →19		1.3		3.6	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		1.7		3.6	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		2		3.6	
V_{IL}	Low-level input threshold voltage	I^2C buffer (I/O type 7)		–0.5		0.3 × V_{CC_INTF}	V
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		–0.3		0.63	
		1.8-V LVTTL (I/O type 1, 6) identified below: (2) CMP_OUT; PARKZ; RESETZ; GPIO_00 through GPIO_19		–0.3		0.5	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		–0.3		0.7	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		–0.3		0.8	
V_{CM}	Steady-state common mode voltage	1.8-V sub-LVDS (DMD high speed) (I/O type 4)		0.8	0.9	1	mV
V_{OH}	High-level output voltage	1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		1.35			V
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		1.7			
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		2.4			
		1.8-V sub-LVDS – DMD high speed (I/O type 4)		0.825	1	1.175	
V_{OL}	Low-level output voltage	I^2C buffer (I/O type 7)	$V_{CC\_INTF} > 2$ V			0.4	V
		I^2C buffer (I/O type 7)	$V_{CC\_INTF} < 2$ V			0.2 × V_{CC_INTF}	
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)				0.45	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)				0.7	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)				0.4	
		1.8-V sub-LVDS – DMD high speed (I/O type 4)		0.625	0.8	0.975	

(1) I/O is high voltage tolerant; that is, if V_{CC} = 1.8 V, the input is 3.3-V tolerant, and if V_{CC} = 3.3 V, the input is 5-V tolerant.
(2) ASIC pins: CMP_OUT; PARKZ; RESETZ; GPIO_00 through GPIO_19 have slightly varied V_{IH} and V_{IL} range from other 1.8-V I/O.
(3) The number inside each parenthesis for the I/O refers to the type defined in Table 1.

Electrical Characteristics[(1)][(2)] (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER[(3)]			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OH}	High-level output current	1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	4 mA	2			mA
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	8 mA	3.5			
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	24 mA	10.6			
		2.5-V LVTTL (I/O type 5)	4 mA	5.4			
		2.5-V LVTTL (I/O type 9, 13)	8 mA	10.8			
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)	24 mA	28.7			
		3.3-V LVTTL (I/O type 5)	4 mA	7.8			
		3.3-V LVTTL (I/O type 9, 13)	8 mA	15			
I_{OL}	Low-level output current	I^2C buffer (I/O type 7)		3			mA
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	4 mA	2.3			
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	8 mA	4.6			
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	24 mA	13.9			
		2.5-V LVTTL (I/O type 5)	4 mA	5.2			
		2.5-V LVTTL (I/O type 9, 13)	8 mA	10.4			
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)	24 mA	31.1			
		3.3-V LVTTL (I/O type 5)	4 mA	4.4			
		3.3-V LVTTL (I/O type 9, 13)	8 mA	8.9			
I_{OZ}	High-impedance leakage current	I^2C buffer (I/O type 7)	$0.1 \times V_{CC\_INTF} < V_I < 0.9 \times V_{CC\_INTF}$	–10		10	µA
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		–10		10	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		–10		10	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		–10		10	
C_I	Input capacitance (including package)	I^2C buffer (I/O type 7)				5	pF
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		2.6		3.5	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		2.6		3.5	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		2.6		3.5	
		1.8-V sub-LVDS – DMD high speed (I/O type 4)				3	

6.7 Internal Pullup and Pulldown Characteristics

see (1)(2)

INTERNAL PULLUP AND PULLDOWN RESISTOR CHARACTERISTICS	VCCIO	MIN	MAX	UNIT
Weak pullup resistance	3.3 V	29	63	kΩ
	2.5 V	38	90	kΩ
	1.8 V	56	148	kΩ
Weak pulldown resistance	3.3 V	30	72	kΩ
	2.5 V	36	101	kΩ
	1.8 V	52	167	kΩ

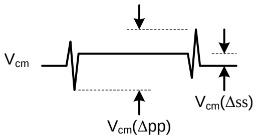
(1) The resistance is dependent on the supply voltage level applied to the I/O.
(2) An external 8-kΩ pullup or pulldown (if needed) would work for any voltage condition to correctly pull enough to override any associated internal pullups or pulldowns.

6.8 High-Speed Sub-LVDS Electrical Characteristics

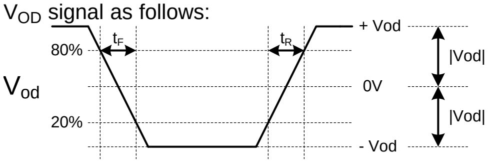
over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{CM}	Steady-state common mode voltage	0.8	0.9	1.0	V
V_{CM} (Δpp)(1)	V_{CM} change peak-to-peak (during switching)			75	mV
V_{CM} (Δss)(1)	V_{CM} change steady state	–10		10	mV
$\lvert V_{OD}\rvert$(2)	Differential output voltage magnitude	150	250	350	mV
V_{OD} (Δ)	V_{OD} change (between logic states)	–10		10	mV
V_{OH}	Single-ended output voltage high		1.00		V
V_{OL}	Single-ended output voltage low		0.80		V
t_R(2)	Differential output rise time			250	ps
t_F(2)	Differential output fall time			250	ps
t_{MAX}	Maximum switching rate			1200	Mbps
DC_{out}	Output duty cycle	45%	50%	55%	
Tx_{term}(1)	Internal differential termination	80	100	120	Ω
Tx_{load}	100-Ω differential PCB trace (50-Ω transmission lines)	0.5		6	inches

(1) Definition of V_{CM} changes:



(2) Note that V_{OD} is the differential voltage swing measured across a 100-Ω termination resistance connected directly between the transmitter differential pins. $\lvert V_{OD}\rvert$ is the magnitude of this voltage swing relative to 0. Rise and fall times are defined for the differential V_{OD} signal as follows:



Differential Output Signal
(Note Vcm is removed when the signals are viewed differentially)

6.9 Low-Speed SDR Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	ID	TEST CONDITIONS	MIN	MAX	UNIT
Operating voltage	V_{CC18} (all signal groups)		1.64	1.96	V
DC input high voltage	V_{IHD}(DC) Signal group 1		0.7 × V_{CC18}	V_{CC18} + 0.5	V
DC input low voltage[1]	V_{ILD}(DC) Signal group 1		–0.50	0.3 × V_{CC18}	V
AC input high voltage[2]	V_{IHD}(AC) Signal group 1		0.8 × V_{CC18}	V_{CC18} + 0.5	V
AC input low voltage	V_{ILD}(AC) Signal group 1		–0.5	0.2 × V_{CC18}	V
Slew rate [3][4][5][6]	Signal group 1		1	3.0	V/ns
	Signal group 2		0.25		
	Signal group 3		0.5		

(1) V_{ILD}(AC) minimum applies to undershoot.
(2) V_{IHD}(AC) maximum applies to overshoot.
(3) Signal group 1 output slew rate for rising edge is measured between V_{ILD}(DC) to V_{IHD}(AC).
(4) Signal group 1 output slew rate for falling edge is measured between V_{IHD}(DC) to V_{ILD}(AC).
(5) Signal group 1: See Figure 1.
(6) Signal groups 2 and 3 output slew rate for rising edge is measured between V_{ILD}(AC) to V_{IHD}(AC).

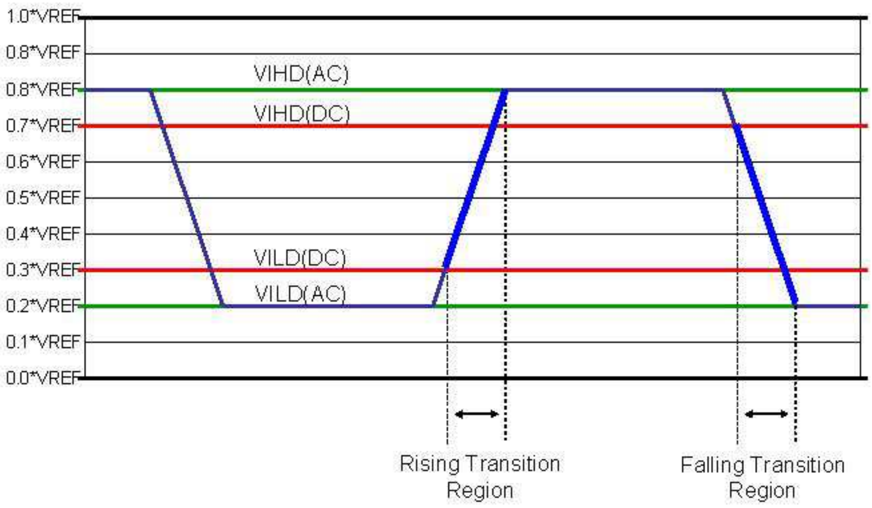


Figure 1. Low Speed (LS) I/O Input Thresholds

6.10 System Oscillators Timing Requirements

see [1]

PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency, MOSC[2]	24-MHz oscillator	23.998	24.002	MHz
t_c	Cycle time, MOSC[2]	24-MHz oscillator	41.663	41.670	ns
$t_{w(H)}$	Pulse duration[3], MOSC, high	50% to 50% reference points (signal)		40 t_c%	
$t_{w(L)}$	Pulse duration[3], MOSC, low	50% to 50% reference points (signal)		40 t_c%	
t_t	Transition time[3], MOSC, $t_t = t_f / t_r$	20% to 80% reference points (signal)		10	ns
t_{jp}	Long-term, peak-to-peak, period jitter[3], MOSC (that is the deviation in period from ideal period due solely to high frequency jitter)			2%	

(1) The I/O pin TSTPT_6 enables the ASIC to use two different oscillator frequencies through a pullup control at initial ASIC power-up. TSTPT_6 should be grounded so that 24 MHz is always selected.
(2) The frequency accuracy for MOSC is ±200 PPM. This includes impact to accuracy due to aging, temperature, and trim sensitivity. The MOSC input cannot support spread spectrum clock spreading.
(3) Applies only when driven through an external digital oscillator.

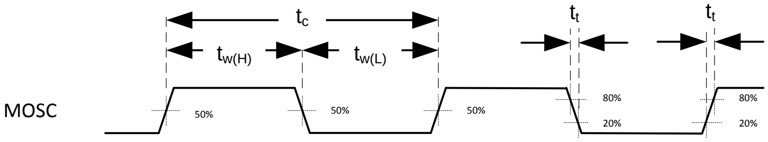


Figure 2. System Oscillators

6.11 Power-Up and Reset Timing Requirements

PARAMETER			MIN	MAX	UNIT
$t_{w(L)}$	Pulse duration, inactive low, RESETZ	50% to 50% reference points (signal)	1.25		µs
t_t	Transition time, RESETZ, $t_t = t_f / t_r$	20% to 80% and 80% to 20% reference points (signal)		0.5	µs

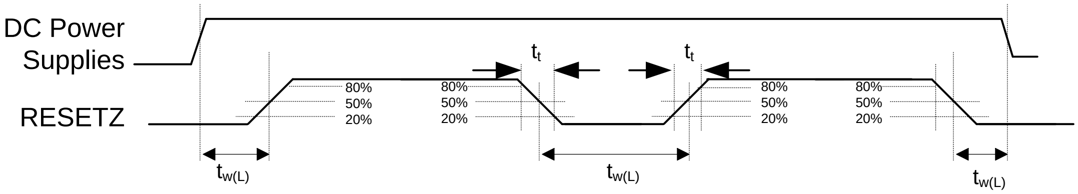


Figure 3. Power-Up and Power-Down RESETZ Timing

6.12 Parallel Interface Frame Timing Requirements

			MIN	MAX	UNIT
t_{p_vsw}	Pulse duration – VSYNC_WE high	50% reference points	1		lines
t_{p_vbp}	Vertical back porch (VBP) – time from the leading edge of VSYNC_WE to the leading edge HSYNC_CS for the first active line (see [1])	50% reference points	2		lines
t_{p_vfp}	Vertical front porch (VFP) – time from the leading edge of the HSYNC_CS following the last active line in a frame to the leading edge of VSYNC_WE (see [1])	50% reference points	1		lines
t_{p_tvb}	Total vertical blanking – time from the leading edge of HSYNC_CS following the last active line of one frame to the leading edge of HSYNC_CS for the first active line in the next frame. (This is equal to the sum of VBP (t_{p_vbp}) + VFP (t_{p_vfp}).)	50% reference points	See [1]		lines
t_{p_hsw}	Pulse duration – HSYNC_CS high	50% reference points	4	128	PCLKs
t_{p_hbp}	Horizontal back porch – time from rising edge of HSYNC_CS to rising edge of DATAEN_CMD	50% reference points	4		PCLKs
t_{p_hfp}	Horizontal front porch – time from falling edge of DATAEN_CMD to rising edge of HSYNC_CS	50% reference points	8		PCLKs
t_{p_thb}	Total horizontal blanking – sum of horizontal front and back porches	50% reference points	See [2]		PCLKs

(1) The minimum total vertical blanking is defined by the following equation: $t_{p\_tvb}(\text{min}) = 6 + [8 \times \text{Max}(1, \text{Source\_ALPF}/ \text{DMD\_ALPF})]$ lines where:
(a) SOURCE_ALPF = Input source active lines per frame
(b) DMD_ALPF = Actual DMD used lines per frame supported

(2) Total horizontal blanking is driven by the maximum line rate for a given source which is a function of resolution and orientation. The following equation can be applied for this: $t_{p\_thb} = \text{Roundup}[(1000 \times f_{clock})/ \text{LR}] - \text{APPL}$
where:
(a) f_{clock} = Pixel clock rate in MHz
(b) LR = Line rate in kHz
(c) APPL is the number of active pixels per (horizontal) line.
(d) If t_{p_thb} is calculated to be less than $t_{p\_hbp} + t_{p\_hfp}$ then the pixel clock rate is too low or the line rate is too high, and one or both must be adjusted.

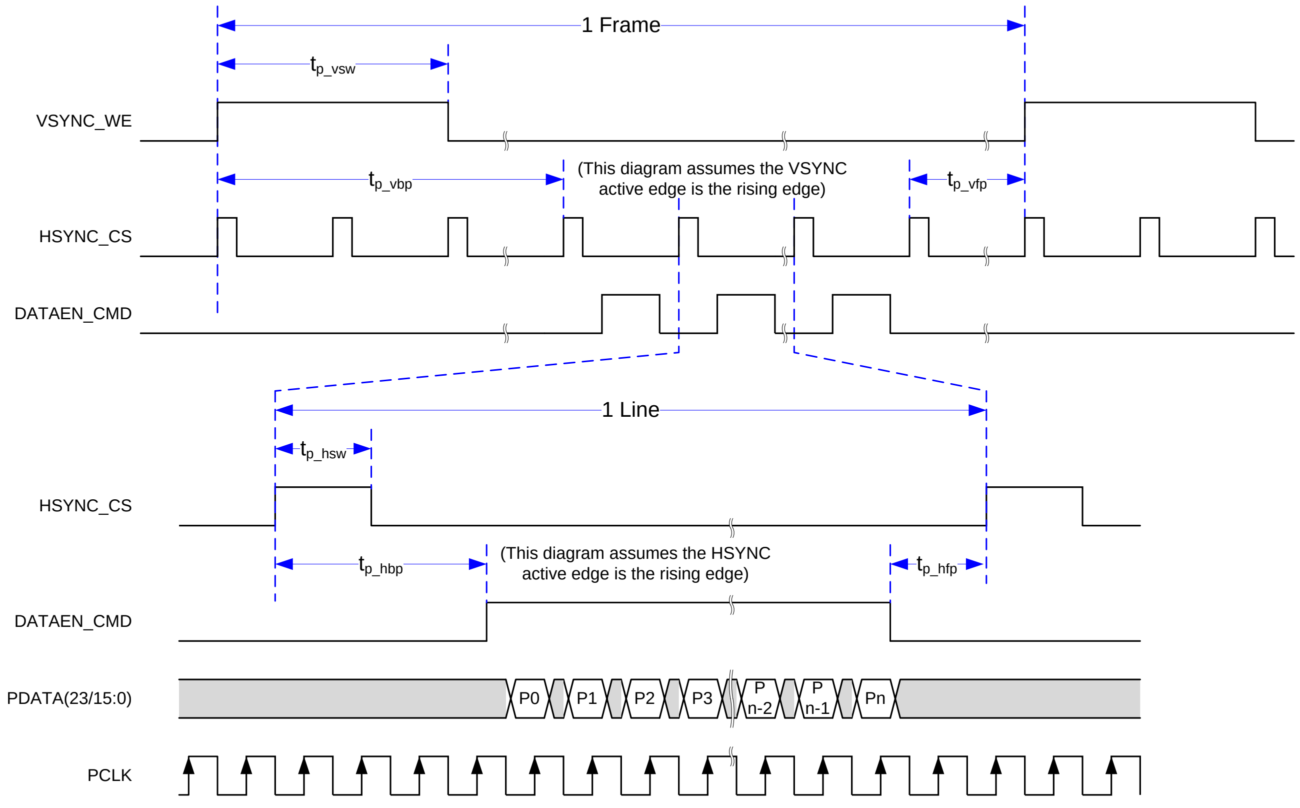


Figure 4. Parallel Interface Frame Timing

6.13 Parallel Interface General Timing Requirements

see (1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		1.0	150.0	MHz
t_{p_clkper}	Clock period, PCLK	50% reference points	6.67	1000	ns
t_{p_clkjit}	Clock jitter, PCLK	Maximum f_{clock}		see (2)	
t_{p_wh}	Pulse duration low, PCLK	50% reference points	2.43		ns
t_{p_wl}	Pulse duration high, PCLK	50% reference points	2.43		ns
t_{p_su}	Setup time – HSYNC_CS, DATEN_CMD, PDATA(23:0) valid before the active edge of PCLK	50% reference points	0.9		ns
t_{p_h}	Hold time – HSYNC_CS, DATEN_CMD, PDATA(23:0) valid after the active edge of PCLK	50% reference points	0.9		ns
t_t	Transition time – all signals	20% to 80% and 80% to 20% reference points	0.2	2.0	ns

(1) The active (capture) edge of PCLK for HSYNC_CS, DATEN_CMD and PDATA(23:0) is software programmable, but defaults to the rising edge.

(2) Clock jitter (in ns) should be calculated using this formula: Jitter = [1 / f_{clock} – 5.76 ns]. Setup and hold times must be met during clock jitter.

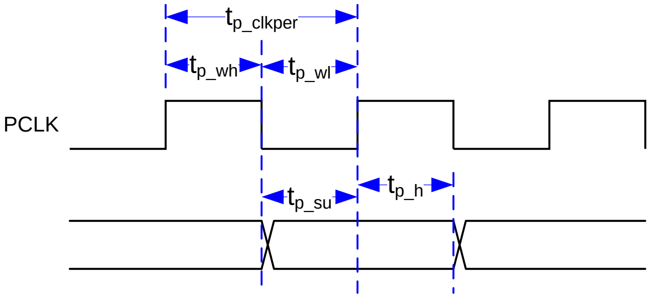


Figure 5. Parallel Interface General Timing

6.14 Flash Interface Timing Requirements

The DLPC3436 ASIC flash memory interface consists of a SPI flash serial interface with a programmable clock rate. The DLPC3436 can support 1- to 16-Mb flash memories.(1)(2)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, SPI_CLK	See (3)	1.42	36.0	MHz
t_{p_clkper}	Clock period, SPI_CLK	50% reference points	27.7	704	ns
t_{p_wh}	Pulse duration low, SPI_CLK	50% reference points	352		ns
t_{p_wl}	Pulse duration high, SPI_CLK	50% reference points	352		ns
t_t	Transition time – all signals	20% to 80% and 80% to 20% reference points	0.2	3.0	ns
t_{p_su}	Setup time – SPI_DIN valid before SPI_CLK falling edge	50% reference points	10.0		ns
t_{p_h}	Hold time – SPI_DIN valid after SPI_CLK falling edge	50% reference points	0.0		ns
t_{p_clqv}	SPI_CLK clock falling edge to output valid time – SPI_DOUT and SPI_CSZ	50% reference points		1.0	ns
t_{p_clqx}	SPI_CLK clock falling edge output hold time – SPI_DOUT and SPI_CSZ	50% reference points	–3.0	3.0	ns

(1) Standard SPI protocol is to transmit data on the falling edge of SPI_CLK and capture data on the rising edge. The DLPC3436 does transmit data on the falling edge, but it also captures data on the falling edge rather than the rising edge. This provides support for SPI devices with long clock-to-Q timing. DLPC3436 hold capture timing has been set to facilitate reliable operation with standard external SPI protocol devices.
(2) With the above output timing, DLPC3436 provides the external SPI device 8.2-ns input set-up and 8.2-ns input hold, relative to the rising edge of SPI_CLK.
(3) This range include the 200 ppm of the external oscillator (but no jitter).

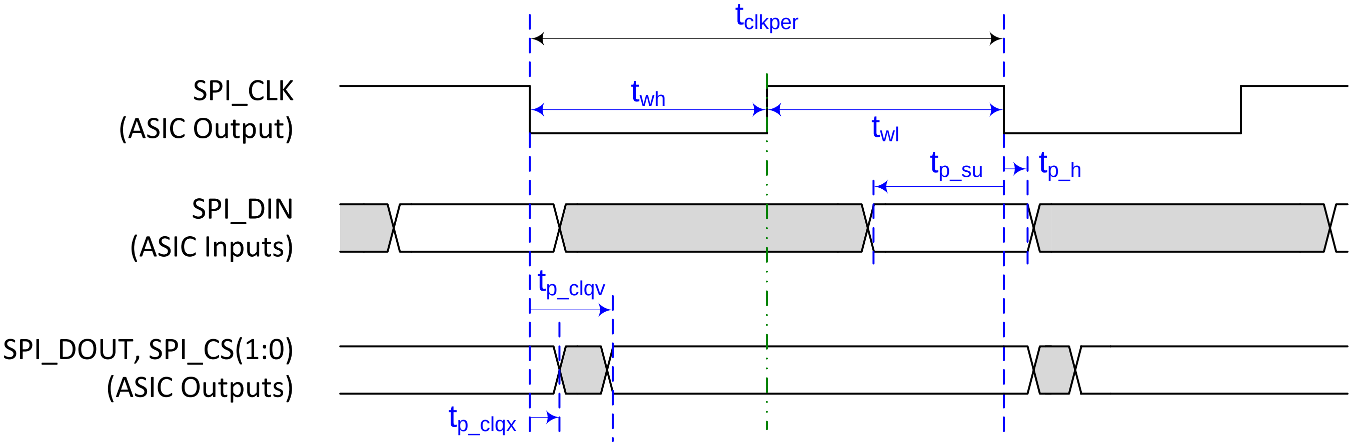
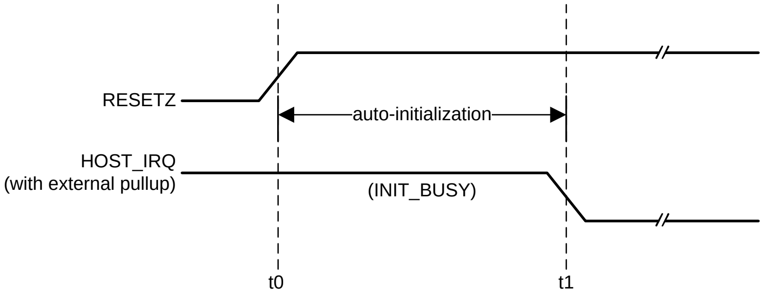


Figure 6. Flash Interface Timing

7 Parameter Measurement Information

7.1 HOST_IRQ Usage Model

- While reset is applied HOST_IRQ resets to tri-state (an external pullup pulls the line high).
- HOST_IRQ remains tri-state (pulled high externally) until the microprocessor boot completes. While the signal is pulled high, this indicates that the ASIC is performing boot-up and auto-initialization.
- As soon as possible after boot-up, the microprocessor drives HOST_IRQ to a logic high state to indicate that the ASIC is continuing to perform auto-initialization (no real state change occurs on the external signal)
- Upon completion of auto-initialization, software sets HOST_IRQ to a logic low state to indicate the completion of auto-initialization. (At the falling edge, the system is said to enter the INIT_DONE state.)
- The 500-ms maximum shown from the rising edge of RESETZ to the falling edge of HOST_IRQ may become longer than 500 ms if many commands are added to the autoinit batch file in flash which automatically runs at power up.



t1 is the first falling edge of HOST_IRQ, At this point the auto-initiation sequence is complete.

t2 is when HOST_IRQ goes low. Ensure that the I^2C device interface does not begin until this point (within 500 ms of the release of RESETZ)

Figure 7. Host IRQ Timing

7.2 Input Frame Rates and 3-D Display Operation

Table 2. Supported Input Source Ranges(1)(2)(3)(4)

INTERFACE	BITS / PIXEL (5)	IMAGE TYPE	SOURCE RESOLUTION RANGE (6)				FRAME RATE RANGE
			HORIZONTAL		VERTICAL		
			Landscape	Portrait	Landscape	Portrait	
Parallel	24	2D - qHD	960	N/A	540	N/A	100 ± 2 Hz, 120 ± 2 Hz
Parallel	24	2D - 1080p	1920	N/A	1080	N/A	50 ± 2 Hz, 60 ± 2 Hz
Parallel	24	3D - qHD(7)	960	N/A	540	N/A	100 ± 2 Hz, 120 ± 2 Hz

(1) The application must remain within specifications for all source interface parameters such as maximum clock rate and maximum line rate.
(2) The maximum DMD size for all rows in the table is 960 × 540.
(3) To achieve the ranges stated, the composer-created firmware used must be defined to support the source parameters used.
(4) These interfaces are supported with the DMD sequencer sync mode command (3Bh) set to auto.
(5) Bits per pixel does not necessarily equal the number of data pins used on the DLPC3436. Fewer pins are used if multiple clocks are used per pixel transfer.
(6) The DLPC3436 supports only landscape orientation.
(7) Formatted as frame sequential.

The DLPC3436 supports both 2D and 3D sources on the parallel interface. The frame and sub-frame timing for 2D sources is shown in Figure 8 while the frame timing for 3D sources is shown in Figure 9.

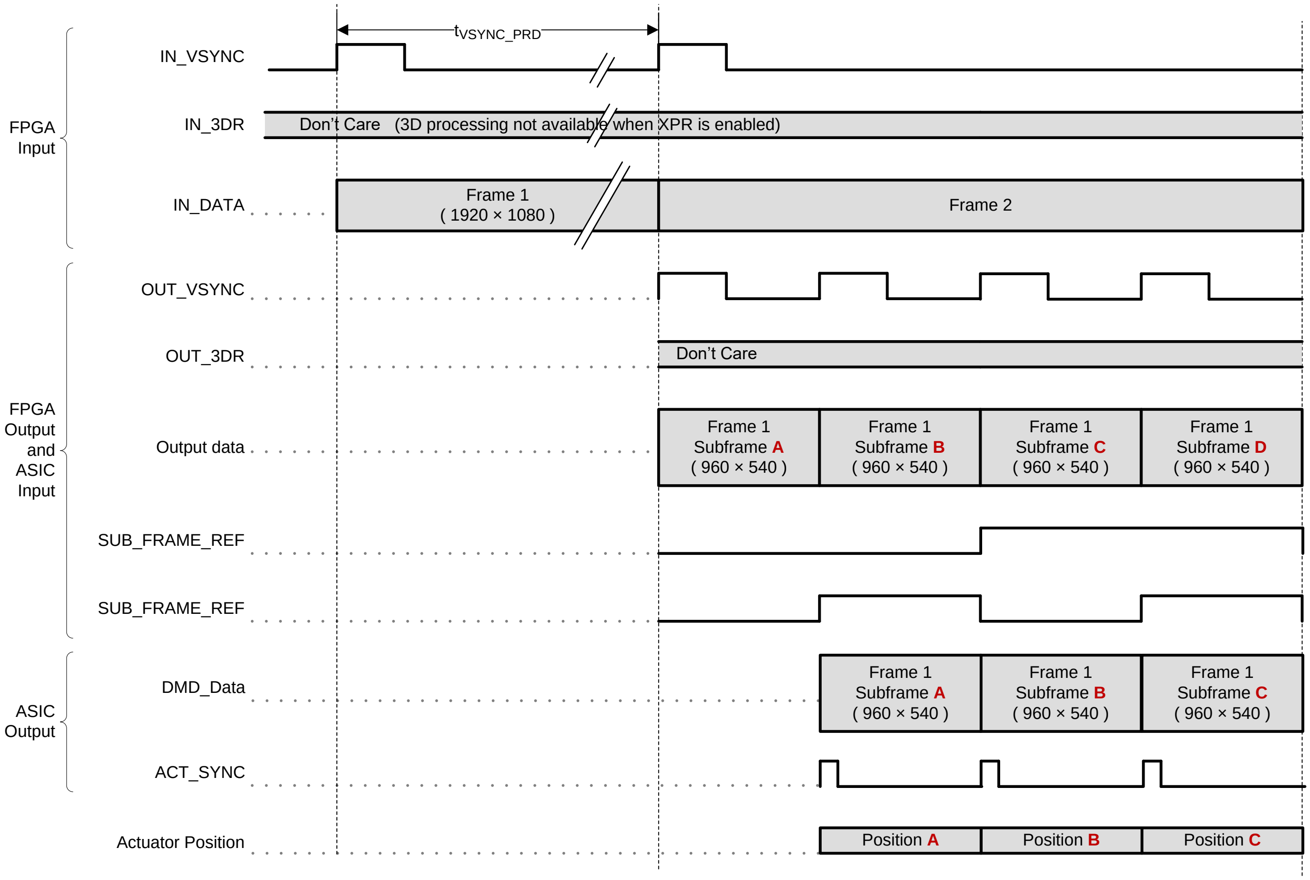


Figure 8. 2D Actuator Frame and Signal Timing

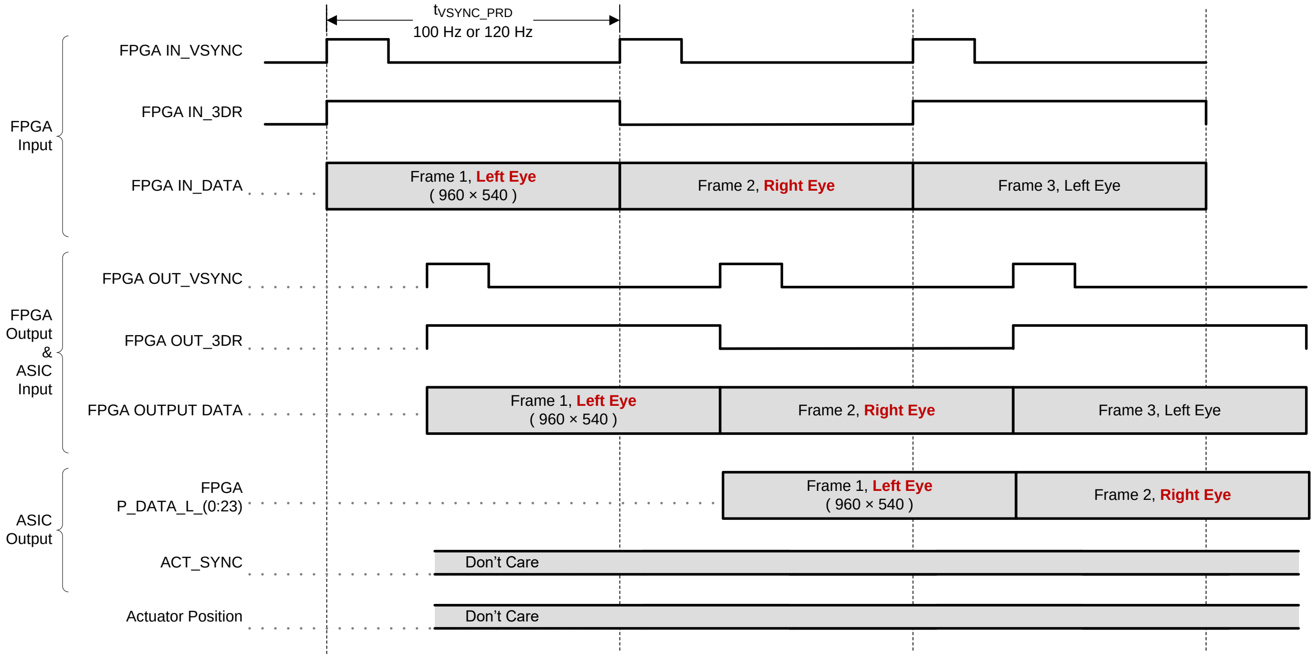


Figure 9. 3D Frame and Signal Timing

7.2.1 Parallel Interface Data Transfer Format

The data format on the PDATA(23:0) bus between the .23 1080p FPGA and the DLPC3436 is always RGB888, as shown in Figure 10.

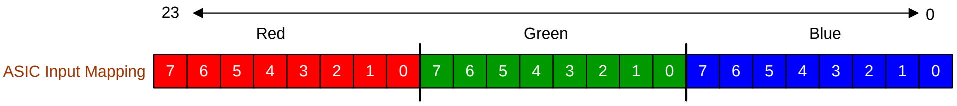


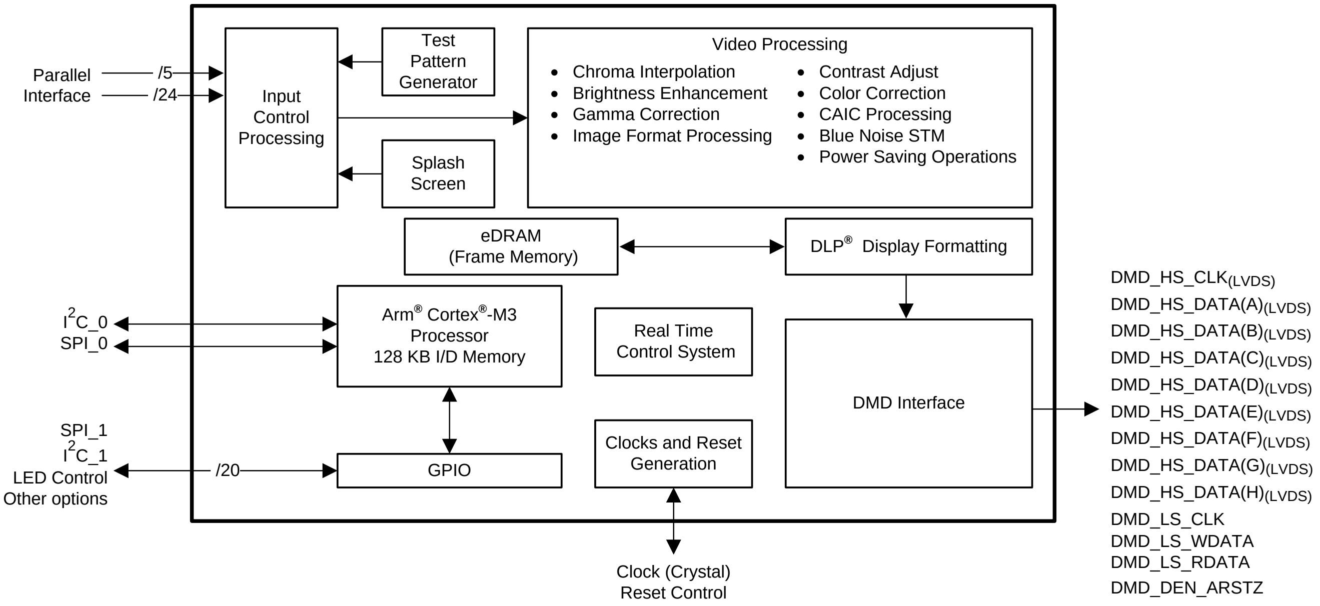
Figure 10. RGB-888 I/O Mapping

8 Detailed Description

8.1 Overview

The DLPC3436 is the display controller for the DLP230NP (.23 1080p) DMD. The DLPC3436 is part of the chipset comprised of the DLPC3436 controller, the DLP230NP (.23 1080p) DMD, and the DLPA2000, DLPA2005, or DLPA3000 PMIC/LED driver. All three components of the chipset must be used in conjunction with each other, along with the XC7Z020-1CLG484I4493 FPGA, for reliable operation of the DLP230NP (.23 1080p) DMD. The DLPC3436 display controller provides interfaces and data/image processing functions that are optimized for small form factor and power-constrained display applications. Applications include smart phone, tablet, laptop, battery-powered mobile accessories, wearable (near-eye) displays, smart home displays, and smart speakers. An application processor is needed to interface with the DLP Pico display sub-system.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Interface Timing Requirements

This section defines the timing requirements for the external interfaces for the DLPC3436 ASIC.

8.3.1.1 Parallel Interface

The parallel interface complies with standard graphics interface protocol, with the addition of the SUB_FRAME signal (which is a necessary output from the XC7Z020-1CLG484I4493 FPGA). The standard graphics interface protocol includes a vertical sync signal (VSYNC_WE), horizontal sync signal (HSYNC_CS), optional data valid signal (DATAEN_CMD), a 24-bit data bus (PDATA), and a pixel clock (PCLK). The polarity of both syncs and the active edge of the clock are programmable. Figure 4 shows the relationship of these signals.

NOTE

VSYNC_WE must remain active at all times (in lock-to-VSYNC mode) or the display sequencer stops and cause the LEDs to be turned off.

8.3.2 Serial Flash Interface

DLPC3436 uses an external SPI serial flash memory device for configuration support. The minimum required size is dependent on the desired minimum number of sequences, CMT tables, and splash options while the maximum supported size is 128 Mb.

For access to flash, the controller uses a single SPI interface operating at a programmable frequency complying to industry standard SPI flash protocol. The programmable SPI frequency is defined to be equal to 180 MHz/N, where N is a programmable value between 5 to 127 providing a range from 36.0 to 1.41732 MHz. Note that this results in a relatively large frequency step size in the upper range (for example, 36 MHz, 30 MHz, 25.7 MHz, 22.5 MHz, and so forth) and thus this must be taken into account when choosing a flash device.

The controller supports two independent SPI chip selects, however, the flash must be connected to SPI chip select zero (SPI0_CSZ0) because the boot routine is only executed from the device connected to chip select zero (SPI0_CSZ0). The boot routine uploads program code from flash to program memory, then transfers control to an auto-initialization routine within program memory. The controller asserts the HOST_IRQ output signal high while auto-initialization is in progress, then drives it low to signal its completion to the host processor. Only after auto-initialization is complete can the controller receive commands through I^2C.

The controller should support any flash device that is compatible with the modes of operation, features, and performance as defined in Table 3 and Table 4.

Table 3. SPI Flash Required Features or Modes of Operation

FEATURE	DLPC3436 REQUIREMENT
SPI interface width	Single
SPI protocol	SPI mode 0
Fast READ addressing	Auto-incrementing
Programming mode	Page mode
Page size	256 B
Sector size	4 kB sector
Block size	any
Block protection bits	0 = Disabled
Status register bit(0)	Write in progress (WIP) {also called flash busy}
Status register bit(1)	Write enable latch (WEN)
Status register bits(6:2)	A value of 0 disables programming protection
Status register bit(7)	Status register write protect (SRWP)
Status register bits(15:8) (that is expansion status byte)	The DLPC3436 only supports single-byte status register R/W command execution, and thus may not be compatible with flash devices that contain an expansion status byte. However, as long as the expansion status byte is considered optional in the byte 3 position and any write protection control in this expansion status byte defaults to unprotected, then the device should be compatible with DLPC3436.

To support flash devices with program protection defaults of either enabled or disabled, the DLPC3436 always assumes the device default is enabled and goes through the process of disabling protection as part of the boot-up process. This process consists of:

- A write enable (WREN) instruction executed to request write enable, followed by
- A read status register (RDSR) instruction is then executed (repeatedly as needed) to poll the write enable latch (WEL) bit
- After the write enable latch (WEL) bit is set, a write status register (WRSR) instruction is executed that writes 0 to all 8-bits (this disables all programming protection)

Prior to each program or erase instruction, the controller issues:

- A write enable (WREN) instruction to request write enable, followed by
- A read status register (RDSR) instruction (repeated as needed) to poll the write enable latch (WEL) bit
- After the write enable latch (WEL) bit is set, the program or erase instruction is executed
- Note the flash automatically clears the write enable status after each program and erase instruction

The specific instruction OpCode and timing compatibility requirements are listed in Table 4 and Table 5. Note however that the controller does not read the flash’s electronic signature ID and thus cannot automatically adapt protocol and clock rate based on the ID.

Table 4. SPI Flash Instruction OpCode and Access Profile Compatibility Requirements

SPI FLASH COMMAND	FIRST BYTE (OPCODE)	SECOND BYTE	THIRD BYTE	FOURTH BYTE	FIFTH BYTE	SIXTH BYTE
Fast READ (1 Output)	0x0B	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0)(1)
Read status	0x05	n/a	n/a	STATUS(0)		
Write status	0x01	STATUS(0)	(2)			
Write enable	0x06					
Page program	0x02	ADDRS(0)	ADDRS(1)	ADDRS(2)	DATA(0)(1)	
Sector erase (4KB)	0x20	ADDRS(0)	ADDRS(1)	ADDRS(2)		
Chip erase	0xC7					

(1) Only the first data byte is shown, data continues.
(2) DLPC3436 does not support access to a second or expansion write status byte.

The specific and timing compatibility requirements for a DLPC3436 compatible flash are listed in Table 5 and Table 6.

Table 5. SPI Flash Key Timing Parameter Compatibility Requirements(1)(2)

SPI FLASH TIMING PARAMETER	SYMBOL	ALTERNATE SYMBOL	MIN	MAX	UNIT
Access frequency (all commands)	f_R	f_C	≤1.42		MHz
Chip select high time (also called chip select deselect time)	t_{SHSL}	t_{CSH}	≤200		ns
Output hold time	t_{CLQX}	t_{HO}	≥0		ns
Clock low to output valid time	t_{CLQV}	t_V		≤ 11	ns
Data in set-up time	t_{DVCH}	t_{DSU}	≤5		ns
Data in hold time	t_{CHDX}	t_{DH}	≤5		ns

(1) The timing values are related to the specification of the flash device itself, not the DLPC3436.
(2) The DLPC3436 does not drive the $\overline{\text{HOLD}}$ or $\overline{\text{WP}}$ (active low write protect) pins on the flash device, and thus these pins should be tied to a logic high on the PCB through an external pullup.

The DLPC3436 supports 1.8-, 2.5-, or 3.3-V serial flash devices. To do so, VCC_FLSH must be supplied with the corresponding voltage. Table 6 contains a list of 1.8-, 2.5-, and 3.3-V compatible SPI serial flash devices supported by the DLPC3436.

8.3.3 Tested Flash Devices

Table 6. DLPC3436 Compatible SPI Flash Device Options (3.3-V Compatible Devices)(1)

DVT(2)	DENSITY (Mb)	VENDOR	PART NUMBER	PACKAGE SIZE
Yes	32 Mb	Winbond	W25Q32FVSSIG	5.2 mm × 7.9 mm, 8-pin SOIC
Yes	64 Mb	Winbond	W25Q64FVSSIG	5.2 mm × 7.9 mm, 8-pin SOIC

(1) The flash supply voltage must match VCC_FLSH on the DLPC3436. Special attention needs to be paid when ordering devices to be sure the desired supply voltage is attained as multiple voltage options are often available under the same base part number.

(2) All of the flash devices shown are compatible with the DLPC3436, but only those marked with yes in the DVT column have been validated during TI validation testing using a TI reference design. Those marked with no can be used at the ODM's own risk. Other parts than those shown can be used if the timing conditions in *Serial Flash Interface* are met.

8.3.4 Serial Flash Programming

Note that the flash can be programmed through the DLPC3436 over I^{2}C or by driving the SPI pins of the flash directly while the controller I/O are tri-stated. SPI0_CLK, SPI0_DOUT, and SPI0_CSZ0 I/O can be tri-stated by holding RESETZ in a logic low state while power is applied to the controller . Note that SPI0_CSZ1 is not tri-stated by this same action.

8.3.5 SPI Signal Routing

The DLPC3436 is designed to support two SPI slave devices on the SPI0 interface, specifically, a serial flash and the DLPAxxxx. This requires routing associated SPI signals to two locations while attempting to operate up to 36 MHz. Take special care to ensure that reflections do not compromise signal integrity. To this end, the following recommendations are provided:

- The SPI0_CLK PCB signal trace from the controller source to each slave device should be split into separate routes as close to the controller as possible. In addition, the SPI0_CLK trace length to each device should be equal in total length.
- The SPI0_DOUT PCB signal trace from the DLPC3436 source to each slave device should be split into separate routes as close to the controller as possible. In addition, the SPI0_DOUT trace length to each device should be equal in total length(use the same strategy as SPI0_CLK).
- The SPI0_DIN PCB signal trace from each slave device to the point where they intersect on their way back to the DLPC3436 should be made equal in length and as short as possible. They should then share a common trace back to the controller .
- SPI0_CSZ0 and SPI0_CSZ1 need no special treatment because they are dedicated signals which drive only one device.

8.3.6 I^{2}C Interface Performance

Both DLPC3436 I^{2}C interface ports support 100-kHz baud rate. By definition, I^{2}C transactions operate at the speed of the slowest device on the bus, thus there is no requirement to match the speed grade of all devices in the system.

8.3.7 Content-Adaptive Illumination Control

Content-adaptive illumination control (CAIC) is an image processing algorithm that takes advantage of the fact that in common real-world image content most pixels in the images are well below full scale for the for the R, G, and B digital channels being input to the DLPC3436. As a result of this the average picture level (APL) for the overall image is also well below full scale, and the system's dynamic range for the collective set of pixel values is not fully utilized. CAIC takes advantage of this headroom between the source image APL and the top of the available dynamic range of the display system.

CAIC evaluates images frame by frame and derives three unique digital gains, one for each of the R, G, and B color channels. During CAIC image processing, each gain is applied to all pixels in the associated color channel. CAIC derives each color channel's gain that is applied to all pixels in that channel so that the pixels as a group collectively shift upward and as close to full scale as possible. To prevent any image quality degradation, the gains are set at the point where just a few pixels in each color channel are clipped. Figure 11 and Figure 12 show an example of the application of CAIC for one color channel.

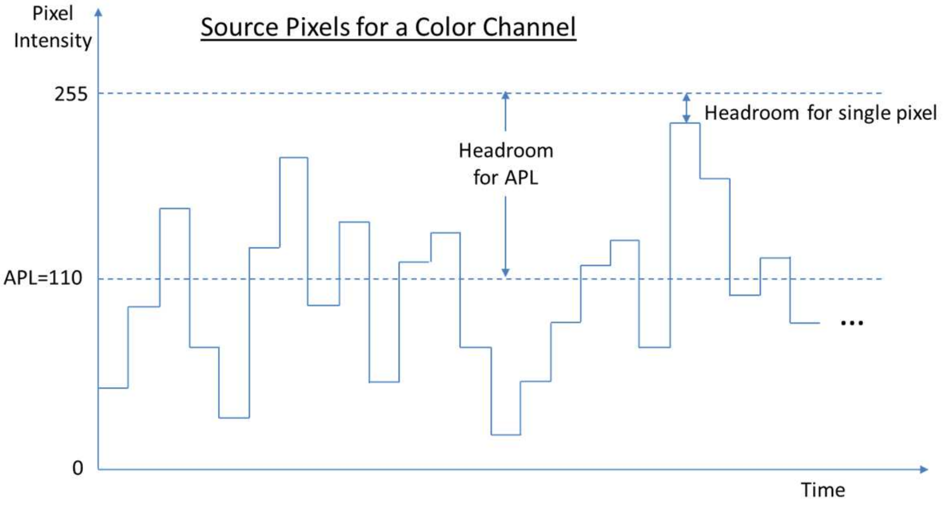


Figure 11. Input Pixels Example

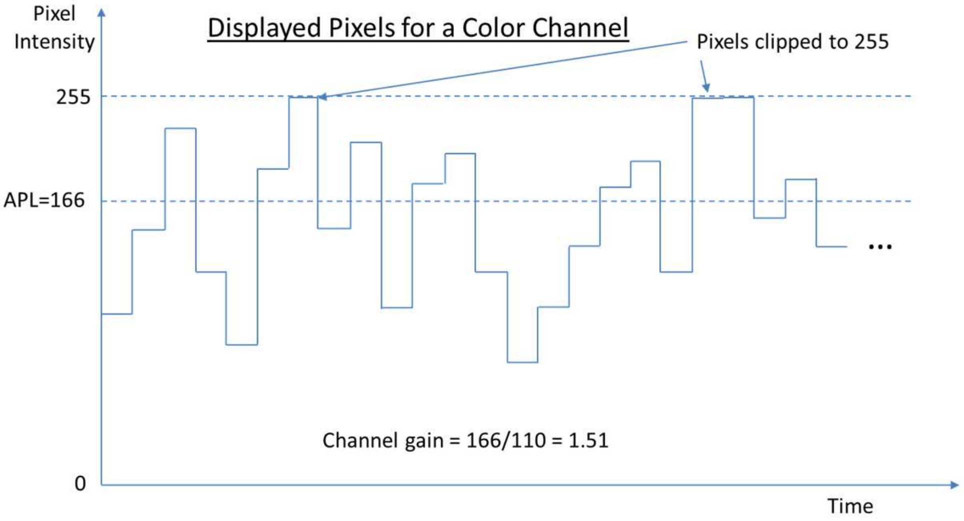


Figure 12. Displayed Pixels After CAIC Processing

Figure 12 shows the gain that is applied to a color processing channel inside the controller. CAIC adjusts the power for the R, G, and B LED. For each color channel of an individual frame, CAIC intelligently determines the optimal combination of digital gain and LED power. The decision regarding how much digital gain to apply to a color channel and how much to adjust the LED power for that color is heavily influenced by the software command settings sent to the controller for configuring CAIC.

As CAIC applies a digital gain to each color channel independently, and adjusts each LED's power independently, CAIC also makes sure that the resulting color balance in the final image matches the target color balance for the projector system. Thus, the effective displayed white point of images is held constant by CAIC from frame to frame.

Because the R, G, and B channels can be gained up by CAIC inside the controller , the LED power can be turned down for any color channel until the brightness of the color on the screen is unchanged. Thus, CAIC can achieve an overall LED power reduction while maintaining the same overall image brightness as if CAIC was not used. Figure 13 shows an example of LED power reduction by CAIC for an image where the R and B LEDs can be turned down in power.

CAIC can alternatively be used to increase the overall brightness of an image while holding the total power for all LEDs constant. In summary, when CAIC is enabled CAIC can operate in one of two distinct modes:

- Power Reduction Mode holds overall image brightness constant while reducing LED power
- Enhanced Brightness Mode holds overall LED power constant while enhancing image brightness

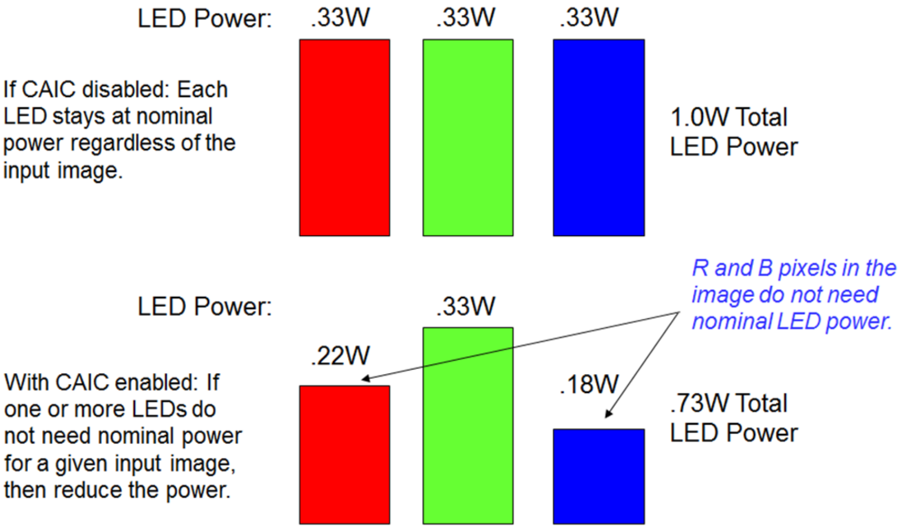


Figure 13. CAIC Power Reduction Mode (for Constant Brightness)

8.3.8 Local Area Brightness Boost

Local area brightness boost (LABB), is an image processing algorithm that adaptively gains up regions of an image that are dim relative to the average picture level. Some regions of the image have significant gain applied, and some regions have little or no gain applied. LABB evaluates images frame by frame and derives the local area gains to be used uniquely for each image. Because many images have a net overall boost in gain even if some parts of the image get no gain, the overall perceived brightness of the image is boosted.

Figure 14 shows a split screen example of the impact of the LABB algorithm for an image that includes dark areas.

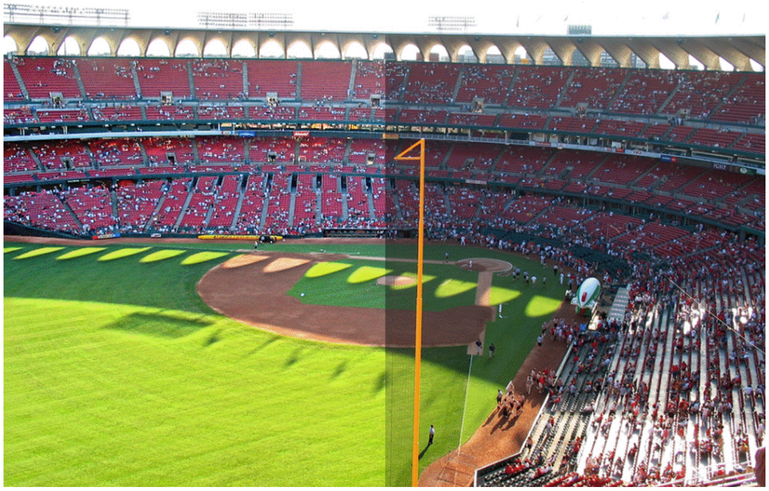


Figure 14. Boosting Brightness in Local Areas of an Image

LABB works best when the decision about the strength of gains used is determined by ambient light conditions. For this reason, there is an option to add an ambient light sensor which can be read by the controller during each frame. Based on the sensor readings, LABB applies higher gains for bright rooms to help overcome any washing out of images. LABB applies lower gains in dark rooms to prevent over-punching of images.

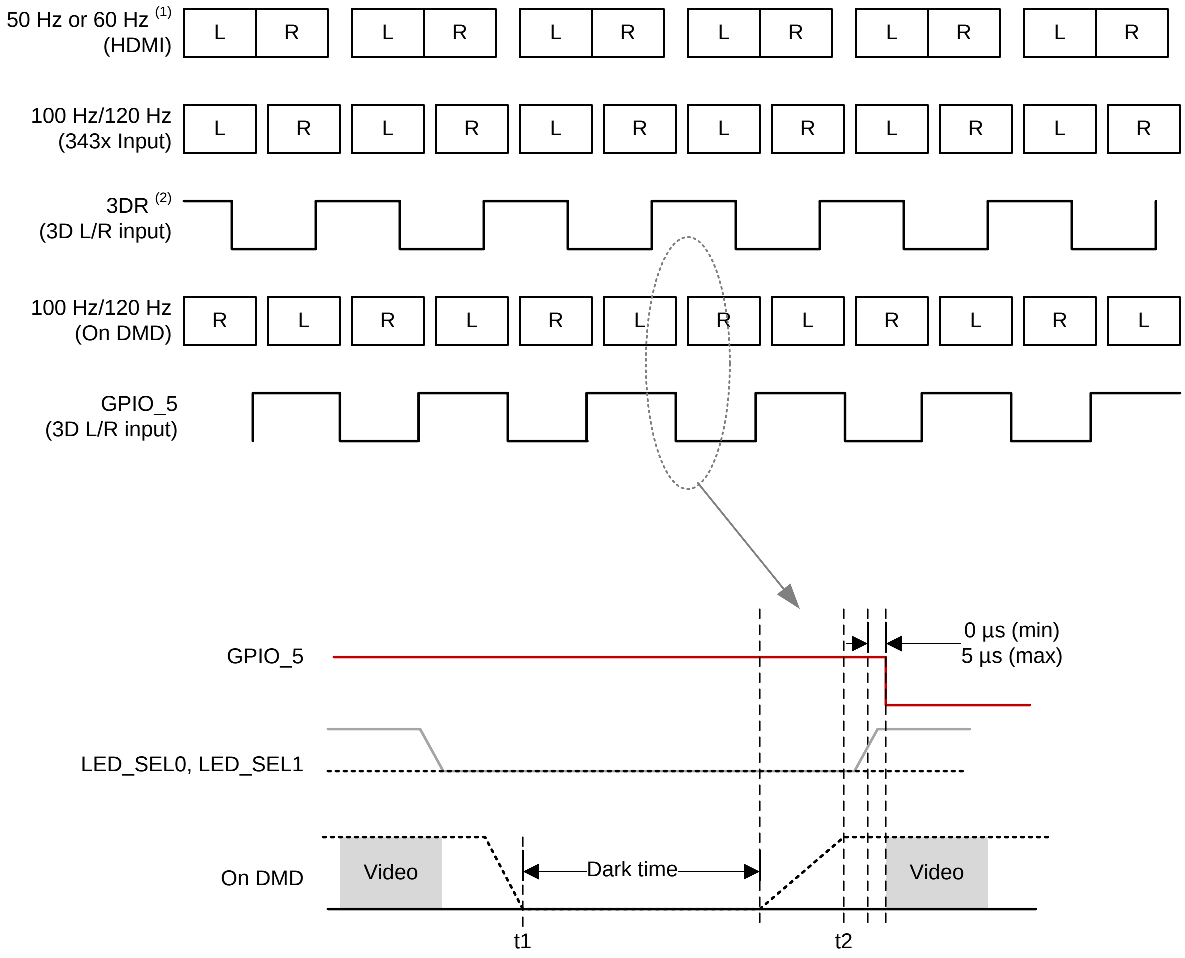
8.3.9 3-D Glasses Operation

For supporting 3D glasses, the DLPC3436 chip set outputs sync information to synchronize the Left eye/Right eye shuttering in the glasses with the displayed DMD image frames.

Two different types of glasses are often used to achieve synchronization. One relies on an IR transmitter on the system PCB to send an IR sync signal to an IR receiver in the glasses. In this case controller output signal GPIO_05 can be used to cause the IR transmitter to send an IR sync signal to the glasses. The timing for signal GPIO_05 is shown in .

The second type of glasses relies on sync information that is encoded into the light being outputted from the projection lens. This is referred to as the DLP Link approach for 3D, and many 3D glasses from different suppliers have been built using this method. This demonstrates that the DLP Link method can work reliable. The advantage of the DLP Link approach is that it takes advantage of existing projector hardware to transmit the sync information to the glasses. This can save cost, size and power in the projector.

For generating the DLP Link sync information, the chipset ourputs one light pulse per DMD frame from the projection lens while the glasses have both shutters closed. To achieve this behavior, the DLPC3436 communicates the DLPAxxxx to turn on the illumination source (typically LEDs or lasers) so that an encoded light pulse is output once per DMD frame. Because the shutters in the glasses are both off when the DLP Link pulse is sent, the projector illumination source remains off except for the when light is sent to create the DLP Link pulse. The timing for the light pulses for DLP Link 3D operation is shown in Figure 15 and Figure 16.



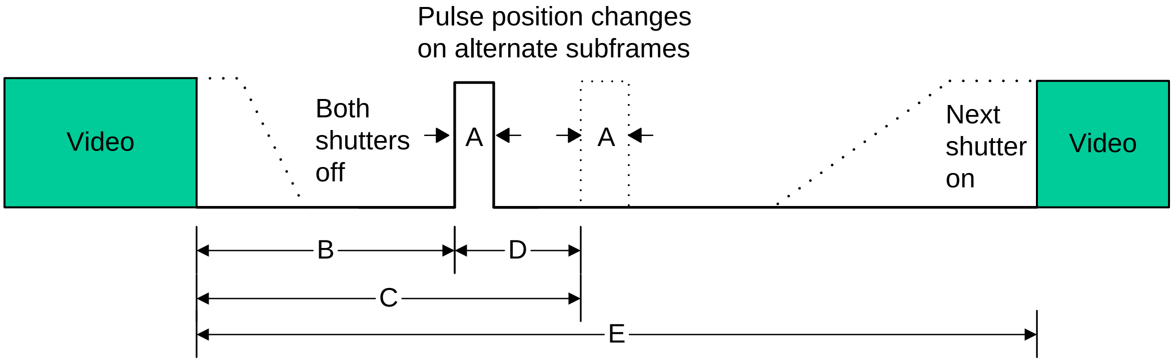
(1) Left = 1, Right = 0

(2) 3DR must toggle 1 ms before VSYNC

t1: both shutters off

t2: next shutter on

Figure 15. DLPC3436 L/R Frame and Signal Timing



NOTE: The period between DLPLink pulses alternates between the subframe period +D and the subframe period –D, where D is the delta period.

Figure 16. 3D DLP Link Pulse Timing

8.3.10 DMD (Sub-LVDS) Interface

The DLPC3436 ASIC DMD interface consists of a HS 1.8-V sub-LVDS output only interface with a maximum clock speed of 600-MHz DDR and a LS SDR (1.8-V LVCMOS) interface with a fixed clock speed of 120 MHz. The controller sub-LVDS interface supports a number of DMD display sizes, and as a function of resolution, not all output data lanes are needed as DMD display resolutions decrease in size. With internal software selection, the controller also supports a limited number of DMD interface swap configurations that can help board layout by remapping specific combinations of DMD interface lines to other DMD interface lines as needed. Table 7 shows the two options available for the DLP230NP (.23 1080p) DMD specifically.

Table 7. DLP230NP (.23 1080p) DMD – ASIC to 8-Lane DMD Pin Mapping Options

DLPC3436 ASIC 8 LANE DMD ROUTING OPTIONS		DMD PINS
OPTION 1 Swap Control = x0	OPTION 2 Swap Control = x2	
HS_WDATA_D_P HS_WDATA_D_N	HS_WDATA_E_P HS_WDATA_E_N	Input DATA_p_0 Input DATA_n_0
HS_WDATA_C_P HS_WDATA_C_N	HS_WDATA_F_P HS_WDATA_F_N	Input DATA_p_1 Input DATA_n_1
HS_WDATA_B_P HS_WDATA_B_N	HS_WDATA_G_P HS_WDATA_G_N	Input DATA_p_2 Input DATA_n_2
HS_WDATA_A_P HS_WDATA_A_N	HS_WDATA_H_P HS_WDATA_H_N	Input DATA_p_3 Input DATA_n_3
HS_WDATA_H_P HS_WDATA_H_N	HS_WDATA_A_P HS_WDATA_A_N	Input DATA_p_4 Input DATA_n_4
HS_WDATA_G_P HS_WDATA_G_N	HS_WDATA_B_P HS_WDATA_B_N	Input DATA_p_5 Input DATA_n_5
HS_WDATA_F_P HS_WDATA_F_N	HS_WDATA_C_P HS_WDATA_C_N	Input DATA_p_6 Input DATA_n_6
HS_WDATA_E_P HS_WDATA_E_N	HS_WDATA_D_P HS_WDATA_D_N	Input DATA_p_7 Input DATA_n_7

8.3.11 Calibration and Debug Support

The DLPC3436 contains a test point output port, TSTPT_(7:0), which provides selected system calibration support as well as ASIC debug support. These test points are inputs while reset is applied and switch to outputs when reset is released. The state of these signals is sampled upon the release of system reset and the captured value configures the test mode until the next time reset is applied. Each test point includes an internal pulldown resistor, thus external pullups must be used to modify the default test configuration. The default configuration (x000) corresponds to the TSTPT_(7:0) outputs remaining tri-stated to reduce switching activity during normal operation. For maximum flexibility, an option to jumper to an external pullup is recommended for TSTPT_(2:0). Pullups on TSTPT_(6:3) are used to configure the ASIC for a specific mode or option. TI does not recommend adding pullups to TSTPT_(7:3) because this has adverse affects for normal operation. This external pullup is only sampled upon a 0-to-1 transition on the RESETZ input, thus changing their configuration after reset is released does not have any effect until the next time reset is asserted and released. Table 8 defines the test mode selection for one programmable scenario defined by TSTPT(2:0).

Table 8. Test Mode Selection Scenario Defined by TSTPT(2:0)(1)

TSTPT(2:0) CAPTURE VALUE	NO SWITCHING ACTIVITY	CLOCK DEBUG OUTPUT
	x000	x010
TSTPT(0)	HI-Z	60 MHz
TSTPT(1)	HI-Z	30 MHz
TSTPT(2)	HI-Z	0.7 to 22.5MHz
TSTPT(3)	HI-Z	HIGH
TSTPT(4)	HI-Z	LOW
TSTPT(5)	HI-Z	HIGH
TSTPT(6)	HI-Z	HIGH
TSTPT(7)	HI-Z	7.5 MHz

(1) These are only the default output selections. Software can reprogram the selection at any time.

8.3.12 DMD Interface Considerations

The sub-LVDS HS interface waveform quality and timing on the DLPC3436 ASIC is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

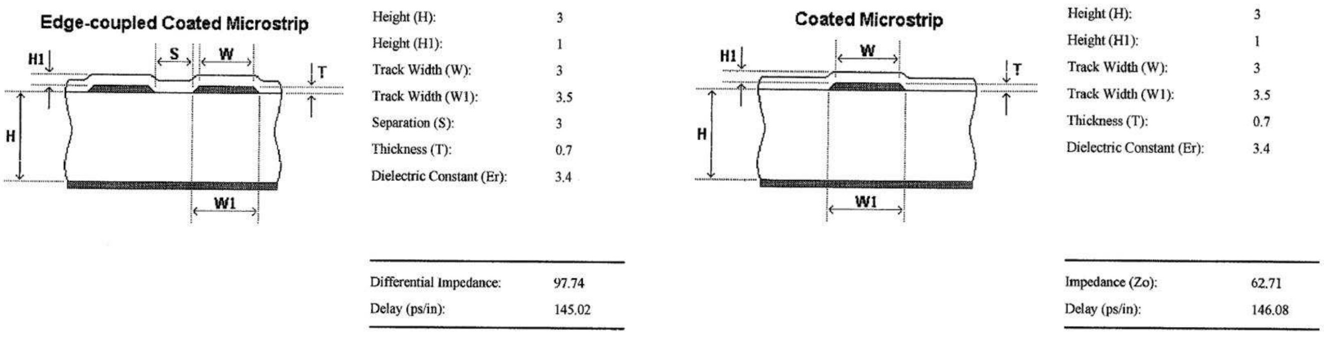
$$\text{Setup Margin} = (\text{DLPC3436 output setup}) - (\text{DMD input setup}) - (\text{PCB routing mismatch}) - (\text{PCB SI degradation}) \quad (1)$$

$$\text{Hold-time Margin} = (\text{DLPC3436 output hold}) - (\text{DMD input hold}) - (\text{PCB routing mismatch}) - (\text{PCB SI degradation})$$

where PCB SI degradation is signal integrity degradation due to PCB affects which includes such things as Simultaneously Switching Output (SSO) noise, cross-talk and Inter-symbol Interference (ISI) noise. (2)

DLPC3436 I/O timing parameters as well as DMD I/O timing parameters can be found in their corresponding data sheets. Similarly, PCB routing mismatch can be budgeted and met through controlled PCB routing. However, PCB SI degradation is a more complicated adjustment.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided as a reference of an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations may also work, but should be confirmed with PCB signal integrity analysis or lab measurements.



Edge-coupled Coated Microstrip	
Height (H):	3
Height (H1):	1
Track Width (W):	3
Track Width (W1):	3.5
Separation (S):	3
Thickness (T):	0.7
Dielectric Constant (Er):	3.4
Differential Impedance:	97.74
Delay (ps/in):	145.02

Coated Microstrip	
Height (H):	3
Height (H1):	1
Track Width (W):	3
Track Width (W1):	3.5
Thickness (T):	0.7
Dielectric Constant (Er):	3.4
Impedance (Zo):	62.71
Delay (ps/in):	146.08

DMD_HS Differential Signals

DMD_LS Signals

Figure 17. DMD Interface Board Stack-Up Details

8.4 Device Functional Modes

The DLPC3436 has two functional modes (ON/OFF) controlled by a single pin PROJ_ON:

- When pin PROJ_ON is set high, the projector automatically powers up and an image is projected from the DMD.
- When pin PROJ_ON is set low, the projector automatically powers down and only microwatts of power are consumed.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DLPC3436 controller requires to be coupled with DLP230NP (.23 1080p) DMD to provide a reliable display solution for many data and video display applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the controller. Applications of interest include DLP signage, Mobile Projectors, Mobile Smart TVs, Smart Speakers, VR and AR headsets & glasses.

9.2 Typical Application

A common application when using DLPC3436 controller with DLP230NP (.23 1080p) and DLPA3000 PMIC/LED driver is for creating a Pico projector embedded in a handheld product. For example, a Pico projector may be embedded in a smart phone, a tablet, a camera, or camcorder. The controller in the Pico projector embedded module typically receives images from a host processor within the product.

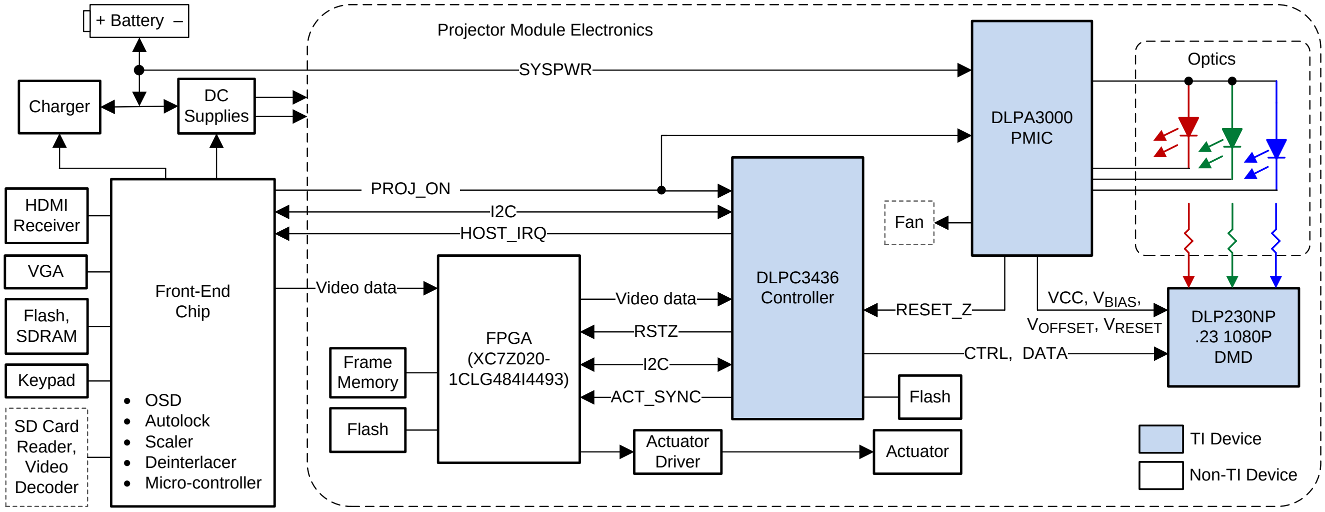


Figure 18. Typical Application Diagram

Typical Application (continued)

9.2.1 Design Requirements

A Pico projector is created by using a DLP chipset comprised of DLP230NP (.23 1080p) DMD, DLPC3436 controller, a XC7Z020-1CLG484I4493 FPGA, and DLPAxxxx PMIC/LED driver. The controller does the digital image processing, the DLPAxxxx provides the needed analog functions for the projector, and DMD is the display device for producing the projected image.

In addition to the three DLP chips in the chipset, other chips may be needed. At a minimum a flash part is needed to store the software and firmware to control the controller . In addition, a flash part is needed to store the FPGA program.

The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector.

The entire pico-projector can be turned on and off by using a single signal called PROJ_ON. When PROJ_ON is high, the projector turns on and begins displaying images. When PROJ_ON is set low, the projector turns off and draws just microamps of current on SYSPWR. When PROJ_ON is set low, the 1.8-V supply can continue to be left at 1.8 V and used by other non-projector sections of the product. If PROJ_ON is low, the DLPAxxxx does not draw current on the 1.8-V supply.

9.2.2 Detailed Design Procedure

For connecting together the DLP230NP (.23 1080p) DMD, DLPC3436 controller, XC7Z020-1CLG484I4493 FPGA, and DLPAxxxx PMIC/LED Driver see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible.

The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

9.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is shown in Figure 19. For the LED currents shown, it is assumed that the same current amplitude is applied to the red, green, and blue LEDs.

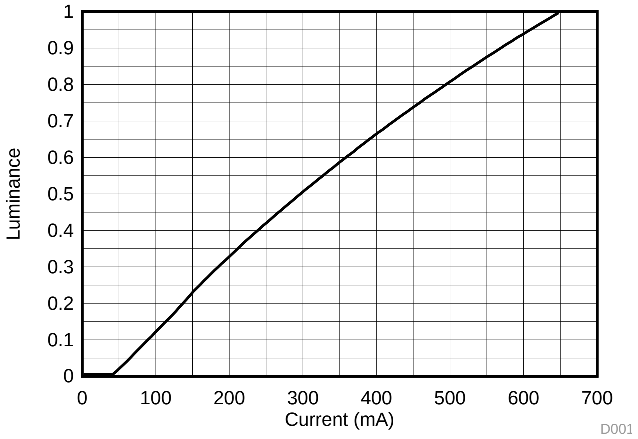


Figure 19. Luminance vs Current

10 Power Supply Recommendations

10.1 System Power-Up and Power-Down Sequence

Although the DLPC3436 requires an array of power supply voltages, (for example, V_{DD}, V_{DDLP12}, $V_{DD\_PLLM/D}$, V_{CC18}, V_{CC_FLSH}, V_{CC_INTF}), because V_{DDLP12} is tied to the 1.1-V V_{DD} supply, then there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the controller (This is true for both power-up and power-down scenarios). Similarly, there is no minimum time between powering-up or powering-down the different supplies if V_{DDLP12} is tied to the 1.1-V V_{DD} supply.

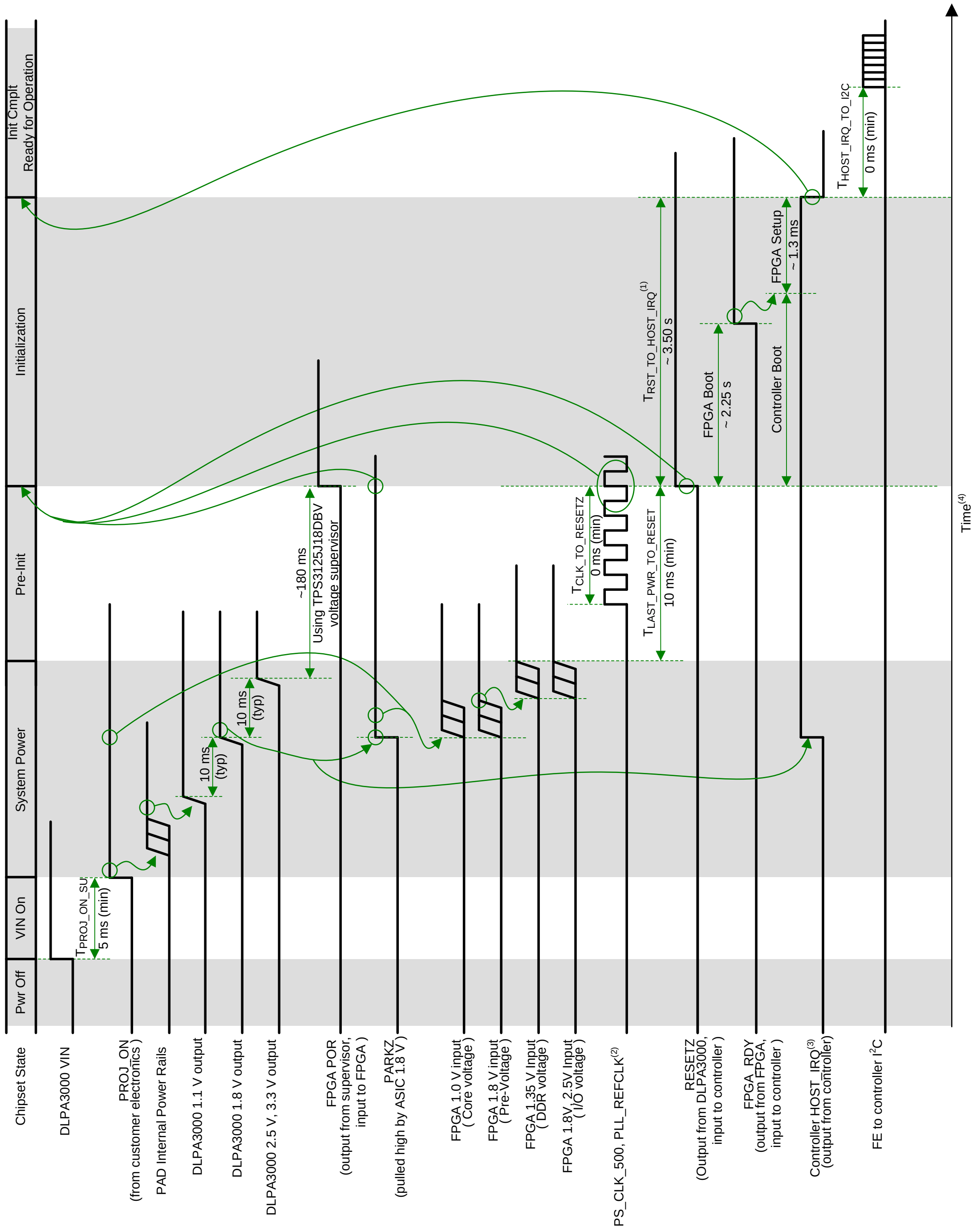
Although there is no risk of damaging the controller if the above power sequencing rules are followed, the following additional power sequencing recommendations must be considered to ensure proper system operation.

- To ensure that DLPC3436 output signal states behave as expected, all controller I/O supplies should remain applied while V_{DD} core power is applied. If V_{DD} core power is removed while the I/O supply (V_{CC_INTF}) is applied, then the output signal state associated with the inactive I/O supply goes to a high impedance state.
- Additional power sequencing rules may exist for devices that share the supplies with the controller , and thus these devices may force additional system power sequencing requirements.

Note that when V_{DD} core power is applied, but I/O power is not applied, additional leakage current may be drawn. This added leakage does not affect normal controller operation or reliability.

Figure 20 and Figure 21 show the controller power-up and power-down sequence for both the normal PARK and fast PARK operations of the controller ASIC.

System Power-Up and Power-Down Sequence (continued)



(1) Actual time from RESETZ high to HOST_IRQ low can vary based upon the software configuration.

(2) PLL_REFCLK can go active anytime before power is applied to the DLP Controller,but must be active and stable before RESETZ goes high.

(3) HOST_IRQ goes high to indicate that the Controller is ready for initialization (triggered by RESETZ going high) to start

(4) Any time dimensions that are not explicitly definedare considered to be negligible

Figure 20. DLPC3436 Power-Up Timing

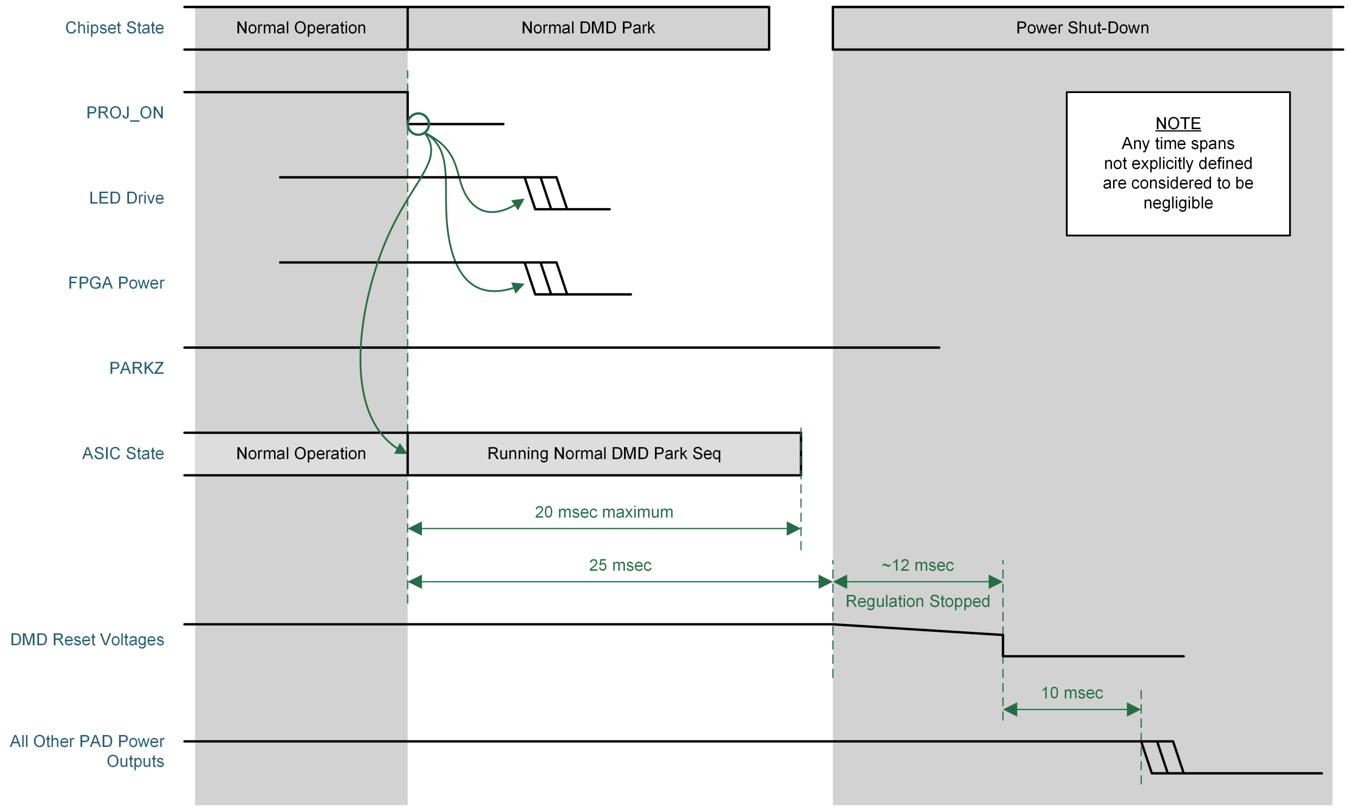


Figure 21. DLPC3436 Normal Power-Down

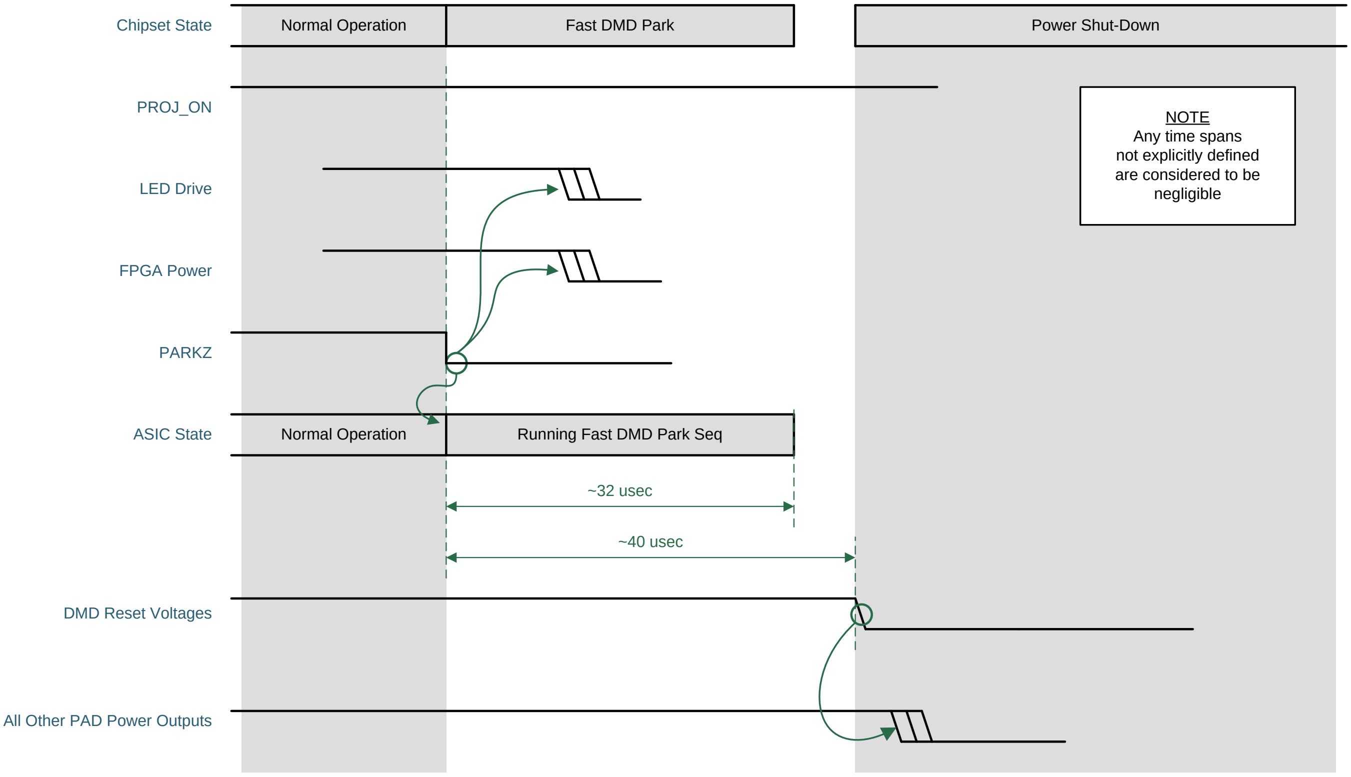


Figure 22. DLPC3436 Fast Power-Down

10.2 DLPC3436 Power-Up Initialization Sequence

It is assumed that an external power monitor hold the DLPC3436 in system reset during power-up. It must do this by driving RESETZ to a logic low state. It should continue to assert system reset until all ASIC voltages have reached minimum specified voltage levels, PARKZ is asserted high, and input clocks are stable. During this time, the controller drives most ASIC outputs to an inactive state. The controller configures all bidirectional signals as inputs to avoid contention. The controller tri-states ASIC outputs that are not driven to an inactive state. These outputs include LED_SEL_0, LED_SEL_1, SPICLK, SPIDOUT, and SPICSZ0 (see RESETZ pin description for full signal descriptions in . After power is stable and the PLL_REFCLK_I clock input to the controller is stable, then RESETZ should be deactivated (set to a logic high). The controller then performs a power-up initialization routine that first locks its PLL followed by loading self configuration data from the external flash. Upon release of RESETZ all controller I/Os become active. Immediately following the release of RESETZ, the controller drives the HOST_IRQ signal high to indicate the progress of the auto initialization routine. However, because a pullup resistor is connected to signal HOST_IRQ, this signal has already gone high before the controller actively drives it high. Upon completion of the chipset auto-initialization routine, the master controller drives HOST_IRQ low to indicate the initialization done state of the controller has been reached.

Note that the host processor must wait for HOST_IRQ to go low before initiating I^2C commands.

10.3 DMD Fast PARK Control (PARKZ)

The PARKZ signal is defined to be an early warning signal that should alert the ASIC 40 µs before DC supply voltages have dropped below specifications in fast PARK operation. This allows the ASIC time to park the DMD, ensuring the integrity of future operation. Note that the reference clock should continue to run and RESETZ should remain deactivated for at least 40 µs after PARKZ has been deactivated (set to a logic low) to allow the park operation to complete.

10.4 Hot Plug Usage

The DLPC3436 provides fail-safe I/O on all host interface signals (signals powered by V_{CC_INTF}). This allows these inputs to be driven high even when no I/O power is applied. Under this condition, the controller does not load the input signal nor draw excessive current that could degrade ASIC reliability. For example, the I^2C bus from the host to other components would not be affected by powering off V_{CC_INTF} to the controller . TI recommends weak pullups or pulldowns on signals feeding back to the host to avoid floating inputs.

If the I/O supply (V_{CC_INTF}) is powered off, but the core supply (V_{DD}) is powered on, then the corresponding input buffer may experience added leakage current, but this does not damage the controller .

10.5 Maximum Signal Transition Time

Unless otherwise noted, 10 ns is the maximum recommended 20% to 80% rise or fall time to avoid input buffer oscillation. This applies to all DLPC3436 input signals. However, the PARKZ input signal includes an additional small digital filter that ignores any input buffer transitions caused by a slower rise or fall time for up to 150 ns.

11 Layout

11.1 Layout Guidelines

11.1.1 PCB Layout Guidelines for Internal ASIC PLL Power

The following guidelines are recommended to achieve desired ASIC performance relative to the internal PLL. The DLPC3436 contains 2 internal PLLs which have dedicated analog supplies (VDD_PLLM , VSS_PLLM, VDD_PLLD, VSS_PLLD). As a minimum, VDD_PLLx power and VSS_PLLx ground pins should be isolated using a simple passive filter consisting of two series Ferrites and two shunt capacitors (to widen the spectrum of noise absorption). It's recommended that one capacitor be a 0.1-µF capacitor and the other be a 0.01-µF capacitor. All four components should be placed as close to the ASIC as possible but it's especially important to keep the leads of the high frequency capacitors as short as possible. Note that both capacitors should be connected across VDD_PLLM and VSS_PLLM / VDD_PLLD and VSS_PLLD respectfully on the ASIC side of the Ferrites.

For the ferrite beads used, their respective characteristics should be as follows:

- DC resistance less than 0.40 Ω
- Impedance at 10 MHz equal to or greater than 180 Ω
- Impedance at 100 MHz equal to or greater than 600 Ω

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, VDD_PLLM and VDD_PLLD must be a single trace from the controller to both capacitors and then through the series ferrites to the power source. The power and ground traces should be as short as possible, parallel to each other, and as close as possible to each other.

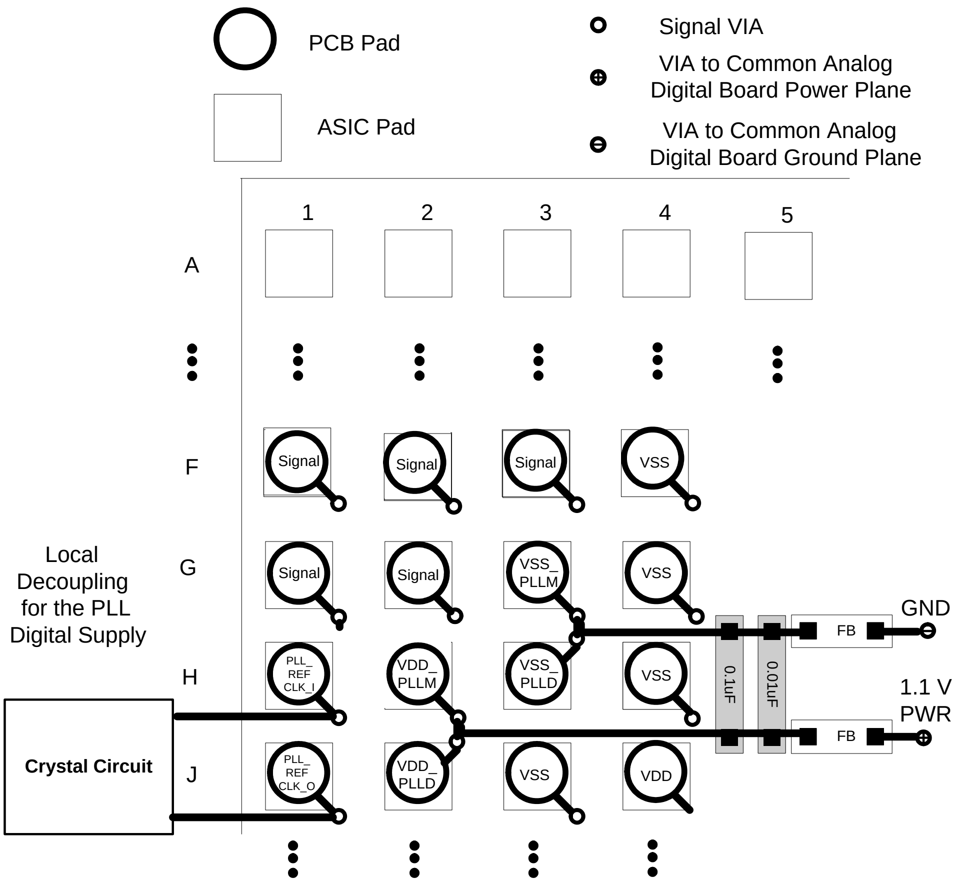
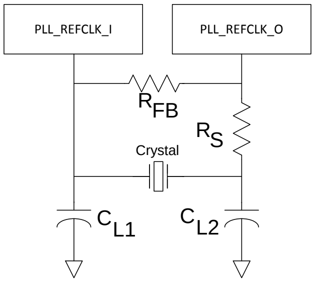


Figure 23. PLL Filter Layout

Layout Guidelines (continued)

11.1.2 DLPC3436 Reference Clock

The DLPC3436 requires an external reference clock to feed its internal PLL. A crystal or oscillator can supply this reference. See Table 10 for the necessary crystal (or oscillator) specifications. When a crystal is used, several discrete components are also required as shown in Figure 24.



A. C_L = Crystal load capacitance (farads)
B. C_{L1} = 2 × (CL – Cstray_pll_refclk_i)
C. C_{L2} = 2 × (CL – Cstray_pll_refclk_o)
D. Where:
  - Cstray_pll_refclk_i = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin pll_refclk_i.
  - Cstray_pll_refclk_o = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin pll_refclk_o.

Figure 24. Required Discrete Components

11.1.2.1 Recommended Crystal Oscillator Configuration

Table 9. Crystal Port Characteristics

PARAMETER	NOM	UNIT
PLL_REFCLK_I TO GND capacitance	1.5	pF
PLL_REFCLK_O TO GND capacitance	1.5	pF

Table 10. Recommended Crystal Configuration(1)(2)

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	24	MHz
Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity)	±200	PPM
Maximum startup time	1.0	ms
Crystal equivalent series resistance (ESR)	120 max	Ω
Crystal load	6	pF
RS drive resistor (nominal)	100	Ω
RFB feedback resistor (nominal)	1	MΩ
CL1 external crystal load capacitor	See equation in Figure 24 notes	pF
CL2 external crystal load capacitor	See equation in Figure 24 notes	pF
PCB layout	A ground isolation ring around the crystal is recommended	

(1) Temperature range of –30°C to +85°C
(2) The crystal bias is determined by the ASIC's VCC_INTF voltage rail, which is variable (not the VCC18 rail).

If an external oscillator is used, then the oscillator output must drive the PLL_REFCLK_I pin on the controller ASIC and the PLL_REFCLK_O pins should be left unconnected.

Table 11. DLPC3436 Recommended Crystal Parts(1)(2)(3)

PASSED DVT	MANUFACTURER	PART NUMBER	SPEED	TEMPERATURE AND AGING	ESR	LOAD CAPACITANCE
Yes	KDS	DSX211G-24.000M-8pF-50-50	24 MHz	±50 ppm	120-Ω max	8 pF
Yes	Murata	XRCGB24M000F0L11R0	24 MHz	±100 ppm	120-Ω max	6 pF
Yes	NDK	NX2016SA 24M EXS00A-CS05733	24 MHz	±145 ppm	120-Ω max	6 pF

(1) These crystal devices appear compatible with the DLPC3436, but only those marked with yes in the DVT column have been validated.
(2) Crystal package sizes: 2.0 × 1.6 mm for all crystals
(3) Operating temperature range: –30°C to +85°C for all crystals

11.1.3 General PCB Recommendations

TI recommends 1-oz. copper planes in the PCB design to achieve needed thermal connectivity.

11.1.4 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends that unused ASIC input pins be tied through a pullup resistor to its associated power supply or a pulldown to ground. For ASIC inputs with internal pullup or pulldown resistors, it is unnecessary to add an external pullup or pulldown unless specifically recommended. Note that internal pullup and pulldown resistors are weak and should not be expected to drive the external line. The DLPC3436 implements very few internal resistors and these are noted in the pin list. When external pullup or pulldown resistors are needed for pins that have built-in weak pullups or pulldowns, use the value 8 kΩ (max).

Unused output-only pins should never be tied directly to power or ground, but can be left open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they should be pulled-up (or pulled-down) using an appropriate, dedicated resistor.

11.1.5 Maximum Pin-to-Pin, PCB Interconnects Etch Lengths

Table 12. Maximum Pin-to-Pin PCB Interconnect Recommendations(1)(2)

DMD BUS SIGNAL	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HS_CLK_P DMD_HS_CLK_N	6.0 152.4	See (3)	inch (mm)
DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	6.0 152.4	See (3)	inch (mm)
DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD_LS_CLK	6.5 165.1	See (3)	inch (mm)
DMD_LS_WDATA	6.5 165.1	See (3)	inch (mm)
DMD_LS_RDATA	6.5 165.1	See (3)	inch (mm)
DMD_DEN_ARSTZ	7.0 177.8	See (3)	inch (mm)

(1) Maximum signal routing length includes escape routing.
(2) Multi-board DMD routing length is more restricted due to the impact of the connector.
(3) Due to board variations, these are impossible to define. Any board designs should SPICE simulate with the ASIC IBIS models to ensure single routing lengths do not exceed requirements.

Table 13. High Speed PCB Signal Routing Matching Requirements

SIGNAL GROUP LENGTH MATCHING				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD	DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	DMD_HS_CLK_P DMD_HS_CLK_N	±1.0 (±25.4)	inch (mm)
	DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
	DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
	DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
	DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
	DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
	DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
	DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD	DMD_LS_WDATA DMD_LS_RDATA	DMD_LS_CLK	±0.2 (±5.08)	inch (mm)

Table 13. High Speed PCB Signal Routing Matching Requirements (continued)

SIGNAL GROUP LENGTH MATCHING				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD	DMD_DEN_ARSTZ	N/A	N/A	inch (mm)

11.1.6 Number of Layer Changes

- Single-ended signals: Minimize the number of layer changes
- Differential signals: Individual differential pairs can be routed on different layers, but the signals of a given pair should not change layers.

11.1.7 Stubs

- Stubs should be avoided

11.1.8 Terminations

- No external termination resistors are required on DMD_HS differential signals.
- The DMD_LS_CLK and DMD_LS_WDATA signal paths should include a 43-Ω series termination resistor located as close as possible to the corresponding ASIC pins.
- The DMD_LS_RDATA signal path should include a 43-Ω series termination resistor located as close as possible to the corresponding DMD pin.
- DMD_DEN_ARSTZ does not require a series resistor.

11.1.9 Routing Vias

- The number of vias on DMD_HS signals should be minimized and should not exceed two.
- Any and all vias on DMD_HS signals should be located as close to the ASIC as possible.
- The number of vias on the DMD_LS_CLK and DMD_LS_WDATA signals should be minimized and not exceed two.
- Any and all vias on the DMD_LS_CLK and DMD_LS_WDATA signals should be located as close to the ASIC as possible.

11.1.10 Thermal Considerations

The underlying thermal limitation for the DLPC3436 is that the maximum operating junction temperature (T_J) not be exceeded (this is defined in the). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the controller , and power dissipation of surrounding components. The controller 's package is designed primarily to extract heat through the power and ground planes of the PCB. Thus, copper content and airflow over the PCB are important factors.

The recommended maximum operating ambient temperature (T_A) is provided primarily as a design target and is based on maximum controller power dissipation and $R_{\theta JA}$ at 0 m/s of forced airflow, where $R_{\theta JA}$ is the thermal resistance of the package as measured using a glater test PCB with two, 1-oz power planes. This JEDEC test PCB is not necessarily representative of the controller PCB; the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance. However, after the PCB is designed and the product is built, TI highly recommended that thermal performance be measured and validated.

To do this, measure the top center case temperature under the worse case product scenario (maximum power dissipation, maximum voltage, maximum ambient temperature) and validated not to exceed the maximum recommended case temperature (T_C). This specification is based on the measured φ_{JT} for the controller package and provides a relatively accurate correlation to junction temperature. Take care when measuring this case temperature to prevent accidental cooling of the package surface. TI recommends a small (approximately 40 gauge) thermocouple. The bead and thermocouple wire should contact the top of the package and be covered with a minimal amount of thermally conductive epoxy. The wires should be routed closely along the package and the board surface to avoid cooling the bead through the wires.

11.2 Layout Example

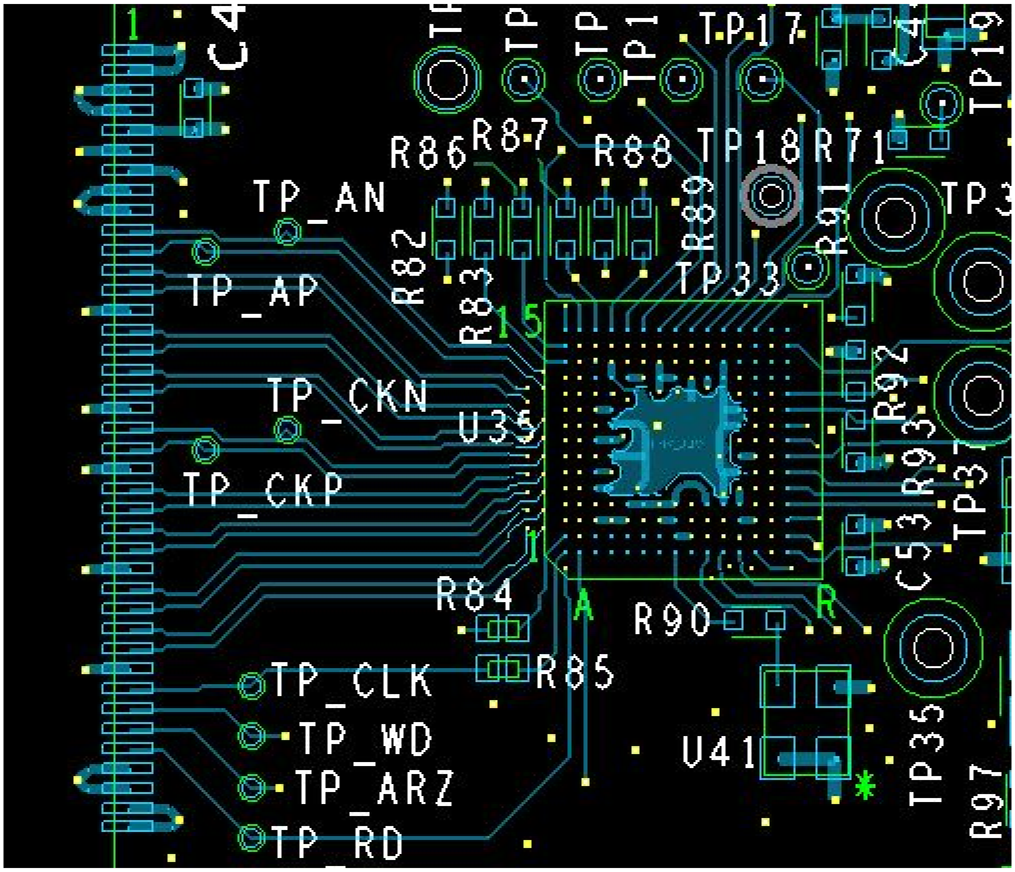


Figure 25. Layout Recommendation

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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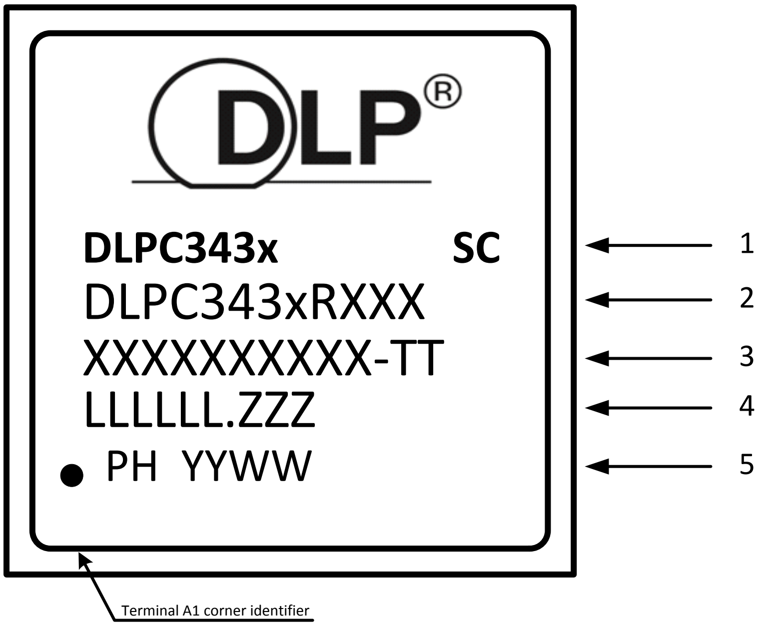
12.1.2 Device Nomenclature

12.1.2.1 Device Markings



Marking Definitions:

Line 1:	DLP® Device Name: DLPC343x where**x** is a "6" for this device. SC: Solder ball composition e1: Indicates lead-free solder balls consisting of SnAgCu G8: Indicates lead-free solder balls consisting of tin-silver-copper (SnAgCu) with silver content less than or equal to 1.5% and that the mold compound meets TI's definition of green.
Line 2:	TI Part Number DLP® Device Name: DLPC343x = **x** is a "6" for this device. **R** corresponds to the TI device revision letter for example A, B or C **XXX** corresponds to the device package designator.
Line 3:	XXXXXXXXXX-TT Manufacturer Part Number
Line 4:	LLLLLL.ZZZ Foundry lot code for semiconductor wafers LLLLLL: Fab lot number ZZZ: Lot split number
Line 5:	PH YYWW ES : Package assembly information PH: Manufacturing site YYWW: Date code (YY = Year :: WW = Week)

Device Support (continued)

NOTE

1. Engineering prototype samples are marked with an **X** suffix appended to the TI part number. For example, 2512737-0001X.

12.1.3 Video Timing Parameter Definitions

Active Lines Per Frame (ALPF) Defines the number of lines in a frame containing displayable data: ALPF is a subset of the TLPF.

Active Pixels Per Line (APPL) Defines the number of pixel clocks in a line containing displayable data: APPL is a subset of the TPPL.

Horizontal Back Porch (HBP) Blanking Number of blank pixel clocks after horizontal sync but before the first active pixel. Note: HBP times are reference to the leading (active) edge of the respective sync signal.

Horizontal Front Porch (HFP) Blanking Number of blank pixel clocks after the last active pixel but before Horizontal Sync.

Horizontal Sync (HS) Timing reference point that defines the start of each horizontal interval (line). The absolute reference point is defined by the active edge of the HS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all horizontal blanking parameters are measured.

Total Lines Per Frame (TLPF) Defines the vertical period (or frame time) in lines: TLPF = Total number of lines per frame (active and inactive).

Total Pixel Per Line (TPPL) Defines the horizontal line period in pixel clocks: TPPL = Total number of pixel clocks per line (active and inactive).

Vertical Sync (VS) Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all vertical blanking parameters are measured.

Vertical Back Porch (VBP) Blanking Number of blank lines after the leading edge of vertical sync but before the first active line.

Vertical Front Porch (VFP) Blanking Number of blank lines after the last active line but before the leading edge of vertical sync.

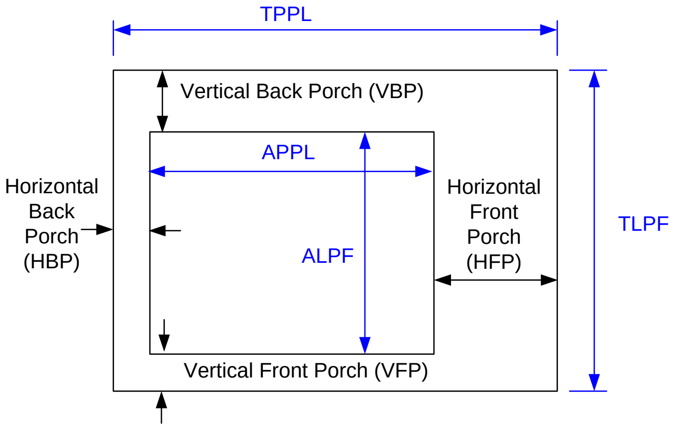


Figure 26. Timing Parameter Diagram

12.2 Documentation Support

12.2.1 Related Documentation

The following table lists quick access links for associated parts of the DLP chipset:

Table 14. Chipset Documentation

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE
DLPA2000	Click here	Click here	Click here	Click here
DLPA2005	Click here	Click here	Click here	Click here
DLPA3000	Click here	Click here	Click here	Click here
DLP230NP	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

IntelliBright, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC3436CZVB	ACTIVE	NFBGA	ZVB	176	260	TBD	Call TI	Call TI			Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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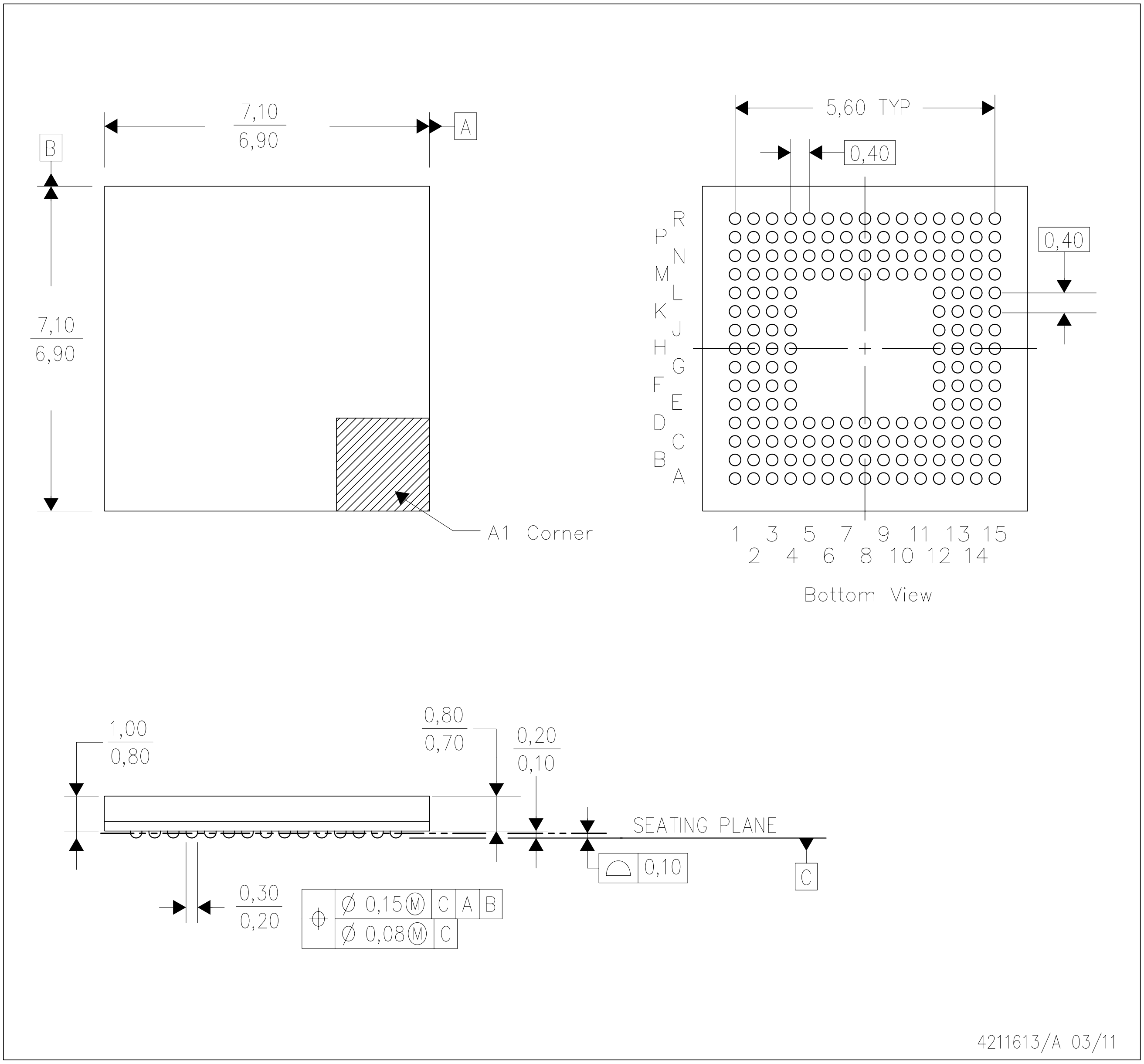
ZVB (S–PBGA–N176) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. This package is Pb–free.

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