LM4954 Boomer™ Audio Power Amplifier Series High Voltage 3 Watt Audio Power Amplifier

Check for Samples: LM4954

FEATURES

- **No Output Coupling Capacitors, Snubber Networks or Bootstrap Capacitors Required**
- **Unity Gain Stable**
- **Externally Configurable Gain**
- **Ultra Low Current Active Low Shutdown Mode**
- **BTL Output can Drive Capacitive Loads Up to 100pF**
- **"Click and Pop" Suppression Circuitry**
- **2.7V - 9.0V Operation**
- **Available in Space-Saving DSBGA Package**

APPLICATIONS

- **Mobile Phones**
- **PDAs**

KEY SPECIFICATIONS

- **Wide Power Supply Voltage Range, 2.7 ≤ V_{DD} ≤ 9V**
- **Output Power: V_{DD} = 7V, 1% THD+N, 2.4W (Typ)**
- **Quiescent Power Supply Current, 3mA (Typ)**
- **PSRR: V_{DD} = 5V and 3V at 217Hz, 80dB (Typ)**
- **Shutdown Power Supply Current, 0.01µA (Typ)**

DESCRIPTION

The LM4954 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 2.4 Watts of continuous average power to an 8Ω BTL load with less than 1% THD+N from a $7V_{DC}$ power supply.

Boomer audio power amplifiers are designed specifically to provide high quality output power with a minimal number of external components. The LM4954 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for lower-power portable applications where minimal space and power consumption are primary requirements.

The LM4954 features a low-power consumption global shutdown mode which is achieved by driving the shutdown pin with logic low. Additionally, the LM4954 features an internal thermal shutdown protection mechanism.

The LM4954 contains advanced pop & click circuitry which eliminates noises that would otherwise occur during turn-on and turn-off transitions.

The LM4954 is unity-gain stable and can be configured by external gain-setting resistors.

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Typical Application

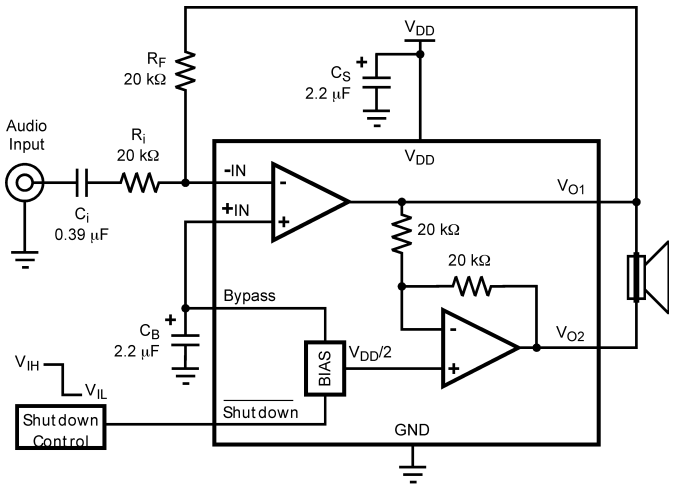


Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

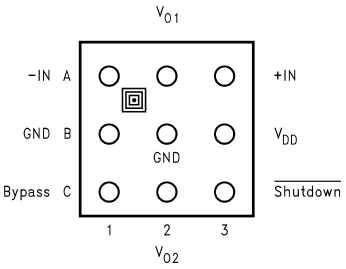


Figure 2. 9 Bump DSBGA
Top View
See Package Number YZR0009

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings(1)(2)(3)

Supply Voltage(1)		9.5V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation(4)		Internally Limited
ESD Susceptibility(5)		2000V
ESD Susceptibility(6)		200V
Junction Temperature		150°C
Thermal Resistance	θ_{JA} (DSBGA)(7)	180°C/W
Soldering Information See AN-112 (SNAA002) “DSBGA Wafers Level Chip Scale Package.”		

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4954, see power derating curves for additional information.
(5) Human body model, 100pF discharged through a 1.5kΩ resistor.
(6) Machine Model, 220pF – 240pF discharged through all pins.
(7) All bumps have the same thermal resistance and contribute equally when used to lower thermal resistance. The θ_{JA} given in the Absolute Maximum Ratings section under Thermal Resistance is for the ITL package without any heat spreading planes on the PCB.

Operating Ratings(1)(2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ 85°C
Supply Voltage		2.7V ≤ V_{DD} ≤ 9V

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.

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Electrical Characteristics V_{DD} = 7V[1][2]

The following specifications apply for V_{DD} = 7V, A_{V-BTL} = 6dB, and R_L = 8Ω unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4954		Units (Limits)
			Typical[3]	Limit[4][5]	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, R_L = 8Ω BTL	3	5	mA (max)
I_{SD}	Shutdown Current	V_{SD} = GND[6]	0.01	1	µA (max)
V_{OS}	Output Offset Voltage		10	25	mV (max)
P_o	Output Power[7]	THD+N = 1% (max); f = 1kHz	2.4	2.2	W (min)
		THD+N = 10% (max); f = 1kHz	3.0		W
THD+N	Total Harmonic Distortion + Noise	P_O = 1Wrms; f = 1kHz A_{V-BTL} = 6dB	0.1		%
		P_O = 1Wrms; f = 1kHz A_{V-BTL} = 26dB	0.4		%
PSRR	Power Supply Rejection Ratio	V_{Ripple} = 200mVsine p-p, C_B = 2.2µF, Input terminated with 10Ω to GND f_{Ripple} = 217Hz, Input Referred	71	54	dB (min)
		V_{Ripple} = 200mVsine p-p, C_B = 2.2µF, Input terminated with 10Ω to ground f_{Ripple} = 1kHz, Input Referred	71	55	dB (min)
V_{SDIH}	Shutdown High Input Voltage			1.2	V (min)
V_{SDIL}	Shutdown Low Input Voltage			0.4	V (max)
T_{WU}	Wake-up Time	C_B = 2.2µF	130		ms
ϵ_{OUT}	Output Noise	A-Wtg, A_{V-BTL} = 6dB Input terminated with 10Ω to GND, Output Referred	20		μV_{RMS}
		A-Wtg, A_{V-BTL} = 26dB Input terminated with 10Ω to GND, Output Referred	100		μV_{RMS}
R_{PD}	Pull Down Resistor on Shutdown		75		kΩ

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
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(3) Typical specifications are specified at 25°C and represent the parametric norm.
(4) Tested limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) Shutdown current is measured in a normal room environment. Exposure to direct sunlight in the TL package will increase I_{SD} by a minimum of 2µA.
(7) The demo board shown has 1.1in^2 (710mm^2) heat spreading planes on the two internal layers and the bottom layer. The bottom internal layer is electrically V_{DD} while the top internal and bottom layers are electrically GND. Thermal performance for the demo board is found on the Power Derating graph in the Typical Performance Characteristics section. 7V operation requires heat spreading planes for the thermal stability.

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Electrical Characteristics V_{DD} = 5V(1)(2)

The following specifications apply for V_{DD} = 5V, $A_{V\text{-}BTL}$ = 6dB, and R_L = 8Ω unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4954		Units (Limits)
			Typical(3)	Limit(4)(5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, R_L = 8Ω BTL	2.7	5	mA (max)
I_{SD}	Shutdown Current	V_{SD} = GND(6)	0.01	1	µA (max)
V_{OS}	Output Offset Voltage		8	25	mV (max)
P_o	Output Power	THD+N = 1% (max); f = 1kHz	1.2	1.1	W (min)
THD+N	Total Harmonic Distortion + Noise	P_O = 600mWrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mVsine p-p, C_B = 2.2µF, Input terminated with 10Ω to GND f_{Ripple} = 217Hz, Input Referred	80	63	dB (min)
		V_{ripple} = 200mVsine p-p, C_B = 2.2µF, Input terminated with 10Ω to GND f_{Ripple} = 1kHz, Input Referred	80		dB
V_{SDIH}	Shutdown High Input Voltage			1.2	V (min)
V_{SDIL}	Shutdown Low Input Voltage			0.4	V (max)
T_{WU}	Wake-up Time	C_B = 2.2µF	130		ms
$\in_{OUT}$	Output Noise	A-Wtg, Input terminated with 10Ω to GND, Output referred	20		μV_{RMS}
R_{PD}	Pul Down Resistor on Shutdown		75		kΩ

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typical specifications are specified at 25°C and represent the parametric norm.
(4) Tested limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) Shutdown current is measured in a normal room environment. Exposure to direct sunlight in the TL package will increase I_{SD} by a minimum of 2µA.

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Electrical Characteristics V_{DD} = 3V(1)(2)

The following specifications apply for V_{DD} = 3V, A_{V-BTL} = 6dB, and R_L = 8Ω unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4954		Units (Limits)
			Typical(3)	Limit(4)(5)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, R_L = 8Ω BTL	2.5	5	mA (max)
I_{SD}	Shutdown Current	V_{SD} = GND(6)	0.01	1	µA (max)
V_{OS}	Output Offset Voltage		5	25	mV (max)
P_o	Output Power	THD+N = 1% (max); f = 1kHz	380	360	mW (min)
THD+N	Total Harmonic Distortion + Noise	P_o = 100mWrms; f = 1kHz	0.18		%
PSRR	Power Supply Rejection Ratio	V_{ripple} = 200mVsine p-p, C_B = 2.2µF, Input teiminated with 10Ω to GND, f_{Ripple} = 217Hz, Input referred	80	63	dB (min)
		V_{ripple} = 200mVsine p-p, C_B = 2.2µF, Input teiminated with 10Ω to GND, f_{Ripple} = 1kHz, Input referred	80		dB
V_{SDIH}	Shutdown High Input Voltage			1.2	V (min)
V_{SDIL}	Shutdown Low Input Voltage			0.4	V (max)
T_{WU}	Wake-Up Time	C_B = 2.2µF	130		ms
$\in_{OUT}$	Output Noise	A-Wtg, Input terminated with 10Ω to GND, Output referred	20		μV_{RMS}
R_{PD}	Pull Down Resistor on Shutdown		75		kΩ

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typical specifications are specified at 25°C and represent the parametric norm.
(4) Tested limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) Shutdown current is measured in a normal room environment. Exposure to direct sunlight in the TL package will increase I_{SD} by a minimum of 2µA.

External Components Description

(See Figure 1)

Components		Functional Description
1.	R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_i at $f_C = 1/(2\pi R_i C_i)$.
2.	C_i	Input coupling capacitor which blocks the DC voltage at the amplifiers input terminals. Also creates a highpass filter with R_i at $f_c = 1/(2\pi R_i C_i)$. Refer to the section, PROPER SELECTION OF EXTERNAL COMPONENTS, for an explanation of how to determine the value of C_i.
3.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_i. $A_{VD} = 2 * (R_f/R_i)$.
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the POWER SUPPLY BYPASSING section for information concerning proper placement and selection of the supply bypass capacitor.
5.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, PROPER SELECTION OF EXTERNAL COMPONENTS, for information concerning proper placement and selection of C_B.

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Typical Performance Characteristics

THD+N vs Output Power
V_{DD} = 7V, R_L = 8Ω, A_V = 6dB,
f = 1kHz, 80kHz BW

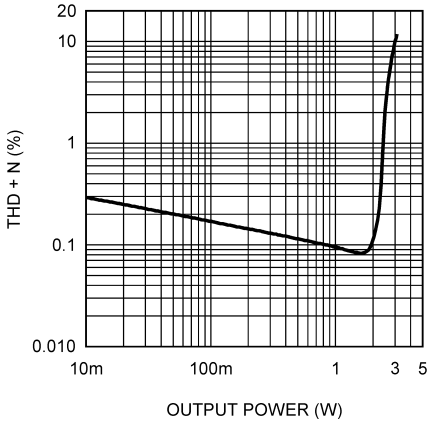


Figure 3.

THD+N vs Frequency
V_{DD} = 7V, R_L = 8Ω, A_V = 6dB,
P_{OUT} = 600mW, 80kHz BW

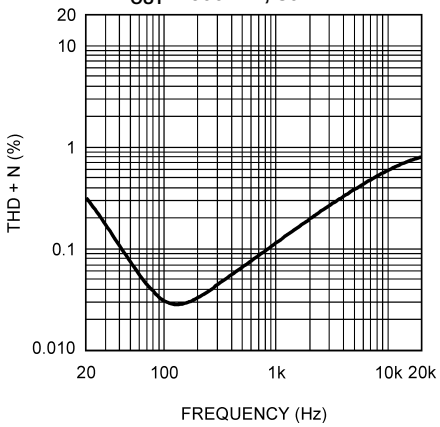


Figure 4.

THD+N vs Output Power
V_{DD} = 7V, R_L = 8Ω, A_V = 26dB,
f = 1kHz, 80kHz BW

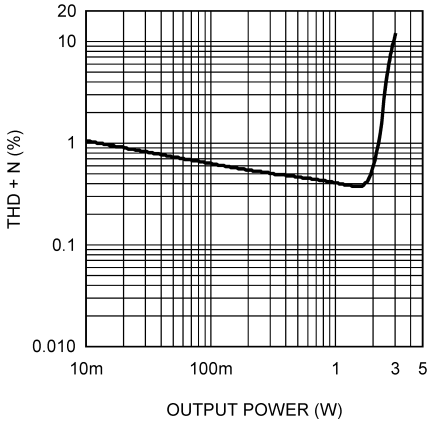


Figure 5.

THD+N vs Frequency
V_{DD} = 7V, R_L = 8Ω, A_V = 26dB,
P_{OUT} = 600mW, 80kHz BW

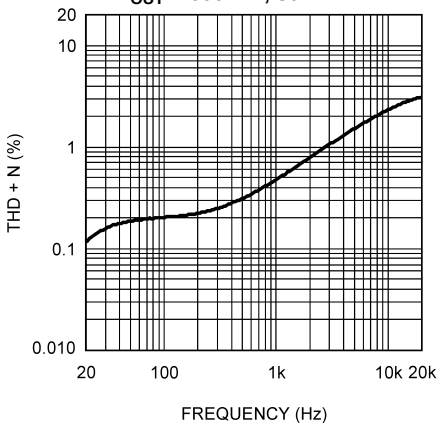


Figure 6.

THD+N vs Output Power
V_{DD} = 5V, R_L = 4Ω, A_V = 6dB,
f = 1kHz, 80kHz BW

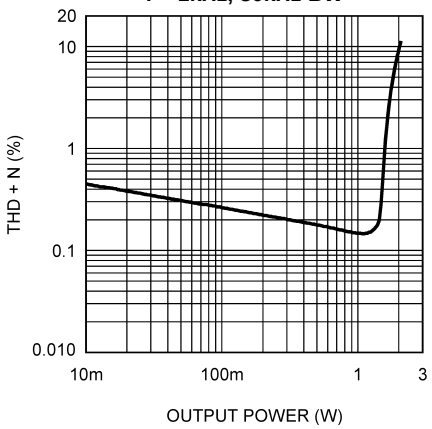


Figure 7.

THD+N vs Frequency
V_{DD} = 5V, R_L = 4Ω, A_V = 6dB,
P_{OUT} = 100mW, 80kHz BW

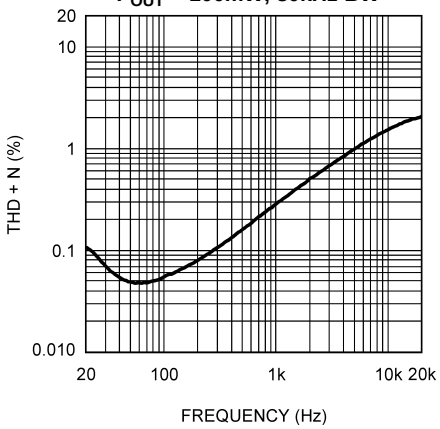


Figure 8.

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Typical Performance Characteristics (continued)

THD+N vs Output Power
V_{DD} = 5V, R_L = 8Ω, A_V = 6dB, f = 1kHz, 80kHz BW

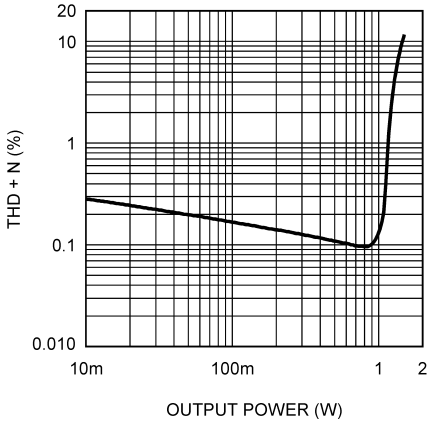


Figure 9.

THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, A_V = 6dB, P_{OUT} = 100mW, 80kHz BW

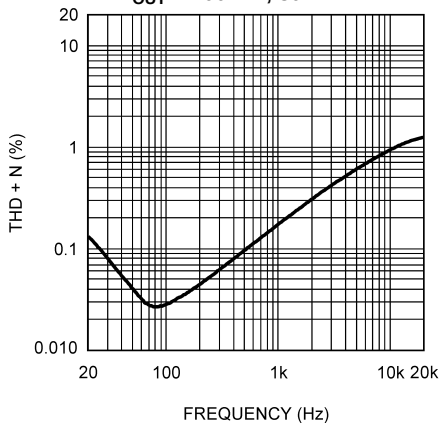


Figure 10.

THD+N vs Output Power
V_{DD} = 3V, R_L = 4Ω, A_V = 6dB, f = 1kHz, 80kHz BW

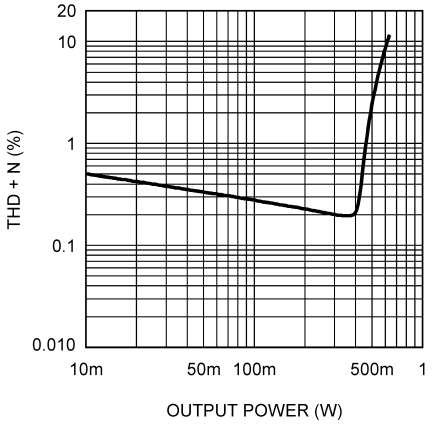


Figure 11.

THD+N vs Frequency
V_{DD} = 3V, R_L = 4Ω, A_V = 6dB, P_{OUT} = 100mW, 80kHz BW

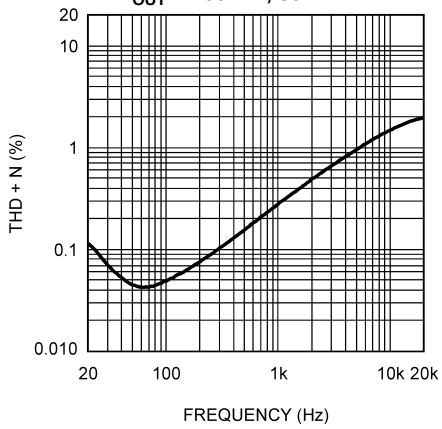


Figure 12.

THD+N vs Output Power
V_{DD} = 3V, R_L = 8Ω, A_V = 6dB, f = 1kHz, 80kHz BW

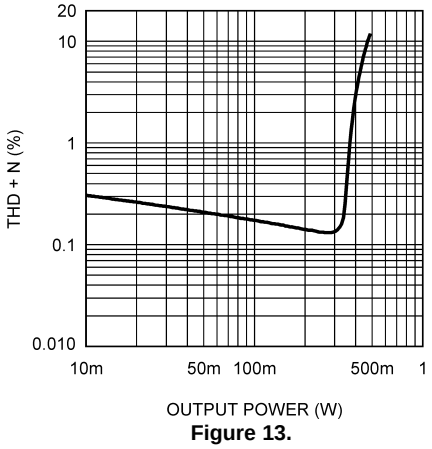


Figure 13.

THD+N vs Frequency
V_{DD} = 3V, R_L = 8Ω, A_V = 6dB, P_{OUT} = 100mW, 80kHz BW

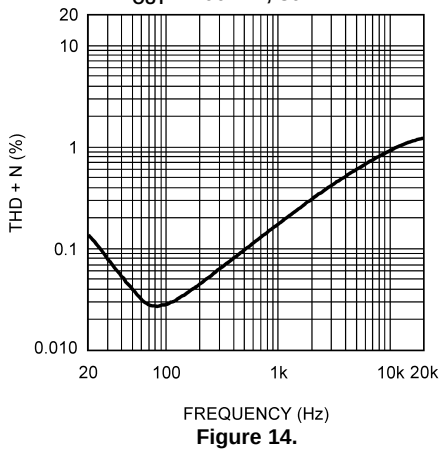


Figure 14.

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Typical Performance Characteristics (continued)

THD+N vs Differential Gain
V_{DD} = 7V, R_L = 8Ω,
P_{OUT} = 600mW, 80kHz BW

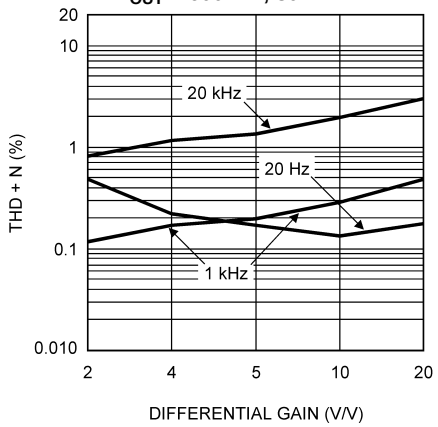


Figure 15.

PSRR vs Frequency
V_{DD} = 7V, V_{RIPPLE} = 200mV_{P-P}
Input Terminated, 80kHz BW

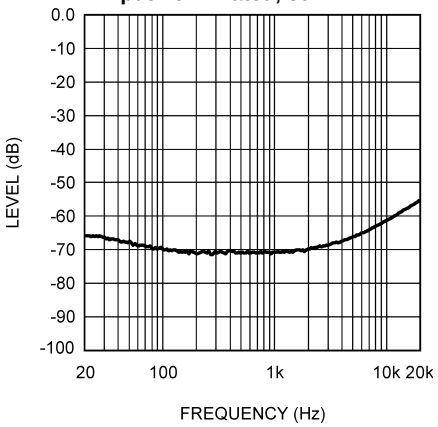


Figure 16.

PSRR vs Frequency
V_{DD} = 5V, V_{RIPPLE} = 200mV_{P-P}
Input Terminated, 80kHz BW

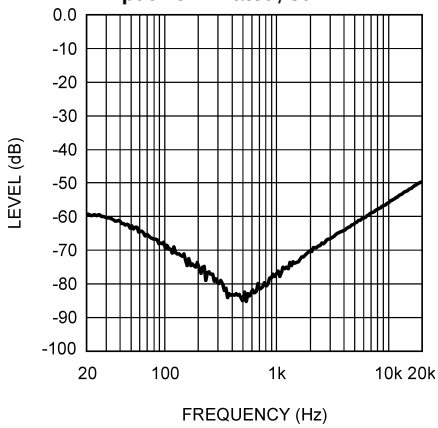


Figure 17.

PSRR vs Frequency
V_{DD} = 3V, V_{RIPPLE} = 200mV_{P-P}
Input Terminated, 80kHz BW

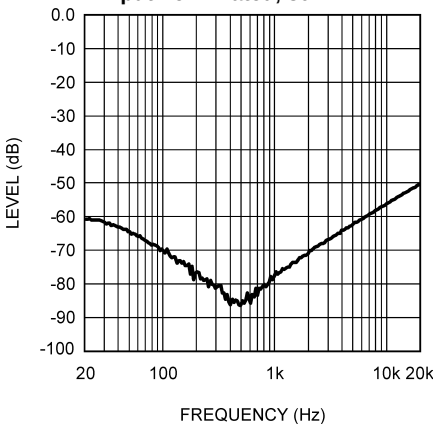


Figure 18.

Output Power vs Supply Voltage
R_L = 4Ω, A_V = 6dB, 80kHz BW

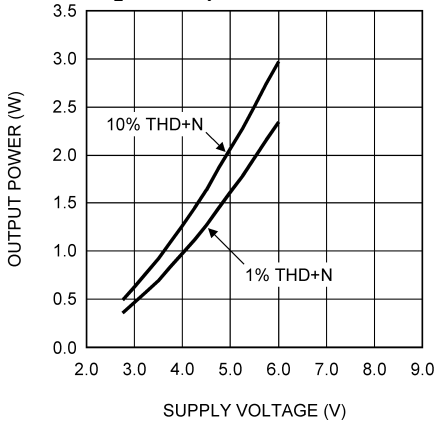


Figure 19.

Output Power vs Supply Voltage
R_L = 8Ω, A_V = 6dB, 80kHz BW

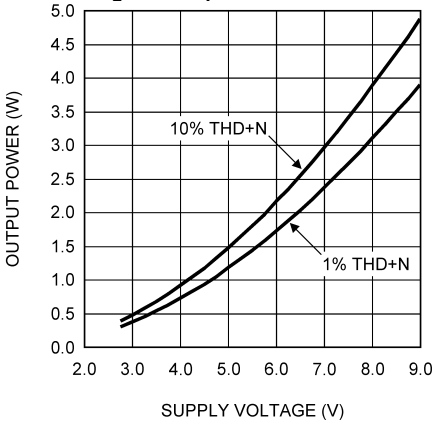


Figure 20.

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Typical Performance Characteristics (continued)

Power Dissipation vs Output Power
V_{DD} = 7V, A_V = 6dB,
THD+N ≤ 1%, 80kHz BW

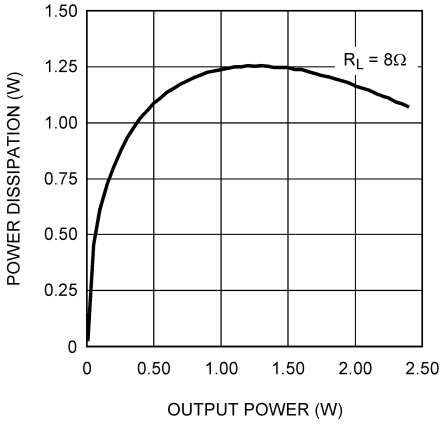


Figure 21.

Power Dissipation vs Output Power
V_{DD} = 5V, A_V = 6dB,
THD+N ≤ 1%, 80kHz BW

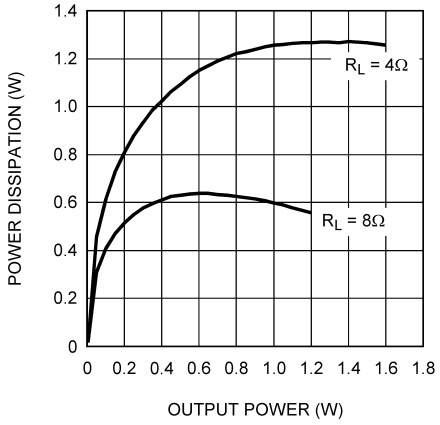


Figure 22.

Power Dissipation vs Output Power
V_{DD} = 3V, A_V = 6dB,
THD+N ≤ 1%, 80kHz BW

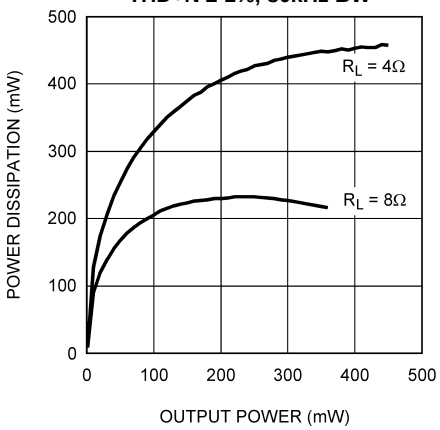


Figure 23.

Power Derating – 9 bump DSBGA
P_{DMAX} = 1.26W, V_{DD} = 7V,
R_L = 8Ω (1) (2)

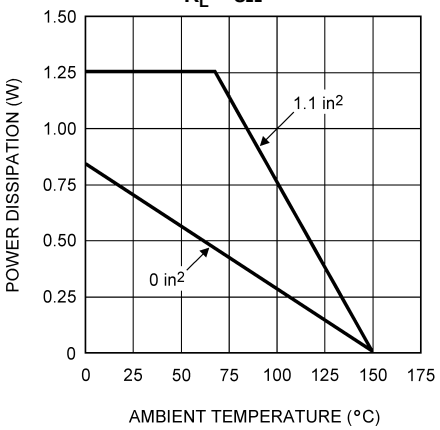


Figure 24.

(1) All bumps have the same thermal resistance and contribute equally when used to lower thermal resistance. The θ_{JA} given in the Absolute Maximum Ratings section under Thermal Resistance is for the ITL package without any heat spreading planes on the PCB.

(2) The demo board shown has 1.1in^2 (710mm^2) heat spreading planes on the two internal layers and the bottom layer. The bottom internal layer is electrically V_{DD} while the top internal and bottom layers are electrically GND. Thermal performance for the demo board is found on the Power Derating graph in the Typical Performance Characteristics section. 7V operation requires heat spreading planes for the thermal stability.

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Typical Performance Characteristics (continued)

Shutdown Threshold vs Supply Voltage
R_L = 8Ω, A_V = 6dB, 80kHz BW

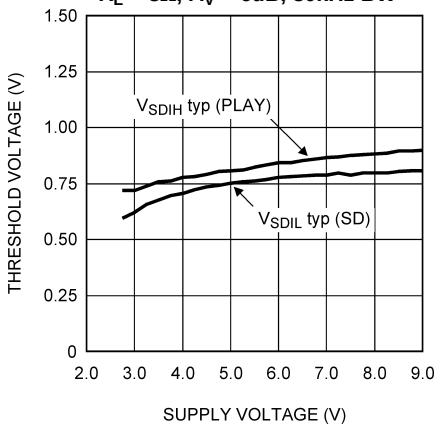


Figure 25.

Supply Current vs Supply Voltage
R_L = 8Ω

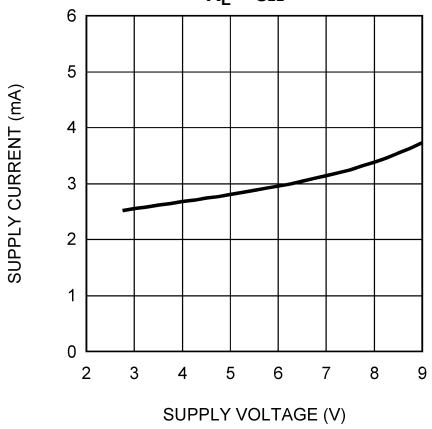


Figure 26.

APPLICATION INFORMATION

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, the LM4954 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_i while the second amplifier's gain is fixed by the two internal 20kΩ resistors. Figure 1 shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the IC is

$$A_{VD} = 2 *(R_f/R_i) \quad (1)$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as “bridged mode” is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the AUDIO POWER AMPLIFIER DESIGN section.

A bridge configuration, such as the one used in LM4954, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the LM4954 has two operational amplifiers in one package, the maximum internal power dissipation is four times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 2.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad (2)$$

It is critical that the maximum junction temperature (T_{JMAX}) of 150°C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced from the free air value, resulting in higher P_{DMAX}. Additional copper foil can be added to any of the leads connected to the LM4954. It is especially effective when connected to V_{DD}, GND, and the output pins. Refer to the application information on the LM4954 reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the Typical Performance Characteristics curves for power dissipation information for different output powers and output loading.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4954. The selection of a bypass capacitor, especially C_B, is dependent upon PSRR requirements, click and pop performance (as explained in the section, PROPER SELECTION OF EXTERNAL COMPONENTS), system cost, and size constraints.

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SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4954 contains a shutdown pin to externally turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the shutdown pin. By switching the shutdown pin to ground, the LM4954 supply current draw will be minimized in idle mode. While the device will be disabled with shutdown pin voltages less than $0.4V_{DC}$, the idle current may be greater than the typical value of 0.01µA. (Idle current is measured with the shutdown pin tied to ground). The LM4954 has an internal 75kΩ pull-down resistor. If the shutdown pin is left floating the IC will automatically enter shutdown mode.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4954 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4954 is unity-gain stable which gives the designer maximum system flexibility. The LM4954 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 Vrms are available from sources such as audio codecs. Please refer to the section, AUDIO POWER AMPLIFIER DESIGN, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 1. The input coupling capacitor, C_i, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Selection Of Input Capacitor Size

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is affected by the size of the input coupling capacitor, C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally $1/2V_{DD}$). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Choosing C_B equal to 2.2µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1µF.

AUDIO POWER AMPLIFIER DESIGN

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the Typical Performance Characteristics section, the supply rail can be easily found.

At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the POWER DISSIPATION section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 3 and Equation 4.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (3)$$

$$A_{VD} = (R_f/R_i)\ 2 \quad (4)$$

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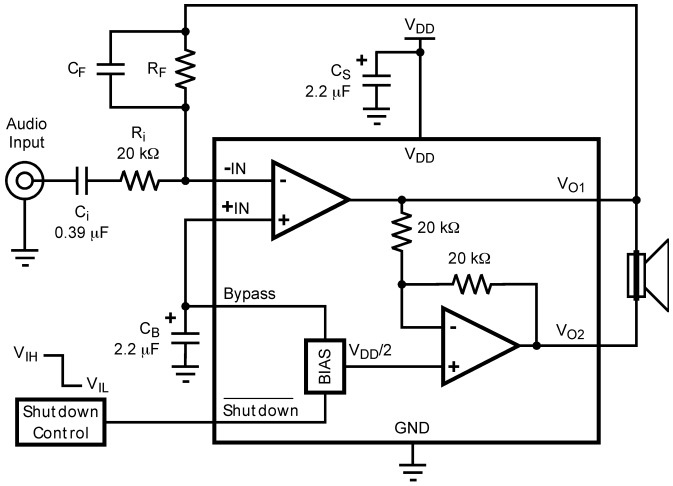


Figure 27. HIGHER GAIN AUDIO AMPLIFIER

The LM4954 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, a feedback capacitor (C_F) may be needed as shown in Figure 27 to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken when calculating the -3dB frequency in that an incorrect combination of R_F and C_F will cause rolloff before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is R_F = 20kΩ and C_F = 25pf. These components result in a -3dB point of approximately 320 kHz. To calculate the value of the capacitor for a given -3dB point, use Equation 5 below:

$$C_F = 1/(2\pi f_{3dB} R_F) \text{ (F)} \quad (5)$$

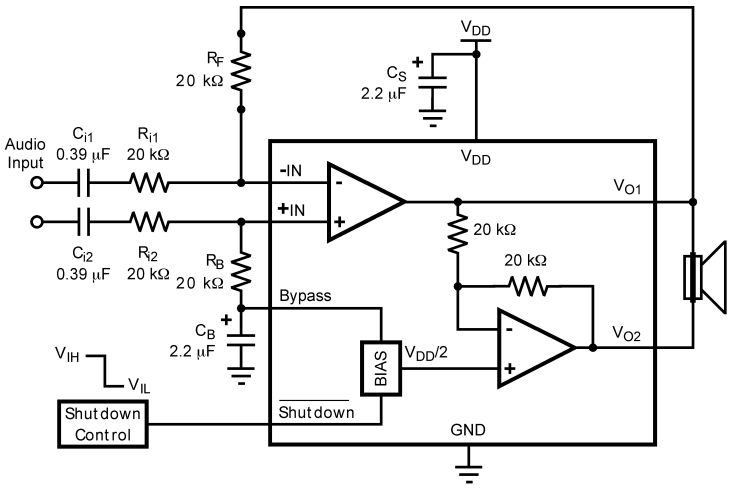


Figure 28. DIFFERENTIAL AMPLIFIER CONFIGURATION FOR LM4954

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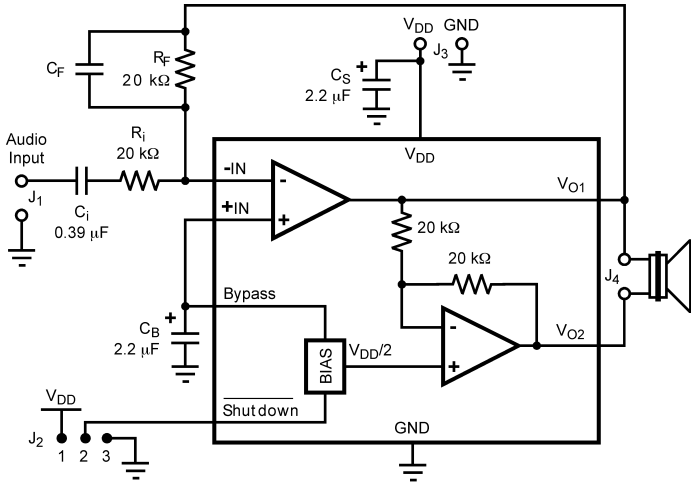


Figure 29. REFERENCE DESIGN BOARD SCHEMATIC

LM4954 DSBGA BOARD ARTWORK(3)

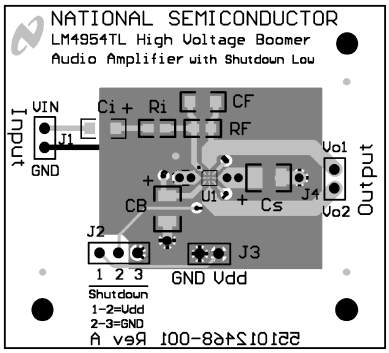


Figure 30. Composite View

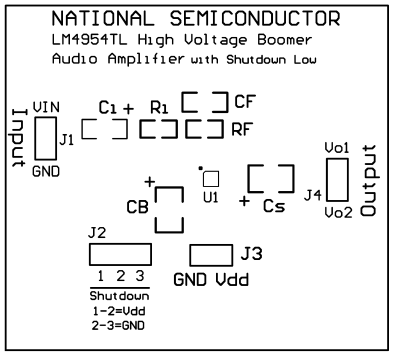


Figure 31. Silk Screen

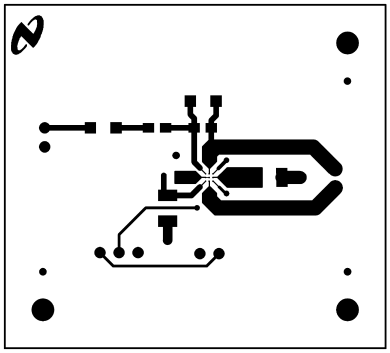


Figure 32. Top Layer

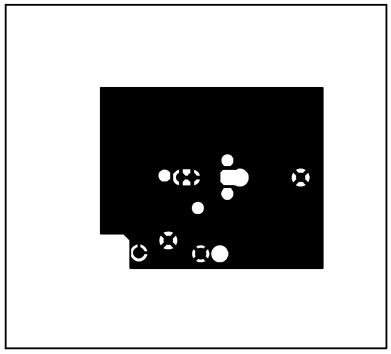


Figure 33. Internal Layer 1, GND

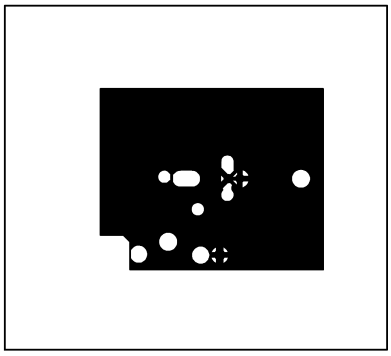


Figure 34. Internal Layer 2, V_{DD}

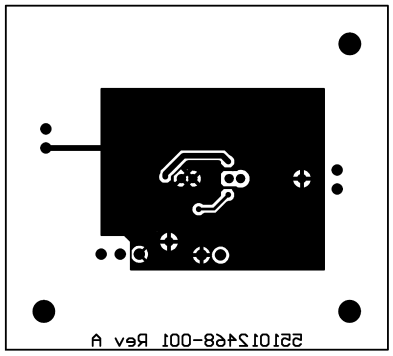


Figure 35. Bottom Layer

(3) All bumps have the same thermal resistance and contribute equally when used to lower thermal resistance. The θ_{JA} given in the Absolute Maximum Ratings section under Thermal Resistance is for the ITL package without any heat spreading planes on the PCB.

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Table 1. Mono LM4954 Reference Design Boards Bill of Materials

Designator	Value	Tolerance	Part Description	Comment
R_i	20kΩ	1%	1/10W, 1% 0805 Resistor	
R_F	20kΩ	1%	1/10W, 1% 0805 Resistor	
C_i	0.39µF	10%	Ceramic 1206 Capacitor, 10%	
C_F				Part not used
C_S	2.2µF	10%	16V Tantalum 1210 Capacitor	
C_B	2.2µF	10%	16V Tantalum 1210 Capacitor	
J_1, J_3, J_4			0.100” 1x2 header, vertical mount	Input, Output, Vdd/GND
J_2			0.100” 1x3 header, vertical mount	Shutdown control

PCB LAYOUT GUIDELINES

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

GENERAL MIXED SIGNAL LAYOUT RECOMMENDATIONS

Power and Ground Circuits

For a two layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique requires a greater amount of design time but will not increase the final price of the board. The only extra parts required may be some jumpers.

Single-Point Power / Ground Connections

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing high frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

Placement of Digital and Analog Components

All digital components and high-speed digital signals traces should be located as far away as possible from analog components and circuit traces.

Avoiding Typical Design / Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

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REVISION HISTORY

Rev	Date	Description
1.1	4/29/05	Added curves 71 and 72. Edited Note 10. Changed Av = 26dB to 6dB under 7V EC table. Edited SHUTDOWN FUNCTION under the Application section.
1.2	6/08/05	Removed all the LLP pkg references. Changed TLA09XXX into YZR0009. Changed X1 and X2 measurements.
1.3	6/15/05	Fixed some typos. Initial WEB release.
1.4	6/20/05	Replaced curve 20129170 with 20129192.
1.5	6/22/05	Split Note 10 and added Note 11. **Re-released to the WEB.**

Changes from Revision A (April 2013) to Revision B **Page**

- Changed layout of National Data Sheet to TI format 17

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4954TL/NOPB	ACTIVE	DSBGA	YZR	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		G F2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

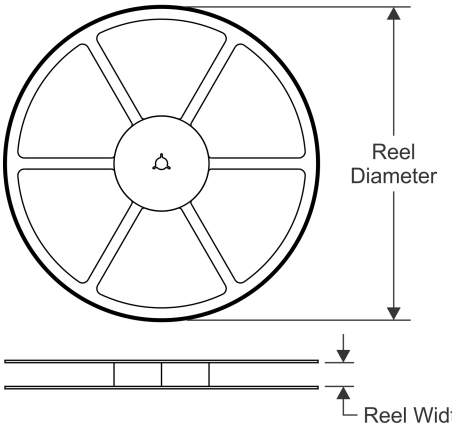
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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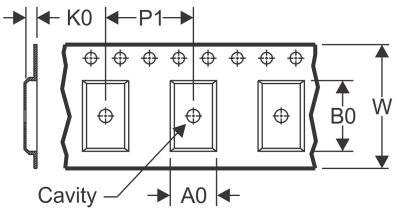
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

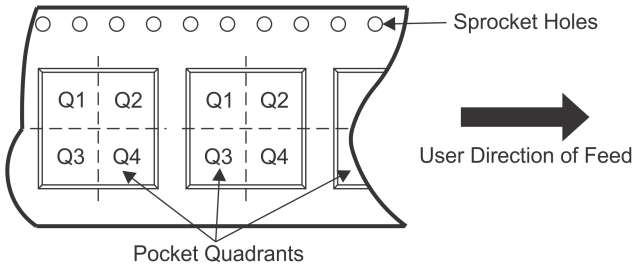


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

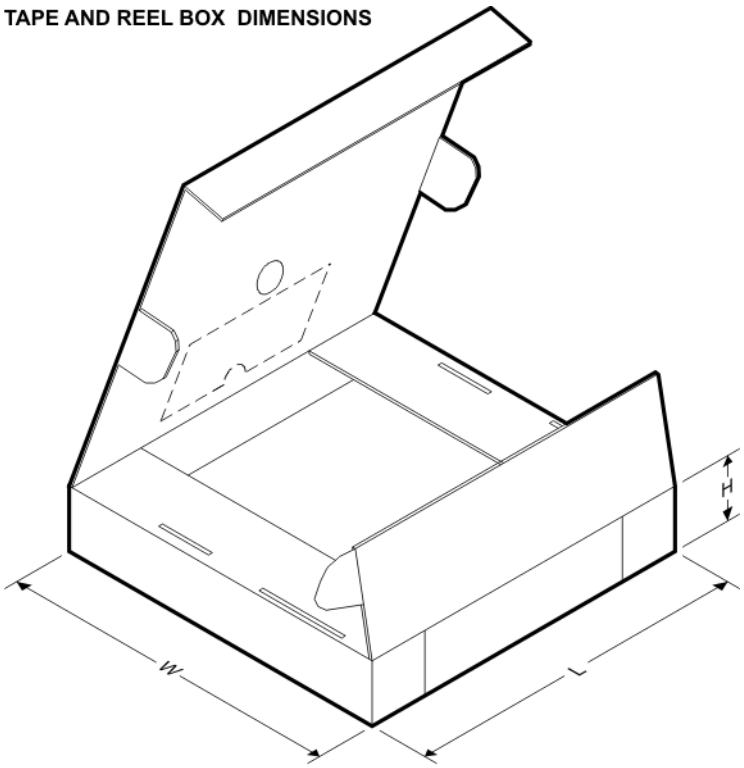
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4954TL/NOPB	DSBGA	YZR	9	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1

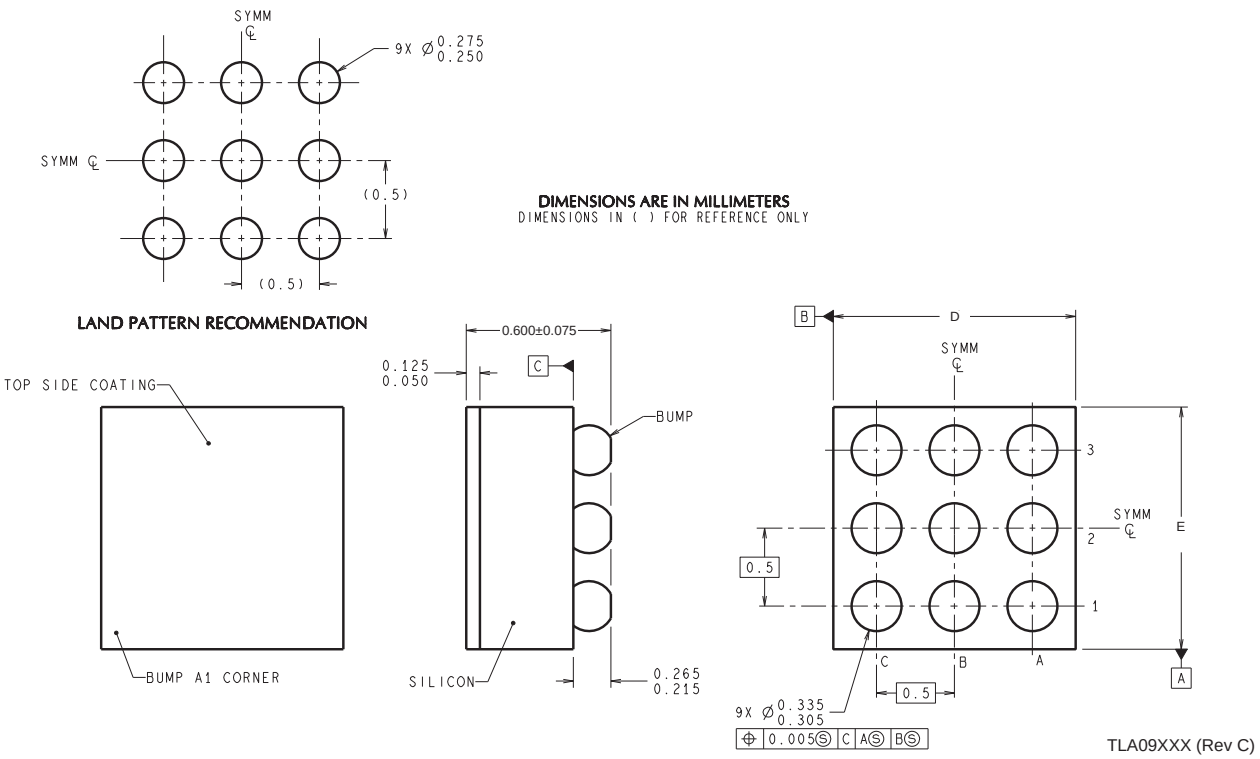
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4954TL/NOPB	DSBGA	YZR	9	250	210.0	185.0	35.0

YZR0009



D: Max = 1.51 mm, Min = 1.45 mm

E: Max = 1.51 mm, Min = 1.45 mm

4215046/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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