

FDMS3604S

MOSFET – N-Channel, POWERTRENCH[®], Power Stage, Asymmetric Dual

General Description

This device includes two specialized N-Channel MOSFETs in a dual PQFN package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 8 m Ω at V_{GS} = 10 V, I_D = 13 A
- Max $r_{DS(on)}$ = 11 m Ω at V_{GS} = 4.5 V, I_D = 11 A

Q2: N-Channel

- Max $r_{DS(on)}$ = 2.6 m Ω at V_{GS} = 10 V, I_D = 23 A
- Max $r_{DS(on)}$ = 3.5 m Ω at V_{GS} = 4.5 V, I_D = 21 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- This Device is Pb-Free and is RoHS Compliant

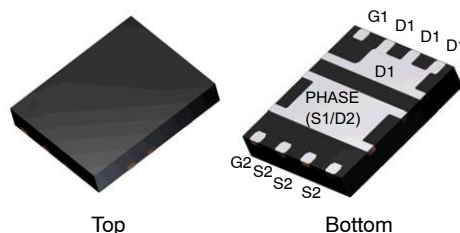
Applications

- Computing
- Communications
- General Purpose Point of Load
- Notebook VCORE



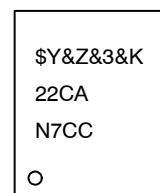
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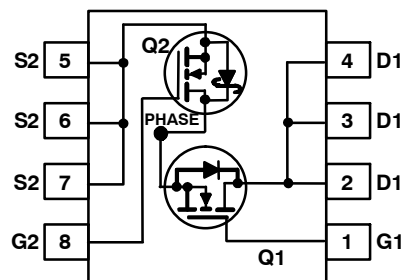
PQFN8 5x6, 1.27P
CASE 483AJ

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
22CA N7CC	= Specific Device Code

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMS3604S

MOSFET MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ Unless Otherwise Noted

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	30	30	V
V_{DSt}	Drain to Source Transient Voltage ($t_{\text{Transient}} < 100 \text{ ns}$)	33	33	V
V_{GS}	Gate to Source Voltage (Note 3)	± 20	± 20	V
I_D	Drain Current –Continuous (Package limited) $T_C = 25^\circ\text{C}$	30	40	A
	–Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	60	130	
	–Continuous $T_A = 25^\circ\text{C}$	13 (Note 1a)	23 (Note 1b)	
	–Pulsed	40	100	
EAS	Single Pulse Avalanche Energy	40 (Note 4)	60 (Note 5)	mJ
P_D	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$	2.2 (Note 1a)	2.5 (Note 1b)	W
	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$	1.0 (Note 1c)	1.0 (Note 1d)	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+150$		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	57 (Note 1a)	50 (Note 1b)	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125 (Note 1c)	120 (Note 1d)	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.5	2	

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
22CA N7CC	FDMS3604S	Power 56	13"	12 mm	3000 Units

FDMS3604S

ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ Unless Otherwise Noted

Symbol	Parameter	Column Head Test Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V I _D = 1 mA, V _{GS} = 0 V	Q1 Q2	30 30			V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C I _D = 10 mA, referenced to 25°C	Q1 Q2		15 12		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	Q1 Q2			1 500	μA
I _{GSS}	Gate to Source Leakage Current, Forwad	V _{GS} = 20 V, V _{DS} = 0 V	Q1 Q2			100 100	nA
ON CHARACTERISTICS							
V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA V _{GS} = V _{DS} , I _D = 1 mA	Q1 Q2	1.1 1.1	2 1.8	2.7 3	V
ΔV _{GS(th)} / ΔT _J	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C I _D = 10 mA, referenced to 25°C	Q1 Q2		−6 −5		mV/°C
r _{DS(on)}	Drain to Source On Resistance	V _{GS} = 10 V, I _D = 13 A V _{GS} = 4.5 V, I _D = 11 A V _{GS} = 10 V, I _D = 13 A , T _J = 125°C	Q1		5.8 8.5 7.8	8 11 10.8	mΩ
		V _{GS} = 10 V, I _D = 23 A V _{GS} = 4.5 V, I _D = 21 A V _{GS} = 10 V, I _D = 23 A , T _J = 125°C	Q2		2.0 3.0 2.6	2.6 3.5 4	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 13 A V _{DS} = 5 V, I _D = 23 A	Q1 Q2		61 130		S
DYNAMIC CHARACTERISTICS							
C _{iss}	Input Capacitance	Q1: V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz Q2: V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Q1 Q2		1340 3240	1785 4310	pF
C _{oss}	Output Capacitance		Q1 Q2		485 1230	645 1635	pF
C _{rss}	Reverse Transfer Capacitance		Q1 Q2		53 103	80 155	pF
R _g	Gate Resistance		Q1 Q2	0.2 0.2	0.6 0.8	2 3	Ω
SWITCHING CHARACTERISTICS							
t _{d(on)}	Turn-On Delay Time	Q1: V _{DD} = 15 V, I _D = 13 A, R _{GEN} = 6 Ω Q2: V _{DD} = 15 V, I _D = 23 A, R _{GEN} = 6 Ω	Q1 Q2		8.2 13	16 23	ns
t _r	Rise Time		Q1 Q2		2.5 4.8	10 10	ns
t _{d(off)}	Turn-Off Delay Time		Q1 Q2		20 31	32 50	ns
t _f	Fall Time		Q1 Q2		2.2 3.4	10 10	ns
Q _g	Total Gate Charge	V _{GS} = 0 V to 10 V	Q1 V _{DD} = 15 V, I _D = 13 A Q2 V _{DD} = 15 V, I _D = 23 A	Q1 Q2	21 47	29 66	nC
Q _g	Total Gate Charge	V _{GS} = 0 V to 4.5 V		Q1 Q2	10 22	14 31	nC
Q _{gs}	Gate to Source Gate Charge			Q1 Q2	3.9 9		nC
Q _{gd}	Gate to Drain “Miller” Charge			Q1 Q2	3.1 5.5		nC

FDMS3604S

ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ Unless Otherwise Noted (continued)

Symbol	Parameter	Column Head Test Conditions	Type	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 13\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}$, $I_S = 23\text{ A}$ (Note 2)	Q1 Q2		0.8 0.8	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1 $I_F = 13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ Q2	Q1 Q2		25 32	40 51	ns
Q_{rr}	Reverse Recovery Charge	$I_F = 23\text{ A}$, $di/dt = 300\text{ A}/\mu\text{s}$	Q1 Q2		9 39	18 62	nC

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 57 °C/W when mounted on
a 1 in² pad of 2 oz copper



b. 50 °C/W when mounted on
a 1 in² pad of 2 oz copper



c. 125 °C/W when mounted on a
minimum pad of 2 oz copper



d. 120 °C/W when mounted on a
minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
- E_{AS} of 40 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 1\text{ mH}$, $I_{AS} = 9\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.3\text{ mH}$, $I_{AS} = 14\text{ A}$.
- E_{AS} of 60 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 1\text{ mH}$, $I_{AS} = 11\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.3\text{ mH}$, $I_{AS} = 18\text{ A}$.

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)

$T_J = 25^\circ\text{C}$ Unless Otherwise Noted

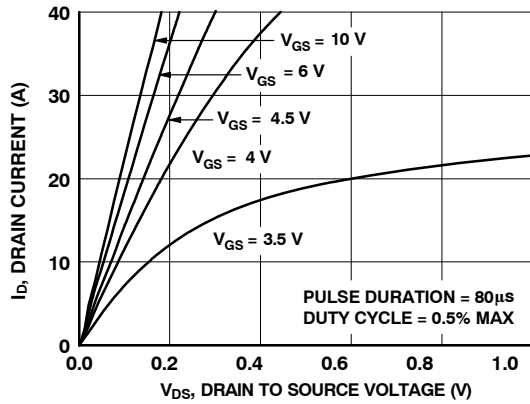


Figure 1. On-Region Characteristics

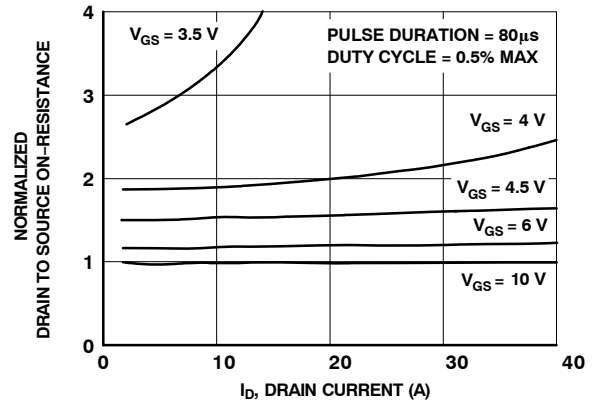


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

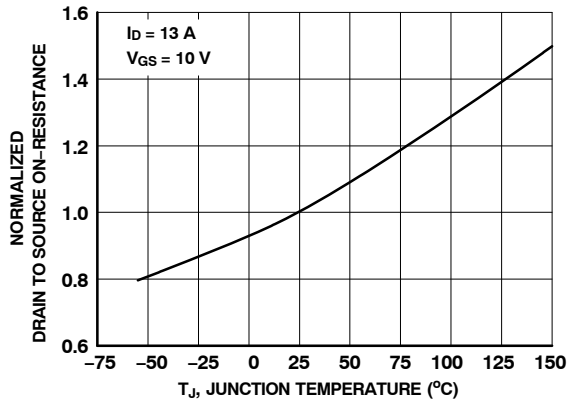


Figure 3. Normalized On Resistance vs Junction Temperature

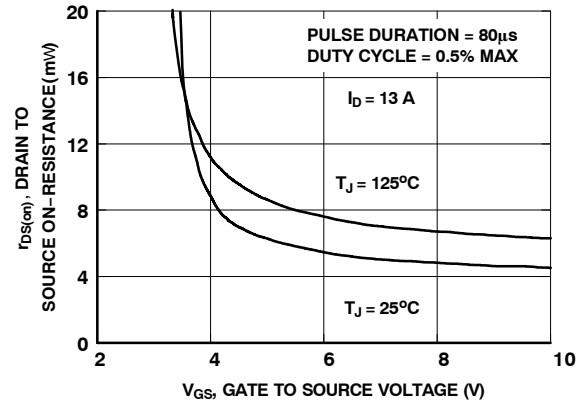


Figure 4. On-Resistance vs Gate to Source Voltage

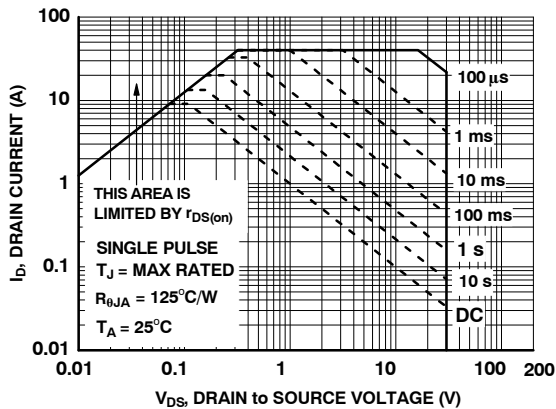


Figure 5. Transfer Characteristics

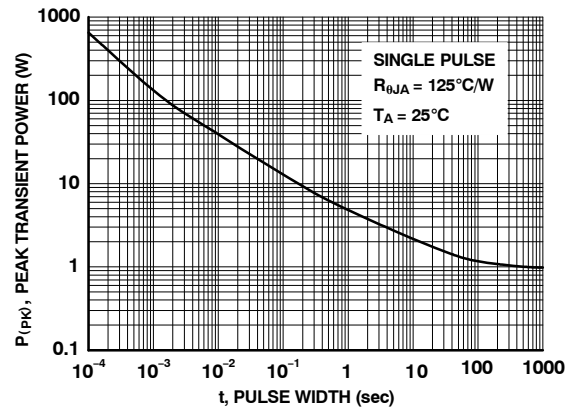


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)

$T_J = 25^\circ\text{C}$ Unless Otherwise Noted (continued)

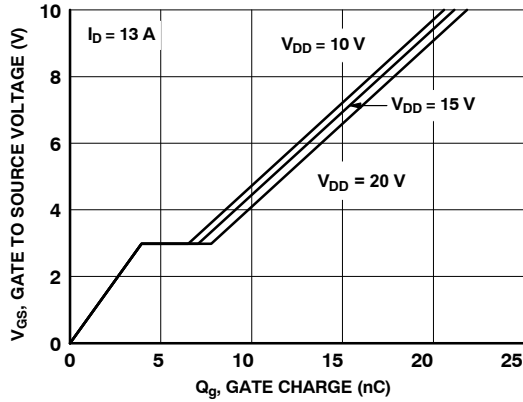


Figure 7. Gate Charge Characteristics

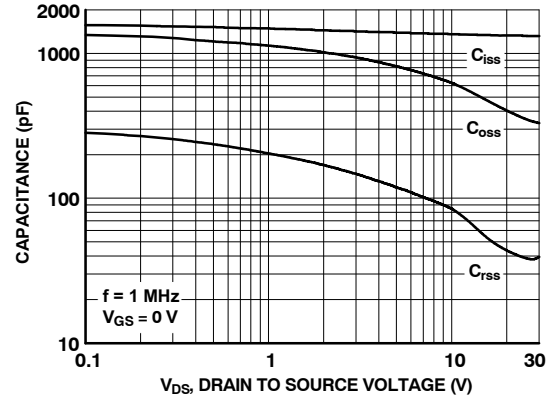


Figure 8. Capacitance vs Drain to Source Voltage

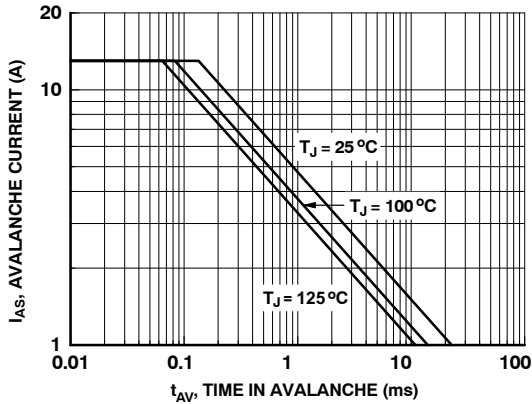


Figure 9. Unclamped Inductive Switching Capability

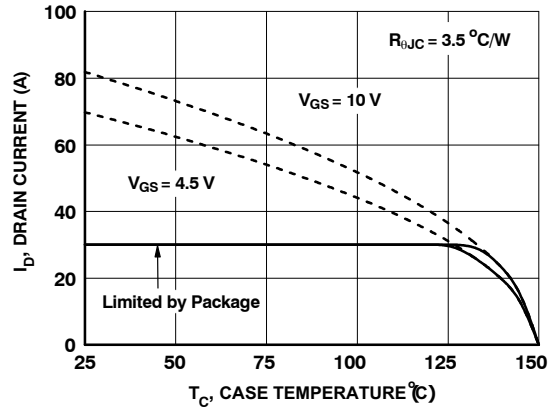


Figure 10. Maximum Continuous Drain Current vs Case Temperature

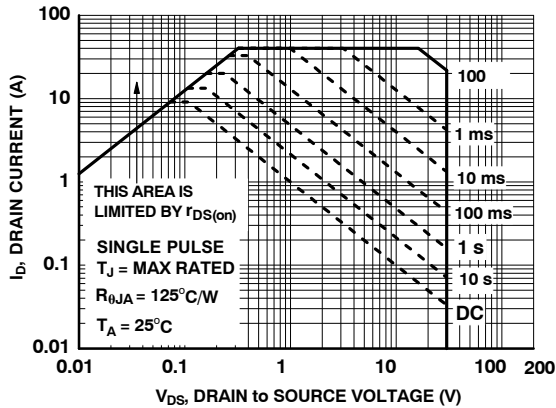


Figure 11. Forward Bias Safe Operating Area

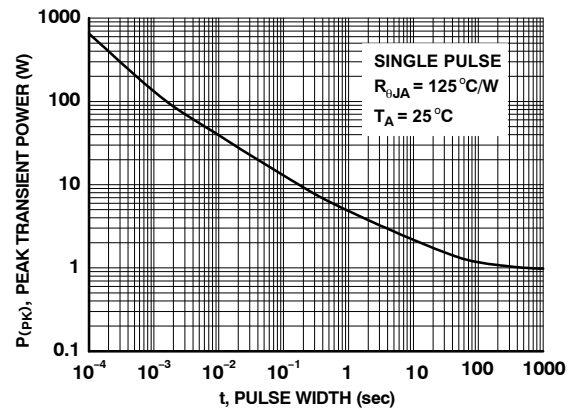
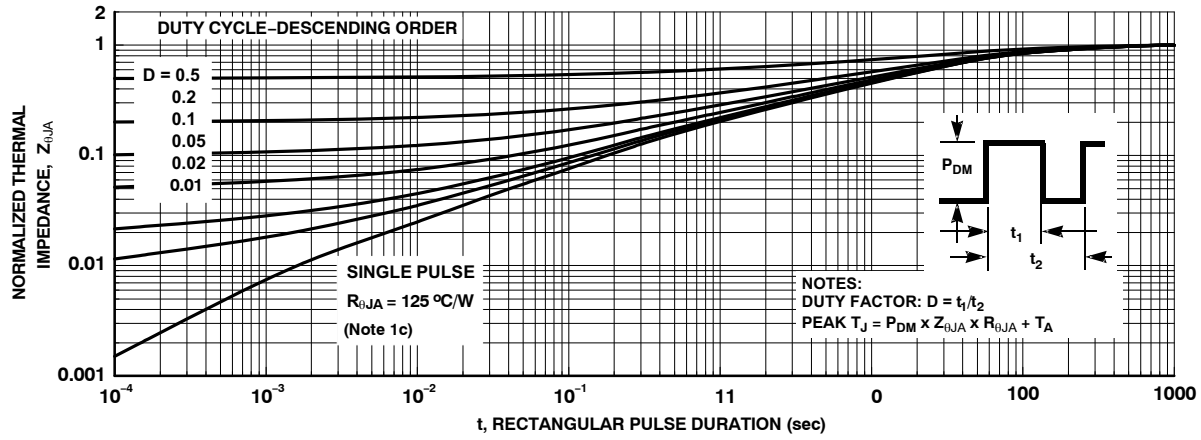


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)

 $T_J = 25^\circ\text{C}$ Unless Otherwise Noted (continued)

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL)

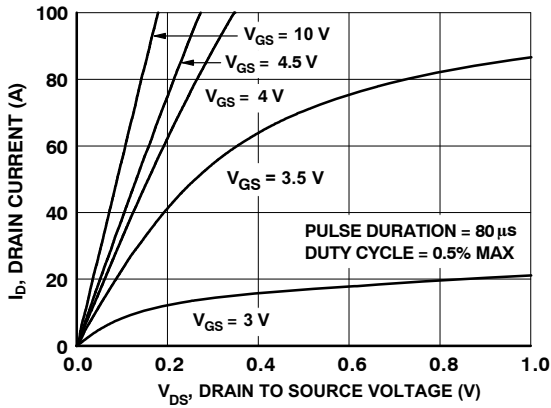
 $T_J = 25^\circ\text{C}$ Unless Otherwise Noted

Figure 14. On-Region Characteristics

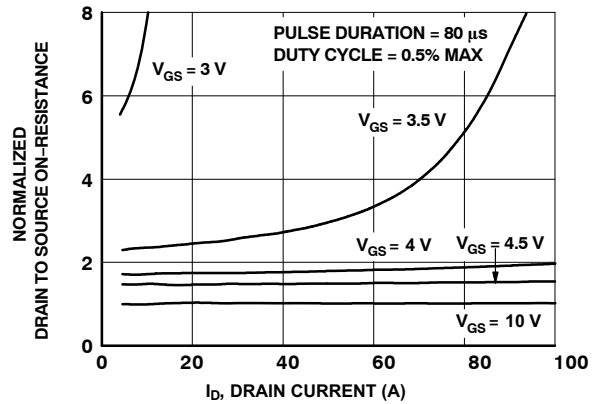


Figure 15. Normalized On-Resistance vs Drain Current and Gate Voltage

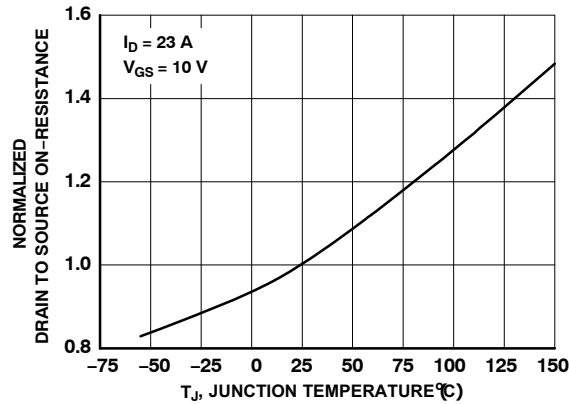


Figure 16. Normalized On-Resistance vs Junction Temperature

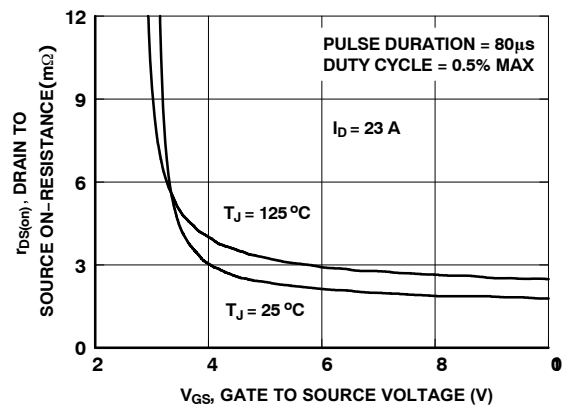


Figure 17. On-Resistance vs Gate to Source Voltage

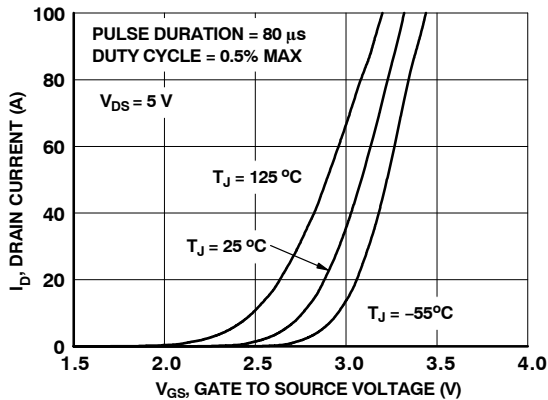


Figure 18. Transfer Characteristics

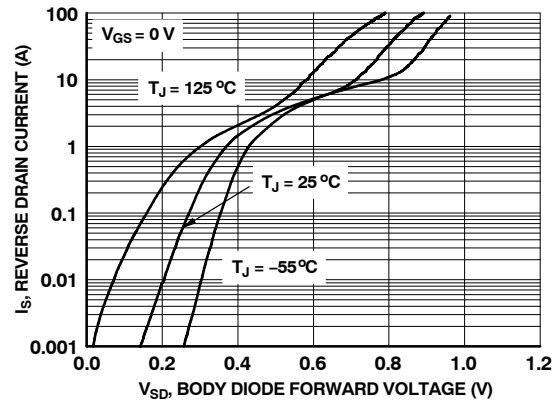


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL)

$T_J = 25^\circ\text{C}$ Unless Otherwise Noted (continued)

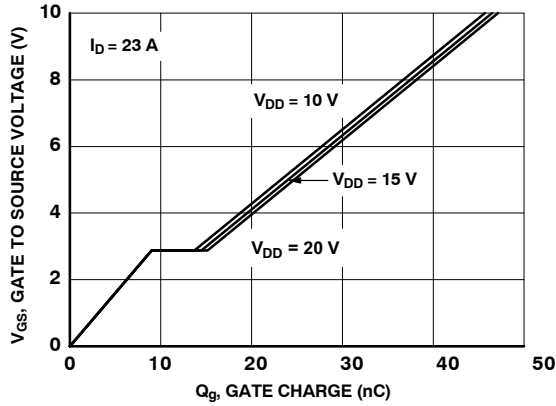


Figure 20. Gate Charge Characteristics

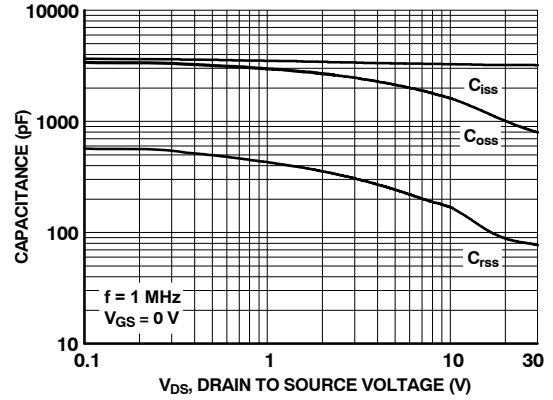


Figure 21. Capacitance vs Drain to Source Voltage

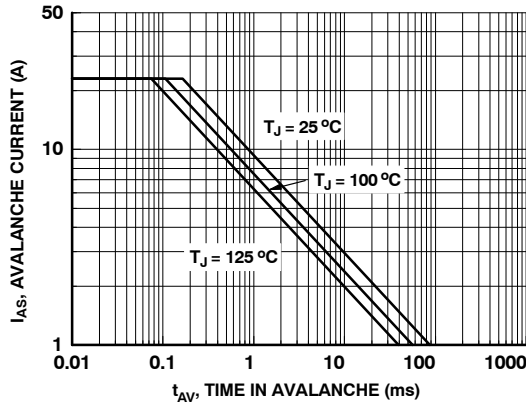


Figure 22. Unclamped Inductive Switching Capability

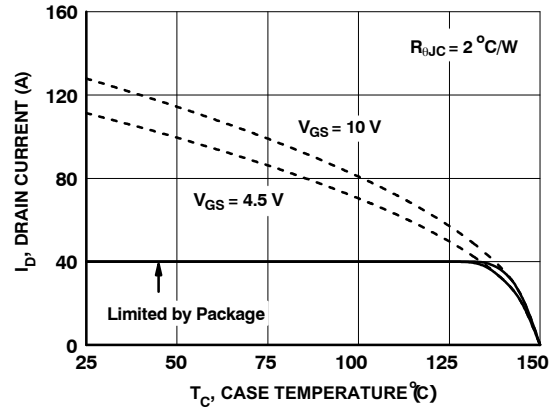


Figure 23. Maximum Continuous Drain Current vs Case Temperature

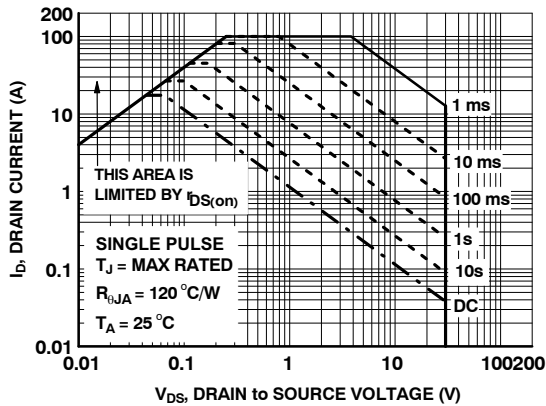


Figure 24. Forward Bias Safe Operating Area

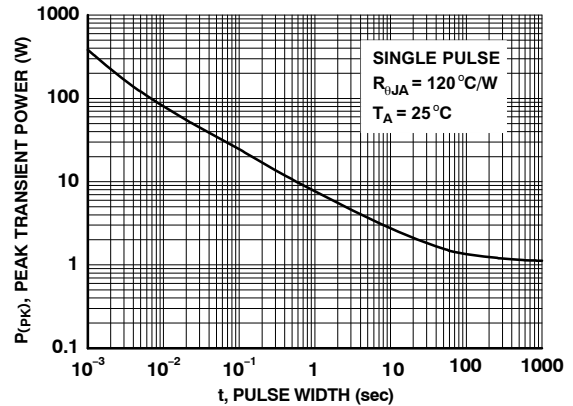


Figure 25. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL)

$T_J = 25^\circ\text{C}$ Unless Otherwise Noted (continued)

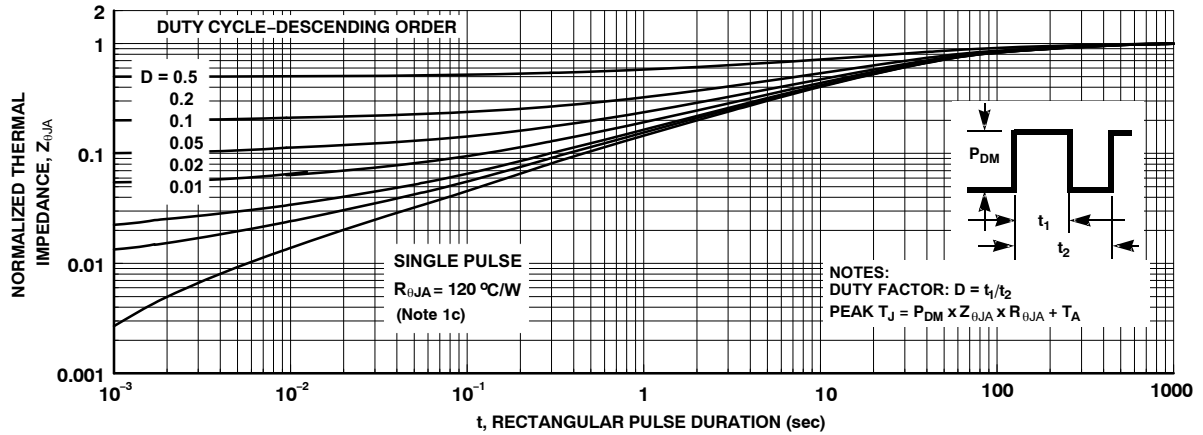


Figure 26. Junction-to-Ambient Transient Thermal Response Curve

SyncFET Schottky Body Diode Characteristics

ON Semiconductor's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMS3604S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

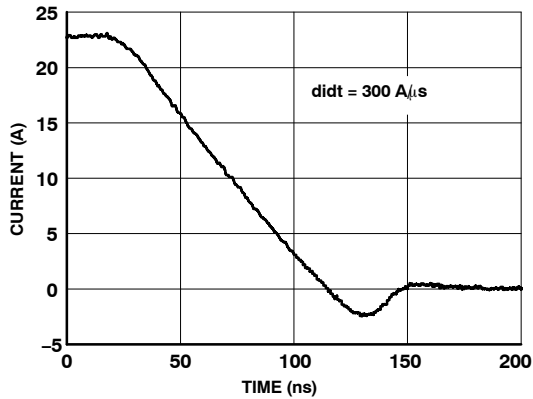


Figure 27. FDMS3604S SyncFET Body Diode Reverse Recovery Characteristics

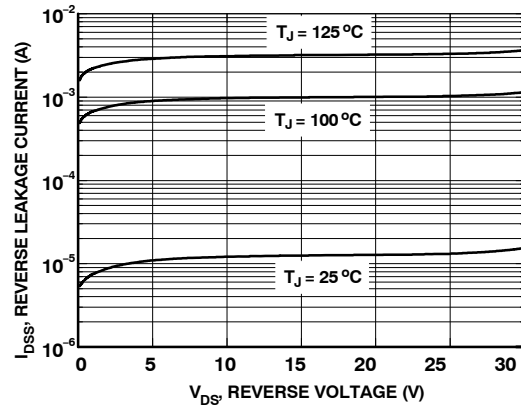


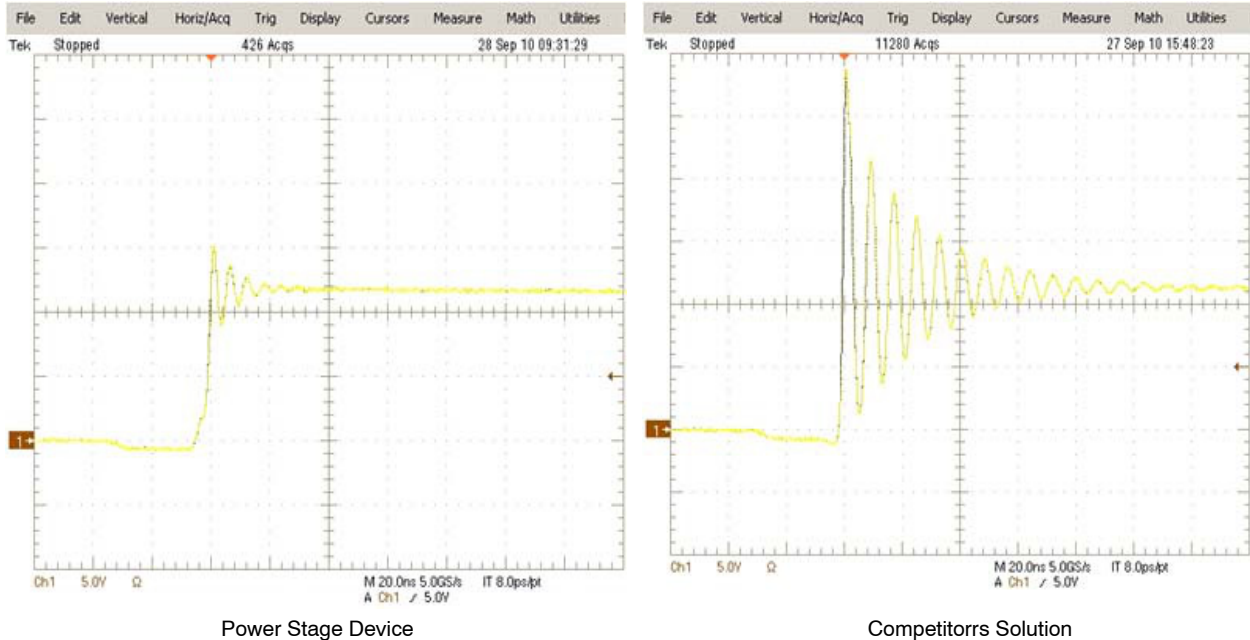
Figure 28. SyncFET Body Diode Reverse Leakage versus Drain-source Voltage

APPLICATION INFORMATION

Switch Node Ringing Suppression

ON Semiconductor's Power Stage products incorporate a proprietary design* that minimizes the peak overshoot, ringing voltage on the switch node (PHASE) without the need of any external snubbing components in a buck converter.

converter. As shown in the Figure 29, the Power Stage solution rings significantly less than competitor solutions under the same set of test conditions.



*Patent Pending

Figure 29. Power Stage Phase Node Rising Edge, High Turn On

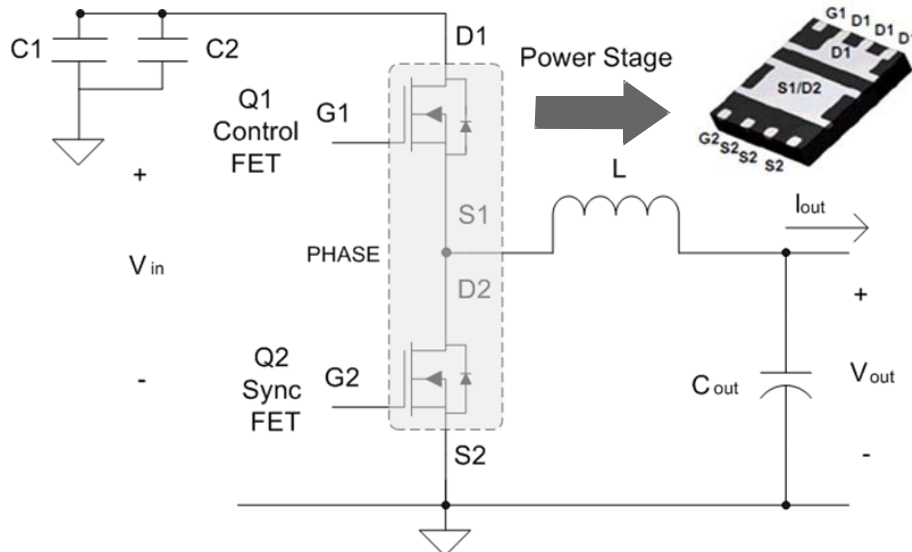


Figure 30. Shows the Power Stage in a Buck Converter Topology

Recommended PCB Layout Guidelines

As a PCB designer, it is necessary to address critical issues in layout to minimize losses and optimize the performance of the power train. Power Stage is a high power density solution and all high current flow paths, such as VIN (D1), PHASE (S1/D2) and GND (S2), should be short and wide

for better and stable current flow, heat radiation and system performance. A recommended layout procedure is discussed below to maximize the electrical and thermal performance of the part.

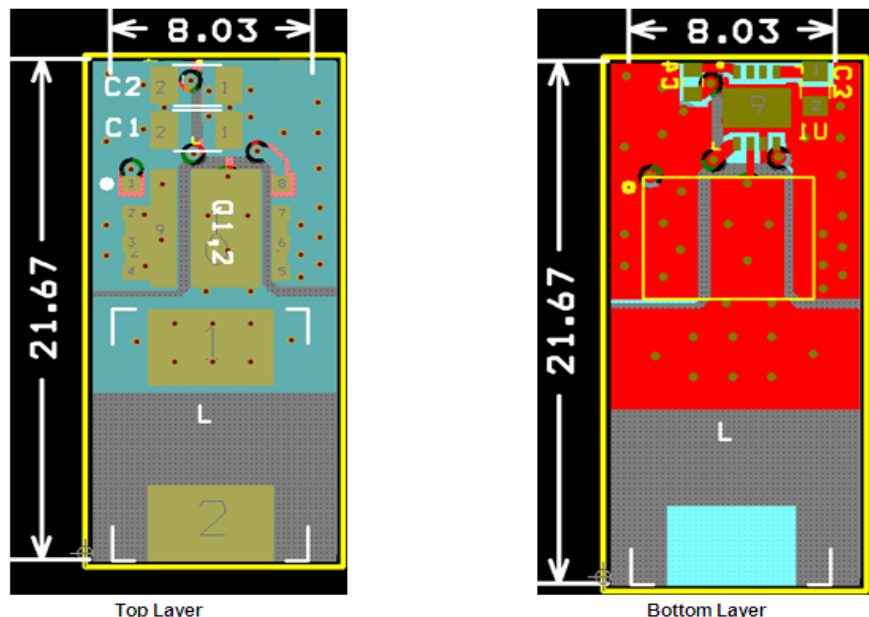


Figure 31. Recommended PCB Layout

Following is a guideline, not a requirement which the PCB designer should consider:

1. Input ceramic bypass capacitors C1 and C2 must be placed close to the D1 and S2 pins of Power Stage to help reduce parasitic inductance and High Frequency conduction loss induced by switching operation. C1 and C2 show the bypass capacitors placed close to the part between D1 and S2. Input capacitors should be connected in parallel close to the part. Multiple input caps can be connected depending upon the application
2. The PHASE copper trace serves two purposes; In addition to being the current path from the Power Stage package to the output inductor (L), it also serves as heat sink for the lower FET in the Power Stage package. The trace should be short and wide enough to present a low resistance path for the high current flow between the Power Stage and the inductor. This is done to minimize conduction losses and limit temperature rise. Please note that the PHASE node is a high voltage and high frequency switching node with high noise potential. Care should be taken to minimize coupling to adjacent traces. The reference layout in Figure 31 shows a good balance between the thermal and electrical performance of Power Stage
3. Output inductor location should be as close as possible to the Power Stage device for lower power loss due to copper trace resistance. A shorter and wider PHASE trace to the inductor reduces the conduction loss. Preferably the Power Stage should be directly in line (as shown in Figure 32) with the inductor for space savings and compactness
4. The POWER trench Technology MOSFETs used in the Power Stage are effective at minimizing phase node ringing. It allows the part to operate well within the breakdown voltage limits. This eliminates the need to have an external snubber circuit in most cases. If the designer chooses to use an RC snubber, it should be placed close to the part between the PHASE pad and S2 pins to dampen the high-frequency ringing
5. The driver IC should be placed close to the Power Stage part with the shortest possible paths for the High Side gate and Low Side gates through a wide trace connection. This eliminates the effect of parasitic inductance and resistance between the driver and the MOSFET and turns the devices on and off as efficiently as possible. At

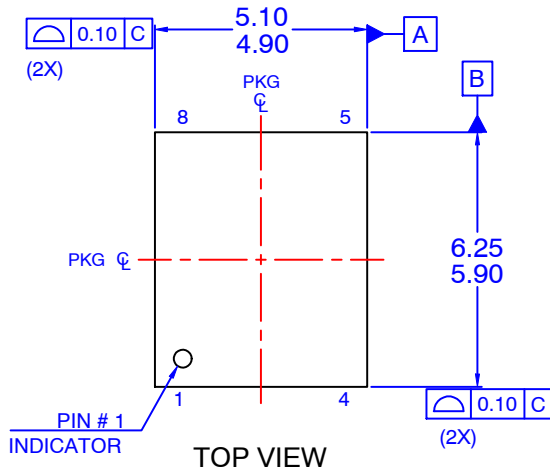
higher-frequency operation this impedance can limit the gate current trying to charge the MOSFET input capacitance. This will result in slower rise and fall times and additional switching losses. Power Stage has both the gate pins on the same side of the package which allows for back mounting of the driver IC to the board. This provides a very compact path for the drive signals and improves efficiency of the part

6. S2 pins should be connected to the GND plane with multiple vias for a low impedance grounding. Poor grounding can create a noise transient offset voltage level between S2 and driver ground. This could lead to faulty operation of the gate driver and MOSFET

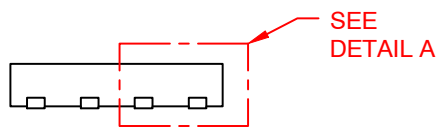
7. Use multiple vias on each copper area to interconnect top, inner and bottom layers to help smooth current flow and heat conduction. Vias should be relatively large, around 8 mils to 10 mils, and of reasonable inductance. Critical high frequency components such as ceramic bypass caps should be located close to the part and on the same side of the PCB. If not feasible, they should be connected from the backside via a network of low inductance vias

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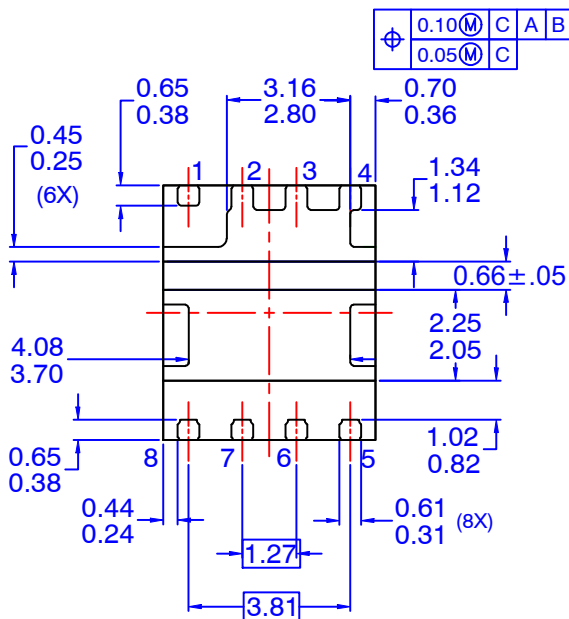
DATE 30 SEP 2016



TOP VIEW

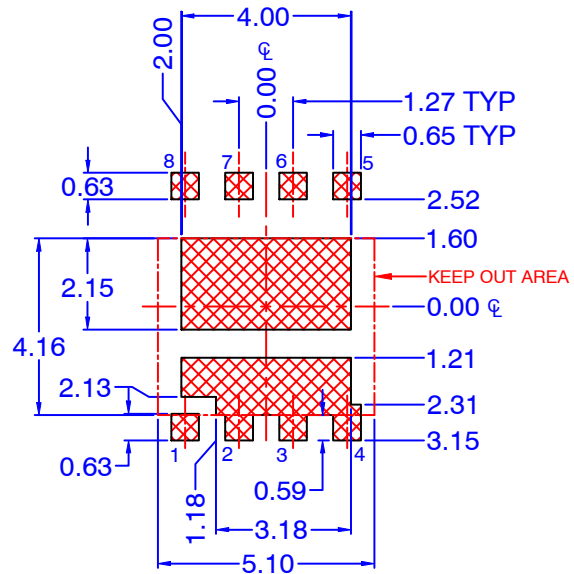


SIDE VIEW

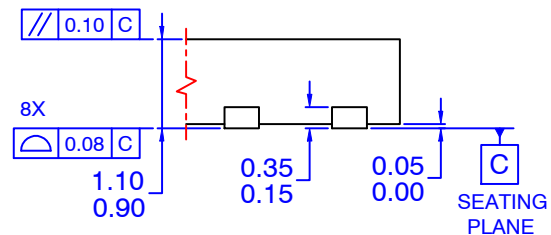


BOTTOM VIEW

OPTION - A (SAWN TYPE)



RECOMMENDED LAND PATTERN
FOR SAWN / PUNCHED TYPE



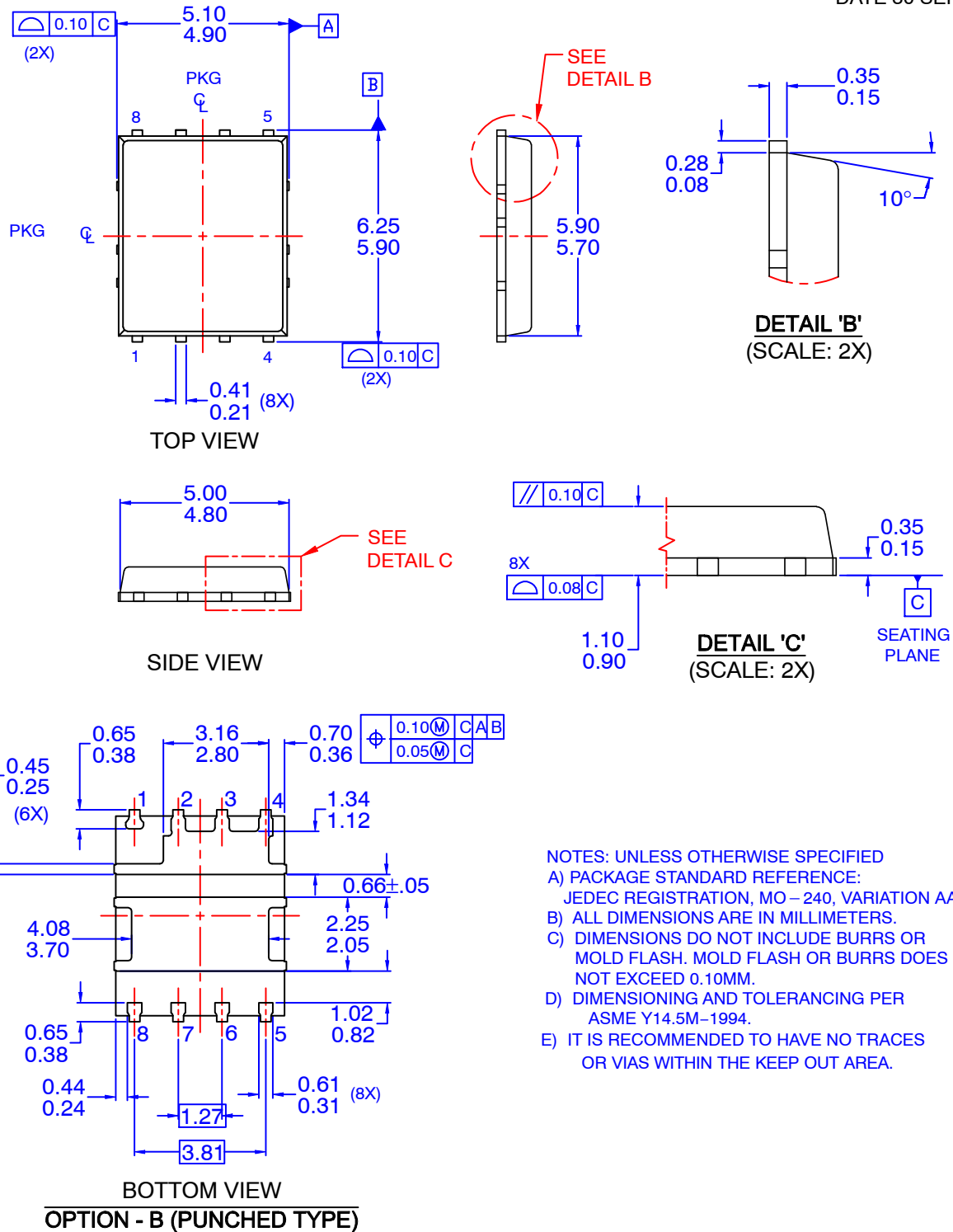
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DESCRIPTION:	PQFN8 5X6, 1.27P	PAGE 1 OF 2

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