ANALOG DEVICES

Xstream™ 6.5 Gbps Quad Buffer Mux/Demux

AD8158

FEATURES

- Quad 2:1 mux/1:2 demux
- Optimized for dc to 6.5 Gbps NRZ data
- Per-lane P/N pair inversion for routing ease
- Programmable input equalization
  - Compensates up to 40 inches of FR4
- Loss-of-signal detection
- Programmable output pre-emphasis up to 12 dB
- Programmable output levels with squelch and disable
- Accepts ac-coupled or dc-coupled differential CML inputs
- 50 Ω on-chip termination
- 1:2 demux supports unicast or bicast operation
- Port-level loopback
- Port or single lane switching
- 1.8 V to 3.3 V flexible core supply
- User-settable I/O supply from V_{CC} to 1.2 V
- Low power, typically 2.0 W in basic configuration
- 100-lead LFCSP
- –40°C to +85°C operating temperature range

APPLICATIONS

- Low cost redundancy switch
- SONET OC48/SDH16 and lower data rates
- XAUI/GbE/FC/Infiniband over backplane
- OIF CEI 6.25 Gbps over backplane
- Serial data-level shift
- 4-/8-/12-lane equalizers or redrivers

FUNCTIONAL BLOCK DIAGRAM

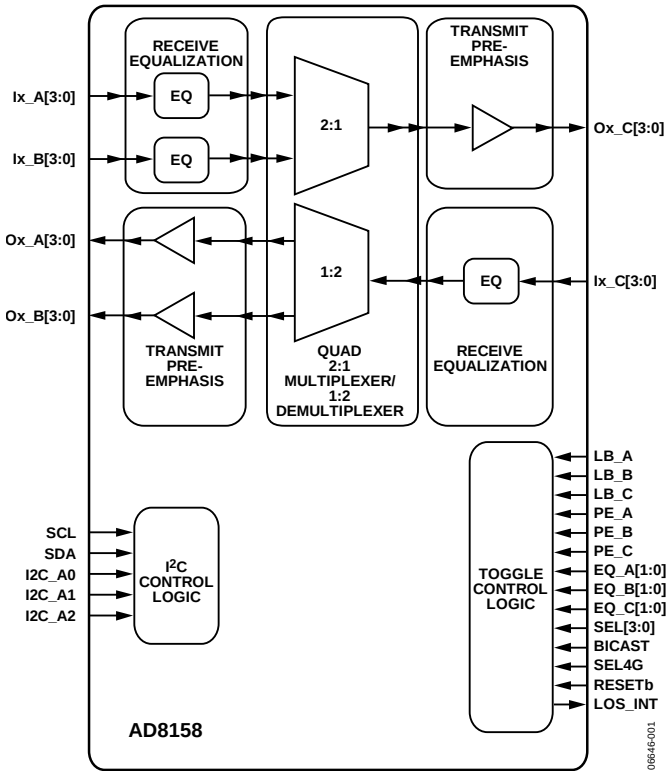


Figure 1.

GENERAL DESCRIPTION

The AD8158 is an asynchronous, protocol-agnostic, quad-lane 2:1 switch with a total of 12 differential CML inputs and 12 differential CML outputs. The signal path supports NRZ signaling with data rates up to 6.5 Gbps per lane. Each lane offers programmable receive equalization, programmable output pre-emphasis, programmable output levels, and loss-of-signal detection.

The nonblocking switch-core of the AD8158 implements a 2:1 multiplexer and 1:2 demultiplexer per lane and supports independent lane switching through the four select pins, SEL[3:0]. Each port is a four-lane link. Every lane implements an asynchronous path supporting dc to 6.5 Gbps NRZ data, fully independent of other lanes. The AD8158 has low latency and very low lane-to-lane skew.

The main application of the AD8158 is to support redundancy on both the backplane and the line interface sides of a serial link. The demultiplexing path implements unicast and bicast capability, allowing the part to support either 1 + 1 or 1:1 redundancy.

The AD8158 is also suited for testing high speed serial links because of its ability to duplicate incoming data. In a port-monitoring application, the AD8158 can maintain link-connectivity with a pass-through connection from Port C to Port A while sending a duplicate copy of the data to test equipment on Port B.

The rich feature set of the AD8158 can be controlled either through external toggle pins or by setting on-chip control registers through the I^2C interface.

Rev. B

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REVISION HISTORY

12/09—Rev. A: Rev. B

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9/09—Rev. 0: Rev. A

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6/08—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = V_{TTI} = V_{TTO} = 1.8 V, DV_{CC} = 3.3 V, V_{EE} = 0 V, R_L = 50 Ω, basic configuration[1], data rate = 6.5 Gbps, data pattern = PRBS7, ac-coupled inputs and outputs, differential input swing = 800 mV p-p, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Data Rate/Channel (NRZ)		DC		6.5	Gbps
Deterministic Jitter (No Channel)	Data rate = 6.5 Gbps, EQ setting = 0		22		ps p-p
Random Jitter (No Channel)	RMS, data rate = 6.5 Gbps		1		ps
Residual Deterministic Jitter with Receive Equalization	Data rate 6.5 Gbps, 20 inch FR4		30		ps p-p
	Data rate 6.5 Gbps, 40 inch FR4		40		ps p-p
Residual Deterministic Jitter with Transmit Preemphasis	Data rate 6.5 Gbps, 10 inch FR4		35		ps p-p
	Data rate 6.5 Gbps, 30 inch FR4		42		ps p-p
Propagation Delay	50% input to 50% output (maximum EQ)		700		ps
Lane-to-Lane Skew	Signal path and switch architecture is balanced and symmetric (maximum EQ)		90		ps
Switching Time	50% logic switching to 50% output data		150		ns
Output Rise/Fall Time	20% to 80% (PE = lowest setting)		62		ps
INPUT CHARACTERISTICS					
Differential Input Voltage Swing	V_{ICM}[2] = V_{CC} − 0.6 V, V_{CC} = V_{MIN} to V_{MAX}, T_A = T_{MIN} to T_{MAX}, LOS control register = 0x05	200		2000	mV p-p diff
Input Voltage Range	Single-ended absolute voltage level, V_L minimum		V_{EE} + 0.6		V
	Single-ended absolute voltage level, V_H maximum		V_{CC} + 0.3		V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Differential, PE = 0, default output level, @ dc	590	725	820	mV p-p diff
Output Voltage Range, Single-Ended Absolute Voltage Level	TX_HEADROOM = 0, V_L minimum		V_{CC} − 1.1		V
	TX_HEADROOM = 0, V_H maximum		V_{CC} + 0.6		V
	TX_HEADROOM = 1, V_L minimum		V_{CC} − 1.3		V
	TX_HEADROOM = 1, V_H maximum		V_{CC} + 0.6		V
Output Current	Port A/B/C, PE_A/B/C = minimum		16		mA
	Port A/B/C, PE_A/B/C = 6 dB, V_{OD} = 800 mV p-p		32		mA
TERMINATION CHARACTERISTICS					
Resistance	Differential, V_{CC} = V_{MIN} to V_{MAX}, T_A = T_{MIN} to T_{MAX}	90	100	110	Ω
LOS CHARACTERISTICS					
DC Assert Level			50		mV p-p diff
DC Deassert Level			300		mV p-p diff
LOS to Output Squelch	LOS_FILT = 0, V_{ID} = 0 to 50% OP/ON settling, V_{CC} = 1.8 V		21		ns
LOS to Output Enable	LOS_FILT = 0, data present to first valid transition, V_{CC} = 1.8 V		67		ns
POWER SUPPLY					
Operating Range					
V_{CC}	V_{EE} = 0 V, TX_HEADROOM = 0	1.6	1.8 to 3.3	3.6	V
	V_{EE} = 0 V, TX_HEADROOM = 1	2.2	3.3	3.6	V
DV_{CC}	DV_{CC} ≥ V_{CC}, V_{EE} = 0 V	1.6	1.8 to 3.3	3.6	V
V_{TTI}		1.2		V_{CC} + 0.3	V
V_{TTO}		1.2		V_{CC} + 0.3	V

Parameter	Conditions	Min	Typ	Max	Unit
Supply Current					
I_{CC}					
V_{CC} = 1.8 V	LB_x = 0, PE = 0 dB on all ports, default		370	450	mA
	LB_x = 1, PE = 6 dB on all ports, default		730	850	mA
V_{CC} = 3.3 V	LB_x = 0, PE = 0 dB on all ports, default		400	460	mA
	LB_x = 1, PE = 6 dB on all ports, default		780	860	mA
I_{TTO}					
V_{TTO} = 1.8 V	LB_x = 0, PE = 0 dB on all ports, default		128	150	mA
	LB_x = 1, PE = 6 dB on all ports, default		367	420	mA
V_{TTO} = 3.3 V	LB_x = 0, PE = 0 dB on all ports, default		134	152	mA
	LB_x = 1, PE = 6 dB on all ports, default		388	422	mA
I_{TTI}			10	20	mA
I_{DVCC}			2	4	mA
THERMAL CHARACTERISTICS					
Operating Temperature Range		−40		+85	°C
θ_{JA}	Still air; JEDEC 4-layer test board, exposed pad soldered		22.2		°C/W
θ_{JC}	Still air; thermal resistance through exposed pad		1.4		°C/W
Maximum Junction Temperature				125	°C
LOGIC CHARACTERISTICS[3]	I^2C, SDA, SCL, control pins				
Input High (V_{IH})	DV_{CC} = 3.3 V	0.7 × DV_{CC}		DV_{CC}	V
Input Low (V_{IL})	DV_{CC} = 3.3 V	V_{EE}		0.3 × DV_{CC}	V
Input High (V_{IH})	DV_{CC} = 1.8 V		0.8 × DV_{CC}	DV_{CC}	V
Input Low (V_{IL})	DV_{CC} = 1.8 V	V_{EE}	0.2 × DV_{CC}		V
Output High (V_{OH})	2 kΩ pull-up resistor to DV_{CC}		DV_{CC}		V
Output Low (V_{OL})	I_{OL} = +3 mA	V_{EE}		0.4	V

[1] Bicast is off, loopback is off on all ports, preemphasis is set to minimum on all ports, and equalization is set to minimum on all ports.
[2] V_{ICM} is the input common-mode voltage.
[3] EQ control pins (EQ_A[1:0], EQ_B[1:0], EQ_C[1:0]) require 5 kΩ in series when $DV_{CC} > V_{CC}$.

I²C TIMING SPECIFICATIONS

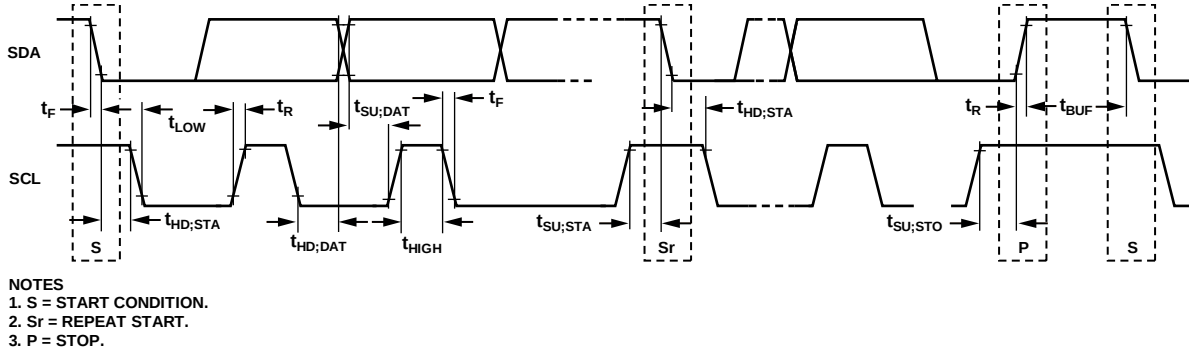


Figure 2. I²C Timing Diagram

Table 2. I²C Timing Parameters

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{SCL}	0	400+	kHz
Hold Time for a Start Condition	$t_{HD;STA}$	0.6		µs
Setup Time for a Repeated Start Condition	$t_{SU;STA}$	0.6		µs
Low Period of the SCL Clock	t_{LOW}	1.3		µs
High Period of the SCL Clock	t_{HIGH}	0.6		µs
Data Hold Time	$t_{HD;DAT}$	0		µs
Data Setup Time	$t_{SU;DAT}$	10		ns
Rise Time for Both SDA and SCL	t_R	1	300	ns
Fall Time for Both SDA and SCL	t_F	1	300	ns
Setup Time for Stop Condition	$t_{SU;STO}$	0.6		µs
Bus Free Time Between a Stop and a Start Condition	t_{BUF}	1		µs
Bus Free Time After a Reset		1		µs
Reset Pulse Width[1]		10		ns

[1] Reset pulse width is defined as the time RESETB is held below the logic low threshold (V_{IL}) listed in Table 1 while the DV_{CC} supply is within the operating range in Table 1.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{CC} to V_{EE}	3.7 V
DV_{CC} to V_{EE}	3.7 V
V_{TTI}	Lower of (V_{CC} + 0.6 V) or 3.6 V
V_{TTO}	Lower of (V_{CC} + 0.6 V) or 3.6 V
V_{CC} to DV_{CC}	0.6 V
Internal Power Dissipation	4.26 W
Differential Input Voltage	2.0 V
Logic Input Voltage	V_{EE} − 0.3 V < V_{IN} < V_{CC} + 0.6 V
Storage Temperature Range	−65°C to +125°C
Junction Temperature	125°C

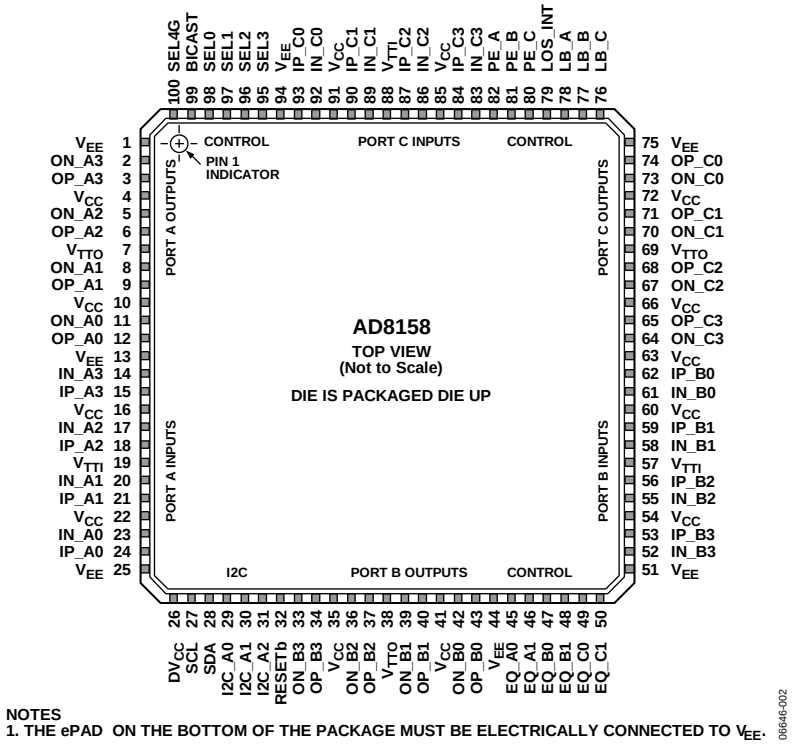
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE ePAD ON THE BOTTOM OF THE PACKAGE MUST BE ELECTRICALLY CONNECTED TO V_{EE}.

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 13, 25, 44, 51, 75, 94, ePAD	V_{EE}	Power	Negative Supply
2	ON_A3	Output	High Speed Output Complement
3	OP_A3	Output	High Speed Output
4, 10, 16, 22, 35, 41, 54, 60, 63, 66, 72, 85, 91	V_{CC}	Power	Positive Supply
5	ON_A2	Output	High Speed Output Complement
6	OP_A2	Output	High Speed Output
7, 38, 69	V_{TTO}	Power	Port A, Port B, and Port C Output Termination Supply
8	ON_A1	Output	High Speed Output Complement
9	OP_A1	Output	High Speed Output
11	ON_A0	Output	High Speed Output Complement
12	OP_A0	Output	High Speed Output
14	IN_A3	Input	High Speed Input Complement
15	IP_A3	Input	High Speed Input
17	IN_A2	Input	High Speed Input Complement
18	IP_A2	Input	High Speed Input
19, 57, 88	V_{TTI}	Power	Port A, Port B, and Port C Input Termination Supply
20	IN_A1	Input	High Speed Input Complement
21	IP_A1	Input	High Speed Input
23	IN_A0	Input	High Speed Input Complement
24	IP_A0	Input	High Speed Input
26	DV_{CC}	Power	Digital Power Supply

Pin No.	Mnemonic	Type	Description
27	SCL	I²C	I²C Clock Pin
28	SDA	I²C	I²C Data Pin
29	I2C_A0	I²C	I²C Address Pin (LSB)
30	I2C_A1	I²C	I²C Address Pin
31	I2C_A2	I²C	I²C Address Pin (MSB)
32	RESETb	Control[1]	Chip Reset. Active Low
33	ON_B3	Output	High Speed Output Complement
34	OP_B3	Output	High Speed Output
36	ON_B2	Output	High Speed Output Complement
37	OP_B2	Output	High Speed Output
39	ON_B1	Output	High Speed Output Complement
40	OP_B1	Output	High Speed Output
42	ON_B0	Output	High Speed Output Complement
43	OP_B0	Output	High Speed Output
45	EQ_A0[2]	Control[1]	Port A Equalizer Control Bit 0 (LSB)
46	EQ_A1[2]	Control[1]	Port A Equalizer Control Bit 1 (MSB)
47	EQ_B0[2]	Control[1]	Port B Equalizer Control Bit 0 (LSB)
48	EQ_B1[2]	Control[1]	Port B Equalizer Control Bit 1 (MSB)
49	EQ_C0[2]	Control[1]	Port C Equalizer Control Bit 0 (LSB)
50	EQ_C1[2]	Control[1]	Port C Equalizer Control Bit 1 (MSB)
52	IN_B3	Input	High Speed Input Complement
53	IP_B3	Input	High Speed Input
55	IN_B2	Input	High Speed Input Complement
56	IP_B2	Input	High Speed Input
58	IN_B1	Input	High Speed Input Complement
59	IP_B1	Input	High Speed Input
61	IN_B0	Input	High Speed Input Complement
62	IP_B0	Input	High Speed Input
64	ON_C3	Output	High Speed Output Complement
65	OP_C3	Output	High Speed Output
67	ON_C2	Output	High Speed Output Complement
68	OP_C2	Output	High Speed Output
70	ON_C1	Output	High Speed Output Complement
71	OP_C1	Output	High Speed Output
73	ON_C0	Output	High Speed Output Complement
74	OP_C0	Output	High Speed Output
76	LB_C	Control[1]	Loopback Enable for Port C, Active High
77	LB_B	Control[1]	Loopback Enable for Port B, Active High
78	LB_A	Control[1]	Loopback Enable for Port A, Active High
79	LOS_INT	Interrupt[1]	Loss of Signal Interrupt, Active High
80	PE_C	Control[1]	Pre-Emphasis Control for Port C, Active High
81	PE_B	Control[1]	Pre-Emphasis Control for Port B, Active High
82	PE_A	Control[1]	Pre-Emphasis Control for Port A, Active High
83	IN_C3	Input	High Speed Input Complement
84	IP_C3	Input	High Speed Input
86	IN_C2	Input	High Speed Input Complement
87	IP_C2	Input	High Speed Input
89	IN_C1	Input	High Speed Input Complement
90	IP_C1	Input	High Speed Input
92	IN_C0	Input	High Speed Input Complement
93	IP_C0	Input	High Speed Input

Pin No.	Mnemonic	Type	Description
95	SEL3	Control[1]	Lane 3 A/B Switch Control
96	SEL2	Control[1]	Lane 2 A/B Switch Control
97	SEL1	Control[1]	Lane 1 A/B Switch Control
98	SEL0	Control[1]	Lane 0 A/B Switch Control
99	BICAST	Control[1]	Enable Bicast Mode for Port A and Port B Outputs, Active High
100	SEL4G	Control[1]	Set Transmitter for Low Speed PE, Active High

[1] Logic level of control pins referred to DV_{CC}.
[2] EQ control pins (EQ_A[1:0], EQ_B[1:0], EQ_C[1:0]) require 5 kΩ in series when $DV_{CC} > V_{CC}$.

TYPICAL PERFORMANCE CHARACTERISTICS

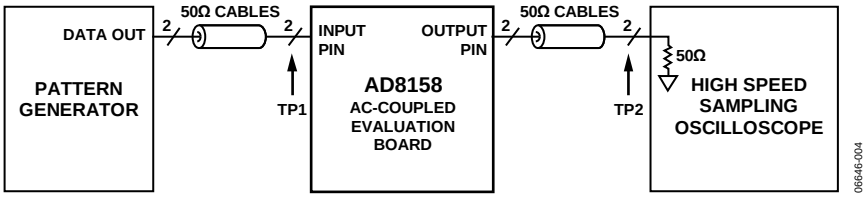


Figure 4. Standard Test Circuit (No Channel)

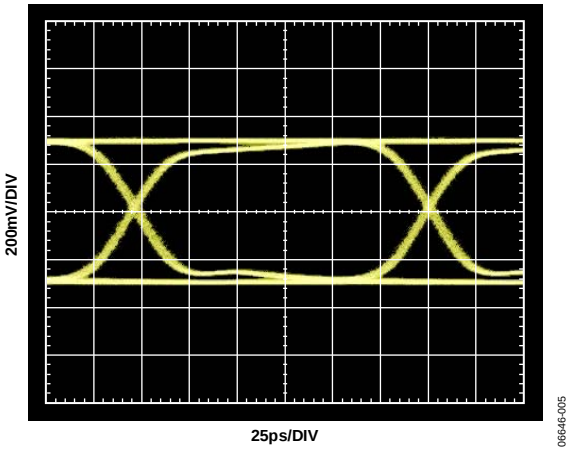


Figure 5. 6.5 Gbps Input Eye (TP1 from Figure 4)

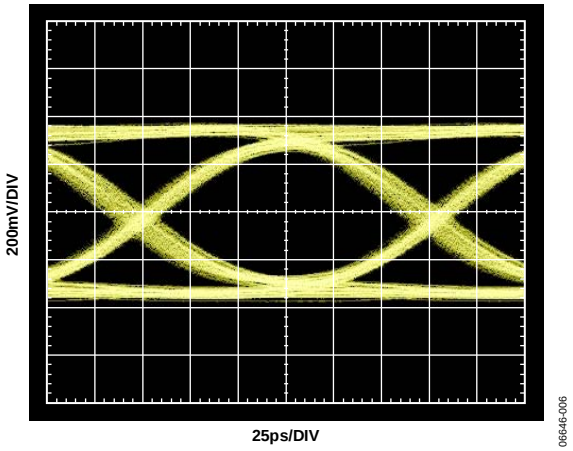


Figure 6. 6.5 Gbps Output Eye, No Channel (TP2 from Figure 4)

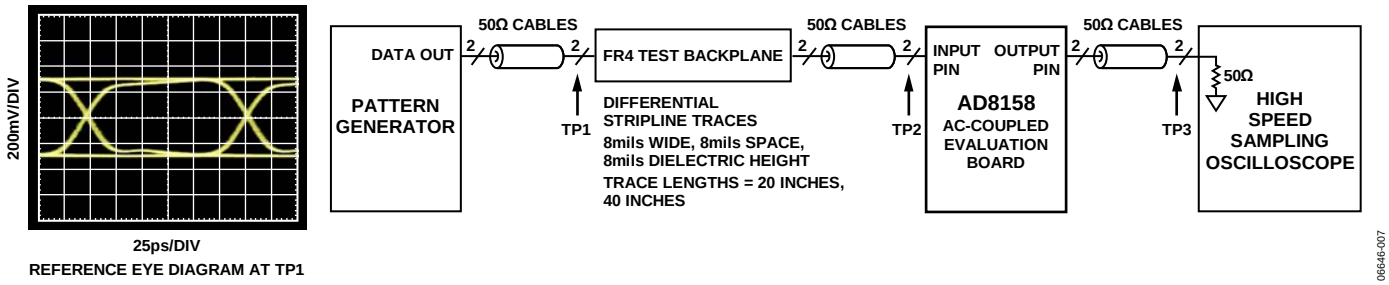


Figure 7. Input Equalization Test Circuit

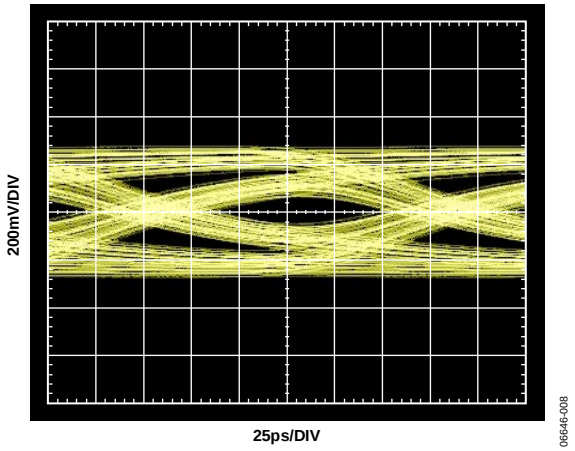


Figure 8. 6.5 Gbps Input Eye, 20 Inch FR4 Input Channel (TP2 from Figure 7)

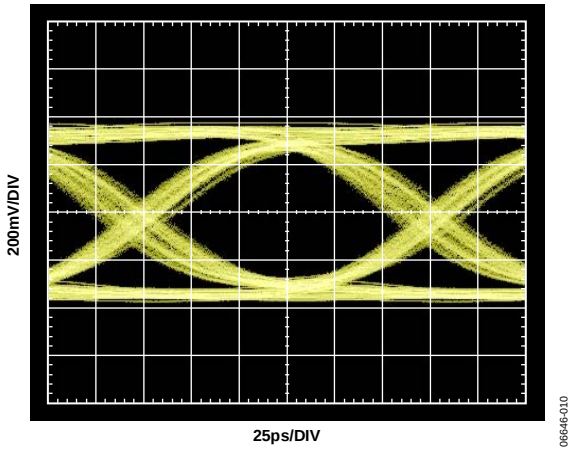


Figure 10. 6.5 Gbps Output Eye, 20 Inch FR4 Input Channel (TP3 from Figure 7)

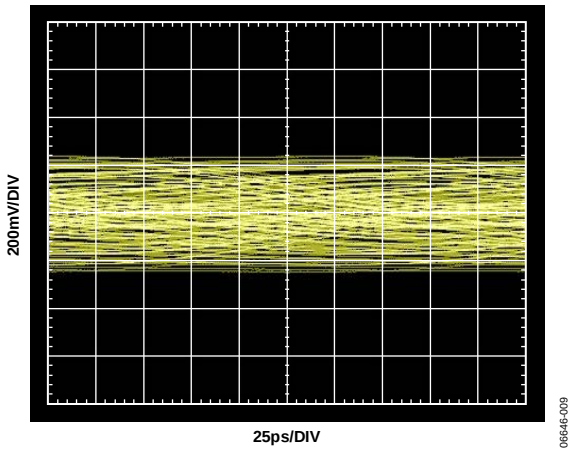


Figure 9. 6.5 Gbps Input Eye, 40 Inch FR4 Input Channel (TP2 from Figure 7)

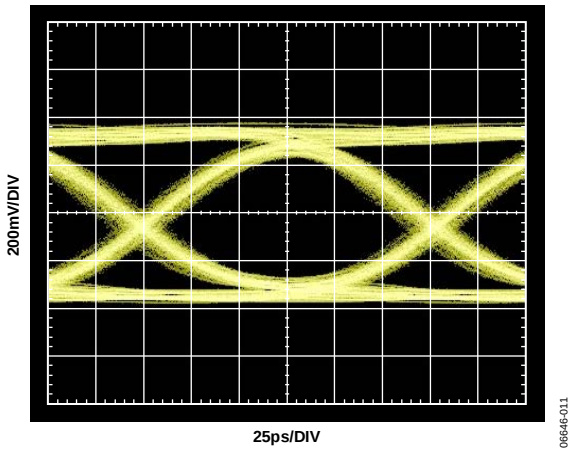


Figure 11. 6.5 Gbps Output Eye, 40 Inch FR4 Input Channel (TP3 from Figure 7)

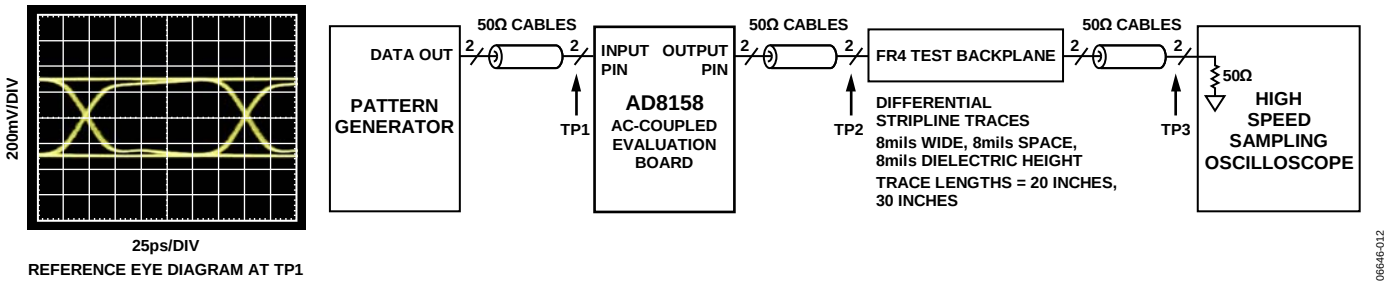


Figure 12. Output Pre-emphasis Test Circuit

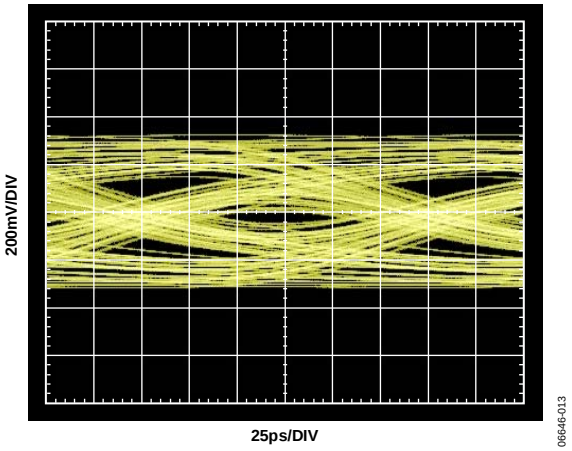


Figure 13. 6.5 Gbps Output Eye, 20 Inch FR4 Input Channel, PE = 0 (TP3 from Figure 12)

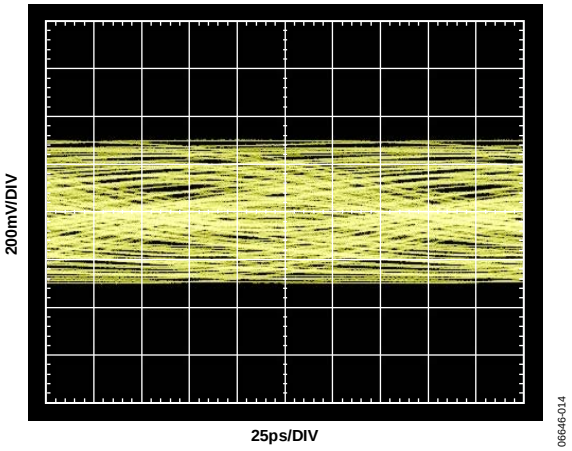


Figure 14. 6.5 Gbps Output Eye, 30 Inch FR4 Input Channel, PE = 0 (TP3 from Figure 12)

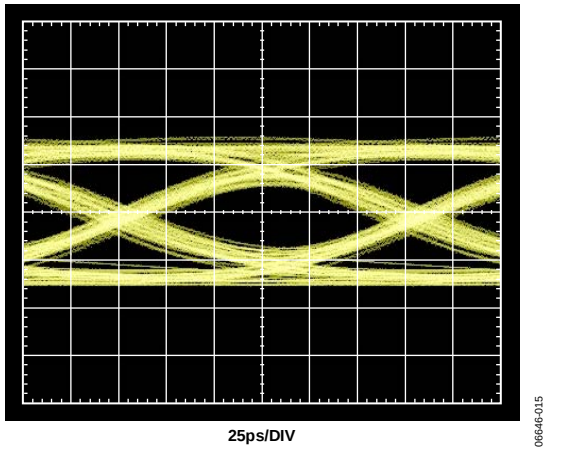


Figure 15. 6.5 Gbps Output Eye, 20 Inch FR4 Input Channel, PE = Best Setting, Default Output Level (TP3 from Figure 12)

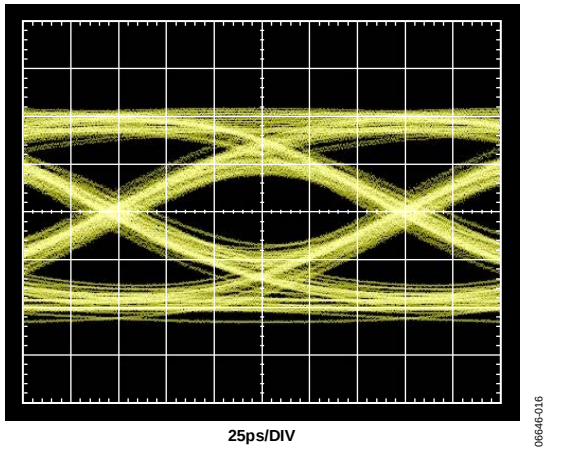


Figure 16. 6.5 Gbps Output Eye, 30 Inch FR4 Input Channel, PE = Best Setting, 200 mV Output Level (TP3 from Figure 12)

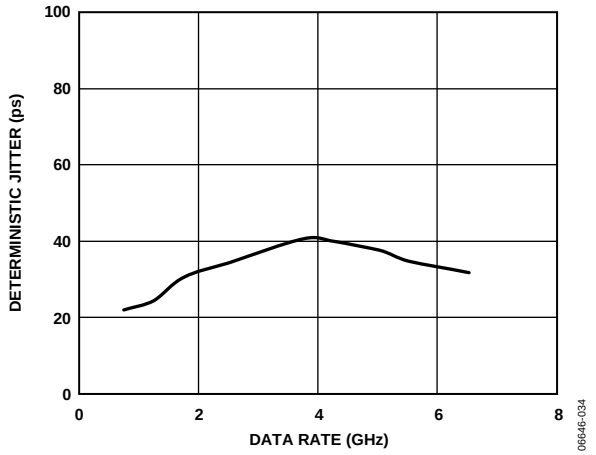


Figure 17. Deterministic Jitter vs. Data Rate

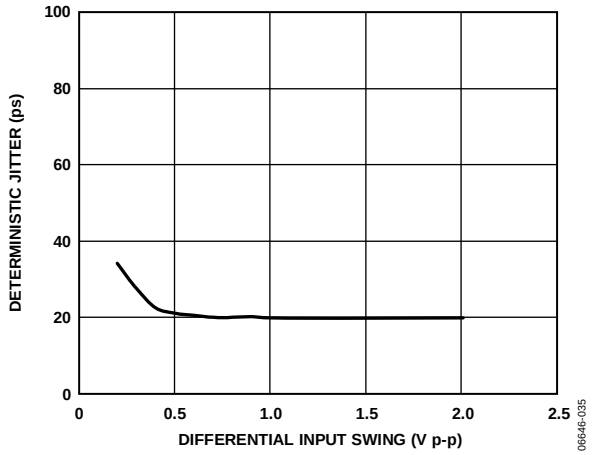


Figure 18. Deterministic Jitter vs. Input Swing

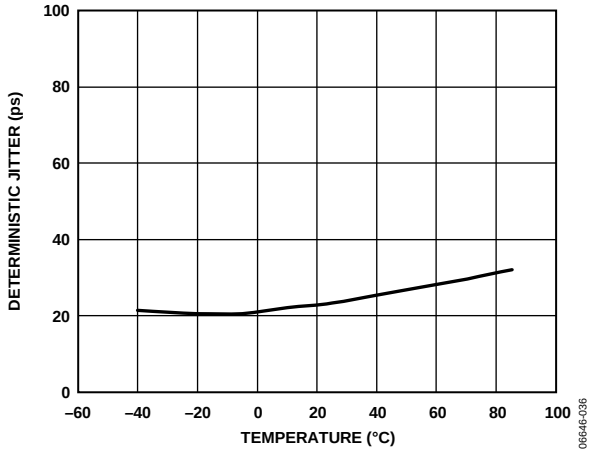


Figure 19. Deterministic Jitter vs. Temperature

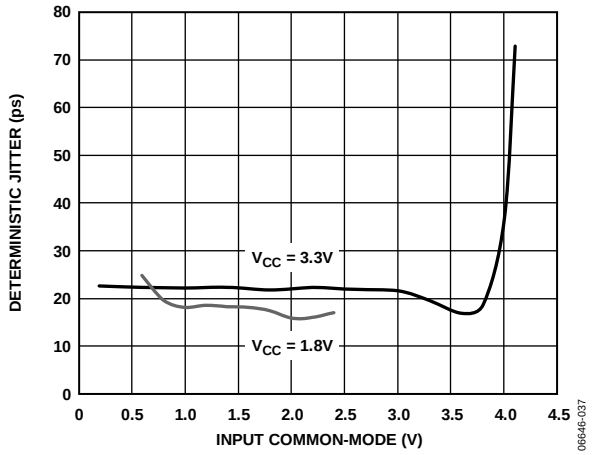


Figure 20. Deterministic Jitter vs. Input Common Mode

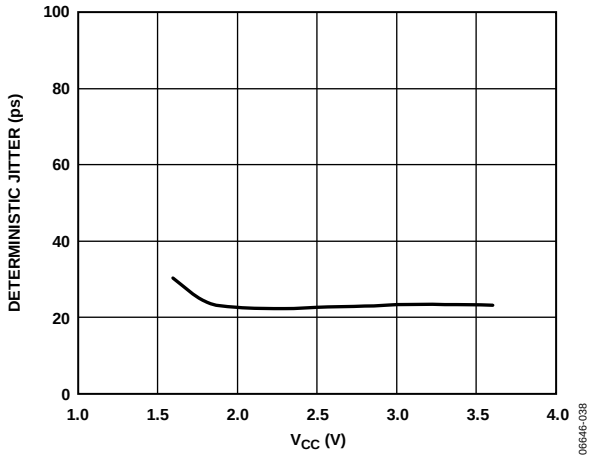


Figure 21. Deterministic Jitter vs. V_{CC}

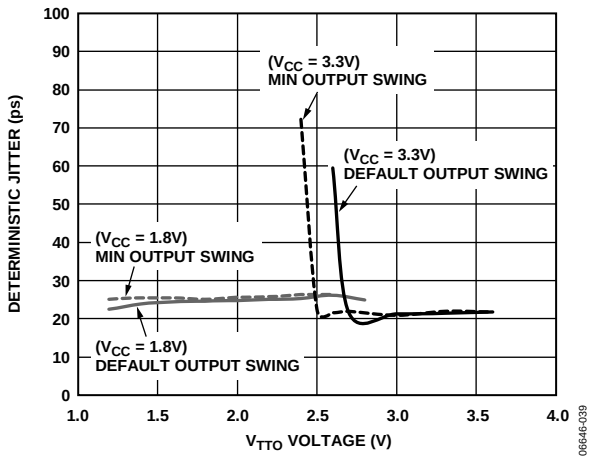


Figure 22. Deterministic Jitter vs. Output Termination Voltage (V_{TTO})

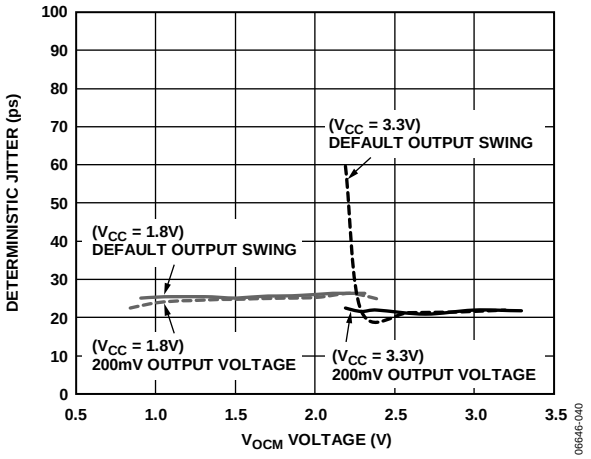


Figure 23. Deterministic Jitter vs. Output Common-Mode Voltage (V_{OCM})

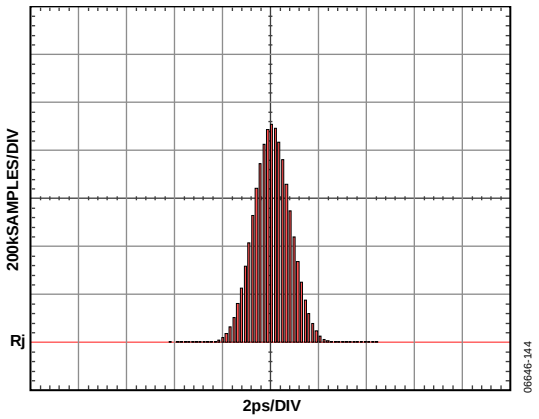


Figure 24. Random Jitter Histogram

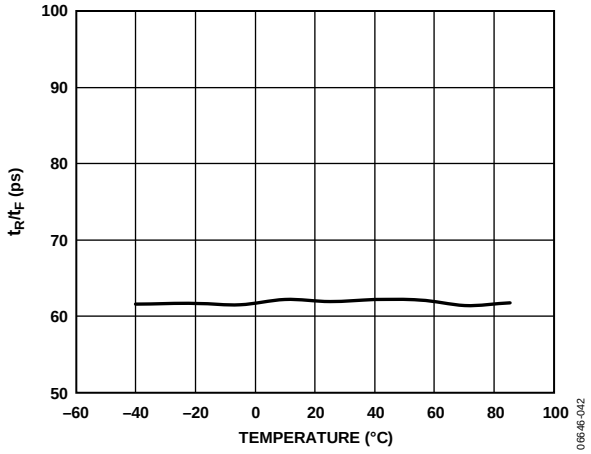


Figure 25. t_R/t_F vs. Temperature

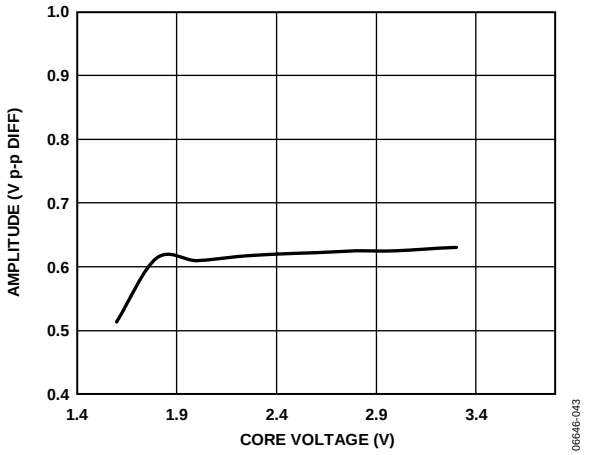


Figure 26. Output Amplitude (Default Setting) vs. V_{CC}

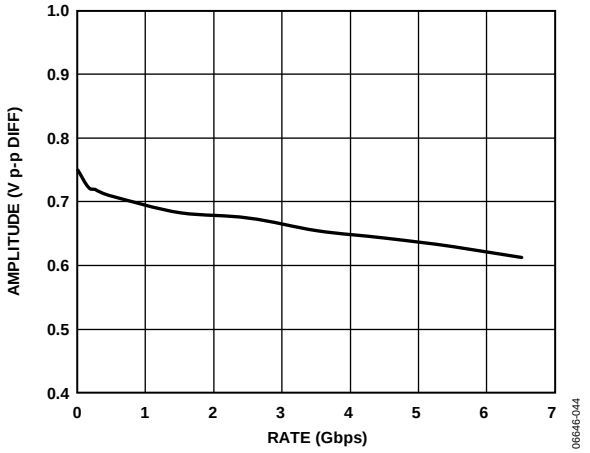


Figure 27. Output Amplitude vs. Rate

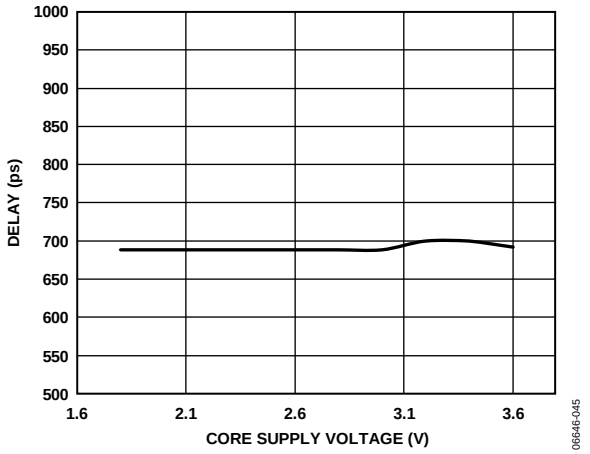


Figure 28. Propagation Delay vs. Core Supply

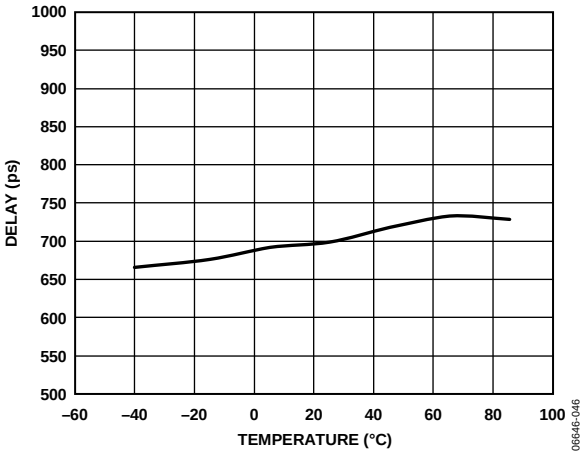


Figure 29. Propagation Delay vs. Temperature

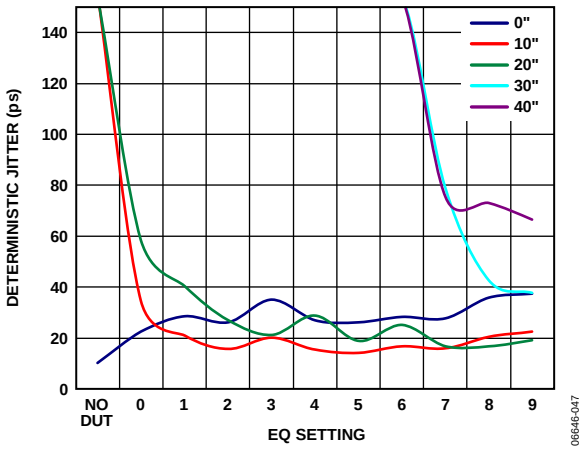


Figure 30. Deterministic Jitter vs. EQ Setting

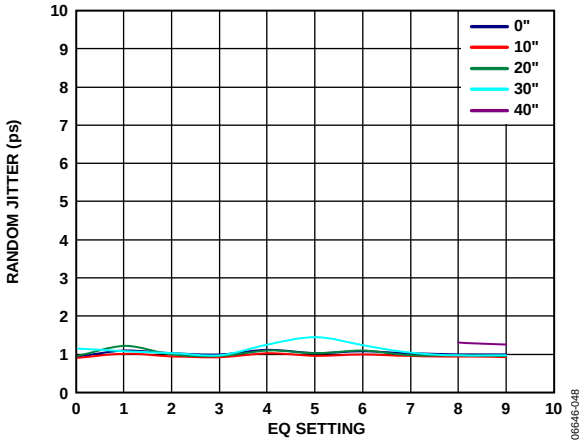


Figure 31. Random Jitter vs. EQ Setting vs. Trace

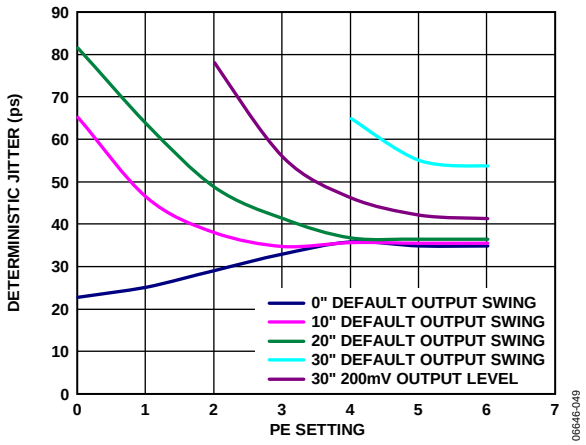


Figure 32. Deterministic Jitter vs. PE Setting

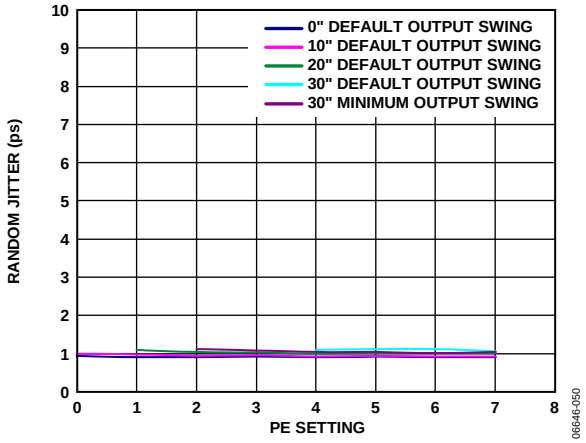


Figure 33. Random Jitter vs. PE Setting

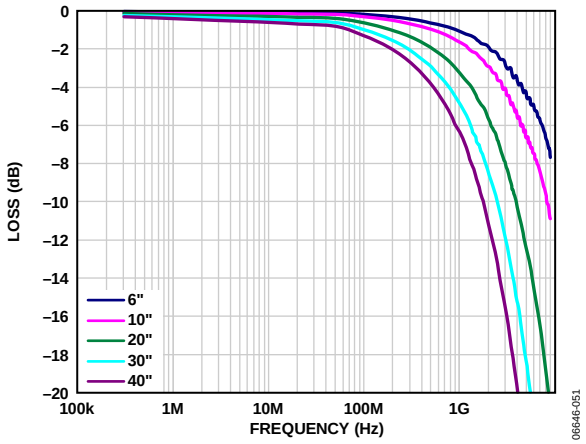


Figure 34. S21 Test Traces

THEORY OF OPERATION

The AD8158 is a buffered, asynchronous, three-port transceiver that allows 2:1 multiplexing and 1:2 demultiplexing among its ports. The 1:2 demux path supports bicast operation, allowing the AD8158 to operate as a port replicator as well as a redundancy switch. The AD8158 offers loopback on each lane, allowing the part to be configured as a twelve-lane equalizer or redriver with FFE.

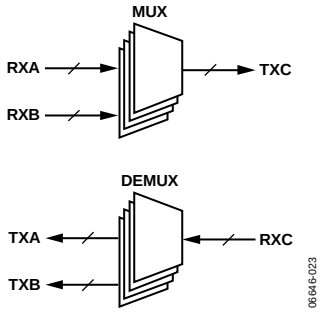


Figure 35. Mux/Demux Paths, Port A to Port C

The part offers extensively programmable transmit output levels and preemphasis settings as well as squelch or full disable. The receivers integrate a programmable, multizero transfer function for aggressive equalization and a programmable loss-of-signal feature. The AD8158 provides a balanced, high speed switch core that maintains low lane-to-lane skew while preserving edge rates.

The I/O on-chip termination resistors are tied to user-settable supplies for increased flexibility. The AD8158 supports a wide primary supply range; V_{CC} can be set from 1.8 V to 3.3 V. These features, together with programmable transmitter output levels, allow for a wide range of dc- and ac-coupled I/O configurations.

The AD8158 supports several control and configuration modes, shown in Table 5. The pin control mode offers access to a subset of the total feature list but allows for a much simplified control scheme. Table 6 compares the features in all control modes.

The primary advantage of using the serial control interface is that it allows finer resolution in setting receive equalization, transmitter preemphasis, loss-of-signal (LOS) behavior, and output levels.

By default, the AD8158 starts in the pin control mode. Strobing the RESETb pin sets all on-chip registers to their default values and uses pins to configure switch connectivity, PE, and EQ levels. In mixed mode, switch connectivity is still controlled through the SEL[3:0], LB_[A:C], and BICAST pins. The user can override PE and EQ settings in mixed mode. In serial mode, all functions are accessed through registers and the control pin inputs are ignored, except RESETb.

The AD8158 register set is controlled through a 2-wire I^2C interface. The AD8158 acts only as an I^2C slave device. The 7-bit slave address for the AD8158 I^2C interface contains the static value b1010 for the upper four bits. The lower three bits are controlled by the input pins, I2C_A[2:0].

Table 5. Control Interface Mode Register

Address	Default	Register Name	Bit	Bit Name	Functionality Description
0x0F	0x00	Control interface mode	7:2	Reserved	Set to 0.
			1:0	Mode[1:0]	00: toggle pin control. Asynchronous control through toggle pins only. 10: mixed control. Switch configuration via toggle pins, register-based control through the I^2C serial interface. 11: serial control. Register-based control through the I^2C serial interface.

Table 6. Features Available Through Toggle Pin or Serial Control

Feature	Pin Control	Serial Control
Switch Features		
BICAST	One pin	One bit
A/B Lane Select	Two pins	Two bits
Loopback	Three pins	Three bits
Speed Select (SEL4G)	One pin	One bit
Rx Features		
EQ Levels	Four settings	10 settings
N/P Swap	Not available	Available
Squelch	Enabled	Three bits
Tx Features		
Programmable Output Levels	±400 mV diff fixed[1]	±200 mV diff/±300 mV diff/±400 mV diff/±600 mV diff
PE Levels	Two settings	>7 settings

[1] ±400 mV diff indicates a 400 mV amplitude signal measured between two differential nodes. The voltage swing at differential I/O pins is described in this data sheet both in terms of the differentially measured voltage range (±400 mV diff, for example) and in terms of peak-to-peak differential swing, denoted as mV p-p diff. An output level setting of ±400 mV diff delivers a differential peak-to-peak output voltage of 800 mV p-p diff.

THE SWITCH (MUX/DEMUX/UNICAST/BICAST/LOOPBACK)

The mux and demux functions of the AD8158 can be controlled either with the toggle pins or through the register map. The multiplexer path switches received data from Input Port A or Input Port B to Output Port C. The SEL[3:0] pins allow switching lanes independently. The demultiplexer path switches received data from Input Port C to Output Port A, Output Port B, or (if bicast mode is enabled) to both Output Port A and Output Port B.

Table 7. Port Selection and Configuration with All Loopbacks Disabled

BICAST	SELx	Output Port A	Output Port B	Output Port C
0	0	Ix_C[3:0]	Idle	Ix_A[3:0]
0	1	Idle	Ix_C[3:0]	Ix_B[3:0]
1	0	Ix_C[3:0]	Ix_C[3:0]	Ix_A[3:0]
1	1	Ix_C[3:0]	Ix_C[3:0]	Ix_B[3:0]

When the device is in unicast mode, the output lanes on either Port A or Port B are in an idle state. In the idle state, the transmitter output current is set to 0, and the P and N sides of the lane are pulled up to the output termination voltage through the on-chip termination resistors. To save power, the unused receiver automatically disables.

The AD8158 supports port-level loopback, illustrated in Figure 36. The loopback control pins override the lane select (SEL[3:0]) and bicast control (BICAST) pin settings at the port level. In serial control mode, Bits [6:4] of Register 0x01 control loopback and are equivalent to asserting Pin LB_A, Pin LB_B, and Pin LB_C. Table 8 summarizes the different loopback configurations.

The loopback feature is useful for system debug, self-test, and initialization, allowing system ASICs to compare Tx and Rx data sent over a single bidirectional link. Loopback can also be used to configure the device as a four- to 12-lane receive equalizer or backplane redriver.

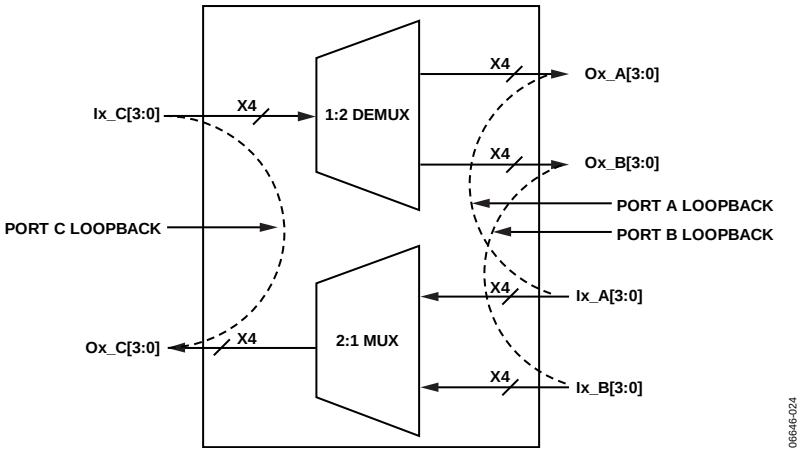


Figure 36. Port-Level Loopback

Table 8. Switch Connectivity vs. Loopback, BICAST, and Port Select Settings

LB_A	LB_B	LB_C	BICAST	SEL[3:0]	Output Port A	Output Port B	Output Port C
0	0	0	0	0000	Ix_C[3:0]	Idle	Ix_A[3:0]
0	0	0	0	1111	Idle	Ix_C[3:0]	Ix_B[3:0]
0	0	0	1	0000	Ix_C[3:0]	Ix_C[3:0]	Ix_A[3:0]
0	0	0	1	1111	Ix_C[3:0]	Ix_C[3:0]	Ix_B[3:0]
0	0	1	0	0000	Ix_C[3:0]	Idle	Ix_C[3:0]
0	0	1	0	1111	Idle	Ix_C[3:0]	Ix_C[3:0]
0	0	1	1	0000	Ix_C[3:0]	Ix_C[3:0]	Ix_C[3:0]
0	0	1	1	1111	Ix_C[3:0]	Ix_C[3:0]	Ix_C[3:0]
0	1	0	0	0000	Ix_C[3:0]	Ix_B[3:0]	Ix_A[3:0]
0	1	0	0	1111	Idle	Ix_B[3:0]	Ix_B[3:0]
0	1	0	1	0000	Ix_C[3:0]	Ix_B[3:0]	Ix_A[3:0]
0	1	0	1	1111	Ix_C[3:0]	Ix_B[3:0]	Ix_B[3:0]
0	1	1	0	0000	Ix_C[3:0]	Ix_B[3:0]	Ix_C[3:0]
0	1	1	0	1111	Idle	Ix_B[3:0]	Ix_C[3:0]
0	1	1	1	0000	Ix_C[3:0]	Ix_B[3:0]	Ix_C[3:0]
0	1	1	1	1111	Ix_C[3:0]	Ix_B[3:0]	Ix_C[3:0]
1	0	0	0	0000	Ix_A[3:0]	Idle	Ix_A[3:0]
1	0	0	0	1111	Ix_A[3:0]	Ix_C[3:0]	Ix_B[3:0]
1	0	0	1	0000	Ix_A[3:0]	Ix_C[3:0]	Ix_A[3:0]
1	0	0	1	1111	Ix_A[3:0]	Ix_C[3:0]	Ix_B[3:0]
1	0	1	0	0000	Ix_A[3:0]	Idle	Ix_C[3:0]
1	0	1	0	1111	Ix_A[3:0]	Ix_C[3:0]	Ix_C[3:0]
1	0	1	1	0000	Ix_A[3:0]	Ix_C[3:0]	Ix_C[3:0]
1	0	1	1	1111	Ix_A[3:0]	Ix_C[3:0]	Ix_C[3:0]
1	1	0	0	0000	Ix_A[3:0]	Ix_B[3:0]	Ix_A[3:0]
1	1	0	0	1111	Ix_A[3:0]	Ix_B[3:0]	Ix_B[3:0]
1	1	0	1	0000	Ix_A[3:0]	Ix_B[3:0]	Ix_A[3:0]
1	1	0	1	1111	Ix_A[3:0]	Ix_B[3:0]	Ix_B[3:0]
1	1	1	0	0000	Ix_A[3:0]	Ix_B[3:0]	Ix_C[3:0]
1	1	1	0	1111	Ix_A[3:0]	Ix_B[3:0]	Ix_C[3:0]
1	1	1	1	0000	Ix_A[3:0]	Ix_B[3:0]	Ix_C[3:0]
1	1	1	1	1111	Ix_A[3:0]	Ix_B[3:0]	Ix_C[3:0]

RECEIVERS

The AD8158 receivers incorporate 50 Ω on-chip termination, ESD protection, and a multizero equalization function capable of delivering up to 18 dB of boost at 4.25 GHz. The AD8158 can compensate signal degradation at 6.5 Gbps from over 40 inches of FR4 backplane trace. The receive path also incorporates a loss-of-signal (LOS) function that squelches the associated transmitter when the midband differential voltage falls below a specified threshold value. Finally, the receivers implement a sign-swapping option (P/N swap), which allows the user to invert the sign of the input signal path and eliminates the need for board-level crossovers in the receive channels.

Input Structure and Allowed Input Levels

The AD8158 tolerates an input common-mode range (measured with zero differential input) of

$$V_{EE} + 0.6\ V < V_{ICM} < V_{CC} + 0.3\ V$$

Typical supply configurations include, but are not limited to, those listed in Table 9.

Table 9. Typical Input Supply Configurations

Configuration	DV_{CC}	V_{CC}	V_{TTI}
Low V_{TTI}, AC-Coupled Input	3.3 V – 1.8 V	1.8 V	1.6 V
Single 1.8 V Supply	3.3 V – 1.8 V	1.8 V	1.8 V
3.3 V Core	3.3 V	3.3 V	1.8 V
Single 3.3 V Supply	3.3 V	3.3 V	3.3 V

When dc-coupling with LVDS, CML, or ECL signals, it can be advantageous to operate with split or negative supplies (see the Applications Information section). In these applications, it is necessary to observe the maximum voltage ratings between V_{CC} and V_{EE} and to select supply voltages for V_{TTO} and V_{TTI} in the range of V_{CC} to V_{EE} to avoid activating the ESD protection devices.

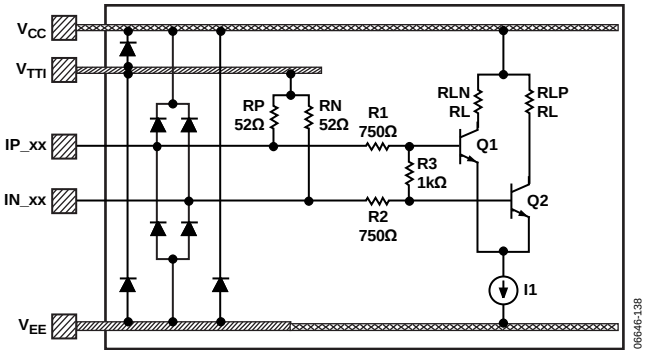


Figure 37. Simplified Receiver Input Structure

Equalizer Settings

Every input lane offers a low power, asynchronous, programmable receive equalizer for NRZ data up to 6.5 Gbps. The pin control interface allows two levels of receive equalization. Register-based control allows the user 10 equalizer settings. Register and pin control boost settings are listed in Table 10. Equalization capability and resulting jitter performance are illustrated in Figure 30, Figure 31, and Figure 34. Figure 34 shows the loss characteristic of various reference channels, and Figure 30 and Figure 31 show resulting DJ and RJ performance vs. equalizer setting against these channels.

The four LSBs of Register 0x41, Register 0x81, and Register 0xC1 allow programming of all the equalizers in a port simultaneously (see Table 13). The 0x42, 0x82, and 0xC2 registers allow per-lane programming of the equalizers (see Table 22). Be aware that writing to the port-level equalizer registers updates and overwrites per-lane settings.

Table 10. Equalizer Settings

Equalization Boost (dB)	EQ Register Setting	EQ[1:0] Pins
0	0	00
2	1	N/A
4	2	01
6	3	N/A
8	4	10
10	5	N/A
12	6	N/A
14	7	N/A
16	8	N/A
18	9	11

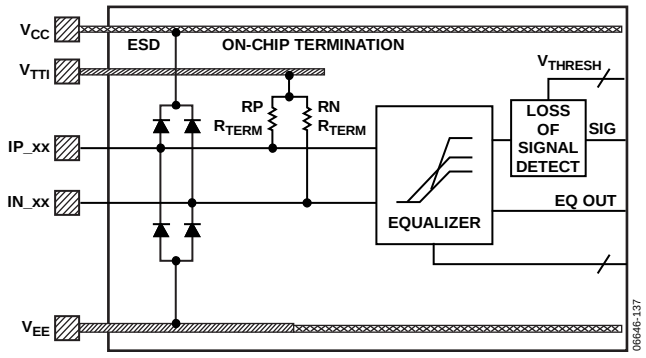


Figure 38. Functional Diagram of the AD8158 Receiver

Lane Disables

By default, the receivers and transmitters enable in an on-demand fashion according to the state of the SEL[3:0], LB_[A:C], and BICAST pins or to the state of the equivalent registers in serial control mode. Register 0x40, Register 0x80, and Register 0xC0 implement per-lane disables for the receivers, and Register 0x48, Register 0x88, and Register 0xC8 implement per-lane transmitter disables. These disables override the default settings. Each bit in the register is named for the lane and function it disables. For example, RXDIS B0 disables the receiver on Lane 0 of Port B whereas TXDIS C1 disables the Lane 1 transmitter of Port C (see Table 11).

Lane Inversion: P/N Swap

The receiver P/N swap function is a convenience intended to allow the user to implement the equivalent of a board-level routing crossover in a much smaller area while eliminating vias (impedance discontinuities) that compromise the high frequency integrity of the signal path. Using this feature to correct an inversion downstream of the receiver may require the user to be aware of the sign of the data when switching connectivity (the mux/demux path). The feature is available on a per-lane setting through Register 0x44, Register 0x84, and Register 0xC4. Setting the bit true flips the sign sense of the P and N inputs for the associated lane. The default setting is 0 (no inversion).

Table 11. Per-Lane Disables

Address	Port	Default	Register Name	Bit	Bit Name	Functionality Description
0x40	Port A	0x00	RX[A/B/C] disable	7:4	Reserved	Set to 0
0x80	Port B	0x00		3	RXDIS [A/B/C]3	0: RX Port [A/B/C], Lane 3, enabled
						1: RX Port [A/B/C], Lane 3, disabled
0xC0	Port C	0x00		2	RXDIS [A/B/C]2	0: RX Port [A/B/C], Lane 2, enabled
						1: RX Port [A/B/C], Lane 2, disabled
				1	RXDIS [A/B/C]1	0: RX Port [A/B/C], Lane 1, enabled
						1: RX Port [A/B/C], Lane 1, disabled
				0	RXDIS [A/B/C]0	0: RX Port [A/B/C], Lane 0, enabled
						1: RX Port [A/B/C], Lane 0, disabled
0x48	Port A	0x00	TX[A/B/C] disable	7:4	Reserved	Set to 0
0x88	Port B	0x00		3	TXDIS [A/B/C]3	0: TX Port [A/B/C], Lane 3 enabled
						1: TX Port [A/B/C], Lane 3 disabled
0xC8	Port C	0x00		2	TXDIS [A/B/C]2	0: TX Port [A/B/C], Lane 2 enabled
						1: TX Port [A/B/C], Lane 2 disabled
				1	TXDIS [A/B/C]1	0: TX Port [A/B/C], Lane 1, enabled
						1: TX Port [A/B/C], Lane 1, disabled
				0	TXDIS [A/B/C]0	0: TX Port [A/B/C], Lane 0, enabled
						1: TX Port [A/B/C], Lane 0, disabled

Table 12. Lane Inversion

Address	Port	Default	Register Name	Bit	Bit Name	Functionality Description
0x44	Port A	0x00	RX[A/B/C] P/N swap	7:4	Reserved	Set to 0
0x84	Port B	0x00		3	PN[A/B/C]3	0: Lane 3 noninverted
						1: Lane 3 inverted
0xC4	Port C	0x00		2	PN[A/B/C]2	0: Lane 2 noninverted
						1: Lane 2 inverted
				1	PN[A/B/C]1	0: Lane 1, noninverted
						1: Lane 1, inverted
				0	PN[A/B/C]0	0: Lane 0, noninverted
						1: Lane 0, inverted

Table 13. Port-Level EQ Setting

Address	Port	Default	Register Name	Bit	Bit Name	Functionality Description
0x41	Port A	0x00	RX[A/B/C] EQ setting	7:4	Reserved	Set to 0
0x81	Port B	0x00		3:0	[A/B/C]EQ[3:0]	
0xC1	Port C	0x00				

LOSS OF SIGNAL (LOS)

The serial control interface allows access to the AD8158 loss-of-signal features (LOS is not available in pin control mode). Each receiver includes a low power, loss-of-signal detector. The loss-of-signal circuit monitors the received data stream and generates a system interrupt when the received signal power falls below a fixed threshold. The threshold is 50 mV p-p diff, referred to the input pins. The LOS circuit monitors the equalized receive waveform and integrates the rms power of the equalized waveform over a selectable interval of either 2 ns or 10 ns. The detectors are enabled on a per-port basis with Bit 0 of the RXA/B/C LOS control registers (0x51, 0x91, 0xD1).

By default, when the receiver detects an LOS event, it squelches its associated transmitter, lowering the output current to submicroamps. This prevents the high gain, wide bandwidth signal path from turning low level system noise on an undriven input pair into a source of hostile crosstalk at the transmitter.

The squelch feature can be disabled with Bit 3 of the global squelch control register (0x04).

The LOS_INT pin evaluates a logical OR of all LOS status register bits for all enabled receivers (LOS status registers are located at 0x45, 0x85, and 0xC5). The upper two bits in the RXA, RXB, and RXC LOS status registers are sticky, whereas the two LSBs are continuously updated to indicate the instantaneous status of LOS for an enabled receiver. The sticky bits are cleared by writing 0 to the RXA, RXB, and RXC LOS status registers. The LOS_INT pin remains high after an LOS event until all sticky registers are cleared and all active status registers (for example, Bits[3:0]) read 0.

The LOS_INT pin can be used to generate an interrupt for the system control software. In a standard implementation, when LOS_INT goes high, the system software registers the interrupt and polls the RXA, RXB, and RXC LOS status registers to determine which input lost signal and whether the signal has been restored.

Table 14. Global Loss-of-Signal Squelch Control Register

Address	Default	Register Name	Bit	Bit Name	Functionality Description
0x04	0x0F	Global Squelch Ctrl	7:4	Reserved	Set to 0
			3	GSQLCH_ENB	0: LOS auto squelch disabled 1: LOS auto squelch enabled
			2:0	Reserved	Set to 1

Table 15. Port-Level Loss-of-Signal Control Registers

Address	Port	Default	Register Name	Bit	Bit Name	Functionality Description
0x51	Port A	0x05	RX[A/B/C] LOS control	7:3	Reserved	Set to 0
0x91	Port B	0x05		2	LOS_FILT	0: LOS filter time constant = 2 ns 1: LOS filter time constant = 10 ns
0xD1	Port C	0x05		1	Reserved	Set to 0
				0	LOS_ENB	0: LOS disabled 1: LOS enabled

Table 16. Port-Level Loss-of-Signal Status Registers

Address	Port	Default	Register Name	Bit	Bit Name	Functionality Description
0x45 0x85 0xC5	Port A Port B Port C	Read only Write 0 to clear	RX[A/B/C] LOS status	7:4	LOS[A/B/C][3:0] sticky	0000: LOS event has not occurred. 0001: LOS event has occurred on Lane 0. 0010: LOS event has occurred on Lane 1. 0100: LOS event has occurred on Lane 2. 1000: LOS event has occurred on Lane 3. 1111: LOS event has occurred on all lanes.
				3:0	LOS[A/B/C][3:0] active	0000: active signals on all lanes. 0001: inactive signal on Lane 0. 0010: inactive signal on Lane 1. 0100: inactive signal on Lane 2. 1000: inactive signal on Lane 3. 1111: inactive signals on all lanes.

TRANSMITTERS

The AD8158 transmitter offers programmable preemphasis, programmable output levels, output disable, and transmit squelch. The SEL4G pin lets the user lower the transmitter frequency of maximum boost from 3.25 GHz to 2.0 GHz, allowing the AD8158 to offer exceptional transmit channel compensation for legacy applications (4.5 Gbps and slower).

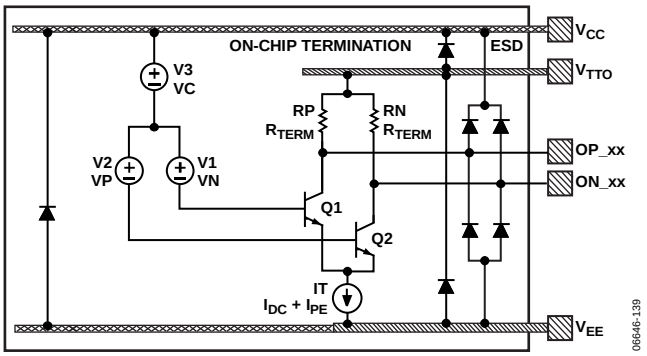


Figure 39. Simplified Transmitter Structure

Output Level Programming and Output Structure

The output level of the transmitter of each lane is independently programmable. In pin control mode, a default output amplitude of 800 mV p-p diff (±400 mV diff) is delivered (see Table 17). Register-based control allows the user to set the transmitter output levels on a per-port or per-lane basis to four predefined levels. Port-level programming overwrites lane-level configuration. The ALEV, BLEV, and CLEV bits in Register 0x49, Register 0x89, and Register 0xC9, respectively, are used to set the output levels for all transmitters. The A[3:0]OLEV[1:0], B[3:0]OLEV[1:0], and C[3:0]OLEV[1:0] bits in Register 0x4C, Register 0x8C, and Register 0xCC allow per-lane settings (see Table 22).

Table 17. Predefined Output Levels

[A/B/C][3:0]OLEV[1]	[A/B/C][3:0]OLEV[0]	Output Level
0	0	±200 mV diff
0	1	±300 mV diff
1	0	±400 mV diff (default)
1	1	± 600 mV diff

Note that the choice of output level influences the output common-mode level. A 600 mV diff output level with a full PE range requires a supply and output termination voltage of 2.5 V or higher (V_{TTO}, $V_{CC} \geq 2.5$ V).

Preemphasis

Transmitter preemphasis levels can be set by pin control or through the control registers. Pin control allows two settings of PE, 0 dB and 6 dB. The control registers provide seven levels of PE. Note that a larger range of boost settings is available for lower output levels. Note that toggle pin control of PE is limited to the 400 mV diff output level settings. Table 18 lists the available preemphasis settings for each output level.

Preemphasis can be programmed per port or per lane. Register 0x49, Register 0x89, and Register 0xC9 set all outputs in a port at once. Registers 0x4A, 0x8A, and 0xCA allow setting PE on a per-lane basis. The following equation sets preemphasis boost:

$$Gain[dB] = 20 \times \log_{10}(1 + \frac{V_{SW-PE} - V_{SW-DC}}{V_{SW-DC}}) \quad (1)$$

Table 18. Setting Transmitter Preemphasis

Output Level (mV diff)	Pin PE_[A/B/C]	Bit PE[2:0]	PE Boost (%)	PE Boost (dB)
200	N/A	000	0	0
200	N/A	001	50	3.52
200	N/A	010	100	6.02
200	N/A	011	150	7.96
200	N/A	100	200	9.54
200	N/A	101	250	10.88
200	N/A	110	300	12.04
300	N/A	000	0	0
300	N/A	001	33	2.5
300	N/A	010	67	4.44
300	N/A	011	100	6.02
300	N/A	100	133	7.36
300	N/A	101	167	8.52
300	N/A	110	200	9.54
400	0	000	0	0
400	N/A	001	25	1.94
400	N/A	010	50	3.52
400	N/A	011	75	4.86
400	1	100	100	6.02
400	N/A	101	125	7.04
400	N/A	110	150	7.96
600	N/A	000	0	0
600	N/A	001	17	1.34
600	N/A	010	33	2.5
600	N/A	011	50	3.52
600	N/A	100	67	4.44
600	N/A	101	83	5.26
600	N/A	110	100	6.02

Squelch and Disable

Each transmitter is equipped with disable and squelch controls. Disable is a full power-down state: the transmitter current is reduced to zero and the output pins pull up to V_{TTO}, but there is a delay of approximately 1 µs associated with reenabling the transmitter. Squelch keeps the output current enabled such that both output pins are at the output common-mode voltage. The transmitter recovers from squelch in less than 64 ns.

Speed Select

The SEL4G pin lets the user lower the transmitter frequency of maximum boost from 3.25 GHz to 2.0 GHz, allowing the AD8158 to offer exceptional transmit channel compensation for legacy applications (4.5 Gbps and slower). SEL4G = 1 lowers the

frequency of maximum boost without sacrificing the amount of boost delivered.

AD8158 POWER CONSUMPTION

There are several sections of the AD8158 that draw varying power depending on the supply voltages, the type of I/O coupling used, and the status of the AD8158 operation. Figure 40 shows a block diagram of these sections.

The first section consists of the input termination resistors. The power dissipated in the termination resistors is due to the input differential swing and any common-mode current resulting from dc-coupling the input.

In the next section (the receiver section), each input is powered only when it is selected, and the disable bits are set to 0. If a receiver is not selected, it is powered down. Thus, the total number of active inputs affects the total power consumption. Furthermore, the loss-of-signal detection circuits can be disabled independent of the receiver for even greater power savings.

The core of the device performs the multiplexer and demultiplexer switching functions. It draws a fixed quiescent current of 2 mA whenever the AD8158 is powered from V_{CC} to V_{EE}. The switch draws an additional 8 × 4.6 mA in normal mux/demux operation and an additional 12 × 4.6 mA with all ports in loopback or with bicast selected. The switch core can be disabled to save power.

An output predriver section draws a current, I_{PRED}, that is related to the programmed output current, I_{TTO}. The predriver current always flows from V_{CC} to V_{EE}. It is treated separately from the output current, which flows from V_{TTO} and may not be the same voltage as V_{CC}.

The final section is the outputs section. For an individual output, the programmed output current flows through two separate paths. One is the on-chip termination resistor, and the other is the transmission line and the destination termination resistor. The nominal parallel impedance of these two paths is 25 Ω. The sum of these two currents flows through the switches and the current source of the AD8158 output circuit and out through V_{EE}. The power dissipated in the transmission line and the destination resistor is not dissipated in the AD8158 but must be supplied from the power supply and is a factor in overall system power. The current in the on-chip termination resistors and the output current source dissipate power in the AD8158 itself.

Outputs

The output current is set by a combination of output level and preemphasis settings (see Table 19). For the two logic switch states, this current flows through an on-chip termination resistor and a parallel path to the destination device and its termination resistor. The power in this parallel path is not dissipated by the AD8158. With preemphasis enabled, some current always flows in both the P and N termination resistors. This preemphasis current gives rise to an output common-mode shift, which varies with ac-coupling or dc-coupling and which is calculated for both cases in Table 19.

Perhaps the most direct method for calculating power dissipated in the output is to calculate the power that would be dissipated if all of I_{TTO} were to flow on-die from V_{TTO} to V_{EE} and to subtract from this the power dissipated off die in the destination device termination resistors and the channel. For this purpose, the destination device and channel can be modeled as 50 Ω load resistors, R_L, in parallel with the AD8158 termination resistors.

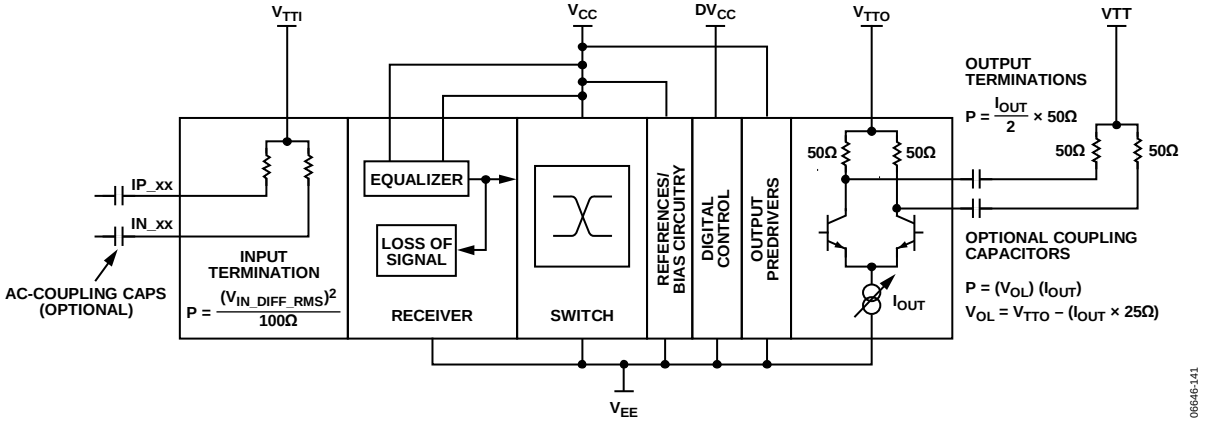


Figure 40. AD8158 Power Distribution Block Diagram

Power Saving Considerations

Whereas the AD8158 power consumption is very low compared to similar devices, careful control of its operating conditions can yield further power savings. Significant power reduction can be realized by operating the part at a lower voltage. Compared to 3.3 V operation, a supply voltage of 1.8 V can result in power savings of ~45%. There is no performance penalty when operting at lower voltage.

A second measure is to disable transmitters when they are not being used. This can be done on a static basis if the output is not used or on a dynamic basis if the output does not have a constant stream of traffic. On transmit disable (Register 0x48, Register 0x88, Register 0xC8), both the predriver and output switch currents are disabled. The LOS-activated squelch disables only the output switch current, I_{TTO}. Superior power saving is achieved by using the TX and RX disable registers to turn off an unused lane as opposed to relying on the AD8158 transmit squelch feature.

Because the majority of the power dissipated is in the output stage, some of its flexibility can be used to lower the power consumption. First, the output current and output preemphasis settings can be programmed to the smallest amount required to maintain BER performance. If an output circuit always has a short length and the receiver has good sensitivity, then a lower output current can be used.

It is also possible to lower the voltage on V_{TTO} to lower the power dissipation. The amount that V_{TTO} can be lowered is dependent on the lowest of all the output's V_{OL} and V_{CC}. This is determined by the output that is operating at the highest programmed output current. Table 1 and Table 19 list minimum output levels.

I²C CONTROL INTERFACE

SERIAL INTERFACE GENERAL FUNCTIONALITY

The AD8158 register set is controlled through a 2-wire I²C interface. The AD8158 acts only as an I²C slave device. The 7-bit slave address for the AD8158 I2C interface contains the static value b1010 for the upper four bits. The lower three bits are controlled by the input pins, I2C_A[2:0].

Therefore, the I²C bus in the system must include an I²C master to configure the AD8158 and other I²C devices that may be on the bus. Data transfers are controlled through the use of the two I²C wires: the SCL input clock pin and the SDA bidirectional data pin.

The AD8158 I²C interface can be run in the standard (100 kHz) and fast (400 kHz) modes. The SDA line changes value only when the SCL pin is low, with two exceptions. To indicate the beginning or continuation of a transfer, the SDA pin is driven low while the SCL pin is high, and to indicate the end of a transfer, the SDA line is driven high while the SCL line is high. Therefore, it is important to control the SCL clock to toggle only when the SDA line is stable unless indicating a start, repeated start, or stop condition.

I²C INTERFACE DATA TRANSFERS: DATA WRITE

To write data to the AD8158 register set, a microcontroller or any other I²C master must send the appropriate control signals to the AD8158 slave device. The following steps must be taken, where the signals are controlled by the I²C master, unless otherwise specified. For a diagram of the procedure, see Figure 41.

1. Send a start condition (while holding the SCL line high, pull the SDA line low).
2. Send the AD8158 part address (seven bits) whose upper four bits are the static value b1010 and whose lower three bits are controlled by the I2C_A[2:0] input pins. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the AD8158 to acknowledge the request.
5. Send the register address (eight bits) to which data is to be written. This transfer should be MSB first.
6. Wait for the AD8158 to acknowledge the request.
7. Send the data (eight bits) to be written to the register whose address was set in Step 5. This transfer should be MSB first.
8. Wait for the AD8158 to acknowledge the request.
9. Do one or more of the following:
   a. Send a stop condition (while holding the SCL line high, pull the SDA line high) and release control of the bus.
   b. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 in this procedure to perform another write.
   c. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of the read procedure (in the I²C Interface Data Transfers: Data Read section) to perform a read from another address.
   d. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 8 of the read procedure (in the I²C Interface Data Transfers: Data Read section) to perform a read from the same address set in Step 5.

In Figure 41, the AD8158 write process is shown. The SCL signal is shown along with a general write operation and a specific example. In this example, the value 0x92 is written to Address 0x6D of an AD8158 device with a part address of 0x53. The part address is seven bits wide and is composed of the AD8158 static upper four bits (b1010) and the pin-programmable lower three bits (I2C_A[2:0]). The address pins are set to b011. In Figure 41, the corresponding step number is visible in the circle under the waveform. The SCL line is driven by the I²C master and never by the AD8158 slave. As for the SDA line, the data in the shaded polygons is driven by the AD8158, whereas the data in the nonshaded polygons is driven by the I²C master. The end phase case shown is that of Step 9a.

It is important to note that the SDA line changes only when the SCL line is low, except for the case of sending a start, stop, or repeated start condition (Step 1 and Step 9 in this case).

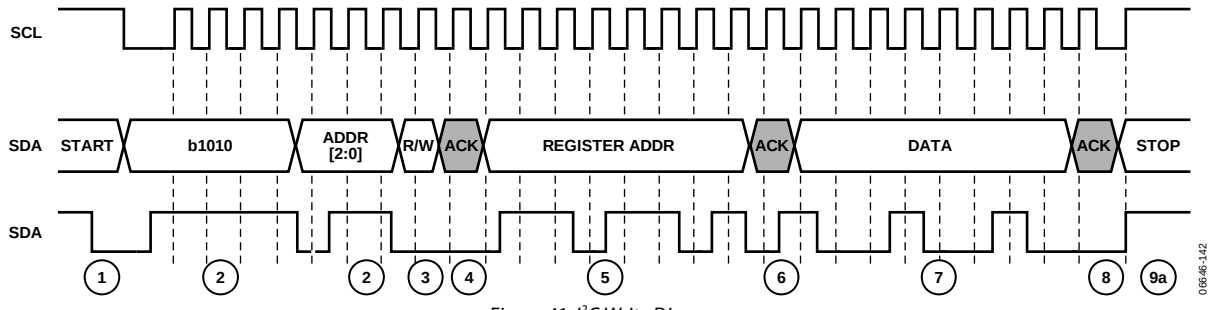


Figure 41. I²C Write Diagram

I²C INTERFACE DATA TRANSFERS: DATA READ

To read data from the AD8158 register set, a microcontroller or any other I²C master must send the appropriate control signals to the AD8158 slave device. The following steps must be taken, where the signals are controlled by the I²C master, unless otherwise specified. For a diagram of the procedure, see Figure 42.

1. Send a start condition (while holding the SCL line high, pull the SDA line low).
2. Send the AD8158 part address (seven bits) whose upper four bits are the static value b1010 and whose lower three bits are controlled by the I2C_A[2:0] input pins. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the AD8158 to acknowledge the request.
5. Send the register address (eight bits) from which data is to be read. This transfer should be MSB first. The register address is kept in memory in the AD8158 until the part is reset or the register address is written over with the same procedure (Step 1 to Step 6).
6. Wait for the AD8158 to acknowledge the request.
7. Send a repeated start condition (while holding the SCL line high, pull the SDA line low).
8. Send the AD8158 part address (seven bits) whose upper four bits are the static value b1010 and whose lower three bits are controlled by the I2C_A[2:0] input pins. This transfer should be MSB first.
9. Send the read indicator bit (1).
10. Wait for the AD8158 to acknowledge the request.
11. The AD8158 then serially transfers the data (eight bits) held in the register indicated by the address set in Step 5.
12. Acknowledge the data.
13. Do one or more of the following:
    a. Send a stop condition (while holding the SCL line high, pull the SDA line high) and release control of the bus.
    b. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of the write procedure (see the I²C Interface Data Transfers: Data Write section) to perform a write.
    c. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of this procedure to perform a read from another address.
    d. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 8 of this procedure to perform a read from the same address.

In Figure 42, the AD8158 read process is shown. The SCL signal is shown along with a general read operation and a specific example. In this example, the value 0x49 is read from Address 0x6D of an AD8158 device with a 0x53 part address. The part address is seven bits wide and is composed of the AD8158 static upper four bits (b1010) and the pin-programmable lower three bits (I2C_A[2:0]). The address pins are set to b011. In Figure 42, the corresponding step number is visible in the circle under the waveform. The SCL line is driven by the I²C master and never by the AD8158 slave. As for the SDA line, the data in the shaded polygons is driven by the AD8158, whereas the data in the nonshaded polygons is driven by the I²C master. The end phase case shown is that of Step 13a.

It is important to note that the SDA line changes only when the SCL line is low, except for the case of sending a start, stop, or repeated start condition, as in Step 1, Step 7, and Step 13. In Figure 42, A is the same as ACK. Equally, Sr represents a repeated start where the SDA line is brought high before SCL is raised. SDA is then dropped while SCL is still high.

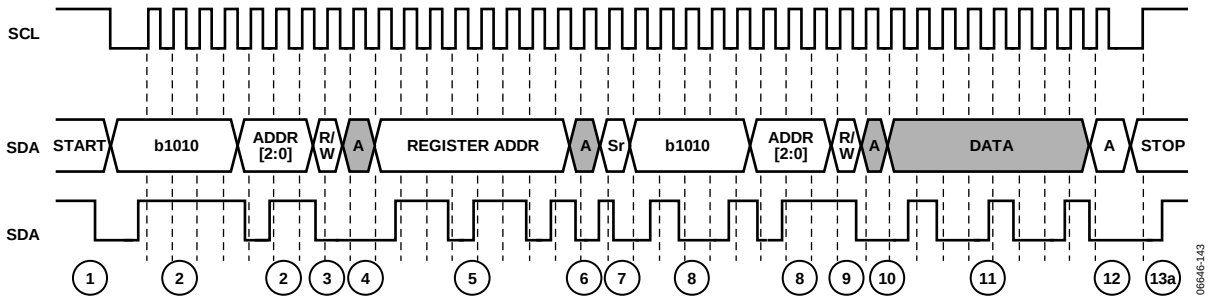


Figure 42. I²C Read Diagram

APPLICATIONS INFORMATION

The main application of the AD8158 is to support redundancy on both the backplane side and the line interface side of a serial link. Each port consists of four lanes to support standards such as XAUI. Figure 43 illustrates redundancy in an XAUI backplane system. Each line card is connected to two switch fabrics (primary and redundant). The device can be configured to support either 1 + 1 or 1:1 redundancy. Also, the AD8158 can enable module redundancy, as shown in Figure 44, and can be used as a four-, eight- or 12-lane signal conditioning device to enable high speed serial communication over long copper links.

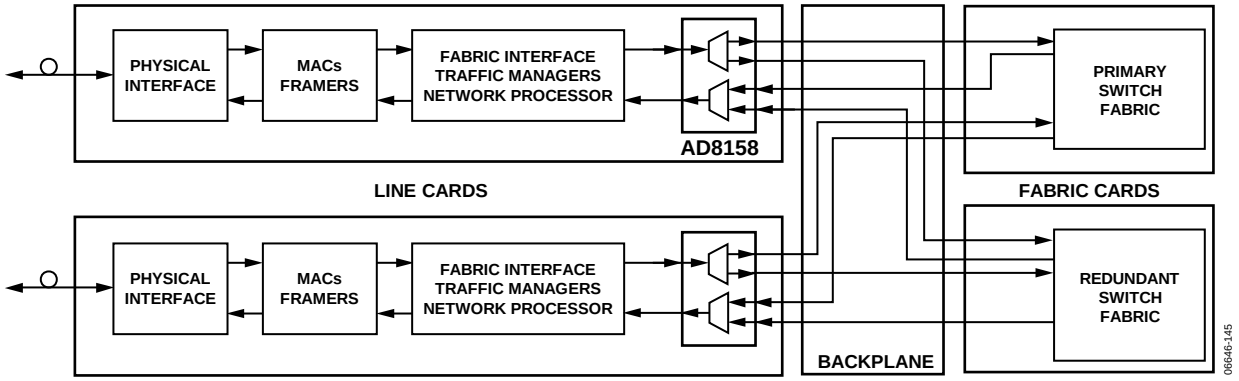


Figure 43. Using the AD8158 for Switch Redundancy

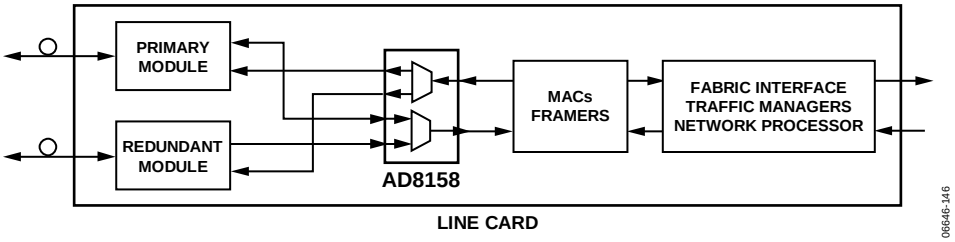


Figure 44. Using the AD8158 for Module Redundancy

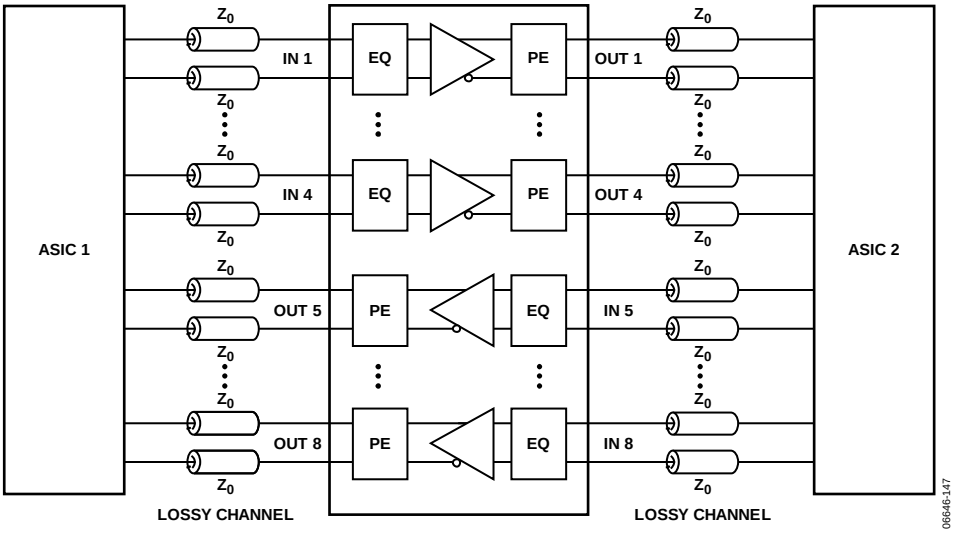


Figure 45. Using the AD8158 for Signal Conditioning

OUTPUT COMPLIANCE

In low voltage applications, users must pay careful attention to both the differential and common-mode signal levels. The choice of output voltage swing, preemphasis setting, supply voltages (V_{CC} and V_{TTO}), and output coupling (ac or dc) affect peak and settled single-ended voltage swings and the common-mode shift measured across the output termination resistors. These choices also affect output current and, consequently, power consumption. For certain combinations of supply voltage and output coupling, output voltage swing and preemphasis settings may violate the single-ended absolute output low voltage, as specified in Table 1. Under these conditions, the performance is degraded; therefore, these settings are not recommended. Table 19 includes annotations that identify these settings.

Table 19 shows the change in output common mode ($\Delta V_{OCM} = V_{CC} - V_{OCM}$) with output level ($V_{SW}$) and preemphasis setting. Table 19 also shows the minimum and maximum peak single-ended output levels ($V_{L\text{-}PE}$ and $V_{H\text{-}PE}$, respectively). The single-ended output levels are calculated for V_{TTO} supplies of 3.3 V and 1.8 V for both ac- and dc-coupled outputs to illustrate the practical challenges of reducing the supply voltage.

TX_HEADROOM

For output levels greater than 400 mV diff (800 mV p-p diff), setting the TX_HEADROOM bit to 1 allows the transmitter an extra 200 mV of output compliance range. When the TX_HEADROOM bit is enabled, a core supply voltage, $V_{CC} \geq 2.5$ V, is required. Enabling TX_HEADROOM increases the core supply current. TX_HEADROOM can be enabled on a per-port basis through Bits[6:4] in Register 0x05. A value of 0 disables the headroom-generating circuitry; a value of 1 enables it.

Example 1: 1.8 V, PE Disabled

Consider a typical application using pin control mode. In this case, the default output level of 400 mV diff (800 mV p-p diff) is selected, and the user can choose preemphasis settings of 0 dB or 6 dB. Table 19 shows that with preemphasis disabled, a dc-coupled transmitter causes a 200 mV common-mode shift across the termination resistors, whereas an ac-coupled transmitter causes twice the common-mode shift. Notice that with V_{CC} and V_{TTO} powered from a 1.8 V supply, the single-ended output voltage swings between 1.8 V and 1.4 V when dc-coupled and between 1.6 V and 1.2 V when ac-coupled. In both cases, these levels are greater than the minimum V_L limit of 725 mV, and V_{CC} satisfies the minimum V_{CC} limit of 1.8 V with the TX_HEADROOM bit set to 0. Note that setting TX_HEADROOM = 1 violates the minimum V_{CC} limit of 2.5 V.

Example 2: 1.8 V, PE = 6 dB

With a PE setting of 6.02 dB, the ac-coupled transmitter has single-ended swings from 1.4 V to 0.6 V, whereas the dc-coupled transmitter outputs swing between 1.8 V and 1 V. The peak minimum single-ended swing ($V_{L\text{-}PE}$) of the ac-coupled transmitter, in this case, exceeds the minimum V_L limit of 725 mV by 125 mV. While theoretically in violation of the specification, in practice, this setting is viable, especially at high data rates. The transmitter theoretical peak voltage is rarely achieved in practice because the high frequency characteristic of the preemphasis is attenuated at the output pins by the low-pass nature of the PC board environment and the channel. For 6.5 Gbps PE (SEL4G = 0), a 30% reduction of overshoot as measured at the PC board is possible. For an output level of 400 mV diff and a PE setting of 6 dB, the user can calculate a maximum overshoot of 400 mV diff but can measure only a 270 mV overshoot. With the preemphasis configured for 4.25 Gbps operation (SEL4G = 1), the measured overshoot more closely matches the theoretical maximum. In this case, the peak minimum voltage limit should be more closely observed.

SIGNAL LEVELS AND COMMON-MODE SHIFT FOR AC-COUPLED AND DC-COUPLED OUTPUTS

Table 19. Output Voltage Range and Output Common-Mode Shift vs. Output Level and PE Setting

Output Levels and PE Boost				Register Setting	Output Current	AC-Coupled Transmitter					DC-Coupled Transmitter				
							$V_{CC} = V_{TTO} = 3.3$ V		$V_{CC} = V_{TTO} = 1.8$ V			$V_{CC} = V_{TTO} = 3.3$ V		$V_{CC} = V_{TTO} = 1.8$ V	
V_{SW-DC}[1] (mV)	V_{SW-PE}[1] (mV)	PE Boost (%)	PE (dB)	TX[A/B/C] Level/PE Control[2]	I_{TTO}[1] (mA)	ΔV_{OCM}[1] (mV)	V_{H-PE}[1] (V)	V_{L-PE}[1] (V)	V_{H-PE}[1] (V)	V_{L-PE}[1] (V)	ΔV_{OCM}[1] (mV)	V_{H-PE}[1] (V)	V_{L-PE}[1] (V)	V_{H-PE}[1] (V)	V_{L-PE}[1] (V)
200	200	0.00	0.00	0x00	8	200	3.2	3	1.7	1.5	100	3.3	3.1	1.8	1.6
200	300	50.00	3.52	0x01	12	300	3.15	2.85	1.65	1.35	150	3.3	3	1.8	1.5
200	400	100.00	6.02	0x02	16	400	3.1	2.7	1.6	1.2	200	3.3	2.9	1.8	1.4
200	500	150.00	7.96	0x03	20	500	3.05	2.55	1.55	1.05	250	3.3	2.8	1.8	1.3
200	600	200.00	9.54	0x04	24	600	3	2.4	1.5	0.9	300	3.3	2.7	1.8	1.2
200	700	250.00	10.88	0x05	28	700	2.95	2.25	1.45	0.75	350	3.3	2.6	1.8	1.1
200	800	300.00	12.04	0x06	32	800	2.9	2.1	1.4	0.6	400	3.3	2.5	1.8	1
300	300	0.00	0.00	0x10	12	300	3.15	2.85	1.65	1.35	150	3.3	3	1.8	1.5
300	400	33.33	2.50	0x11	16	400	3.1	2.7	1.6	1.2	200	3.3	2.9	1.8	1.4
300	500	66.67	4.44	0x12	20	500	3.05	2.55	1.55	1.05	250	3.3	2.8	1.8	1.3
300	600	100.00	6.02	0x13	24	600	3	2.4	1.5	0.9	300	3.3	2.7	1.8	1.2
300	700	133.33	7.36	0x14	28	700	2.95	2.25	1.45	0.75	350	3.3	2.6	1.8	1.1
300	800	166.67	8.52	0x15	32	800	2.9	2.1	1.4	0.6	400	3.3	2.5	1.8	1
300	900	200.00	9.54	0x16	36	900	2.85	1.95	1.35	0.45	450	3.3	2.4	1.8	0.9
400	400	0.00	0.00	0x20	16	400	3.1	2.7	1.6	1.2	200	3.3	2.9	1.8	1.4
400	500	25.00	1.94	0x21	20	500	3.05	2.55	1.55	1.05	250	3.3	2.8	1.8	1.3
400	600	50.00	3.52	0x22	24	600	3	2.4	1.5	0.9	300	3.3	2.7	1.8	1.2
400	700	75.00	4.86	0x23	28	700	2.95	2.25	1.45	0.75	350	3.3	2.6	1.8	1.1
400	800	100.00	6.02	0x24	32	800	2.9	2.1[3]	1.4	0.6	400	3.3	2.5	1.8	1
400	900	125.00	7.04	0x25	36	900	2.85	1.95[4]	1.35	0.45	450	3.3	2.4	1.8	0.9
400	1000	150.00	7.96	0x26	40	1000	2.8	1.8[4]	1.3	0.3	500	3.3	2.3	1.8	0.8
600	600	0.00	0.00	0x30	24	600	3	2.4	1.5	0.9	300	3.3	2.7	1.8	1.2
600	700	16.67	1.34	0x31	28	700	2.95	2.25	1.45	0.75	350	3.3	2.6	1.8	1.1
600	800	33.33	2.50	0x32	32	800	2.9	2.1[3]	1.4	0.6[5]	400	3.3	2.5	1.8	1
600	900	50.00	3.52	0x33	36	900	2.85	1.95[4]	1.35	0.45[4]	450	3.3	2.4	1.8	0.9
600	1000	66.67	4.44	0x34	40	1000	2.8	1.8[4]	1.3	0.3[4]	500	3.3	2.3	1.8	0.8
600	1100	83.33	5.26	0x35	44	1100	2.75	1.65[4]	1.25	0.15[4]	550	3.3	2.2	1.8	0.7
600	1200	100.00	6.02	0x36	48	1200	2.7	1.5[4]	1.2	0[4]	600	3.3	2.1[3]	1.8	0.6[5]

[1] Symbol definitions are shown in Table 20.
[2] TX[A/B/C] level/PE control registers are port level control registers at Address 0x49, Address 0x89, and Address 0xC9. Per-lane level and PE control are in separate registers.
[3] This setting requires TX_HEADROOM = 1 to ensure adequate output compliance.
[4] This setting is not recommended for ac-coupled outputs because the theoretical output low level is below the minimum output voltage limit listed in Table 1.
[5] This setting is not recommended because the output level is below the minimum output voltage limit listed in Table 1. Use V_{CC} = 2.5 V and TX_HEADROOM = 1.

Table 20. Symbol Definitions

Symbol	Formula	Definition
I_{DC}	Programmable	Output current that sets output level
I_{PE}	Programmable	Output current for PE delayed tap
I_{TTO}	$I_{DC} + I_{PE}$	Total transmitter output current
V_{DPP-DC}	$25\ \Omega \times I_{DC} \times 2$	Peak-to-peak differential voltage swing of nonpreemphasized waveform
V_{DPP-PE}	$25\ \Omega \times I_{TTO} \times 2$	Peak-to-peak differential voltage swing of preemphasized waveform
V_{SW-DC}	$V_{DPP-DC}/2 = V_{H-DC} - V_{L-DC}$	DC single-ended voltage swing
V_{SW-PE}	$V_{DPP-PE}/2 = V_{H-PE} - V_{L-PE}$	Preemphasized single-ended voltage swing
$\Delta V_{OCM_DC-COUPLED}$	$25\ \Omega \times I_{TTO}/2$	Output common-mode shift, dc-coupled outputs
$\Delta V_{OCM_AC-COUPLED}$	$50\ \Omega \times I_{TTO}/2$	Output common-mode shift, ac-coupled outputs
V_{OCM}	$V_{TTO} - \Delta V_{OCM} = (V_{H-DC} + V_{L-DC})/2$	Output common-mode voltage
V_{H-DC}	$V_{TTO} - \Delta V_{OCM} + V_{DPP-DC}/2$	DC single-ended output high voltage
V_{L-DC}	$V_{TTO} - \Delta V_{OCM} - V_{DPP-DC}/2$	DC single-ended output low voltage
V_{H-PE}	$V_{TTO} - \Delta V_{OCM} + V_{DPP-PE}/2$	Maximum single-ended output voltage
V_{L-PE}	$V_{TTO} - \Delta V_{OCM} - V_{DPP-PE}/2$	Minimum single-ended output voltage

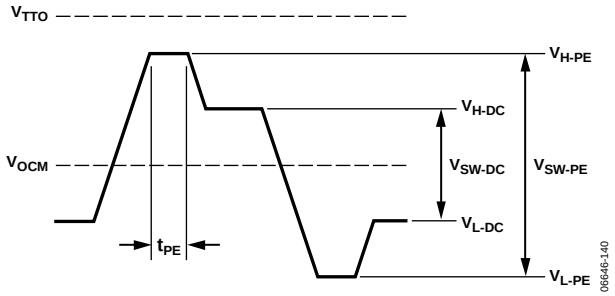


Figure 46. V_H, V_L, and V_{OCM}

SUPPLY SEQUENCING

Ideally, all power supplies should be brought up to the appropriate levels simultaneously (power supply requirements are set by the supply limits in Table 1 and the absolute maximum ratings listed in Table 3). In the event that the power supplies to the AD8158 are brought up separately, the supply power-up sequence is as follows: DV_{CC} is powered first, followed by V_{CC}, and lastly V_{TTI} and V_{TTO}. The power-down sequence is reversed, with V_{TTI} and V_{TTO} being powered off first.

V_{TTI} and V_{TTO} contain ESD protection diodes to the V_{CC} power domain (see Figure 38 and Figure 39). To avoid a sustained high current condition in these devices ($I_{SUSTAINED}$ < 64 mA), the V_{TTI} and V_{TTO} supplies should be powered on after V_{CC} and should be powered off before V_{CC}.

If the system power supplies have a high impedance in the powered off state, then supply sequencing is not required provided the following limits are observed:

- Peak current from V_{TTI} or V_{TTO} to V_{CC} < 200 mA
- Sustained current from V_{TTI} or V_{TTO} to V_{CC} < 64 mA

RESET

On initial power up or at any point during operation the AD8158 register set can be restored to the default values by pulling the RESETB pin low. Reset pulse width is defined as the time RESETB is held below the logic low threshold (V_{IL}) listed in Table 1 while the DV_{CC} supply is within the operating range in Table 1. During normal operation the RESETB pin must be pulled up to DV_{CC}. A software reset is available by writing value 0x01 to the Reset register at address 0x00. This register is write only.

SINGLE SUPPLY vs. MULTIPLE SUPPLY OPERATION

The AD8158 supports a flexible supply voltage of 1.8 V to 3.3 V. For some dc-coupled links, 1.2 V or ground-referenced signaling may be desired. In these cases, the AD8158 can be run with a split supply configuration. An example is shown in Figure 47.

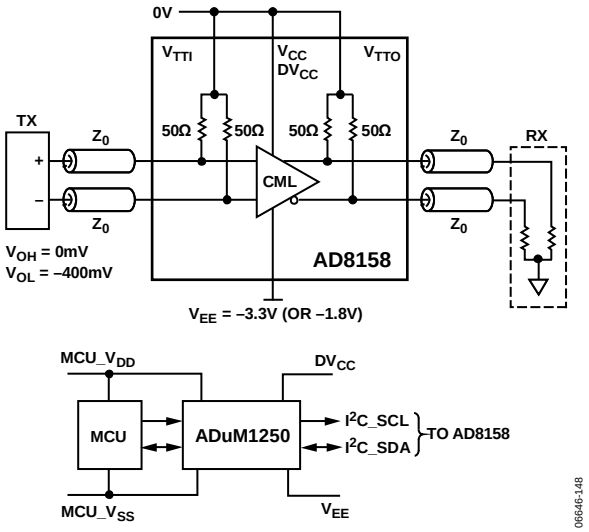


Figure 47. Multiple Supply Operation

Table 21. Alternate Supply Configuration Examples

Signal Level	V_{CC}, V_{TTI}, V_{TTO}	V_{EE}
1.2 V CML	1.2 V	$-2.1\ V \le V_{EE} \le -0.6\ V$
GND – 400 mV diff	GND	$-3.3\ V \le V_{EE} \le -1.8\ V$

The AD8158 control signals are always referenced between DV_{CC} and V_{EE} and, when using a split supply configuration, logic level-shift circuits should be used. The evaluation board design shows the use of the Analog Devices, Inc., ADUM1250 I^2C isolator and a level shifter to level-shift the SCL and SDA signals (for information about the evaluation board, see the Ordering Guide).

Evaluation of DC-Coupled Links

When evaluating the AD8158 dc-coupled, note that most lab equipment is ground referenced whereas the AD8158 high speed I/O are connected by 50 Ω on-die termination resistors to V_{TTI} and V_{TTO}. To interface the AD8158 to ground-referenced, high speed instrumentation (for example, the 50 Ω inputs of a high speed oscilloscope), it is necessary to level-shift the outputs by either using a dc-blocking network or powering the AD8158 between ground and a negative supply.

For example, to evaluate 1.8 V dc-coupled transmitter performance with a 50 Ω ground-referenced oscilloscope, use the following supply configuration:

$V_{CC} = V_{TTO} = V_{TTI} = Ground$

$V_{EE} = -1.8\ V$

$Ground < DVCC < 1.5\ V$

PRINTED CIRCUIT BOARD (PCB) LAYOUT GUIDELINES

The high speed differential inputs and outputs should be routed with 100 Ω controlled impedance differential transmission lines. The transmission lines, either microstrip or stripline, should be referenced to a solid low impedance reference plane. An example of a PCB cross-section is shown in Figure 48. The trace width (W), differential spacing (S), height above reference plane (H), and dielectric constant of the PCB material determine the characteristic impedance. Adjacent channels should be kept apart by a distance greater than 3 W to minimize crosstalk.

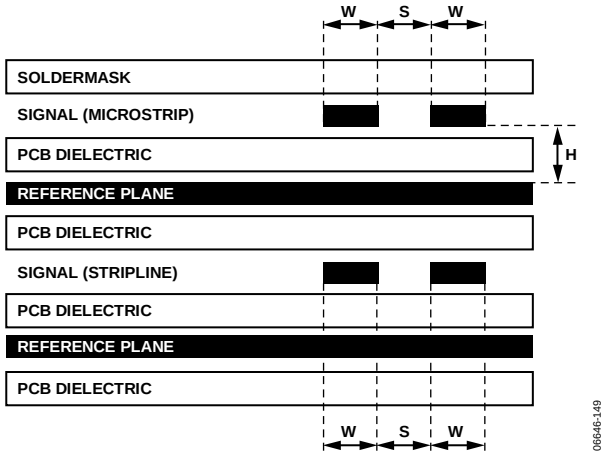


Figure 48. Example of a PCB Cross-Section

Thermal Paddle Design

The LFCSP is designed with an exposed thermal paddle to conduct heat away from the package and into the PCB. By incorporating thermal vias into the PCB thermal paddle, heat is dissipated more effectively into the inner metal layers of the PCB. To ensure device performance at elevated temperatures, it is important to have a sufficient number of thermal vias incorporated into the design. An insufficient number of thermal vias results in a θ_{JA} value larger than specified in Table 1. Additional PCB footprint and assembly guidelines are described in the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

It is recommended that a via array of 4 × 4 or 5 × 5 with a diameter of 0.3 mm to 0.33 mm be used to set a pitch between 1.0 mm and 1.2 mm. A representative of these arrays is shown in Figure 49.

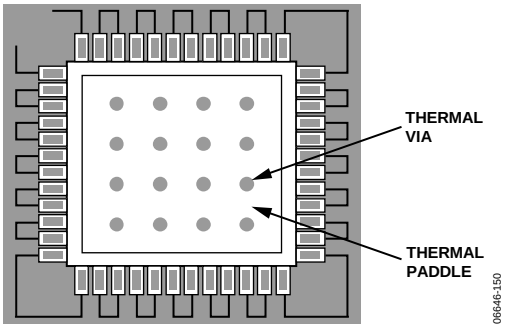


Figure 49. PCB Thermal Paddle and Via

Stencil Design for the Thermal Paddle

To effectively remove heat from the package and to enhance electrical performance, the thermal paddle must be soldered (bonded) to the PCB thermal paddle, preferably with minimum voids. However, eliminating voids may not be possible because of the presence of thermal vias and the large size of the thermal paddle for larger size packages. Also, outgassing during the reflow process may cause defects (splatter, solder balling) if the solder paste coverage is too big. It is recommended that smaller multiple openings in the stencil be used instead of one big opening for printing solder paste on the thermal paddle region. This typically results in 50% to 80% solder paste coverage. Figure 50 shows how to achieve these levels of coverage.

Voids within solder joints under the exposed paddle can have an adverse affect on high speed and RF applications, as well as on thermal performance. Because the LFCSP package incorporates a large center paddle, controlling solder voiding within this region can be difficult. Voids within this ground plane can increase the current path of the circuit. The maximum size for a void should be less than via pitch within the plane. This assures that any one via is not rendered ineffectual when any void increases the current path beyond the distance to the next available via.

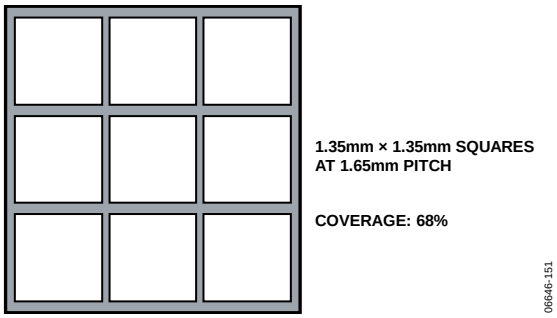


Figure 50. Typical Thermal Paddle Stencil Design

Large voids in the thermal paddle area should be avoided. To control voids in the thermal paddle area, solder masking may be required for thermal vias to prevent solder wicking inside the via during reflow, thus displacing the solder away from the interface between the package thermal paddle and thermal paddle land on the PCB. There are several methods employed for this purpose, such as via tenting (top or bottom side), using dry film solder mask; via plugging with liquid photo-imagible (LPI) solder mask from the bottom side; or via encroaching. These options are depicted in Figure 51. In case of via tenting, the solder mask diameter should be 100 microns larger than the via diameter.

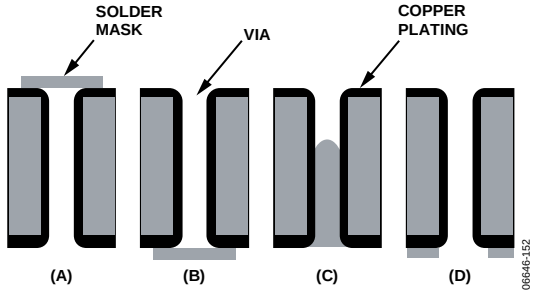


Figure 51. Solder Mask Options for Thermal Vias: (A) Via Tenting from the Top; (B) Via Tenting from the Bottom; (C)Via Plugging, Bottom; and (D) Via Encroaching, Bottom

A stencil thickness of 0.125 mm is recommended for 0.4 mm and 0.5 mm pitch parts. The stencil thickness can be increased to 0.15 mm to 0.2 mm for coarser pitch parts. A laser-cut, stainless steel stencil is recommended with electropolished trapezoidal walls to improve the paste release. Because not enough space is available underneath the part after reflow, it is recommended that no clean Type 3 paste be used for mounting the LFCSP. Inert atmosphere is also recommended during reflow.

REGISTER MAP

All registers are port-level and global registers, unless otherwise noted.

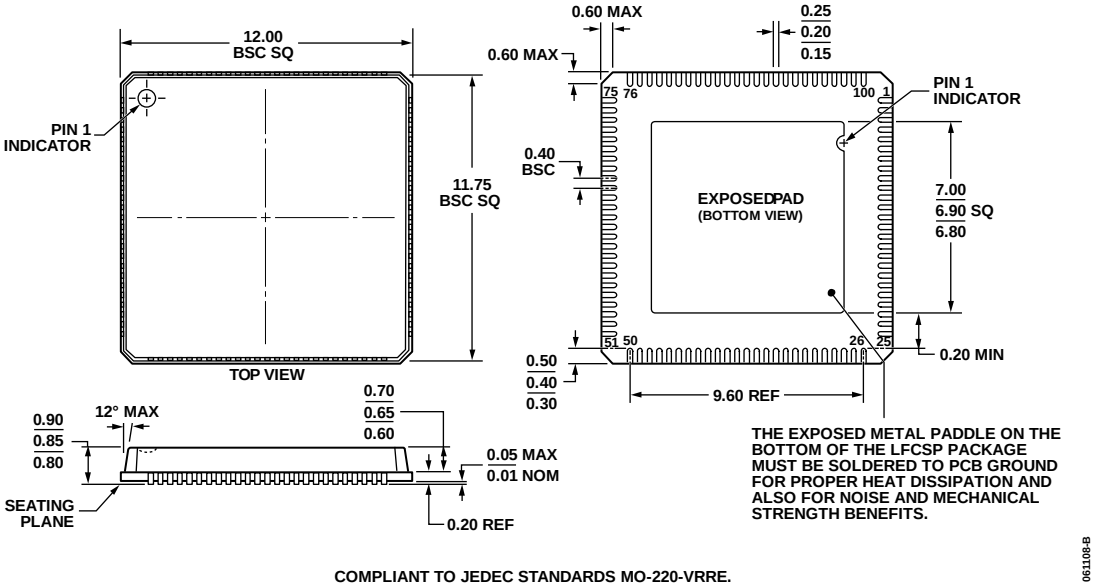
Table 22. Register Definitions

Mnemonic	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
Reset	0x00								RESET	
Switch Control 1	0x01		LBC	LBB	LBA	SELAb/B[3]	SELAb/B[2]	SELAb/B[1]	SELAb/B[0]	0x00
Switch Control 2	0x02				SEL4G				BICAST	0x00
Global Squelch Ctrl	0x04					GSQLCH_ENB				0x0F
Switch Core/ Headroom	0x05		TX_HEAD ROOM_C	TX_HEAD ROOM_B	TX_HEAD ROOM_A				XCORE_ENB	0x01
Mode	0x0F							MODE[1]	MODE[0]	0x00
RXA Disable	0x40					RXDIS A3	RXDIS A2	RXDIS A1	RXDIS A0	0x00
RXA Setting	0x41					AEQ[3]	AEQ[2]	AEQ[1]	AEQ[0]	0x00
RXA LOS Control	0x51	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	LOS_FILT	Set to 0	LOS_ENB	0x05
RXA Lane 1/ RXA Lane 0 Setting	0x42[1]	A1EQ[3]	A1EQ[2]	A1EQ[1]	A1EQ[0]	A0EQ[3]	A0EQ[2]	A0EQ[1]	A0EQ[0]	0x00
RXA Lane 3/ RXA Lane 2 Setting	0x43[1]	A3EQ[3]	A3EQ[2]	A3EQ[1]	A3EQ[0]	A2EQ[3]	A2EQ[2]	A2EQ[1]	A2EQ[0]	0x00
RXA P/N Swap	0x44[1]					PNA3	PNA2	PNA1	PNA0	0x00
RXA LOS Status	0x45[1]	LOSA3 Sticky	LOSA2 Sticky	LOSA1 Sticky	LOSA0 Sticky	LOSA3 Active	LOSA2 Active	LOSA1 Active	LOSA0 Active	
TXA Disable	0x48					TXDIS A3	TXDIS A2	TXDIS A1	TXDIS A0	0x00
TXA Level/PE Control	0x49			ALEV[1]	ALEV[0]		APE[2]	APE[1]	APE[0]	0x20
TXA Lane1/ TXA Lane 0 PE Setting	0x4A[1]		A1PE[2]	A1PE[1]	A1PE[0]		A0PE[2]	A0PE[1]	A0PE[0]	0x00
TXA Lane2/3 PE Setting	0x4B[1]		A3PE[2]	A3PE[1]	A3PE[0]		A2PE[2]	A2PE[1]	A2PE[0]	0x00
TXA Per-Lane Level Setting	0x4C[1]	A3OLEV[1]	A3OLEV[0]	A2OLEV[1]	A2OLEV[0]	A1OLEV[1]	A1OLEV[0]	A0OLEV[1]	A0OLEV[0]	0xAA
RXB Disable	0x80					RXDIS B3	RXDIS B2	RXDIS B1	RXDIS B0	0x00
RXB Setting	0x81					BEQ[3]	BEQ[2]	BEQ[1]	BEQ[0]	0x00
RXB LOS Ctrl	0x91	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	LOS_FILT	Set to 0	LOS_ENB	0x05
RXB Lane 1/ RXB Lane 0 Setting	0x82[1]	B1EQ[3]	B1EQ[2]	B1EQ[1]	B1EQ[0]	B0EQ[3]	B0EQ[2]	B0EQ[1]	B0EQ[0]	0x00
RXB Lane 3/ RXB Lane 2 Setting	0x83[1]	B3EQ[3]	B3EQ[2]	B3EQ[1]	B3EQ[0]	B2EQ[3]	B2EQ[2]	B2EQ[1]	B2EQ[0]	0x00
RXB P/N Swap	0x84[1]					PNB3	PNB2	PNB1	PNB0	0x00
RXB LOS Status	0x85[1]	LOSB3 Sticky	LOSB2 Sticky	LOSB1 Sticky	LOSB0 Sticky	LOSB3 Active	LOSB2 Active	LOSB1 Active	LOSB0 Active	
TXB Disable	0x88					TXDIS B3	TXDIS B2	TXDIS B1	TXDIS B0	0x00
TXB Level/PE Control	0x89			BLEV[1]	BLEV[0]		BPE[2]	BPE[1]	BPE[0]	0x20
TXB Lane1/ TXB Lane 0 PE Setting	0x8A[1]		B1PE[2]	B1PE[1]	B1PE[0]		B0PE[2]	B0PE[1]	B0PE[0]	0x00
TXB Lane2/ TXB Lane 3 PE Setting	0x8B[1]		B3PE[2]	B3PE[1]	B3PE[0]		B2PE[2]	B2PE[1]	B2PE[0]	0x00
TXB Per-Lane Level Setting	0x8C[1]	B3OLEV[1]	B3OLEV[0]	B2OLEV[1]	B2OLEV[0]	B1OLEV[1]	B1OLEV[0]	B0OLEV[1]	B0OLEV[0]	0xAA

Mnemonic	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
RXC Disable	0xC0					RXDIS C3	RXDIS C2	RXDIS C1	RXDIS C0	0x00
RXC Setting	0xC1					CEQ[3]	CEQ[2]	CEQ[1]	CEQ[0]	0x00
RXC LOS Ctrl	0xD1	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	LOS_FILT	Set to 0	LOS_ENB	0x05
RXC Lane 1/ RXC Lane 0 Setting	0xC2[1]	C1EQ[3]	C1EQ[2]	C1EQ[1]	C1EQ[0]	C0EQ[3]	C0EQ[2]	C0EQ[1]	C0EQ[0]	0x00
RXC Lane 3/ RXC Lane 2 Setting	0xC3[1]	C3EQ[3]	C3EQ[2]	C3EQ[1]	C3EQ[0]	C2EQ[3]	C2EQ[2]	C2EQ[1]	C2EQ[0]	0x00
RXC P/N Swap	0xC4[1]					PNC3	PNC2	PNC1	PNC0	0x00
RXC LOS Status	0xC5[1]	LOSC3 Sticky	LOSC2 Sticky	LOSC1 Sticky	LOSC0 Sticky	LOSC3 Active	LOSC2 Active	LOSC1 Active	LOSC0 Active	
TXC Disable	0xC8					TXDIS C3	TXDIS C2	TXDIS C1	TXDIS C0	0x00
TXC Level/PE Control	0xC9			CLEV[1]	CLEV[0]		CPE[2]	CPE[1]	CPE[0]	0x20
TXC Lane1/ TXC Lane 0 PE Setting	0xCA[1]		C1PE[2]	C1PE[1]	C1PE[0]		C0PE[2]	C0PE[1]	C0PE[0]	0x00
TXC Lane2/ TXC Lane 3 PE Setting	0xCB[1]		C3PE[2]	C3PE[1]	C3PE[0]		C2PE[2]	C2PE[1]	C2PE[0]	0x00
TXC Per-Lane Level Setting	0xCC[1]	C3OLEV[1]	C3OLEV[0]	C2OLEV[1]	C2OLEV[0]	C1OLEV[1]	C1OLEV[0]	C0OLEV[1]	C0OLEV[0]	0xAA

[1] Per-lane registers.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VRRE.

Figure 52. 100-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
12 mm × 12 mm Body, Very Thin Quad
(CP-100-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8158ACPZ	−40°C to +85°C	100-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-100-1
AD8158-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

I2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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