

DM388 Camera Start Kit

User's Guide



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About This Manual

This document is for the DM388 processor module.

Related Documentation

Information regarding the DM388 processor can be found at <http://www.ti.com>.

Board History

PCB Revision	History
PRDN_REV A	Production

Acronyms

The following is a list of acronyms used in this document.

CCS	Code Composer Studio™
DSP	Digital signal processor
EEPROM	Electrically Erasable Programmable Read-Only Memory
I²C	Inter-integrated circuit
JTAG	Joint test action group
LED	Light emitting diode
MMC	Multimedia card
UART	Universal asynchronous receiver transmitter
USB	Universal serial bus
XDS100	Texas Instruments emulator

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Connecting to DM388 CSK

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The DM388 CSK is based on DaVinci™ technology. These digital-media processors are highly integrated, cost-effective, low-power, and have programmable platforms that leverage TI's DaVinci processor technology to meet the processing requirements of HD video conferencing, Skype™ endpoints, IP netcam, digital signage, media players and adapters, mobile medical imaging, network projectors, home audio and video equipment, and similar devices in SD, HD, and 4K × 2K resolutions.

The DM388 camera starter kit is a development platform with the DM388 processor module connected to a CSK carrier card over board-to-board connectors. Features of the DM388 module and CSK carrier card are detailed in the subsections that follow.

DM388 camera starter kit contents:

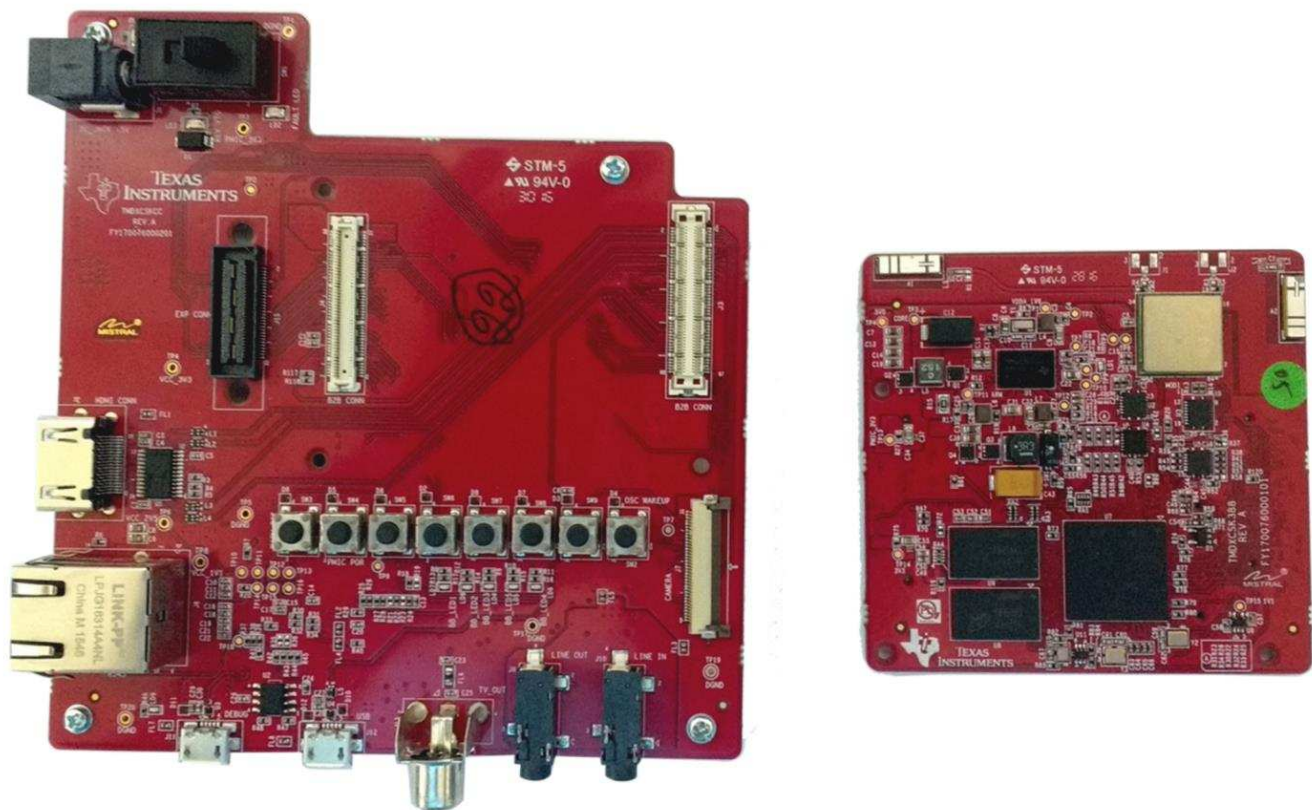
- TMDSCSK388 module
- CSK carrier card
- Camera module (LI-CAM-AR0331-324-1.8) with FPC cable

1.1 Connecting TMDSCSK388 Module to CSK Carrier Card

Use the following instructions to connect the TMDSCSK388 module to the CSK carrier card.

1. Align the CSK carrier card and the DM388 module (see [Figure 1-1](#)).

Figure 1-1. Aligned DM388 and CSK Carrier Card



2. Place the DM388 module over the board-to-board connectors of the CSK carrier card, then gently press the devices together (see [Figure 1-2](#) and [Figure 1-3](#)).

Figure 1-2. DM388 Module Above CSK Carrier Card

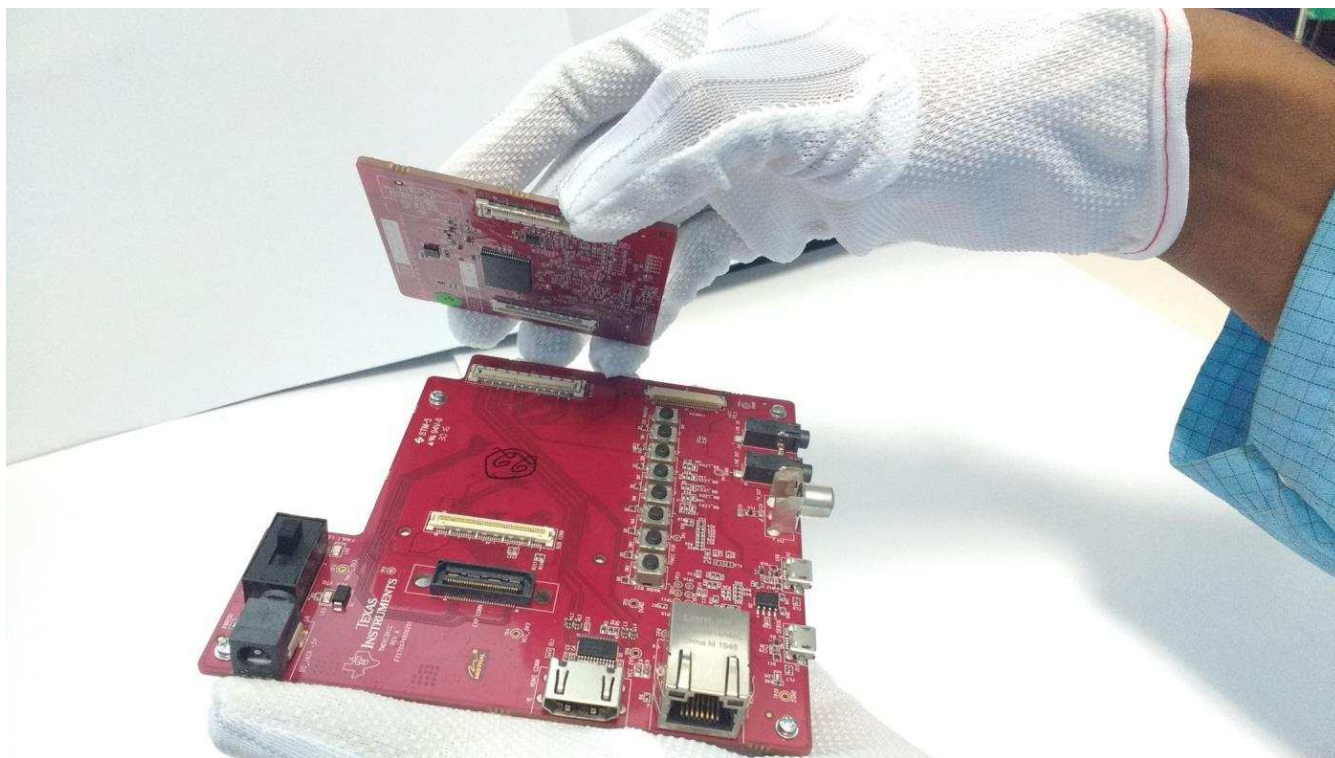


Figure 1-3. Connecting DM388 and CSK Carrier Card

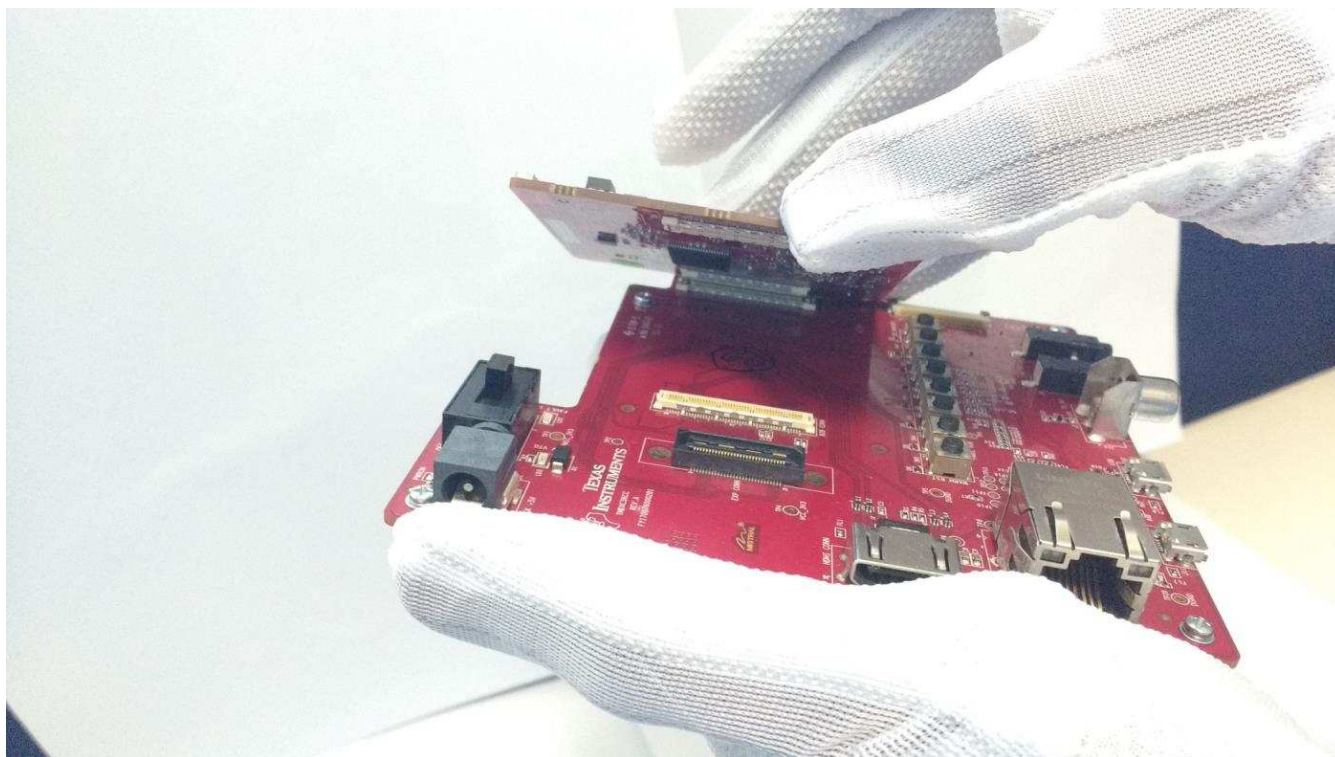
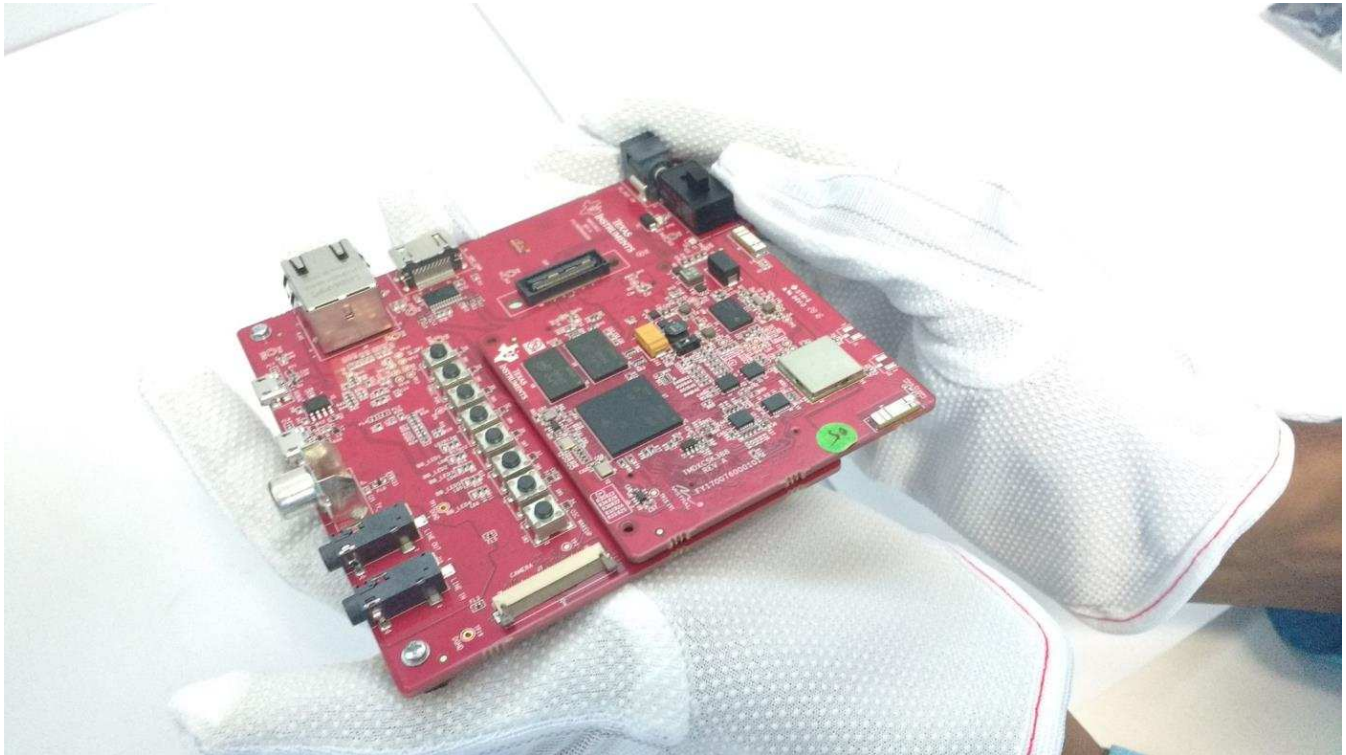


Figure 1-4. Connected Devices



TMDSCSK388 Module

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2.1 Key Features

The DM388 module is a high-performance DaVinci™ digital-media signal processor from TI.

- Up to 1000-MHz ARM® Cortex®-A8 RISC processor DSP internal memories
- Imaging subsystem
- Programmable high-definition video image coprocessing (HDVICP v2) engine
- HD video processing subsystem (HDVPSS)
- 32-bit DDR2, DDR3, and DDR3L SDRAM interface
 - Supports up to 400 MHz for DDR2, 533 MHz for DDR3, and 533 MHz for DDR3L
 - Up to two × 16 devices, 2GB of total address space
- Dynamic Memory Manager (DMM)
- General-Purpose Memory Controller (GPMC)
 - 8- or 16-bit multiplexed address and data bus
 - 512MB of total address space divided among up to eight chip selects
- Enhanced direct memory access (EDMA) controller
- Ethernet switch with dual 10-, 100-, or 1000-Mbps external interfaces (EMAC software)
- Dual USB 2.0 ports with integrated PHYs
- One PCI Express 2.0 port with integrated PHY
- Eight 32-bit general-purpose timers
- Four serial peripheral interfaces (SPIs), up to 48 MHz
- Three MMCs, SDs, and SDIO serial interfaces (up to 48 MHz)
- Four inter-integrated circuit (I²C bus) ports
- Two multichannel audio serial ports (McASP)
- Four audio tracking logic (ATL) modules
- On-chip ARM ROM bootloader (RBL)
- Power, reset, and clock management
- 32KB of embedded trace buffer (ETB) and 5-pin trace interface for debug
- 1.8- and 3.3-V dual voltage buffers for general I/O

The DM388 processor module is a low cost, small form factor, higher performance, easy-to-use system-on-module. The development platform has the interfaces that can help build application devices:

- Camera
- Ethernet
- HDMI
- CSI
- McASP
- UART
- I²C
- TVOUT
- USB

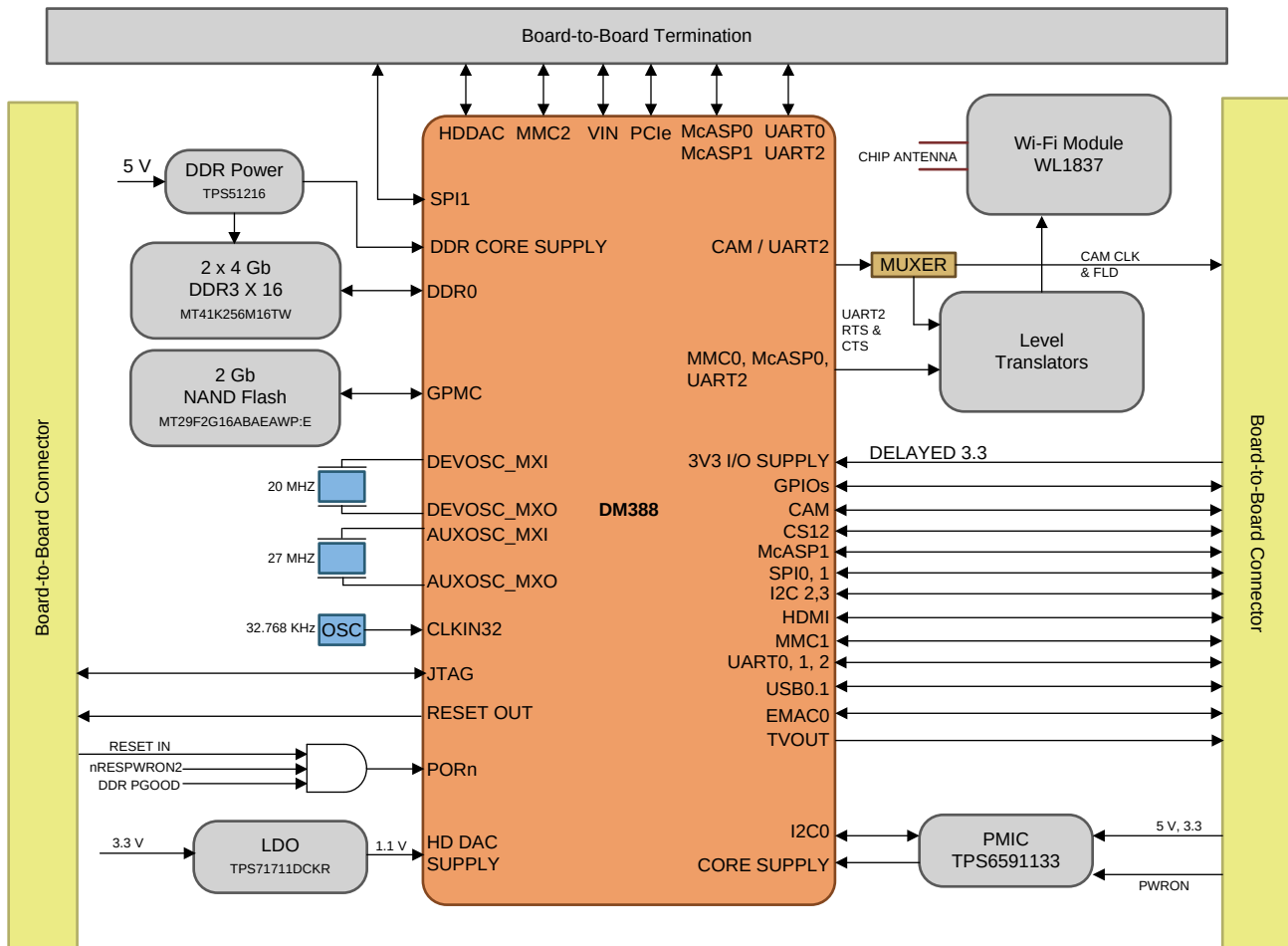
The following is a list of key features of the DM388 processor module.

- TI's DM388 high performance DaVinci digital media signal processor based on ARM v7 architecture
- WiLink 8 Wi-Fi module with 2.4-GHz, single-ended PCB antenna
- 2Gb NAND flash
- 1GB DDR3
- TI's TPS6591133 for power management
- Two board-to-board connectors support:
 - USB
 - UART
 - MMC
 - McASP
 - TVOUT
 - CAMERA
 - CSI
 - HDMI
 - GMII
 - JTAG
 - 10 GPIOs
- Options for UFL connectors (not mounted)
- Additional signals are terminated on board to DNI connector for future expansion
- Powered by carrier card through board-to-board connector

2.2 Block Diagram

Figure 2-1 shows the TMDSCSK388 block diagram.

Figure 2-1. TMDSCSK388 Block Diagram



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Figure 2-2 and Figure 2-3 show the top view and bottom view of the TMDSCSK388 module, respectively.

Figure 2-2. TMDSCSK388 Top View

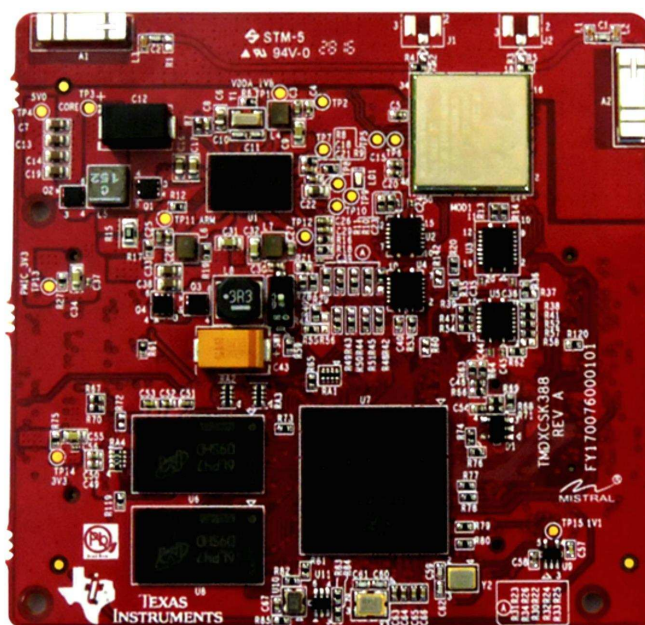
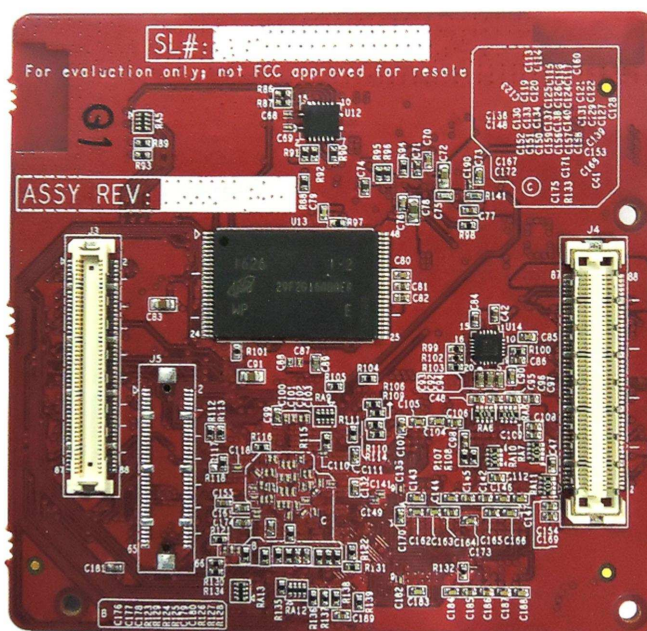


Figure 2-3. TMDSCSK388 Bottom View



2.3 Power Supply

The DM388 processor is powered by the CSK carrier through the board-to-board connectors.

The CSK carrier card is powered by a +5-V, 3-A, DC power adapter plugged in to the DC power jack (J1). On the CSK carrier card, +5-V is converted into the required supply voltages by using regulators.

[Table 2-1](#) lists the power ICs in the TMDSCSK388 module.

Table 2-1. DM388 Power ICs

Power IC		Purpose
TPS6591133	(U11)	All voltages for the processor
TPS51216RUK R	(U14)	1V5 and 0.75 generation for DDR3
TPS71711DCK R	(U9)	1V1 generation for HD-DAC

The power management IC TPS6591133 (U1) generates and sequences the following powers to the DM388 processor:

- Core voltage
 - CORE_CVDD
 - CVDD_HDVICP
 - CVDD_ARM
- Internal LDO voltages
 - TPS_VDAC_1V8
 - TPS_HDMI_CSI_1V8
 - TPS_GPIO_3V3
 - PLL_1V8
 - TPS_LDO5_3V3
 - TPS_LDO6_3V3
 - TPS_USB_3V3
 - TPS_USB_1V8
- I/O voltages
 - TPS_VDDA_1V8
- VRTC voltages
 - VRTC

The I2C0 interface if the DM388 module controls the TPS6591133 device.

TMDSCSK388 Module Interface Details

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3.1 Clock Distribution

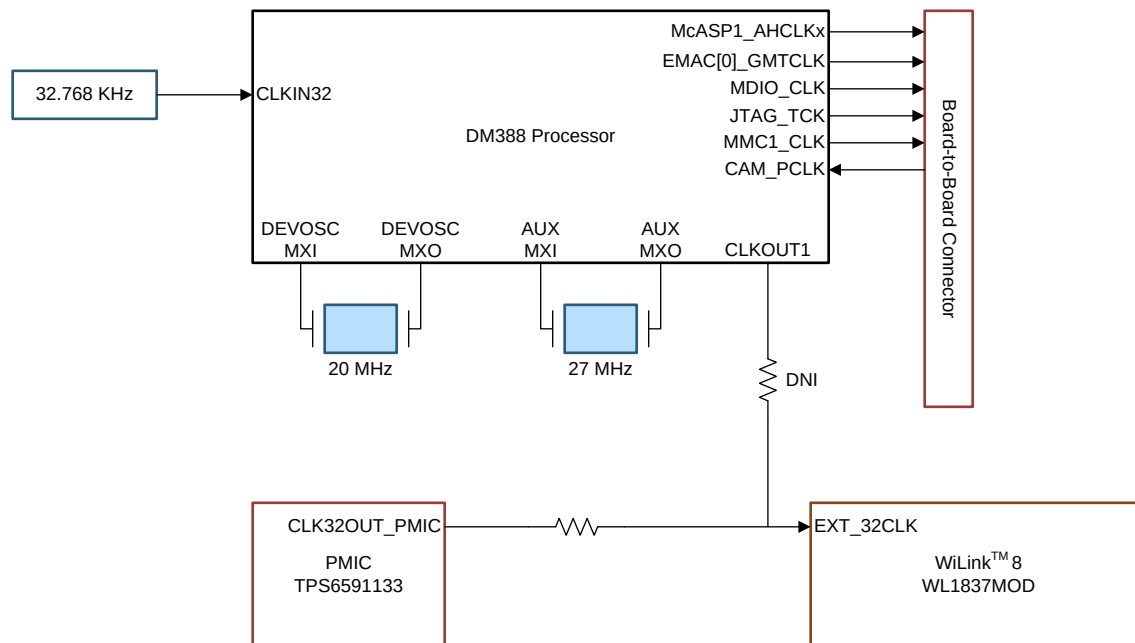
The DM388 module contains the following reference clocks:

- Y1 – 32.768-kHz real-time clock (RTC) to the power management IC (TPS6591133)
- Y2 – 20-MHz crystal for the device oscillator inputs
- Y3 – 27-MHz crystal for the auxiliary oscillator inputs
- U5 – 32.768-KHz oscillator for the reference clock

The slow clock to the WLAN WiLink WL1837 module is provided by CLKOUT1 from the processor or by CLK32OUT from the PMIC. The default clock is from PMIC.

Figure 3-1 shows the board-clock distribution circuit.

Figure 3-1. Clock Distribution



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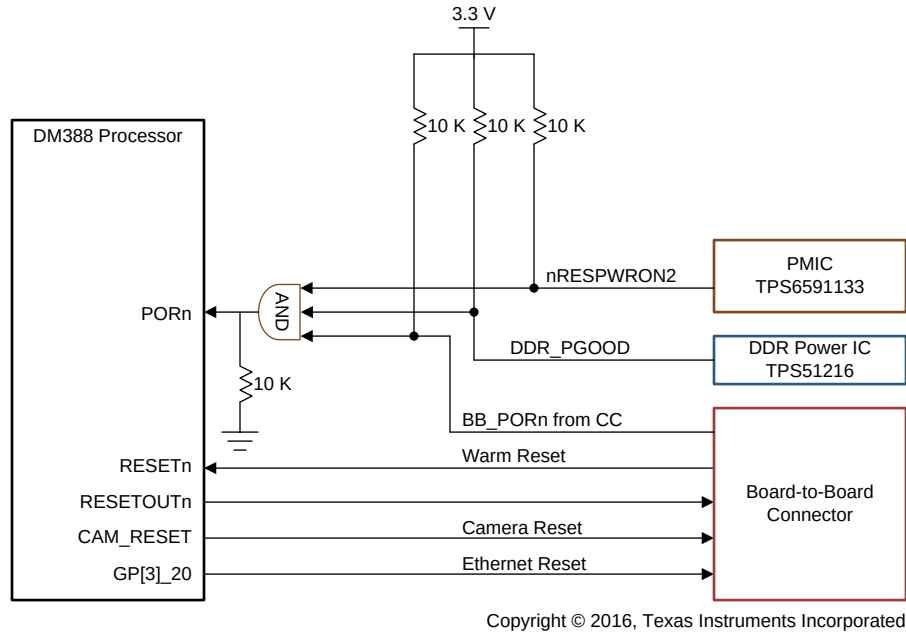
3.2 Reset Circuit and Distribution

Power good from PMIC TPS6591133 (nRESPWRO2), power good from DDR power IC (DDR_PG00D), and reset from the CSK carrier card are monitored to generate the power-on reset (PORn) to the DM388 processor. A 3-input AND gate is used to implement the reset logic. Warm reset for the processor is the input from the CSK carrier card through the board-to-board connector.

The reset to the parallel camera module and the externally connected Ethernet are reset from the DM388 processor through the board-to-board connectors.

Figure 3-2 shows the board-reset circuit and distribution.

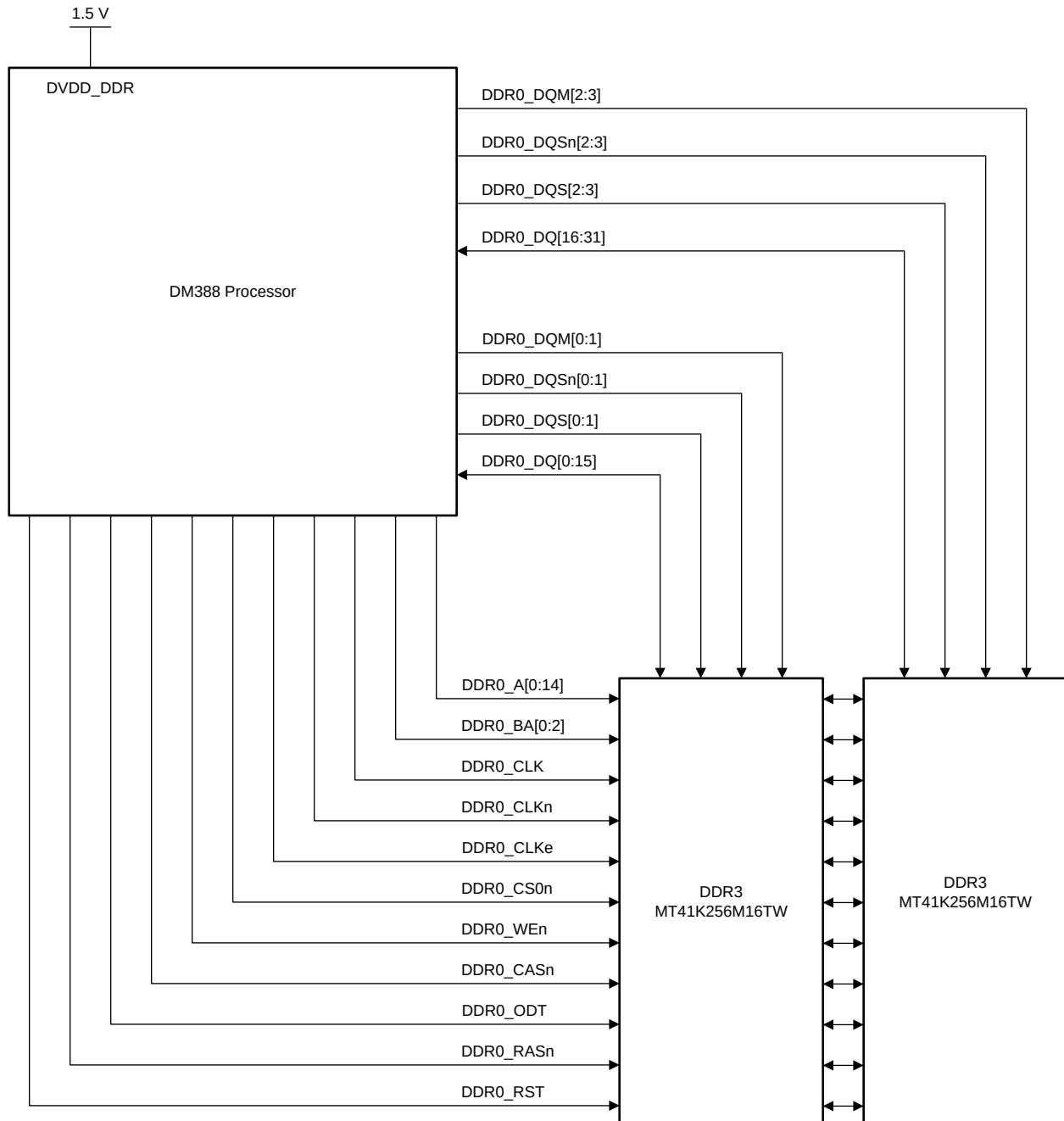
Figure 3-2. Reset Circuit and Distribution



3.3 DDR3 Interface

The DM388 processor supports 32-bit data DDR2, DDR3, DDR3L, and SDRAM interfaces. The two 4-Gb (256M x16) DDR3L chips (MT41K256M16TW-107 [backward compatible to DDR3]) from Micron are used to obtain a memory size of 1 GB. The DDR3L chips are routed using Fly-by topology, shown in [Figure 3-3](#).

Figure 3-3. DDR3 Bank0 Interface



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3.4 DDR Timing Control and Software Leveling

Table 3-1 provides the calculated seed values. For more information about DDR3 leveling, refer to [TI814x-DDR3-Init-U-Boot](#).

Table 3-1. Calculated Seed Values

Parameters				
DDR3 clock frequency	533 MHz			
Invert Clkout	0			
Trace Length (inches)				
	Byte 0	Byte 1	Byte 2	Byte 3
CK trace	1.8241295	1.8241295	1.3182095	1.3182095
DQS trace	0.7416985	0.5462986	0.9314172	0.6275384
Seed Values (per byte lane)				
WR DQS	1A	1F	9	10
RD DQS	34	34	34	34
RD DQS GATE	85	7B	82	73
Seed Values to Input to Program				
WR DQS	14			
RD DQS	34			
RD DQS GATE	7D			

The following code snippet shows the optimum values obtained after running the DDR3_SlaveRatio_ByteWiseSearch_TI814x.out file in CCS.

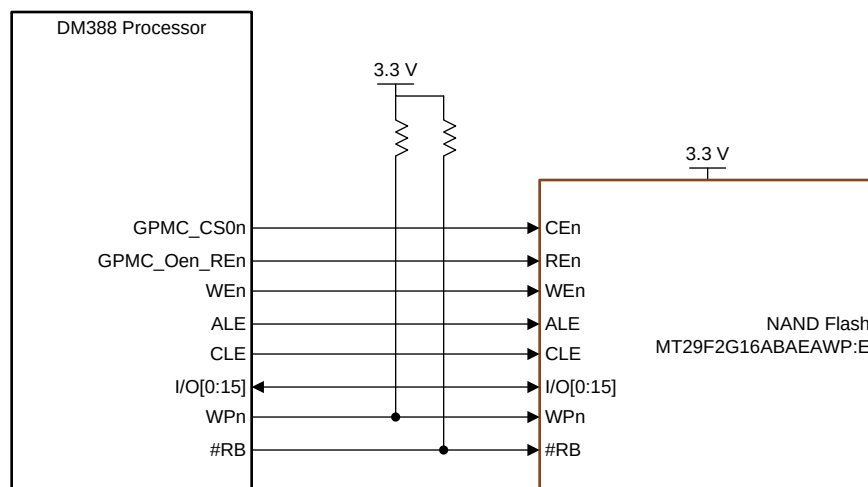
```
*****
                BYTE3  BYTE2  BYTE1  BYTE0
*****
Read DQS MAX      6e    72    75    72
Read DQS MIN       2     7     9     6
Read DQS OPT      37    3c    3e    3d
*****
Read DQS GATE MAX    13c   13e   130   11e
Read DQS GATE MIN     0     0     0     0
Read DQS GATE OPT    99    9a    98    91
*****
Write DQS MAX      a0    a0    94    9b
Write DQS MIN       0     0     0     0
Write DQS OPT      51    51    4a    4a
*****
Write DATA MAX     bf    bf    bf    c2
Write DATA MIN     4e    4c    4e    51
Write DATA OPT     88    88    87    8a
*****
```

3.5 NAND Flash Interface

The DM388 processor supports a 2-Gb NANDFLASH MT29F2G16ABA from Micron, with a 16-bit data width interfaced to the general purpose memory controller (GPMC) interface of the processor. The NAND flash is interfaced to GPMC chip select #0.

Figure 3-4 shows the connection details of the NAND flash in the TMDSCSK388 module. The operating voltage of the GPMC interface and NAND flash is 3.3 V.

Figure 3-4. NAND Flash Interface



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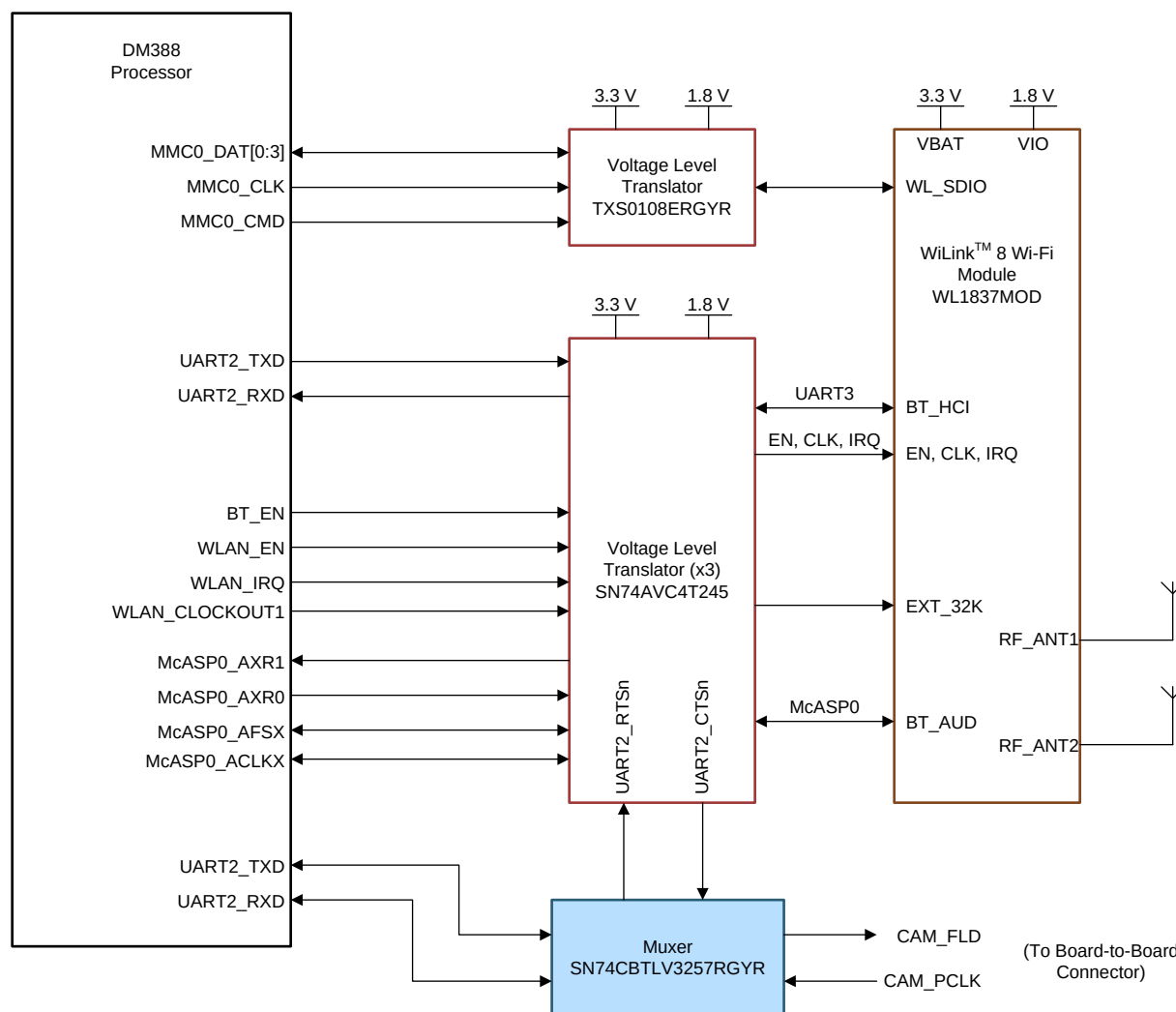
3.6 Wi-Fi and BT Interface

The WiLink 8 module is a WLAN baseband processor and RF transceiver support of IEEE standard 802.11a, 802.11b, 802.11g, and 802.11n. The device can be configured for 20-MHz or 40-MHz SISO, and 20-MHz 2×2 MIMO at 2.4 GHz for high throughput (80 Mbps [TCP] and 100 Mbps [UDP]). The device supports a 4-bit SDIO host interface.

Flow controls signals of UART2 (RTSn and CTSn) are muxed with the camera field and pixel-clock signals; a multiplexer, U4 (SN74CBTLV3257RGYR), is used to separate those signals. UART signals are fed to the voltage translators, and CAM signals are connected to board-to-board connectors. Four voltage level translators (TXS0108ERHYR [U3] for MMC, SN74AVC4T245[U2, U5, U12] for McASP, UART, EN, CLK, and IRQ) convert I/O voltages of the DM388 (3.3 V) to I/O voltages of the Wi-Fi module (1.8 V).

Figure 3-5 shows the Wi-Fi and BT interface.

Figure 3-5. Wi-Fi and BT Interface



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3.7 Board-to-Board Interface

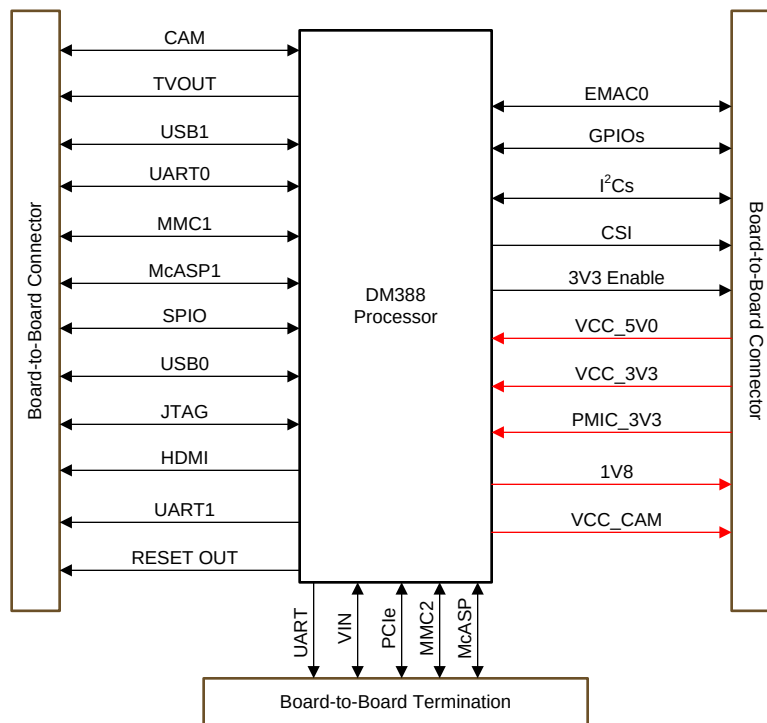
The DM388 processor module supports parallel camera interface, TVOUT, EMAC, McASP, MMC, USB, UART, SPI, JTAG, I²C, HDMI, CSI, and GPIO's over board-to-board connectors. See [Chapter 6](#) for more information about the board-to-board interfaces.

A board-to-board termination connector is provided in the DM388 SOM module, and supports video IN, PCIe, MMC, McASP, and HDDAC.

By default, the board-to-board connector is not assembled on the DM388 SOM module. The connector can be populated and used with a third-party carrier card.

[Figure 3-6](#) shows the board-to-board interface.

Figure 3-6. Board-to-Board Interface



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3.8 Boot Mode Configuration

The DM388 module supports MMC and NAND boot mode configurations. By Default, switch SW1 is configured for NAND flash boot mode. However, other boot modes must be selected by the resistor mount and demount option.

Figure 3-7 shows the boot mode configurations.

Figure 3-7. Boot Mode Configurations

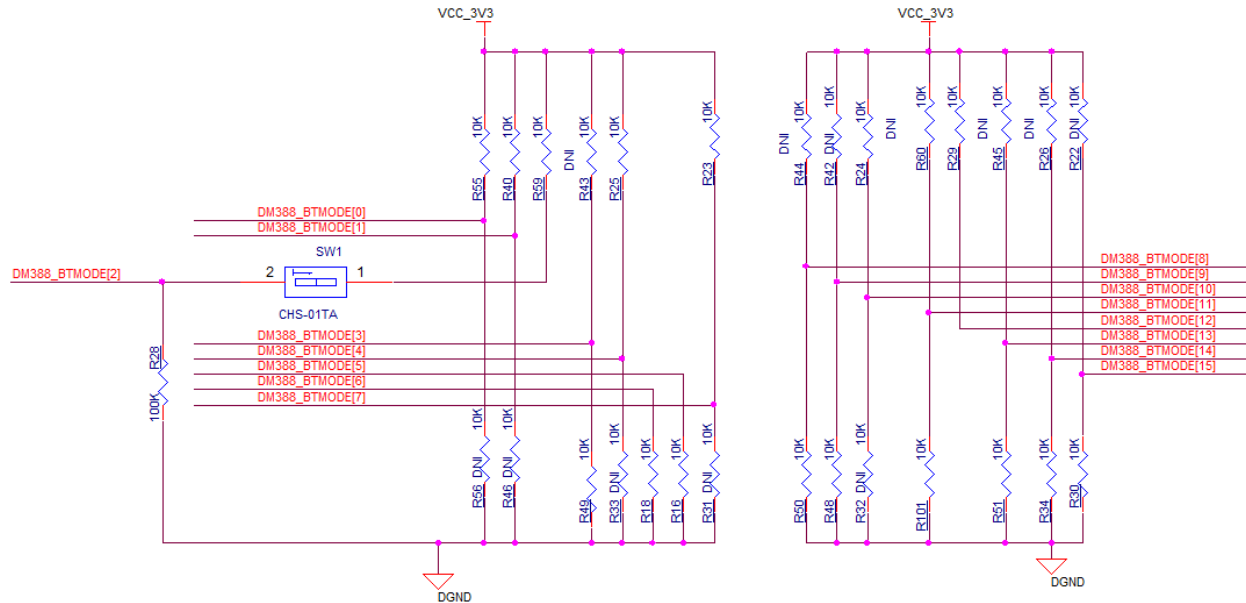


Table 3-2 provides the boot mode selection and information.

Table 3-2. Boot Mode Selection

Boot Mode Pin	Default Setting	Description
BTMODE15	0	GPMC CS0 wait disabled
BTMODE14	0	GPMC CS0 address and data not muxed
BTMODE13	0	
BTMODE12	1	GPMC CS0 16-bit data bus
BTMODE11	0	RSTOUT is asserted when a watchdog timer reset, POR, RESET, emulation, software-global cold reset, or software-global warm reset occurs
BTMODE10	0	GPMC option A
BTMODE9	0	MII (GMII) ethernet PHY mode
BTMODE8	0	
BTMODE7	1	RGMII internal delay disabled
BTMODE6	0	RSV
BTMODE5	0	RSV
BTMODE[4:0]	10011	NAND boot
	10111	MMC boot

Table 3-3 provides the SW1 switch-selection information.

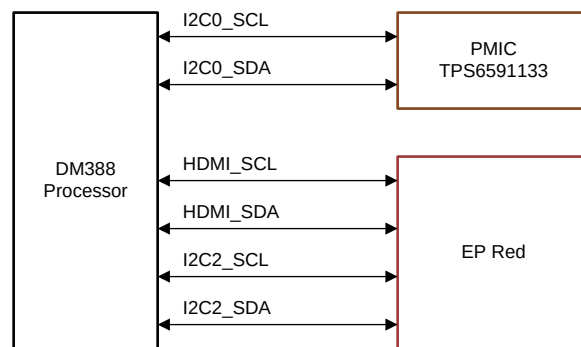
Table 3-3. SW1 Switch Selection

SW1	Selection
ON	MMC boot
OFF	NAND

3.9 I²C Interface

The DM388 processor module supports an I²C interface that is connected to PMIC and the board-to-board connector. Refer to Section 3.10 for I²C addresses of individual devices. Figure 3-8 shows the I²C connection on the TMDSCSK388 module.

Figure 3-8. I²C Interface



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3.10 I²C Address Mapping

Table 3-4 provides the address mapping for I²C interfaces on the TMDSCSK388 module.

Table 3-4. I²C Address Mapping

Master	I ² C	Slave Device	7-Bit Address
DM388 Processor	I2C0	PMIC	0x2D (general purpose)
	HDMI SCL HDMI SDA	Display device	Depends on connected HDMI monitor
		Board-to-board connector → audio codec (TLV320AIC3104)	0x18
	I2C2	Board-to-board connector → level translator → camera module	0x10 (camera sensor)
			0x2D (LVDS module)

3.11 GPIO Mapping

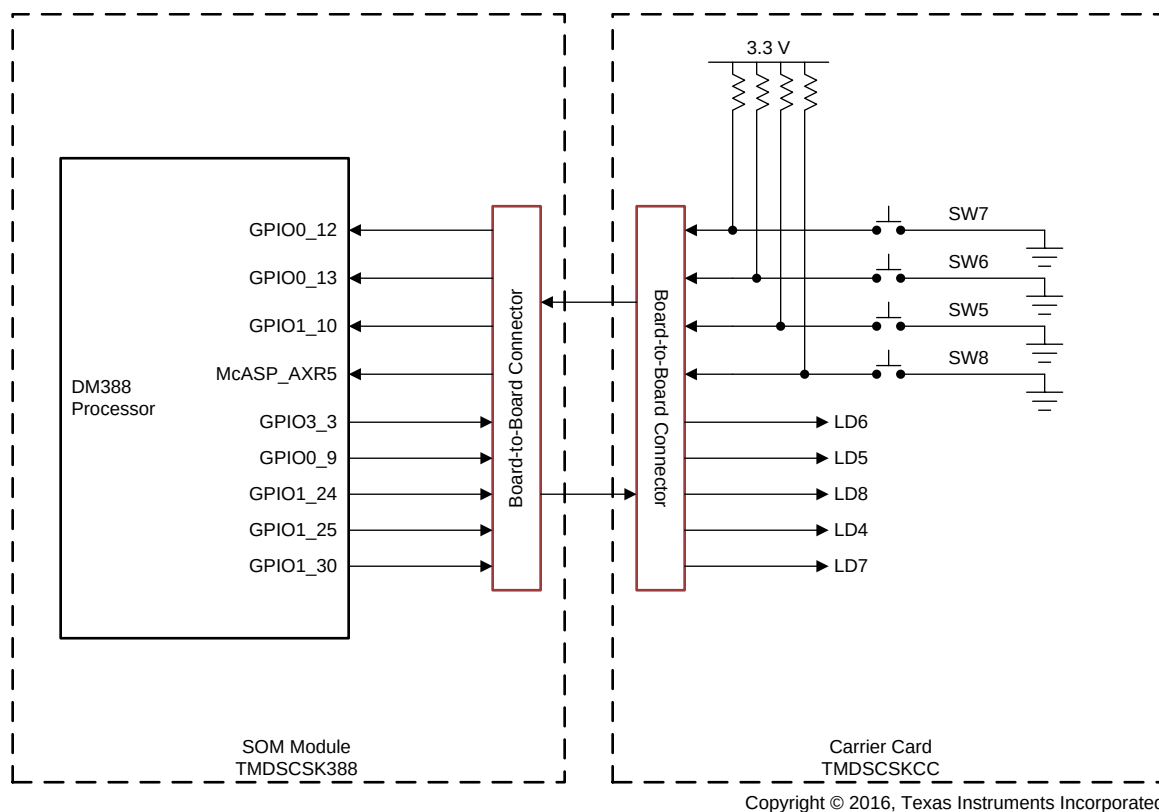
Table 3-5 provides the GPIO mapping for the TMDSCSK388 module.

Table 3-5. GPIO Mapping

GPIO Name	DM388 GPIO	Purpose	Internal or External PU or PD
DM388_GPMC_WPn	GP1[26]	Write protect to NAND flash	External PU
DM388_WLAN_IRQ	GP1[13]	Interrupt from WL1837 MOD	External PU
DM388_WLAN_EN	GP2[6]	WLAN enable signal to Wi-Fi module (WL1837)	Internal PD
DM388_BT_EN	GP2[5]	Bluetooth enable signal to Wi-Fi module (WL1837)	Internal PD
DM388_TPS_SLEEP	GP1[15]	PMIC sleep input	Internal PU
DM388_MUX_SEL	GP[16]	Selection signal to camera and UART muxer	External PD
ENET_RSTn	GP3[20]	Ethernet reset	Internal PU
DM388_MMC1_DAT6	GP0[12]	Switch	Internal PU
GP0_12			
DM388_MMC1_DAT7	GP0[13]	Switch	Internal PU
GP0_13			
DM388_GP1[10]	GP1[10]	Switch	Internal PD
DM388_McASP0_AXR5	MCA[0]_AXR[5]	Switch	Internal PD
DM388_GP3[3]	GP3[3]	LED	Internal PD
DM388_GP0[9]	GP0[9]	LED	Internal PD
DM388_GP1[24]	GP1[24]	LED	Internal PU
DM388_GP1[25]	GP1[25]	LED	Internal PU
DM388_GP1[30]	GP1[30]	LED	Internal PU

Figure 3-9 shows the GPIO mapping of LEDs and switches.

Figure 3-9. GPIO Mapping of LEDs and Switches



TMDSCSK388 Module Physical Specifications

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4.1 Board Layout

Figure 4-1 and Figure 4-2 show the top and bottom view of the TMDSCSK388 assembly layout. The DM388 board is 2.856 × 2.755 inches (72.55 mm × 70 mm), has eight layers, and is powered through the board-to-board connector.

Figure 4-1. TMDSCSK388 Assembly Layout (Top View)

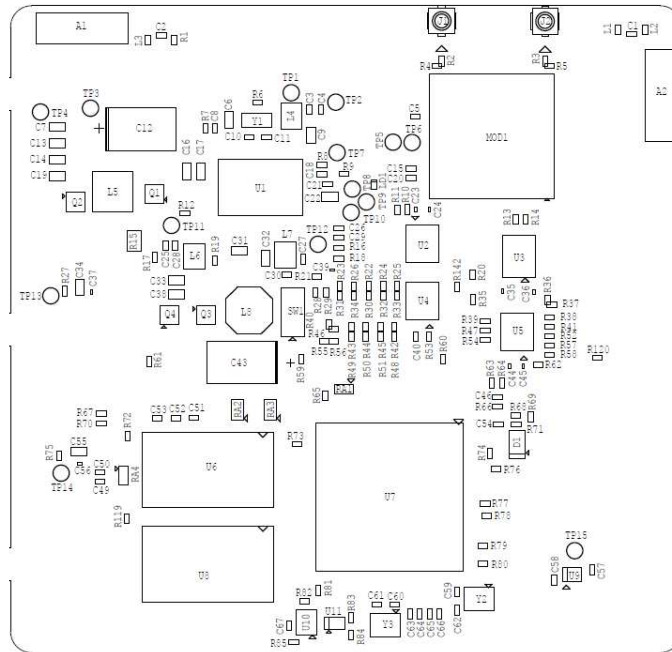
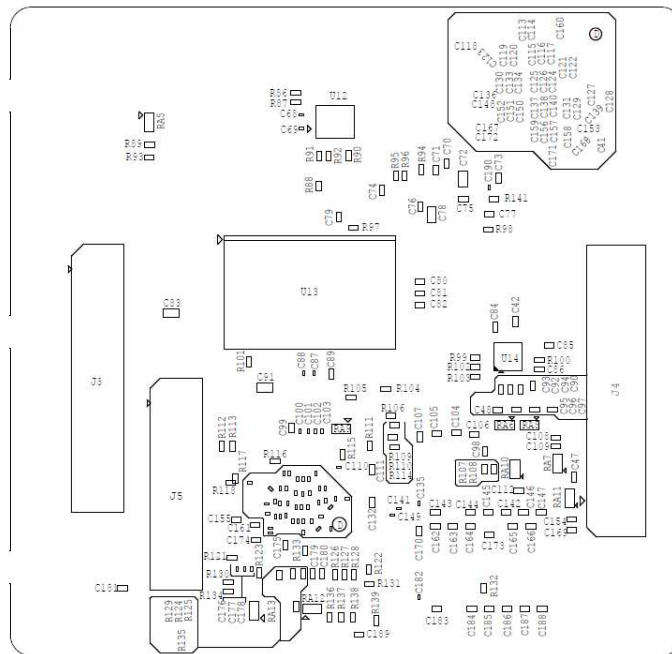


Figure 4-2. TMDSCSK388 Assembly Layout (Bottom View)



4.2 Connector Index

Table 4-1 provides the connectors that are on the TMDSCSK388 module.

Table 4-1. TMDSCSK388 Module Connectors

Connector	Part Number	Pins	Function
J1	U.FL-R-SMT-1(01)	3	RF UFL connector for high frequency signals (DNI)
J2			
J3	FX11LA-80P/8-SV(71)	80	Board-to-board connector (male)
J4	FX11LA-80S/8-SV(71)	80	Board-to-board connector (female)
J5	FX11LA-60P/6-SV(71)	60	Board-to-board termination (DNI)

Figure 4-3 and Figure 4-4 show the locations of the connectors on the TMDSCSK388 module.

Figure 4-3. TMDSCSK388 Connectors (Top)

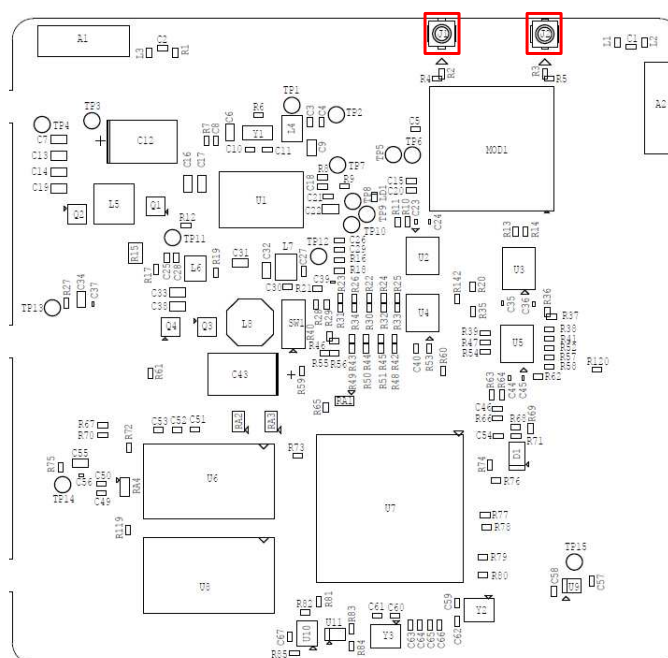
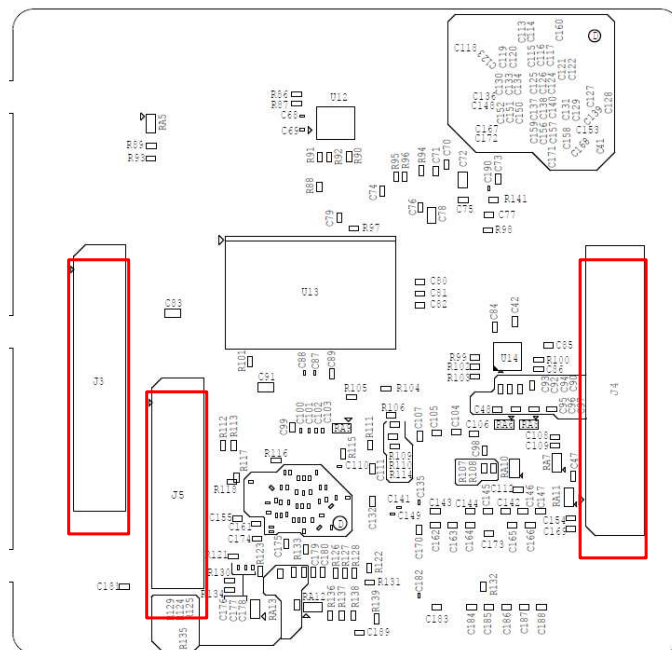


Figure 4-4. TMDSCSK388 Connectors (Bottom)


4.2.1 UFL Connector (J1 and J2)

Table 4-2 provides the UFL connector information.

Table 4-2. UFL Connector J1 and J2

Number	Pin Description	Remarks
1	RF_ANT1	Signal
2	GND	Ground
3	GND	Ground

4.2.2 Board-to-Board Male Connector (J3)

Table 4-3 provides the board-to-board male connector information for J3.

Table 4-3. Board-to-Board Male Connector (J3)

Number	Pin Description	Pin Description in CC (J3)
1	DM388_CAM_DAT0	BB_CAM_DAT0
2	DM388_HDMI_CLKN	BB_HDMI_CLKN
3	DM388_CAM_DAT1	BB_CAM_DAT1
4	DM388_HDMI_CLKP	BB_HDMI_CLKP
5	DM388_CAM_DAT2	BB_CAM_DAT2
6	DGND	DGND
7	DM388_CAM_DAT3	BB_CAM_DAT3
8	DM388_HDMI_DN0	BB_HDMI_D0N
9	DM388_CAM_DAT4	BB_CAM_DAT4
10	DM388_HDMI_DP0	BB_HDMI_D0P
11	DGND	DGND
12	DGND	DGND
13	DM388_CAM_DAT5	BB_CAM_DAT5
14	DM388_HDMI_DN1	BB_HDMI_D1N
15	DM388_CAM_DAT6	BB_CAM_DAT6
16	DM388_HDMI_DP1	BB_HDMI_D1P
17	DM388_CAM_DAT7	BB_CAM_DAT7
18	DGND	DGND
19	DM388_CAM_DAT8	BB_CAM_DAT8
20	DM388_HDMI_DN2	BB_HDMI_D2N
21	DM388_CAM_DAT9	BB_CAM_DAT9
22	DM388_HDMI_DP2	BB_HDMI_D2P
23	DM388_CAM_DAT10	BB_CAM_DAT10
24	DGND	DGND
25	DM388_CAM_DAT11	BB_CAM_DAT11
26	DM388_UART1_TXD	BB_EXP_UART_TXD
27	DM388_CAM_DAT12	BB_CAM_DAT12
28	DM388_UART1_RXD	BB_EXP_UART_RXD
29	DM388_CAM_DAT13	BB_CAM_DAT13
30	DM388_EMU0	BB_EMU0
31	DM388_CAM_DAT14	BB_CAM_DAT14
32	DM388_EMU1	BB_EMU1
33	DGND	DGND
34	DGND	DGND
35	DM388_CAM_DAT15	BB_CAM_DAT15
36	DM388_TMS	BB_FT2232_TMS
37	DM388_CAM_HS	BB_CAM_HS
38	DM388_TCLK	BB_FT2232_TCK
39	DM388_CAM_VS	BB_CAM_VS
40	DM388_RTCK	BB_FT2232_RTCK
41	DM388_CAM_FLD	NC
42	DM388_TRSTn	BB_FT2232_TRSTN
43	DM388_CAM_PCLK	BB_CAM_PCLK
44	DM388_TDI	BB_FT2232_TDI
45	DM388_CAM_WEn	NC

Table 4-3. Board-to-Board Male Connector (J3) (continued)

Number	Pin Description	Pin Description in CC (J3)
46	DM388_TDO	BB_FT2232_TDO
47	DM388_CAM_RESET	BB_CAM_RESET
48	DM388_WARM_RSTn	BB_WARM_RESET
49	DM388_CAM_STROBE	NC
50	DM388_RSTOUT	BB_RSTOUTn
51	DM388_CAM_SHUTTER	NC
52	DM388_GP0[9]	BB_LED5
53	TV_OUT0	BB_TVOUT0
54	CC_RST	BB_PORn
55	DGND	DGND
56	DGND	DGND
57	DM388_USB1_VBUSIN	NC
58	DM388_USB0_VBUSIN	BB_USB0_VBUSIN
59	DM388_USB1_DP	NC
60	DM388_USB0_ID	BB_USB0_ID
61	DM388_USB1_DM	NC
62	DM388_USB0_DM	BB_USB0_DM
63	DM388_USB1_DRVVBUS	NC
64	DM388_USB0_DP	BB_USB0_DP
65	DM388_USB1_ID	NC
66	DM388_USB0_DRVVBUS	BB_USB0_DRVVBUS
67	DGND	DGND
68	DM388_SPI[0]_SCLK	BB_EXP_SPI_SCLK
69	DM388_UART0_TXD	BB_FT2232_UART_RX
70	DM388_SPI0_SCS[0]n	BB_EXP_SPI_SCS
71	DM388_UART0_RXD	BB_FT2232_UART_TX
72	DM388_SPI[0]_D[0]	BB_EXP_SPI_D0
73	OSC_WAKE	BB_OSC_WAKEUP
74	DM388_SPI[0]_D[1]	BB_EXP_SPI_D1
75	DM388_MMC1_SDCD	BB_SD0_CD
76	DM388_MMC1_DAT3	BB_SD0_DAT3
77	DGND	DGND
78	DGND	DGND
79	DM388_MCA[1]_AHCLKX	BB_AIC_MCLK
80	DM388_MMC1_CLK	BB_SD0_CLK
81	DM388_McASP1_ACLKX	BB_AIC_BCLK
82	DM388_MMC1_CMD	BB_SD0_CMD
83	DM388_McASP1_AFSX	BB_AIC_WCLK
84	DM388_MMC1_DAT0	BB_SD0_DAT0
85	DM388_McASP1_AXR0	BB_AIC_DIN
86	DM388_MMC1_DAT1	BB_SD0_DAT1
87	DM388_McASP1_AXR1	BB_AIC_DOUT
88	DM388_MMC1_DAT2	BB_SD0_DAT2

4.2.3 Board-to-Board Male Connector (J4)

Table 4-4 provides the board-to-board connector information for J4.

Table 4-4. Board-to-Board Male Connector (J4)

Number	Pin Description in SOM	Pin Description in CC (J4)
1	DM388_GMII_TXD[7]	BB_ETH_TX_D7
2	DM388_I2C2_SCL	BB_I2C_SCL
3	DM388_GMII_TXD[6]	BB_ETH_TX_D6
4	DM388_I2C2_SDA	BB_I2C_SDA
5	DM388_GMII_TXD[5]	BB_ETH_TX_D5
6	DM388_HDMI_CEC	BB_HDMI_CEC
7	DM388_GMII_TXD[4]	BB_ETH_TX_D4
8	DM388_HDMI_HPDET	BB_HDMI_HPDET
9	DM388_GMII_TXD[3]	BB_ETH_TX_D3
10	DM388_PMIC_PWRON	BB_PMIC_POR
11	DGND	DGND
12	DGND	DGND
13	DM388_GMII_TXD[2]	BB_ETH_TX_D2
14	DM388_GMII_CRS	BB_ETH_CS
15	DM388_GMII_TXD[1]	BB_ETH_TX_D1
16	BB_VCC3V3	VCC_3V3
17	DM388_GMII_TXD[0]	BB_ETH_TX_D0
18	BB_VCC3V3	VCC_3V3
19	DM388_GMII_MTCLK	BB_ETH_TX_CLK
20	BB_VCC3V3	VCC_3V3
21	DM388_GP3[4]	BB_EXP_GP0[30]
22	VCC_CAM	VCC_CAM
23	DGND	DGND
24	TPS_VDDA_1V8	VCC_1V8
25	DM388_GMII_GMTCLK	BB_ETH_GTX_CLK
26	NC	NC
27	DM388_GMII_TXEN	BB_ETH_TX_EN
28	DGND	DGND
29	DM388_HDMI_SCL	BB_HDMI_CODECS_SCL
30	DM388_McASP0_AXR2	BB_EXP_GP1[26]
31	DM388_HDMI_SDA	BB_HDMI_CODECS_SDA
32	DM388_McASP0_AXR3	BB_EXP_GP0[29]
33	DGND	DGND
34	DGND	DGND
35	DM388_MDIO_CLK	BB_ETH_MDC
36	DM388_McASP0_AXR4	BB_EXP_GP1[25]
37	DM388_MDIO_DAT	BB_ETH_MDIO
38	DM388_CSI_DX0	BB_EXP_CSI_DX0
39	DM388_GMII_RCLK	BB_ETH_RX_CLK
40	DM388_CSI_DY0	BB_EXP_CSI_DY0
41	DM388_GMII_RXDV	BB_ETH_RX_DV
42	DGND	DGND
43	DM388_GMII_RXER	BB_ETH_RX_ER
44	DM388_CSI_DX1	BB_EXP_CSI_DX1
45	DGND	DGND

Table 4-4. Board-to-Board Male Connector (J4) (continued)

Number	Pin Description in SOM	Pin Description in CC (J4)
46	DM388_CSI_DY1	BB_EXP_CSI_DY1
47	DM388_GMII_RXD[0]	BB_ETH_RX_D0
48	DGND	DGND
49	DM388_GMII_RXD[1]	BB_ETH_RX_D1
50	DM388_CSI_DX2	BB_EXP_CSI_DX2
51	DM388_GMII_RXD[2]	BB_ETH_RX_D2
52	DM388_CSI_DY2	BB_EXP_CSI_DY2
53	DM388_GMII_RXD[3]	BB_ETH_RX_D3
54	DM388_GMII_COL	BB_ETH_COL
55	DGND	DGND
56	DGND	DGND
57	DM388_GMII_RXD[4]	BB_ETH_RX_D4
58	DM388_CSI_DX3	BB_EXP_CSI_DX3
59	DM388_GMII_RXD[5]	BB_ETH_RX_D5
60	DM388_CSI_DY3	BB_EXP_CSI_DY3
61	DM388_GMII_RXD[6]	BB_ETH_RX_D6
62	DGND	DGND
63	DM388_GMII_RXD[7]	BB_ETH_RX_D7
64	DM388_CSI_DX4	BB_EXP_CSI_DX4
65	DGND	DGND
66	DM388_CSI_DY4	BB_EXP_CSI_DY4
67	DM388_GP1[30]	BB_LED1
68	EN_LS_3V3	BB_uPIO_PWR_EN
69	DM388_GP1[24]	BB_LED2
70	DM388_MMC1_DAT6/GP0_12	BB_SWITCH1
71	DM388_GP1[25]	BB_LED3
72	DM388_MMC1_DAT7/GP0_13	BB_SWITCH2
73	DM388_GP3[3]	BB_LED4
74	DM388_GP1[14]	BB_EXP_GP0[31]
75	DM388_GP1[10]	BB_SWITCH3
76	PMIC_3V3	PMIC_3V3
77	DGND	DGND
78	DGND	DGND
79	DM388_McASP0_AXR5	BB_SWITCH4
80	PMIC_3V3	PMIC_3V3
81	ENET_RSTn	BB_ETH_RESET
82	PMIC_3V3	PMIC_3V3
83	VCC_5V0	DC_VCC5V0
84	PMIC_3V3	PMIC_3V3
85	VCC_5V0	DC_VCC5V0
86	PMIC_3V3	PMIC_3V3
87	VCC_5V0	DC_VCC5V0
88	PMIC_3V3	PMIC_3V3

4.2.4 Board-to-Board Termination (J5)

Table 4-5 provides the board-to-board termination information for J5.

Table 4-5. Board-to-Board Termination (J5)

Pin Number	Pin Description	Pin Number	Pin Description
1	DM388_PCl_e_RXP0	34	DGND
2	TPS_INT1	35	DM388_UART2_TXD
3	DM388_PCl_e_RXN0	36	HDDAC_HSYNC
4	DM388_MMC2_DAT3	37	DM388_UART0_RTSn
5	DGND	38	HDDAC_VSYNC
6	DM388_MMC2_DAT4	39	DM388_UART0_CTSn
7	DM388_PCl_e_TXP0	40	DM388_VIN[0]A_CLK
8	DM388_MMC2_CMD	41	HDDAC_C
9	DM388_PCl_e_TXN0	42	DM388_VIN[0]A_DE
10	DM388_MMC2_DAT2	43	VBACKUP
11	DGND	44	DM388_VIN[0]B_CLK
12	DGND	45	DM388_VIN[0]A_D[10]_BD[2]
13	DM388_SERDES_CLKP	46	DM388_VIN[0]A_D[0]
14	DM388_MMC2_DAT5	47	DM388_VIN[0]A_D[8]_BD[0]
15	DM388_SERDES_CLKN	48	DM388_VIN[0]A_D[9]_BD[1]
16	DM388_MMC2_DAT6	49	DM388_VIN[0]A_D[1]
17	DGND	50	DM388_VIN[0]A_D[2]
18	DM388_MMC2_DAT7	51	DM388_VIN[0]A_D[12]_BD[4]
19	DM388_VIN[0]A_VSYNC	52	DM388_VIN[0]A_D[3]
20	DM388_MMC2_SCLK	53	DM388_VIN[0]A_D[5]
21	DM388_McASP1_ACLKR	54	DM388_VIN[0]A_D[4]
22	DM388_MMC2_DAT1	55	DGND
23	DM388_McASP0_ACLKR	56	DGND
24	DM388_MMC2_DAT0	57	DM388_VIN[0]A_D[7]
25	DM388_McASP0_AFSR	58	DM388_USB0_CE
26	DM388_VIN[0]A_FLD	59	DM388_VIN[0]A_D[6]
27	DM388_McASP1_AFSR	60	DM388_USB1_CE
28	HDDAC_A	61	DM388_SPI1_SCS[0]n
29	DM388_SPI1_D[1]	62	DM388_SPI1_D[0]
30	HDDAC_B	63	DGND
31	DM388_SPI1_SCLK	64	DGND
32	DM388_VIN[0]A_HSYNC	65	DGND
33	DGND	66	DGND

4.3 Switches, Test Points, and LEDs

The TMDSCSK388 module has one switch for selecting boot mode. Users can select NAND boot or SD boot by turning switch SW1 to ON or OFF. [Table 4-6](#) provides the module switch information.

Table 4-6. TMDSCSK388 Module Switch Information

Switch Number	Description		
SW1	SWITCH1	ON	MMC BOOT
		OFF	NAND

[Table 4-7](#) provides the test points available on the DM388 module.

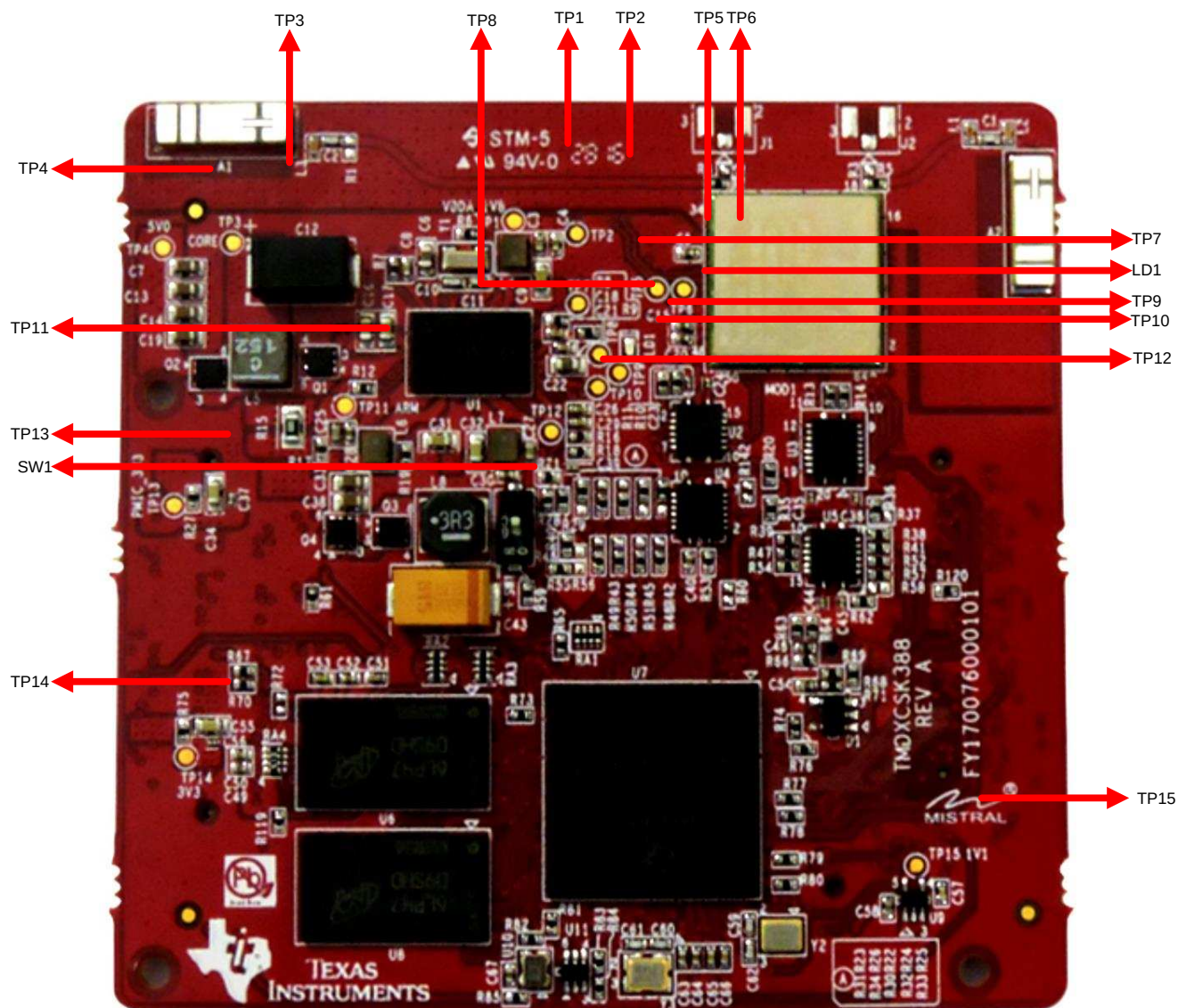
Table 4-7. TMDSCSK388 Test Points

Test Point	Signal
TP1	TPS_VDDA_1V8
TP2	HDRST
TP3	TPS_CORE_CVDD
TP4	VCC_5V0
TP5	BT_UART_DBG
TP6	WL_UART_DBG
TP7	TPS_VDAC_1V8
TP8	TPS_INT1
TP9	PWRHOLD
TP10	GPIO6
TP11	TPS_CVDD_ARM
TP12	GPIO2
TP13	PMIC_3V3
TP14	VCC_3V3
TP15	TPS_VHD_1V1

The TMDSCSK388 provides one green LED (LD1) for power indication. This LED provides the status of the 5-V power input from the CSK carrier card.

Figure 4-5 shows the position of the LED, test points, and switches on the board.

Figure 4-5. LED, Test Points, and Switches



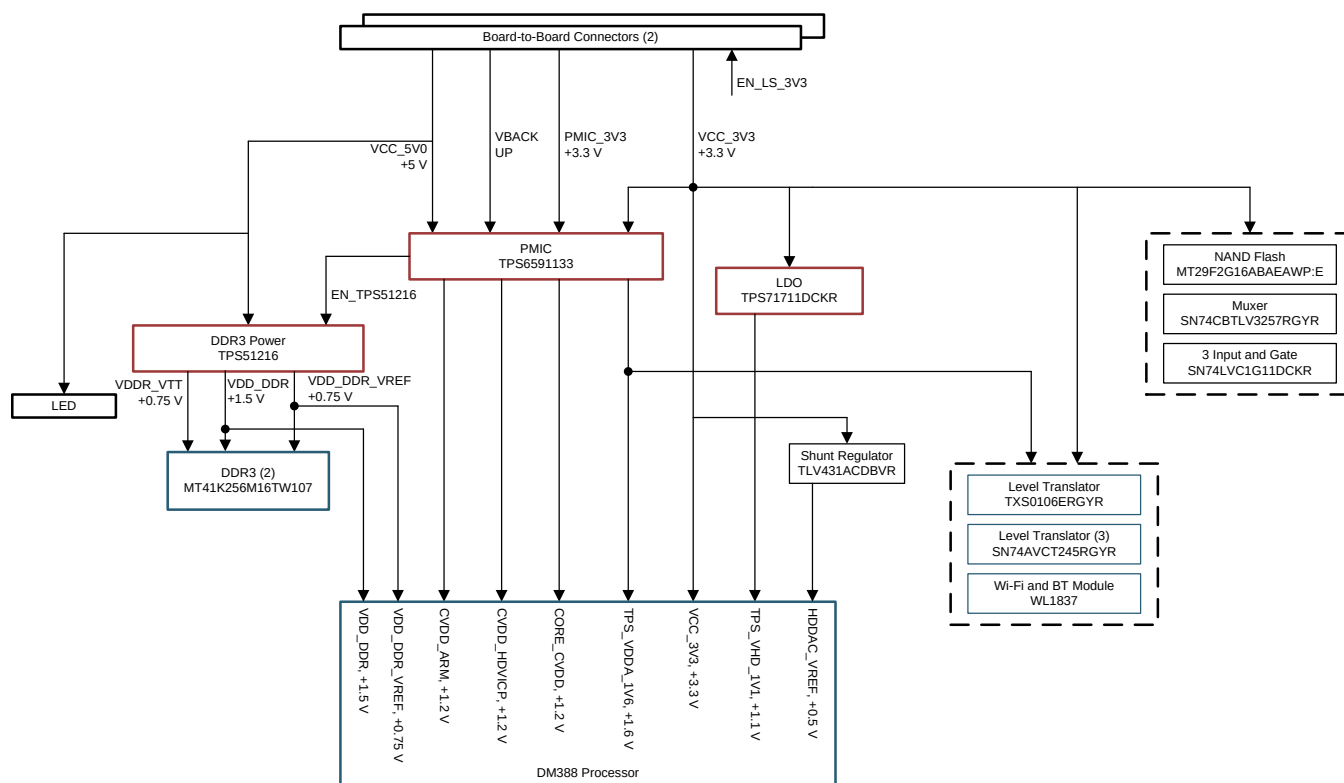
TMDSCSK388 Power Requirements

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5.3 Power-up Sequence.....	43

5.1 Power Distribution

Figure 5-1 shows the power distribution diagram.

Figure 5-1. Power Distribution



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5.2 Power Supply Calculation

Table 5-1 provides the power supply calculations.

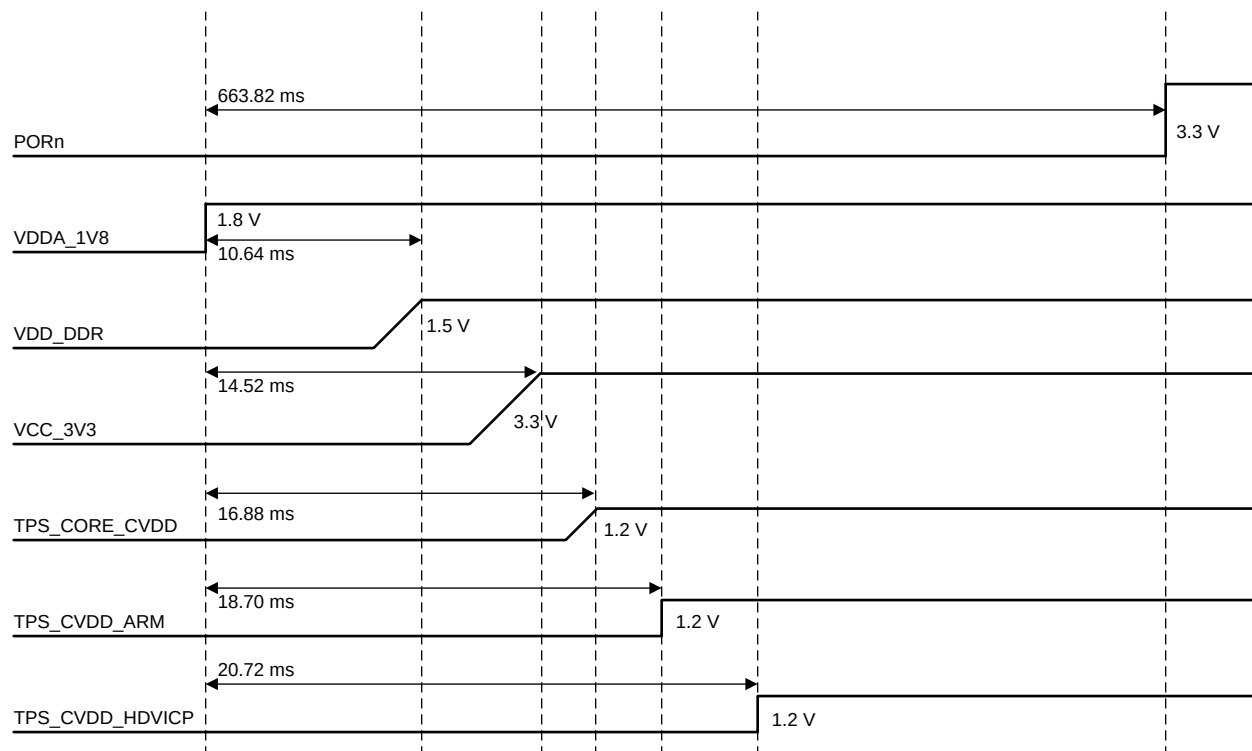
Table 5-1. Power Supply Calculations

Part Number	Quantity	CVDD CORE_CVDD	CVDD_ARM PMIC VDD1	CVDD_HDVI CP PMIC VDD2	VDD_1V8 PMIC VIO	TPS51216 VCC_1V5	TPS71711DC KR TPS VHD 1V1	VCC_3V3 Carrier Card	DDR_VIT 0.75	PMIC_3V3	VCC_5V0
TMS320DM388	1	1125	365	0	53	402	150	139		382.6968984	
DDR3 MT41K256M16T W	4					520			272		
MT29F4G16ABA EAWP	1							30			
TXS0108EPWR	1				.036	.036		.108			
WL1837MOD	1							909.0909091			
SN74AVC4T245 RGYR	3				300			300			
SN74LVC1G11D CKR	1							100			
SN74CBTLV3257 RGYR	1							128			
LED	1										
Total (mA)		1125	365	0	353.036	922.036		1606.198909	272	382.6968984	320.6470588
Input Voltage		5	3.3	3.3	3.3	5	3.3	5	1.5	5	5
Efficiency		0.85	0.85	0.8	0.85	0.8		0.85	0.85	0.85	0.75
Quiescent current (mA)											
Output voltage		1.2	1.2	1.2	1.8	1.5	1.1	3.3	0.75	3.3	3.3
Current drawn from input		317.6470588	156.1497326	0	226.5471658	345.7635	150	1247.166212	160	297.1528858	504
Current drawn from VCC_5V0	2210.72965 6 mA										

5.3 Power-up Sequence

Figure 5-2 shows the power-up sequence required for the processor.

Figure 5-2. Power Sequencing



Overview of TMDSCSKCC

Topic	Page
6.1 Key Features	45
6.2 Block Diagram	46
6.3 Power Supply	49
6.4 Overvoltage Protection Circuit.....	50

6.1 Key Features

The camera starter-kit carrier card is a standalone development platform that enables users to exhibit the video processing capabilities of the TMS320DM388, TMS320DM8127, and TMS320DM369 processors and the peripherals. The CSK carrier-card interfaces to processor modules such as the TMDSCSK388, TMDSCSK8127, and TMDSCSK369. The key features of the CSK carrier card are:

- Board-to-board connectors for the DMX processor module
- Micro SD card slot
- Audio codec (TLV320AIC3104IRHBR)
- Micro USB connector
- 4 user keys and 5 LEDs
- 2 reset switches and 1 oscillator wake-up switch
- On-board XDS100 JTAG emulator
- FTDI chip FT2232HL for JTAG and UART through a micro USB connector
- Audio line-in (MIC) and headphone out
- Powered through a 5-V DC jack

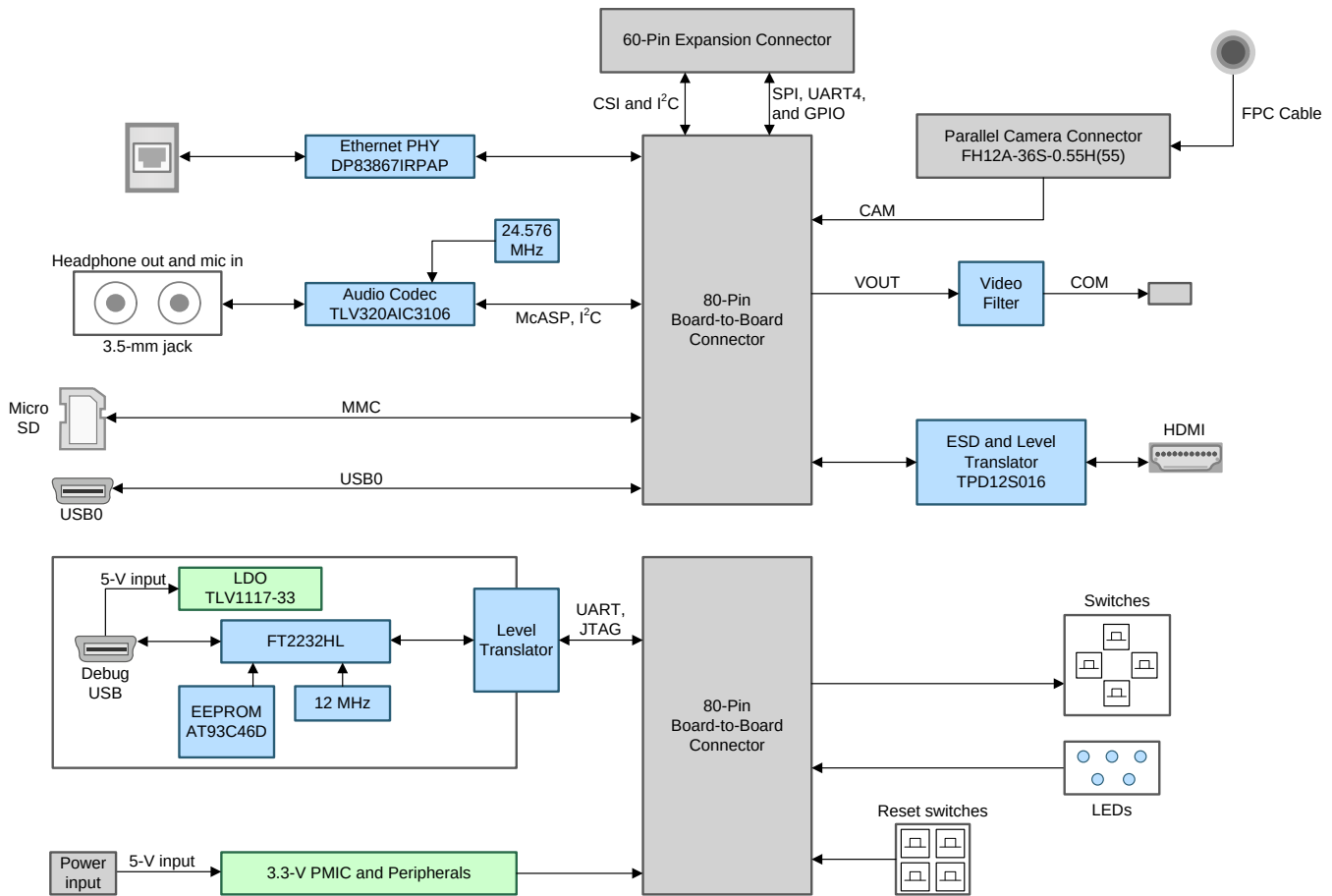
The key features of the WDR HD camera module (LI-CAM-AR0331-324-1.8) are:

- 1/3-inch, 3.1-megapixel CMOS high-definition digital imager
- Active imaging pixels: 2052 H x 1536 V
- Pixel size: 2.2 μm $\times$ 2.2 μm
- 12-bit digital output with line and frame synchronization
- Support for 1080p at 60 fps
- Simple two-wire serial interface
- Maximum dynamic range: up to 100 dB
- Low-noise CMOS imaging technology that achieves CCD image quality
- Direct interface to the TI IP-Camera

6.2 Block Diagram

Figure 6-1 shows the block diagram of the CSK carrier card.

Figure 6-1. CSK Carrier Card Block Diagram



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Figure 6-2 shows the top view of the CSK carrier card.

Figure 6-2. CSK Carrier Card (Top)

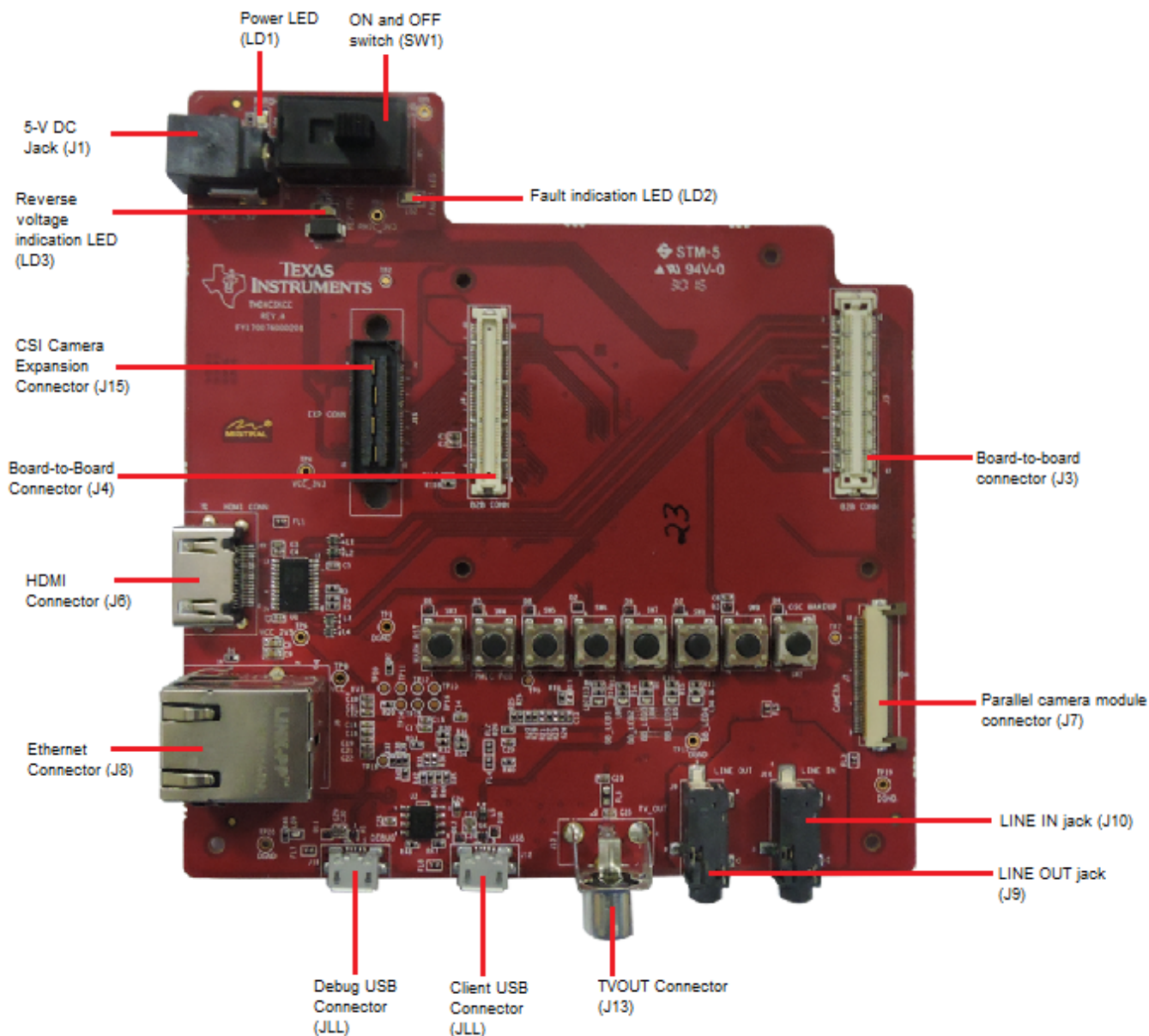
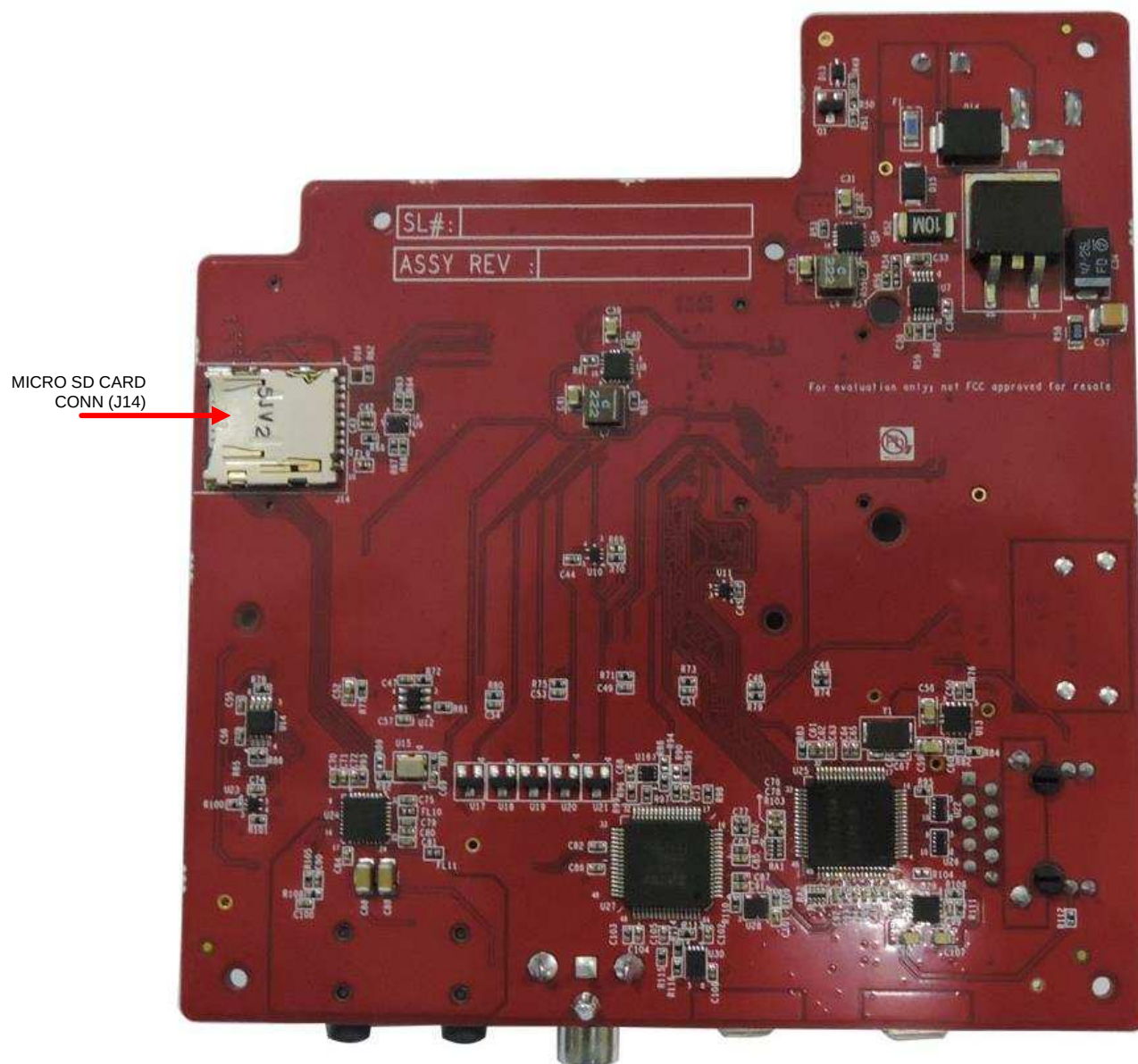


Figure 6-3 shows the bottom view of the CSK carrier card.

Figure 6-3. CSK Carrier Card (Bottom)



6.3 Power Supply

The CSK carrier card is powered through a 5-V DC jack. The power enable from the board-to-board connector enables +3.3 V. The +3.3-V input is converted into the required supply voltages by using the regulator. [Table 6-1](#) provides the regulators that are used on the CSK carrier card.

Table 6-1. CSK Carrier Card Regulators

Regulator	Purpose
TPS62142RGTT (U5)	3V3 generation
TPS62142RGTT (U8)	3V3 generation
TPS7A8101DRBT (U29)	2V5 generation
TPS7A8101DRBT (U13)	1V1 generation

- Processor module power: PMIC_3V3
- I/O voltage: VCC_3V3

The TPS62142RGTT (U5) is enabled by default to generate 3.3 V when SW1 is turned ON. This 3.3 V is used to power on the DMx processor module.

Another TPS62142RGTT (U8) is enabled by GPIO, which is driven by the DMx processor to generate the 3.3-V I/O voltage for the CSK carrier card.

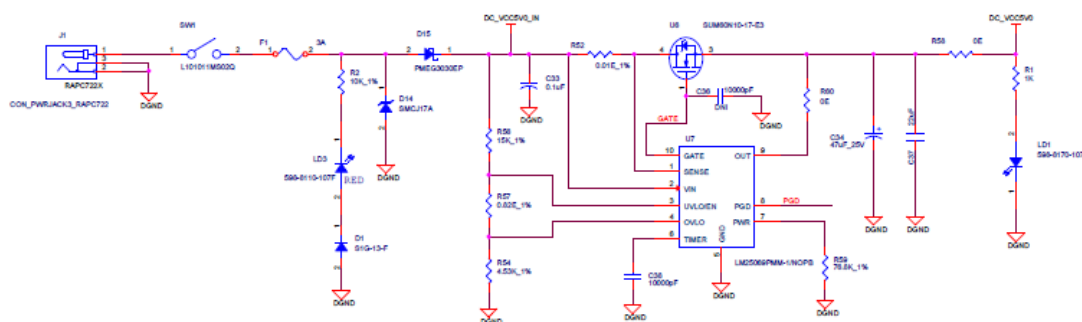
The TPS7A8101DRBT (U13 and U29) regulators are used to generate 1.1 V and 2.5 V, respectively, for Ethernet PHY.

6.4 Overvoltage Protection Circuit

The voltage protection circuit on the CSK carrier card protects the board from overvoltage, undervoltage, transient-voltage, and reverse-voltage input cases. The safe operation input-voltage range is 4.5 V to 5.25 V. Any voltage that is not in this range is considered a fault and the voltage protection circuit isolates the board from this input. LED LD2 indicates if the DC input applied to the board is within a safe input range.

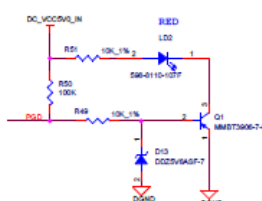
Figure 6-4 shows the overvoltage protection circuit.

Figure 6-4. Overvoltage Protection Circuit



Condition	LED Status (LD3)
Reverse Voltage	ON

Fault Indication



Note:-

When fault is indicated, set to proper voltage and power cycle the board.

Condition	LED Status (LD2)
DC_VCCSV0_IN between 4.5 to 5.25V	OFF
DC_VCCSV0_IN above 5.25V or below 4.5V	ON

CSK Carrier Card Interface

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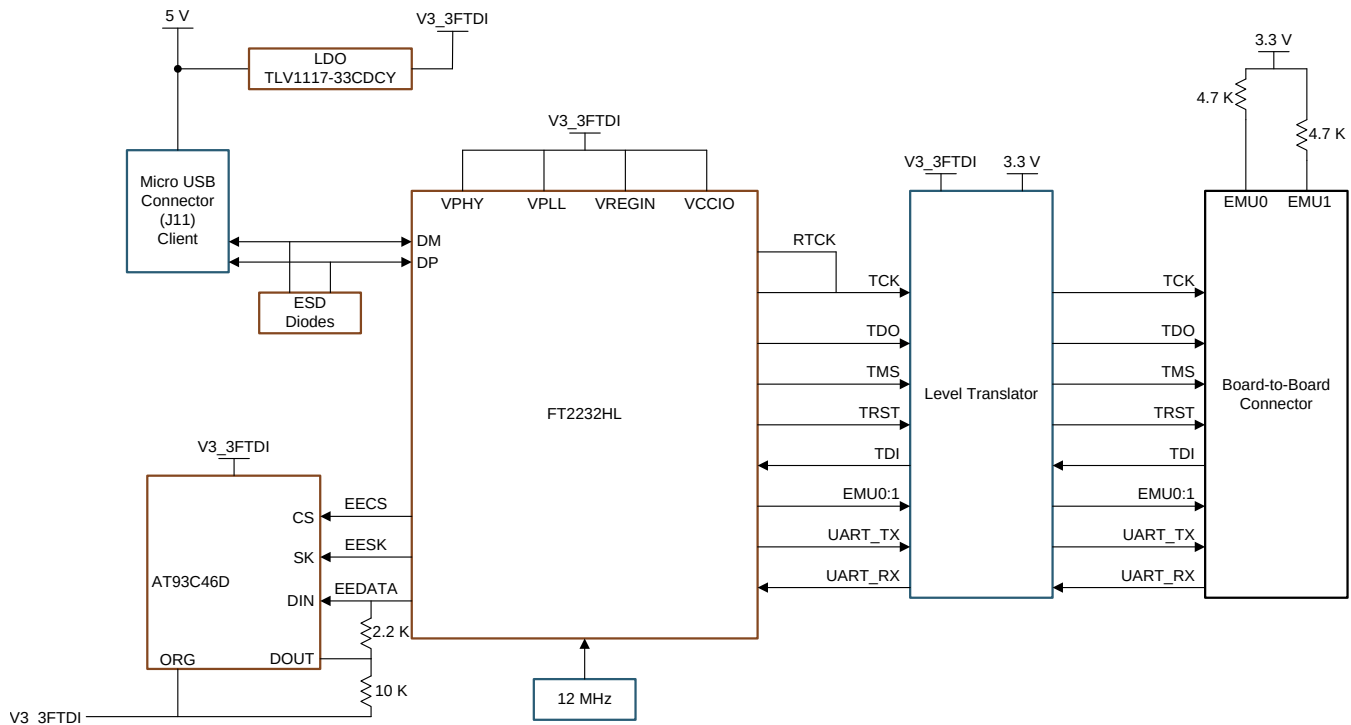
7.1 XDS100 On-Board Emulator Interface

The CSK carrier card contains an on-board XDS100 USB emulator with a FT2232HL chip. One of the FT2232HL ports is configured for UART and JTAG.

All of the JTAG lines are connected to the board-to-board connector using voltage level translators (SN74AVC2T244, SN74AVC4T245 and SN74AVC2T245) because the FT2232HL is powered by the TLV1117-33CDCY LDO (5.0 V to 3.3 V) through the micro USB connector (J11). EEPROM (AT93C46D, 1 Kb) is interfaced to FT2232 to store configuration data.

Figure 7-1 shows the on-board emulator interface.

Figure 7-1. XDS100 On-Board Emulator Interface



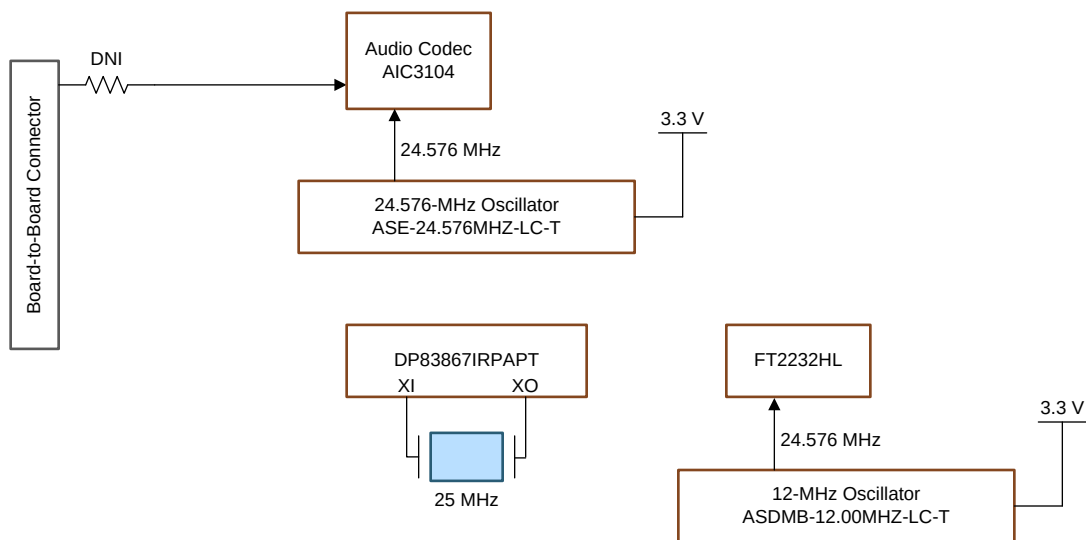
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7.2 Clock Distribution

One 12-MHz oscillator (connected to the UART-to-USB converter [FT2232HL]) and one 24.576-MHz oscillator (connected to the audio codec [AIC3104]) are used in the CSK carrier card. In this configuration, the audio codec is configured as the McASP and McBSP master, and the DMX processor as a McASP and McBSP slave.

Figure 7-2 shows the block distribution diagram.

Figure 7-2. Clock Distribution



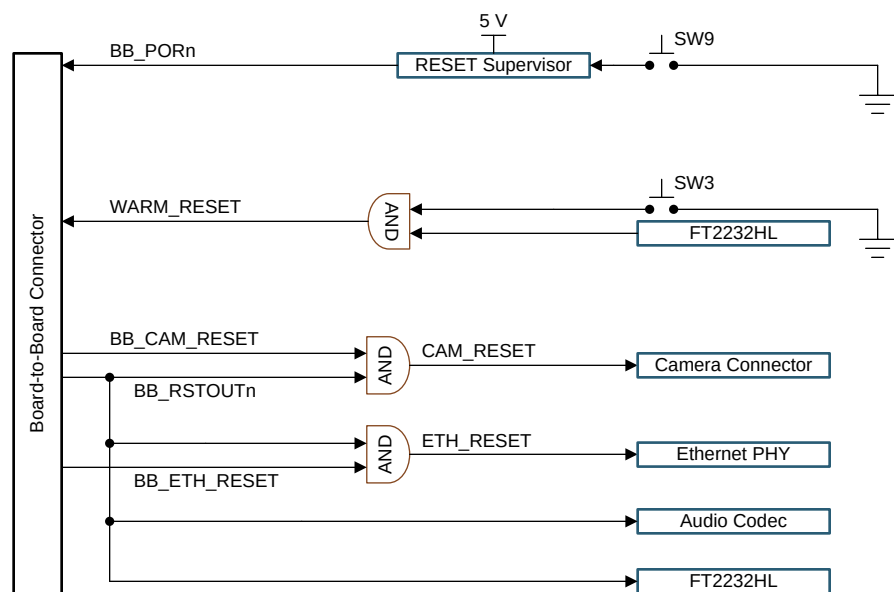
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7.3 Reset Circuit and Distribution

The DMx Processor is reset from switch 9 (PORn), switch 3 (warm reset), or from the system reset (FT2232HL). The DMx processor provides reset out to camera, Ethernet PHY, audio codec, and FT2232HL. The camera module is reset from an AND operation of reset out from the DMx processor and camera reset GPIO. The Ethernet PHY is reset from an AND operation of reset out from the DMx processor and Ethernet reset GPIO. See [Table 3-5](#) to configure GPIOs for camera- and Ethernet-reset functionality.

[Figure 7-3](#) shows the reset circuit and distribution diagram.

Figure 7-3. Reset Circuit and Distribution



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7.4 Camera Interface

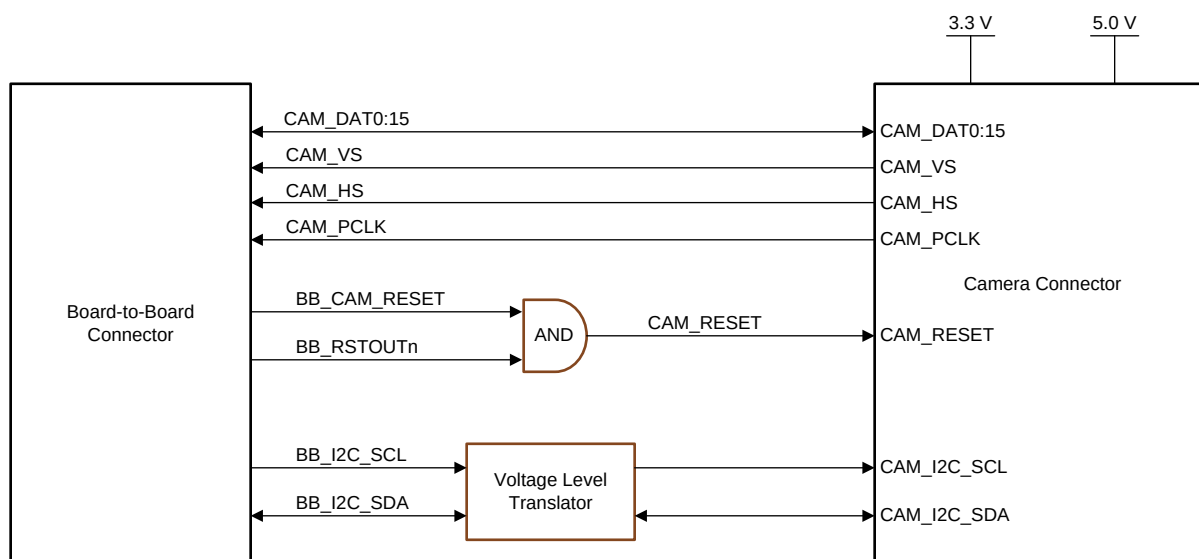
The leopard-imaging camera module (LI-CAM-AR0331-324-1.8) interfaces to the CSK carrier card with a standard 36-pin ZIP connector. The LI-CAM-AR0331-324-1.8 is a high-resolution, wide dynamic range, digital-camera module.

The device incorporates an Aptina 1/3-inch, 3.1M, CMOS WDR digital image sensor (AR0331) with an active-imaging pixel array of 2052H × 1536V. The LI-CAM-AR0331 WDR camera module produces clear, sharp digital pictures, and it is capable of capturing both continuous video and single frames, making it the perfect choice for surveillance industry with high dynamic range video. The camera supports 1080p at 30 fps H.264 streaming on TI's DM385 IPNC platform.

The CSK carrier card also supports the 3.3-V and 1.8-V I²C and RESET camera modules.

Figure 7-4 shows the parallel camera interface.

Figure 7-4. Parallel Camera Interface



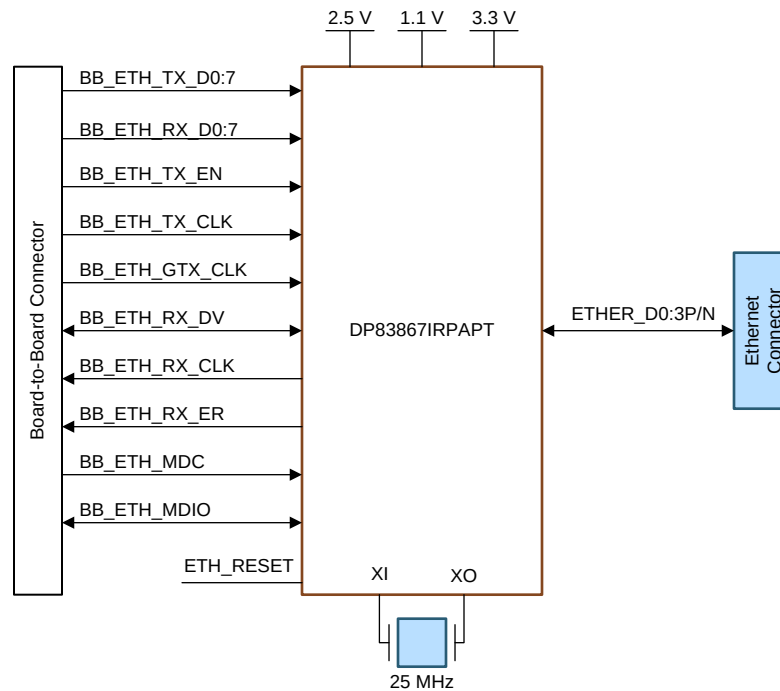
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7.5 Ethernet Interface

The CSK Carrier card supports GMII and MII interfaces (see [Figure 7-5](#)). The DP83867 is a robust, low power, fully featured, physical-layer transceiver with integrated PMD sub-layers to support 10BASE-Te, 100BASE-TX, and 1000BASE-T Ethernet protocols. Optimized for ESD protection, the DP83867 exceeds the 8-kV IEC 61000-4-2 (direct contact) standard. This device interfaces directly to the MAC layer through the IEEE 802.3 MII standard, the IEEE 802.3 GMII standard, or reduced GMII (RGMII).

The DP83867 Ethernet PHY can be configured for GMII (TMDSCSK388 and TMDSCSK8127) or MII (TMDSCSK369) through register configuration. The PHY address of DP83867 is 0x19(h).

Figure 7-5. Ethernet Interface

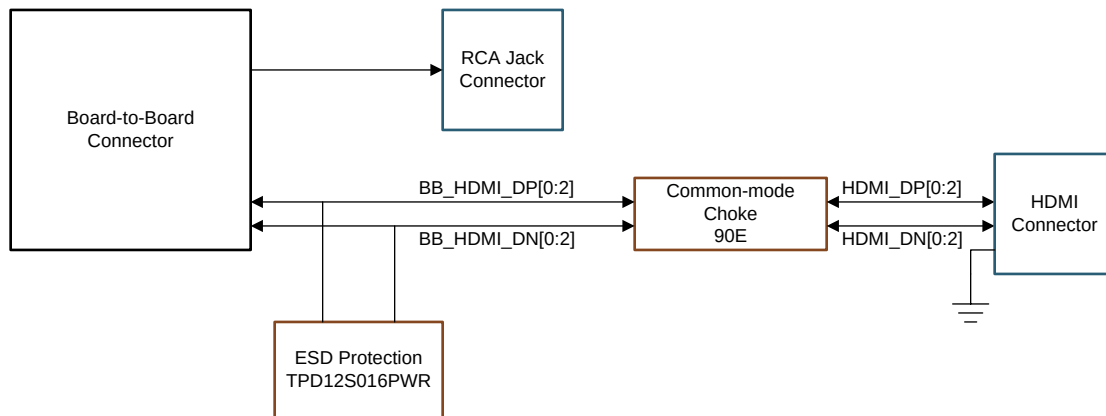


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7.6 HDMI and TVOUT Interfaces

The CSK carrier card supports an HDMI interface, shown in Figure 7-6.

Figure 7-6. HDMI and TVOUT Interface



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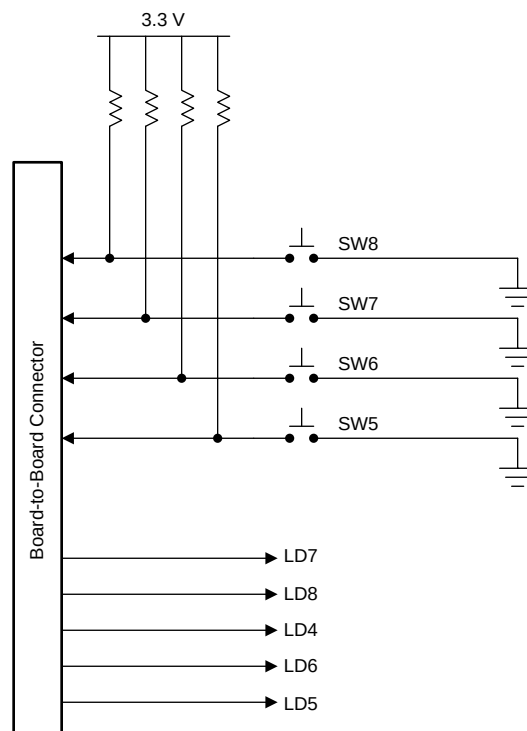
NOTE: The TMDSCSK369 processor module does not support an HDMI interface. Only the TMDSCSK8127 and TMDSCSK388 processor modules support HDMI interfaces.

7.7 LED and Switch Interface

Four push buttons and five green LEDs are provided for user input and status. Refer to to configure GPIOs for switch and LED functionality.

Figure 7-7 shows the switch and LED connections.

Figure 7-7. Switch and LED Connections

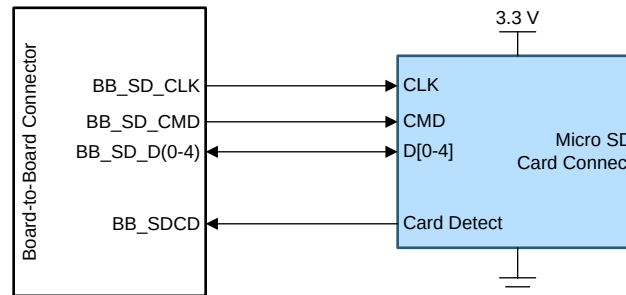


7.8 Micro SD Card Interface

The micro SD card connector is connected to the SD interface of the board-to-board connector, shown in [Figure 7-8](#).

The card-detect pin from the SD card connector is connected to the GPIO to ensure the presence of the SD card.

Figure 7-8. Micro SD Card Interface



Refer to [Section 7.13](#) for SD card connection details, and to [Table 3-5](#) to configure the GPIO for SD card detect.

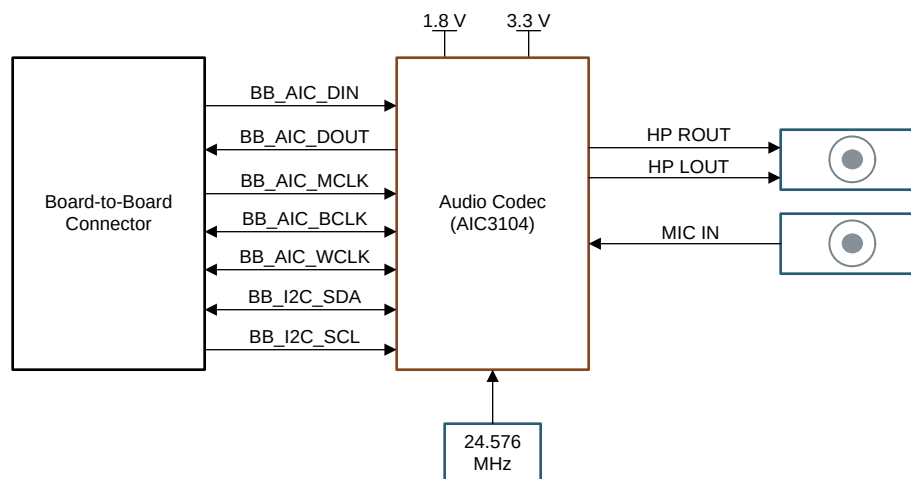
7.9 Audio Codec Interface

The TLV320AIC3104 device is a flexible, low power, low-voltage stereo audio codec with programmable inputs and outputs, PowerTune™ codec capabilities, fixed predefined and parameterizable signal processing blocks, integrated PLL, and flexible digital interfaces.

This audio codec is interfaced to the I2S2 port and I²C of the TMS320DMx processor modules. The codec supports McASP and McBSP configurations. A 24.576-MHz optional oscillator is provided for master clock generation. The audio line in and line out is provided through 3.5-mm audio jacks.

[Figure 7-9](#) shows the audio codec interface.

Figure 7-9. Audio Codec Interface



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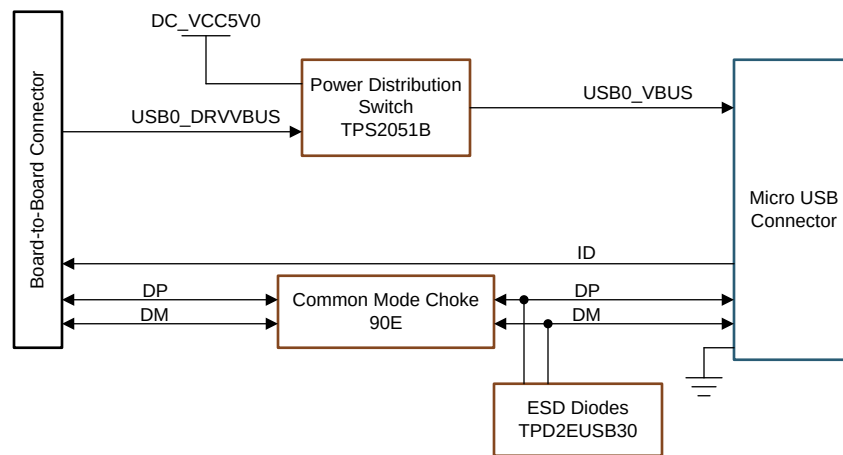
7.10 USB Interface

The TMS320DMx processor modules support a USB host and device controller that provides a low-cost connectivity solution for consumer portable devices by providing a mechanism for data transfer to a USB host up to 480 Mbps. The USB controller complies with the USB 2.0 standard high-speed and full-speed functions.

The USB signals of the CSK carrier card are terminated at micro USB B-type connector J12, shown in [Figure 7-10](#). ESD diodes are provided for the USB signals. The USB ID pin on the connector is connected to the USB ID pin of the TMS320DMx processors for host and device configuration.

The drive-bus signal (USB0_DRVVBUS) from the TMS320DMx processor controls the power distribution switch (TPS2051B), which supplies VBUS (+5 V) from the CSK carrier card to the USB device that is connected to the micro USB connector. By default, the power distribution switch is disabled (pulled low). The DMx processor should drive the USB0_DRVVBUS signal high to enable the power distribution switch. The TPS2051B supports a maximum current of 500 mA at 5 V from the CSK carrier card.

Figure 7-10. USB Interface

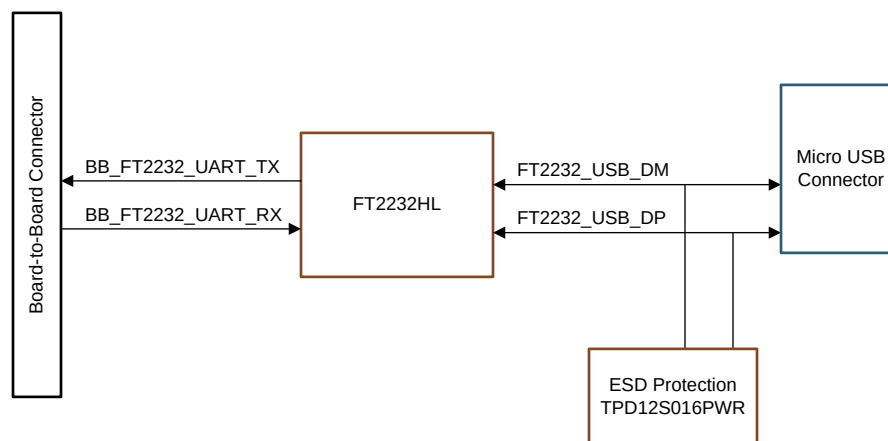


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7.11 UART Interface

The UART interfaces of the board-to-board connector is connected to the FT2232 chip (for UART to USB functionality), shown in [Figure 7-11](#).

Figure 7-11. UART Interface



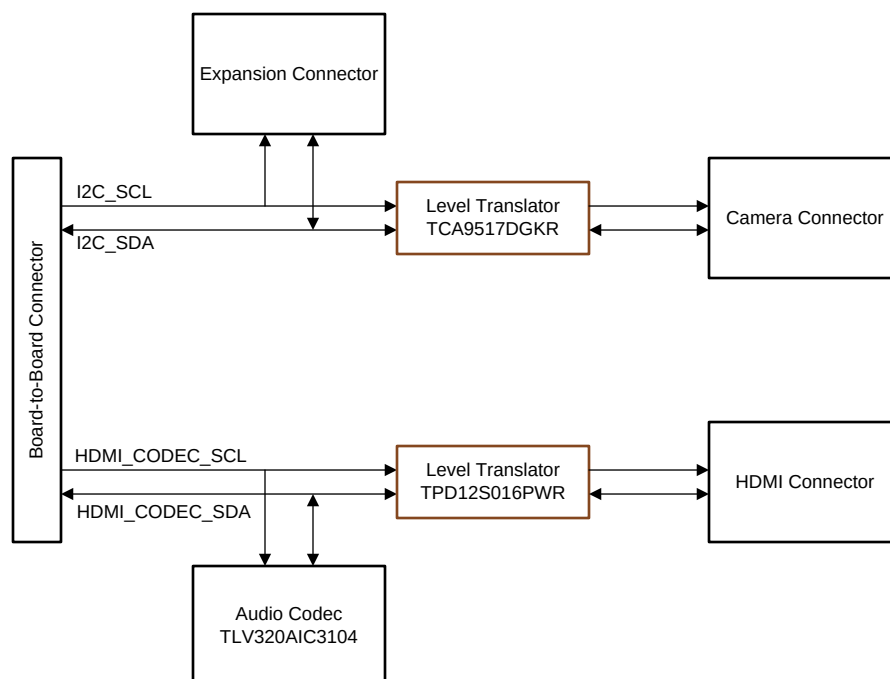
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7.12 I²C Interface

The CSK carrier card supports an I²C interface that is connected through the expansion connector and a camera connector using a level translator (TCA9517DGKR) and a board-to-board connector, shown in [Figure 7-12](#).

Another I²C interface from the board-to-board connector is connected to the audio codec and HDMI connector from level translator TPD12S016PWR.

Figure 7-12. I²C Interface

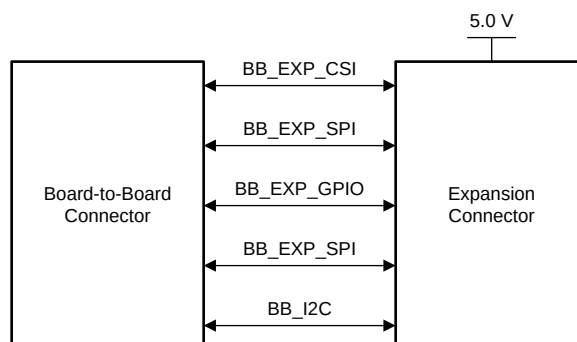


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7.13 Connection Between Expansion Connector and CSK Carrier Card

The CSK carrier card supports CSI, SPI, I²C, UART, and GPIO interfaces that are connected to the expansion connector interface from the board-to-board connector, shown in [Figure 7-13](#).

Figure 7-13. Expansion Connector Interface



NOTE: The TMDSCSK369 processor module does not support CSI and UART interfaces, shown in [Figure 7-13](#). Only TMDSCSK8127 and TMDSCSK388 processor modules support CSI and UART interfaces from the board-to-board connector to the expansion connector.

CSK Carrier Board Physical Specifications

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8.1 Board Layout

The CSK carrier card dimension is 4.4 inches × 4.724 inches (116 mm × 37.94 mm). The CSK carrier card has six layers and is powered through connector J1.

Figure 8-1 and Figure 8-2 show the top and bottom views of the assembly layout, respectively.

Figure 8-1. CSK Carrier Card Assembly Layout (Top)

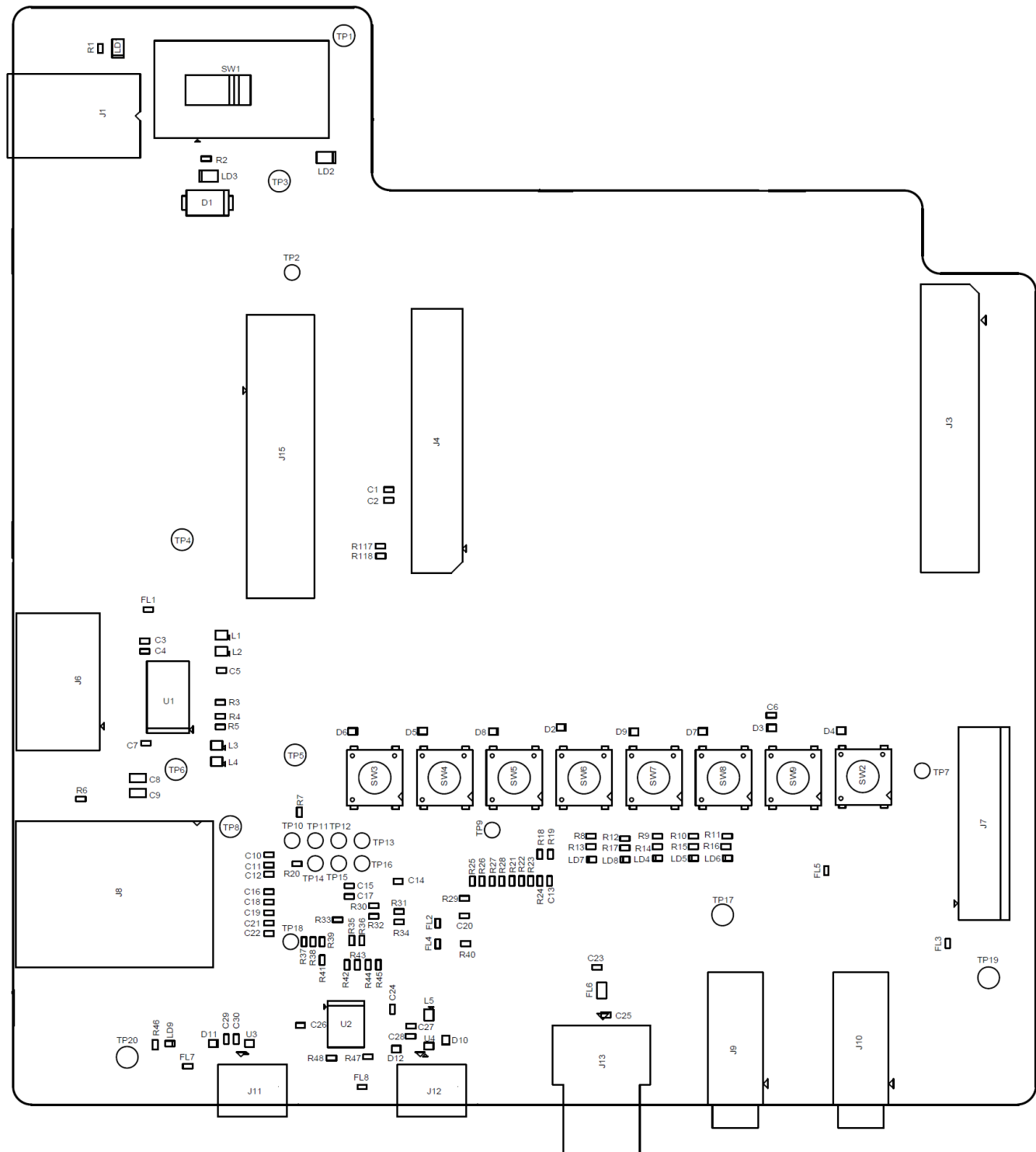
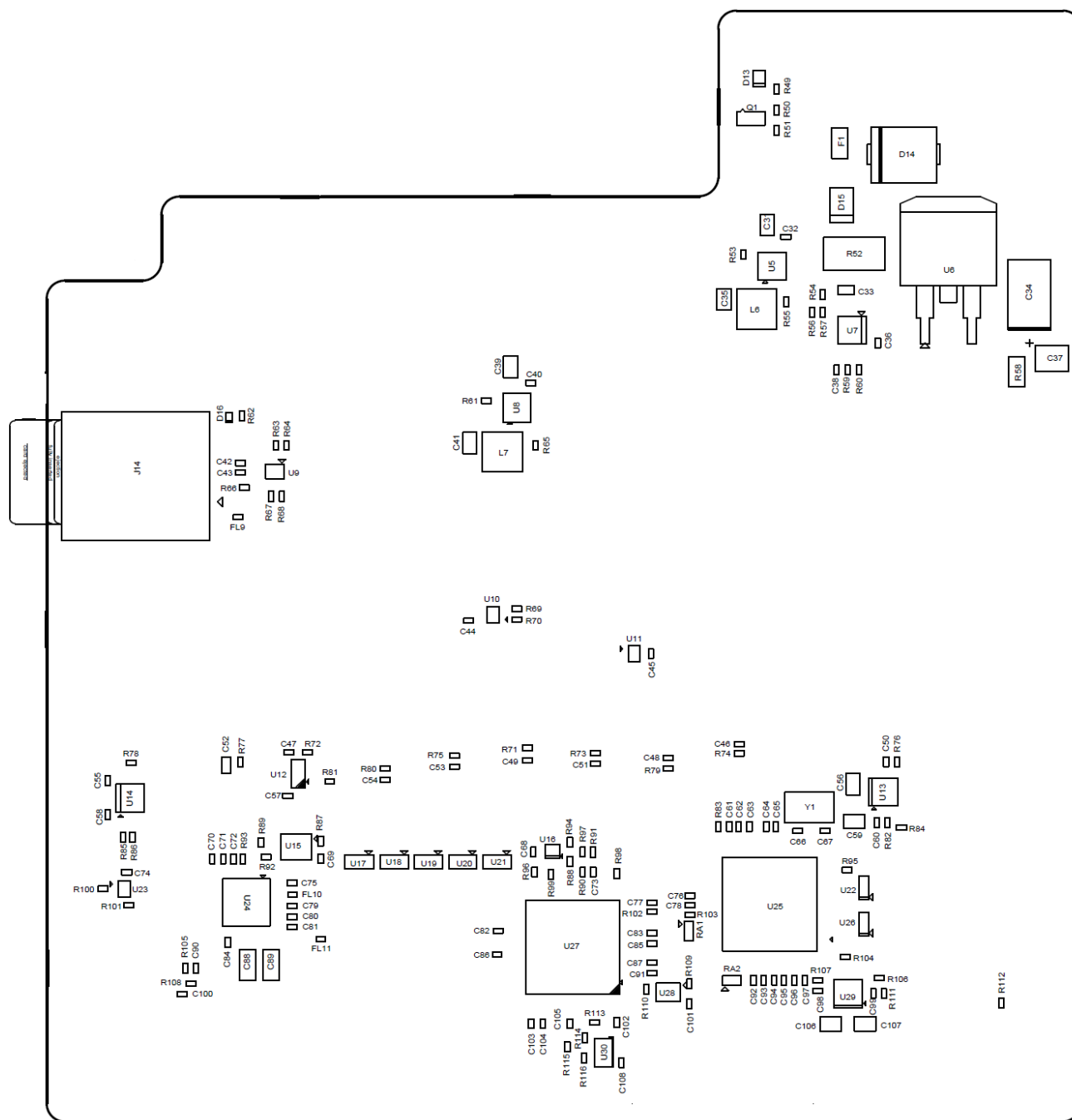


Figure 8-2. CSK Carrier Card Assembly Layout (Bottom)



8.2 Connector Index

The CSK carrier card has several connectors that provide access to various interfaces on the board. [Table 8-1](#) shows the CSK carrier card connectors.

Table 8-1. CSK Carrier Card Connectors

Connector	Part Number	Pins	Functions
J1	RAPC722X	3	DC power jack
J3	FX11LA-80S/8-SV(71)	88	Board-to-board connector
J4	FX11LA-80P/8-SV(71)	88	Board-to-board connector
J15	QSH-030-01-L-D-A	64	Expansion connector
J6	10029449-001RLF	23	HDMI out type-A connector
J7	FH12A-36S-0.5SH(55)	36	Camera FPC connector
J8	LPJG16314A4NL	16	RJ45 connector
J9	STX-3500-4NTR	4	Stereo-audio jack
J10			
J11	ZX62-AB-5PA(31)	5	Micro USB connector
J12			
J13	RCJ-014	4	Composite video-out RCA connector
J14	DM3AT-SF-PEJM5	14	Micro SD card connector

Figure 8-3 and Figure 8-4 show the top and bottom connectors, respectively, on the CSK carrier card.

Figure 8-3. CSK Carrier Card Connectors (Top)

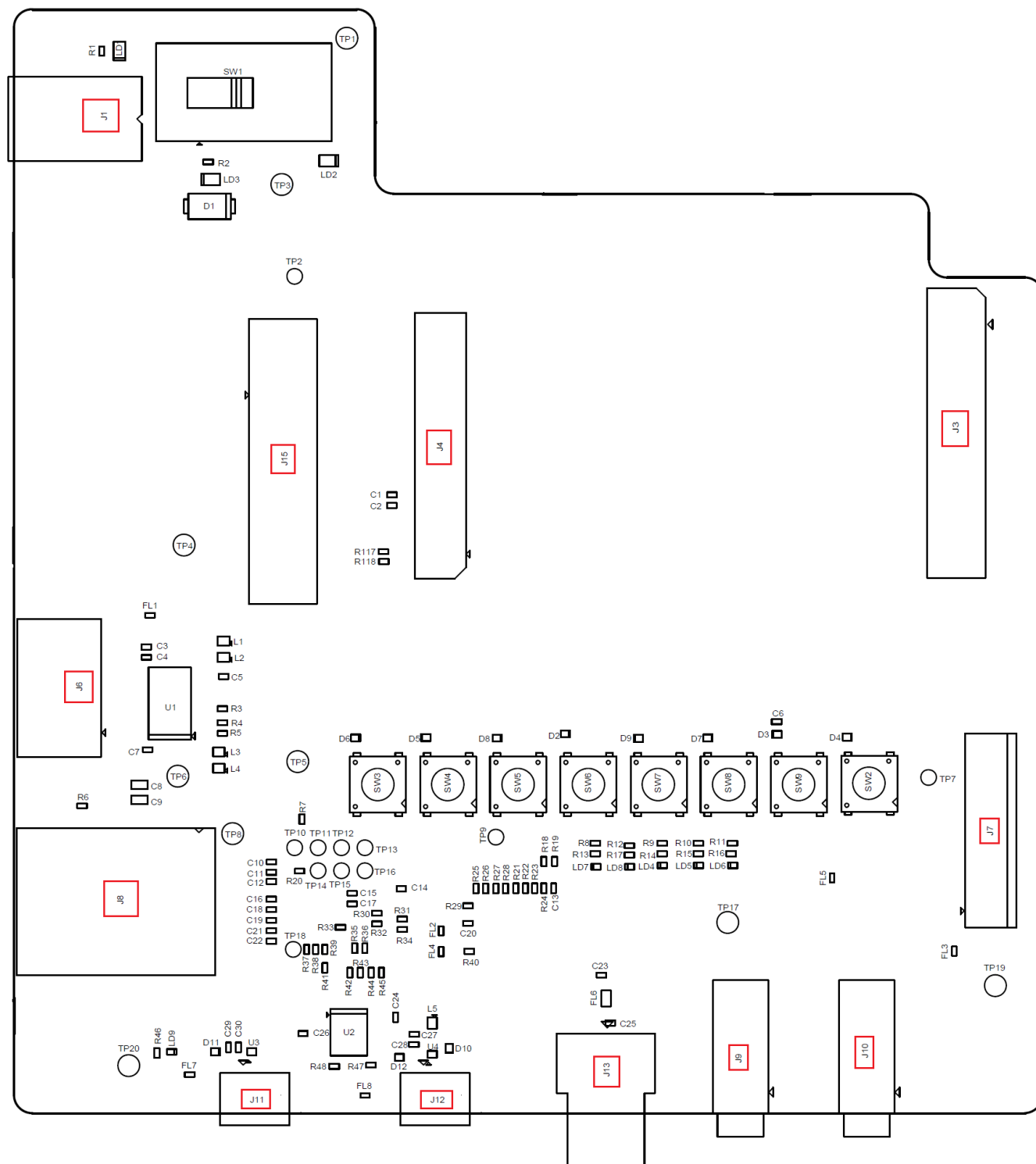
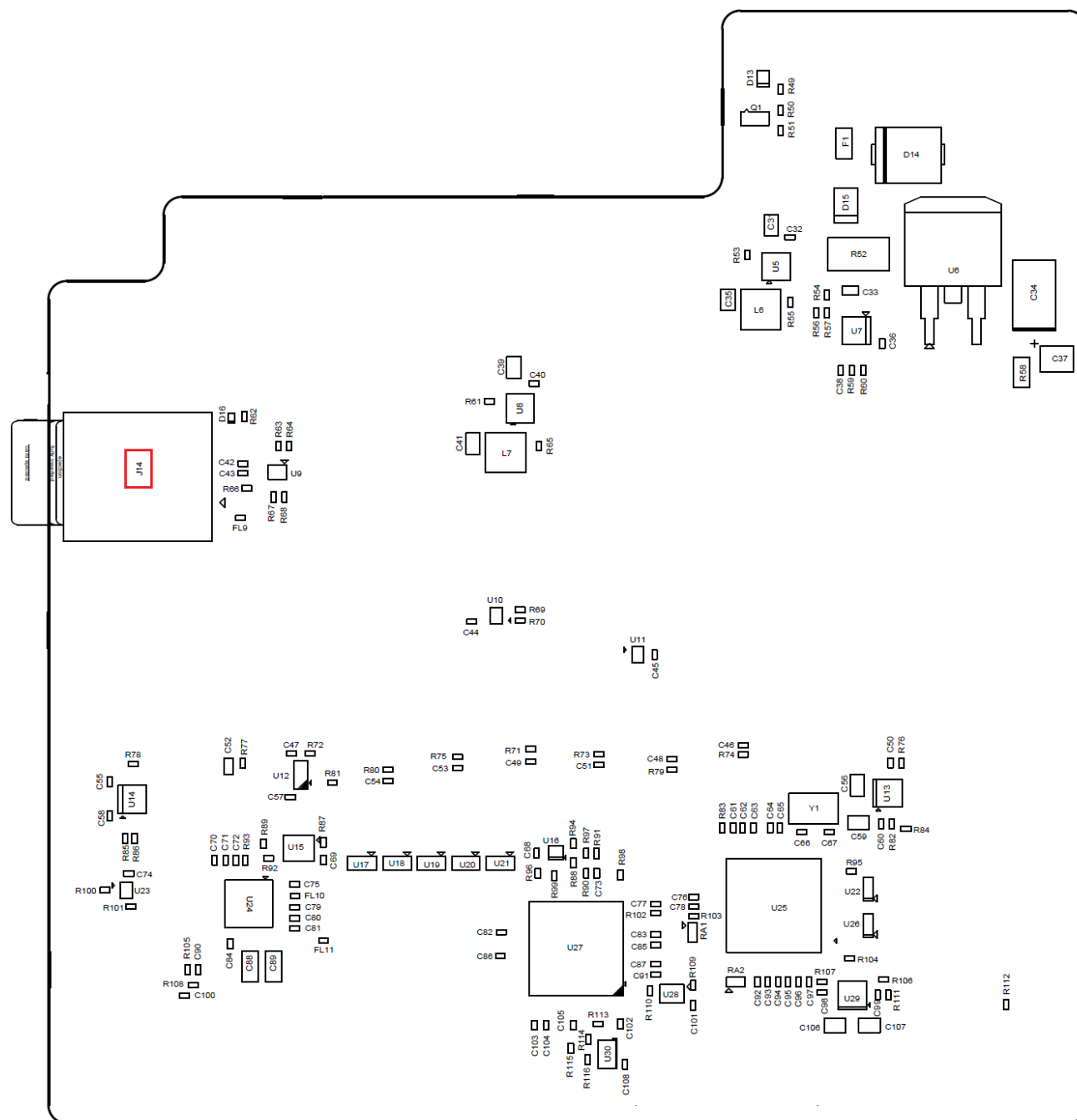


Figure 8-4. CSK Carrier Card Connectors (Bottom)



8.2.1 DC Power Jack (J1)

Table 8-2 provides the DC power-jack pin information.

Table 8-2. DC Power Jack (J1)

Pin Number	Pin Description
1	+5 V
2	GND
3	GND

8.2.2 Board-to-Board Connector (J3)

Table 8-3 provides the board-to-board connector (J3) pin information.

Table 8-3. Board-to-Board Connector (J3)

Pin Number	Pin Description in CC	Pin Number	Pin Description in CC
1	BB_CAM_DAT0	45	NC
2	BB_HDMI_CLKN	46	BB_FT2232_TDO
3	BB_CAM_DAT1	47	BB_CAM_RESET
4	BB_HDMI_CLKP	48	BB_WARM_RESET
5	BB_CAM_DAT2	49	NC
6	DGND	50	BB_RSTOUTn
7	BB_CAM_DAT3	51	NC
8	BB_HDMI_D0N	52	BB_LED5
9	BB_CAM_DAT4	53	BB_TVOUT0
10	BB_HDMI_D0P	54	BB_PORn
11	DGND	55	DGND
12	DGND	56	DGND
13	BB_CAM_DAT5	57	NC
14	BB_HDMI_D1N	58	BB_USB0_VBUSIN
15	BB_CAM_DAT6	59	NC
16	BB_HDMI_D1P	60	BB_USB0_ID
17	BB_CAM_DAT7	61	NC
18	DGND	62	BB_USB0_DM
19	BB_CAM_DAT8	63	NC
20	BB_HDMI_D2N	64	BB_USB0_DP
21	BB_CAM_DAT9	65	NC
22	BB_HDMI_D2P	66	BB_USB0_DRVVBUS
23	BB_CAM_DAT10	67	DGND
24	DGND	68	BB_EXP_SPI_SCLK
25	BB_CAM_DAT11	69	BB_FT2232_UART_RX
26	BB_EXP_UART_TXD	70	BB_EXP_SPI_SCS
27	BB_CAM_DAT12	71	BB_FT2232_UART_TX
28	BB_EXP_UART_RXD	72	BB_EXP_SPI_D0
29	BB_CAM_DAT13	73	BB_OSC_WAKEUP
30	BB_EMU0	74	BB_EXP_SPI_D1
31	BB_CAM_DAT14	75	BB_SDCD
32	BB_EMU1	76	BB_SD0_DAT3
33	DGND	77	DGND
34	DGND	78	DGND
35	BB_CAM_DAT15	79	BB_AIC_MCLK

Table 8-3. Board-to-Board Connector (J3) (continued)

Pin Number	Pin Description in CC	Pin Number	Pin Description in CC
36	BB_FT2232_TMS	80	BB_SD0_CLK
37	BB_CAM_HS	81	BB_AIC_BCLK
38	BB_FT2232_TCK	82	BB_SD0_CMD
39	BB_CAM_VS	83	BB_AIC_WCLK
40	BB_FT2232_RTCK	84	BB_SD0_DAT0
41	NC	85	BB_AIC_DIN
42	BB_FT2232_TRSTN	86	BB_SD0_DAT1
43	BB_CAM_PCLK	87	BB_AIC_DOUT
44	BB_FT2232_TDI	88	BB_SD0_DAT2

8.2.3 Board-to-Board Connector (J4)

Table 8-4 provides the board-to-board connector (J4) pin information.

Table 8-4. Board-to-Board Connector (J4)

Pin Number	Pin Description in CC	Pin Number	Pin Description in CC
1	BB_ETH_TX_D7	45	DGND
2	BB_I2C_SCL	46	BB_EXP_CSI_DY1
3	BB_ETH_TX_D6	47	BB_ETH_RX_D0
4	BB_I2C_SDA	48	DGND
5	BB_ETH_TX_D5	49	BB_ETH_RX_D1
6	BB_HDMI_CEC	50	BB_EXP_CSI_DX2
7	BB_ETH_TX_D4	51	BB_ETH_RX_D2
8	BB_HDMI_HPDET	52	BB_EXP_CSI_DY2
9	BB_ETH_TX_D3	53	BB_ETH_RX_D3
10	BB_PMIC_POR	54	BB_ETH_COL
11	DGND	55	DGND
12	DGND	56	DGND
13	BB_ETH_TX_D2	57	BB_ETH_RX_D4
14	BB_ETH_CS	58	BB_EXP_CSI_DX3
15	BB_ETH_TX_D1	59	BB_ETH_RX_D5
16	VCC_3V3	60	BB_EXP_CSI_DY3
17	BB_ETH_TX_D0	61	BB_ETH_RX_D6
18	VCC_3V3	62	DGND
19	BB_ETH_TX_CLK	63	BB_ETH_RX_D7
20	VCC_3V3	64	BB_EXP_CSI_DX4
21	BB_EXP_GP0[30]	65	DGND
22	VCC_CAM	66	BB_EXP_CSI_DY4
23	DGND	67	BB_LED1
24	VCC_1V8	68	BB_uPIO_PWR_EN
25	BB_ETH_GTX_CLK	69	BB_LED2
26	NC	70	BB_SWITCH1
27	BB_ETH_TX_EN	71	BB_LED3
28	DGND	72	BB_SWITCH2
29	BB_HDMI_CODEC_SCL	73	BB_LED4
30	BB_EXP_GP1[26]	74	BB_EXP_GP0[31]
31	BB_HDMI_CODEC_SDA	75	BB_SWITCH3
32	BB_EXP_GP0[29]	76	PMIC_3V3
33	DGND	77	DGND
34	DGND	78	DGND
35	BB_ETH_MDC	79	BB_SWITCH4
36	BB_EXP_GP1[25]	80	PMIC_3V3
37	BB_ETH_MDIO	81	BB_ETH_RESET
38	BB_EXP_CSI_DX0	82	PMIC_3V3
39	BB_ETH_RX_CLK	83	DC_VCC5V0
40	BB_EXP_CSI_DY0	84	PMIC_3V3
41	BB_ETH_RX_DV	85	DC_VCC5V0
42	DGND	86	PMIC_3V3
43	BB_ETH_RX_ER	87	DC_VCC5V0
44	BB_EXP_CSI_DX1	88	PMIC_3V3

8.2.4 Expansion Connector (J15)

Table 8-5 provides the expansion connector (J15) pin information.

Table 8-5. Expansion Connector (J15)

Pin Number	Pin Description	Pin Number	Pin Description
1	DC_VCC5V0	33	NC
2	DC_VCC5V0	34	BB_EXP_CSI_DX4
3	DC_VCC5V0	35	NC
4	NC	36	DGND
5	NC	37	NC
6	NC	38	BB_EXP_CSI_DY3
7	BB_EXP_SPI_SCS	39	NC
8	NC	40	BB_EXP_CSI_DX3
9	BB_EXP_SPI_SCLK	41	NC
10	BB_EXP_GP1[25]	42	DGND
11	BB_EXP_SPI_D0	43	NC
12	BB_EXP_SPI_D1	44	BB_EXP_CSI_DY2
13	BB_EXP_GP0[30]	45	NC
14	BB_EXP_GP1[26]	46	BB_EXP_CSI_DX2
15	NC	47	NC
16	BB_EXP_GP0[29]	48	DGND
17	NC	49	NC
18	DGND	50	BB_EXP_CSI_DY1
19	NC	51	BB_I2C_SDA
20	NC	52	BB_EXP_CSI_DX1
21	NC	53	BB_I2C_SCL
22	NC	54	DGND
23	NC	55	BB_EXP_UART_TXD
24	DGND	56	BB_EXP_CSI_DY0
25	NC	57	BB_EXP_UART_RXD
26	NC	58	BB_EXP_CSI_DX0
27	NC	59	BB_EXP_GP0[31]
28	NC	60	DGND
29	NC	61	DGND
30	DGND	62	DGND
31	NC	63	DGND
32	BB_EXP_CSI_DY4	64	DGND

NOTE: The TMDSCSK369 processor module does not support a CSI interface. Only the TMDSCSK8127 and TMDSCSK388 processor modules support CSI interfaces.

8.2.5 HDMI Out Type-A Connector (J6)

Table 8-6 provides the HDMI out type-A connector (J6) pin information.

Table 8-6. HDMI Out Type-A Connector (J6)

Pin Number	Pin Description	Pin Number	Pin Description
1	FLT_HDMI_D2P	13	CE_REMOTE_OUT
2	DGND	14	NC
3	FLT_HDMI_D2N	15	DDC_CLK
4	FLT_HDMI_D1P	16	DDC_DAT
5	DGND	17	DGND
6	FLT_HDMI_D1N	18	5V_OUT_HDMI
7	FLT_HDMI_D0P	19	HDMI_HP_OUT
8	DGND	20	Shield GND
9	FLT_HDMI_D0N	21	Shield GND
10	FLT_HDMI_D0N	22	Shield GND
11	DGND	23	Shield GND
12	FLT_HDMI_CLKN		

NOTE: The TMDSCSK369 Processor module does not support HDMI interfaces. Only the TMDSCSK8127 and TMDSCSK388 processor modules support HDMI interfaces.

8.2.6 Camera FPC Connector (J7)

Table 8-7 provides the camera FPC connector (J7) pin information.

Table 8-7. Camera FPC Connector (J7)

Pin Number	Pin Description	Pin Number	Pin Description
1	BB_CAM_DAT15	19	BB_CAM_DAT8
2	BB_CAM_DAT14	20	BB_CAM_DAT9
3	NC	21	BB_CAM_DAT10
4	CAM_RESET	22	BB_CAM_DAT11
5	NC	23	BB_CAM_DAT12
6	NC	24	BB_CAM_DAT13
7	CAM_I2C_SDA	25	BB_CAM_HS
8	CAM_I2C_SCL	26	BB_CAM_VS
9	BB_CAM_DAT0	27	DGND
10	BB_CAM_DAT1	28	BB_CAM_PCLK
11	DGND	29	DGND
12	DGND	30	TP7
13	BB_CAM_DAT2	31	DGND
14	BB_CAM_DAT3	32	DC_VCC5V0
15	BB_CAM_DAT4	33	DC_VCC5V0
16	BB_CAM_DAT5	34	VCC_3V3
17	BB_CAM_DAT6	35	VCC_3V3
18	BB_CAM_DAT7	36	VCC_3V3

8.2.7 RJ45 Connector (J8)

Table 8-8 provides the RJ45 connector (J8) pin information.

Table 8-8. RJ45 Connector (J8)

Pin Number	Pin Description
1	DGND
2	NC
3	ETHER0_D3P
4	ETHER0_D3N
5	ETHER0_D2P
6	ETHER0_D2N
7	ETHER0_D1P
8	ETHER0_D1N
9	ETHER0_D0P
10	ETHER0_D0N
11	RIGHT LED
12	RIGHT LED
13	LEFT LED
14	LEFT LED
15	SHIELD GND
16	SHIELD GND

8.2.8 Stereo-Audio Jack (J9 and J10)

The CSK carrier card has two 3.5-mm female stereo jacks that are connected to the AIC3104 audio codec.

- HP OUT is for connecting to headphones. See Table 8-9 for pin information.
- MIC IN is for connecting to a microphone input. See Table 8-10 for pin information.

Table 8-9. HP OUT

Pin Number	Description
1	GND
2	LEFT_OUT
3	RIGHT_OUT
4	NC

Table 8-10. MIC IN

Pin Number	Description
1	GND
2	LEFT_IN
3	RIGHT_IN
4	NC

8.2.9 Micro USB Connector (J11 and J12)

The CSK carrier card has two micro USB connectors. Micro USB connector J11 provides access to the XDS100V2 on-board emulator. The USB host and device port of the DMx device is available through the J12 USB connector. [Table 8-11](#) provides the micro USB connector (J11 and J12) pin information.

Table 8-11. Micro USB Connector

Pin Number	Description
1	VDD
2	D–
3	D+
4	ID
5	GND
6	USB0_GND
7	USB0_GND
8	USB0_GND
9	USB0_GND

8.2.10 Composite Video OUT RCA Connector (J13)

[Table 8-12](#) provides the composite video OUT RCA connector (J13) pin information.

Table 8-12. Composite Video OUT RCA Connector

Pin Number	Description
1	VIDEO OUT
2	DGND
3	DGND
4	DGND

8.2.11 Micro SD Card Connector (J14)

The micro SD card holder is located on the bottom side of the board, and it provides an interface to micro SD cards. The connector is a 14-pin SD card holder.

[Table 8-13](#) provides the micro SD card connector (J14) pin information.

Table 8-13. Micro SD Card Connector (J14)

Pin Number	Pin Description
1	DAT2
2	CD/DAT3
3	CMD
4	VDD
5	CLOCK
6	VSS
7	DAT0
8	DAT1
9	CD1
10	SDCD_GND
11	SDCD_GND
12	CD2
13	SDCD_GND
14	SDCD_GND

8.3 Push Buttons

The CSK carrier card has nine switches. Out of the nine switches, four are for general purposes. Refer to [Table 3-5](#) to configure the switch functionality. [Table 8-14](#) details the functionality of each switch.

Table 8-14. CSK Carrier Card Switches

Switch-Button Number	Description
SW1	Power ON and OFF switch
SW2	Oscillator wakeup
SW3	Warm reset
SW4	PMIC reset
SW5	General purpose
SW6	General purpose
SW7	General purpose
SW8	General purpose
SW9	Power on reset

8.4 Test Points

The CSK carrier card has 23 test points. [Table 8-15](#) provides the test point and corresponding signals.

Table 8-15. Test Points of CSK Carrier Card

Test Point	Signal
TP1	DGND
TP5	
TP17	
TP19	
TP20	
TP2	PMIC 3V3 PGOOD
TP3	PMIC 3V3
TP4	VCC 3V3
TP6	VCCA_2V5
TP7	CAMERA CLOCKOUT
TP8	VCC_1V1
TP9	VCC_3V3 PGOOD
TP10	VDDA1P8
TP11	ETHERNET CLOCKOUT
TP12	ETHERNET JTAG TDO
TP13	ETHERNET JTAG TMS
TP14	ETHERNET_JTAG_RESET
TP15	ETHERNET_JTAG_TCLK
TP16	ETHERNET_JTAG_TDI
TP18	ETHERNET SPEED
TP21	VCC 5V0
TP22	VCC CAM
TP23	VCC 1V8

8.5 System LEDs

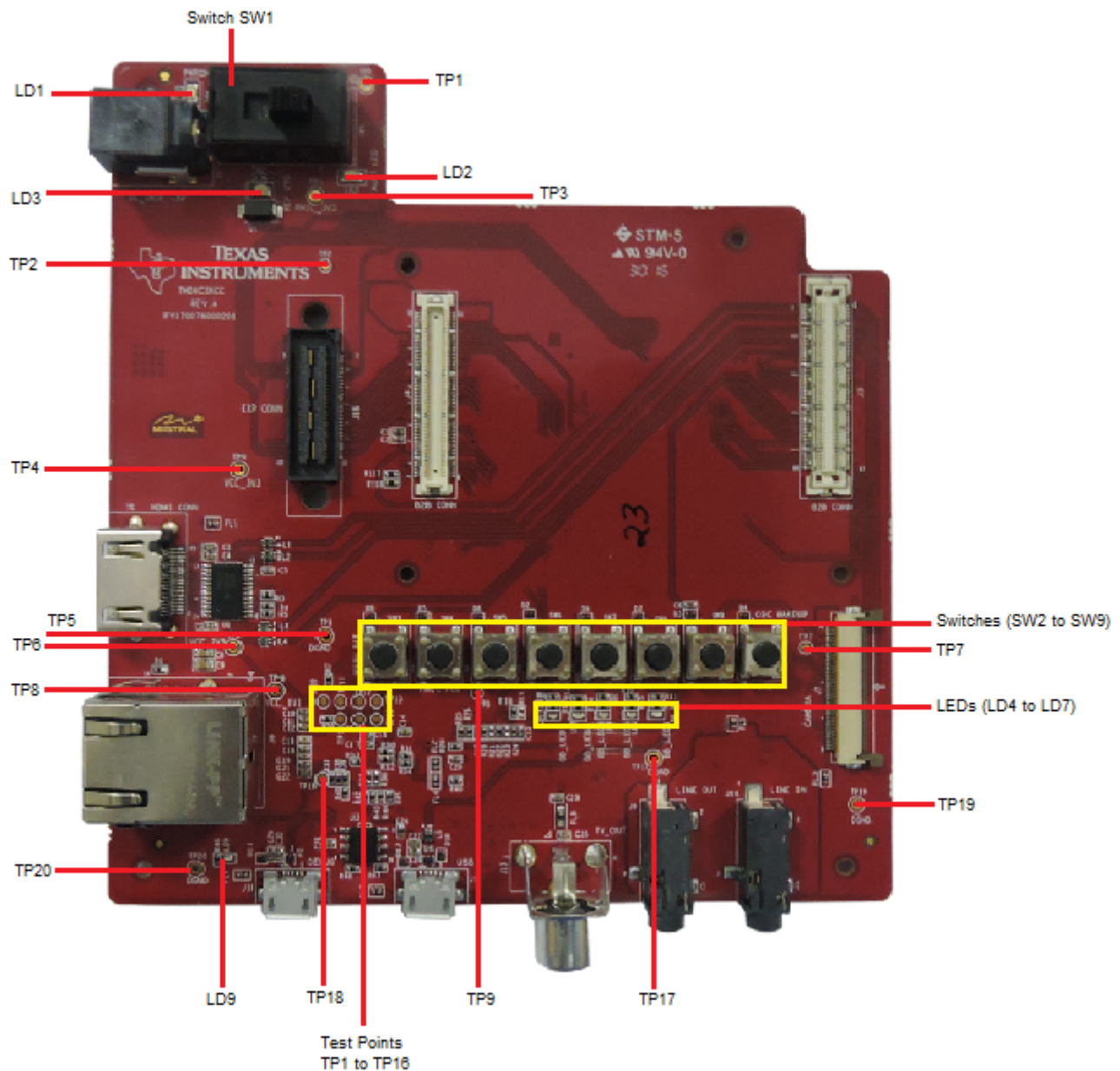
The CSK carrier card has three LEDs. Refer to [Table 3-5](#) to configure the LED functionality for LED1, LED2, and LED3. [Table 8-16](#) provides the LED information.

Table 8-16. LED Information

LED	Color	Description
LD1	Green	LED1
LD2		LED2
LD3		LED3
LD4		Board-power LED
LD5		FT2232 power-enable LED

Figure 8-5 shows the position of LEDs, test points, and push buttons on the CSK carrier card.

Figure 8-5. LEDs, Test Points, and Push Buttons on CSK Carrier Card



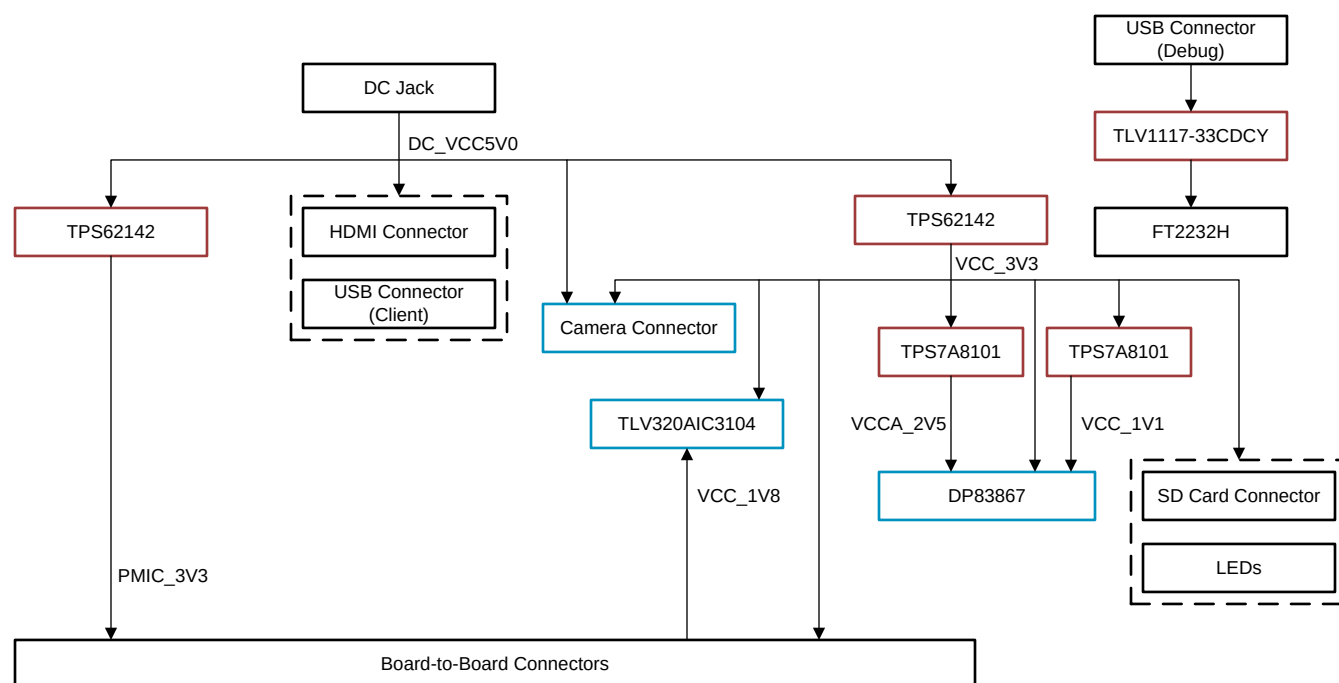
CSK Carrier Card Power Requirements

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9.1 Power Distribution

Figure 9-1 shows the power distribution diagram.

Figure 9-1. CSK Carrier Power Distribution



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9.2 Power Supply Calculation

Table 9-1 provides the power supply calculation information.

Table 9-1. Power Supply Calculation

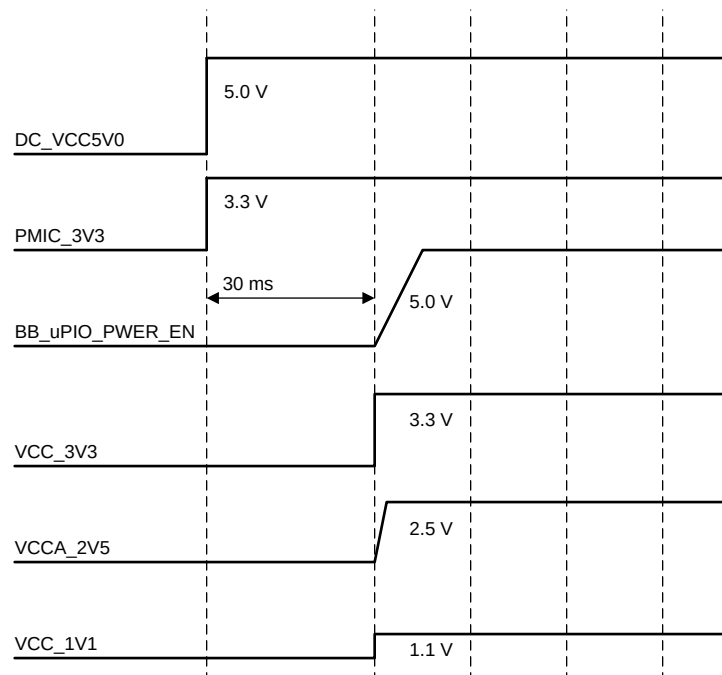
Input Supply (V)		5				PMIC3V3	VCC_3V3	
Regulatory Efficiency						0.9	0.86	
Input Voltage		Board-to-Board Connect	3.3	3.3	5	5	5	
Output Voltage		1.8	2.5	1.1		3.3	3.3	
Regulator Name		TPS6216DSGT	TPS7A8101	TPS7A8101		TPS62142RGTT (U5)	TPS62142RGTT (U8)	5-V DC IN
		Active	Active	Active		Active	Active	Active
Description	Part Number							
Ethernet PHY external regulator	TPS7A8101 (2.5 V)						141	108.2093023
	TPS7A8101 (1.1 V)						125	95.93023256
Audio codec	TLV320AIC3104	2.5					170	130.4651163
Camera module	LI-CAM-AR0331-324-1.8				800		300	–
Ethernet PHY	DP83867IRPAPT		141	125			22	16.88372093
Expansion connector (CSI camera)								0
Micro SD card							80	61.39534884
LED × 5							10	7.674418605
24.576-MHz oscillator							15	11.51162791
Current Consumption ⁽¹⁾						0	863	1232.069767
Power Consumption (mW)						0	2847.9	6160.348837
								5-V DC IN
		Active				TMDSCSK388		2210.73
Current Consumption on 5-V power input ⁽¹⁾		1232.069767				TMDSCSK8127		2660.863
Power Consumption on 5-V power input (mW)		6160.348837				TMDSCSK369		1052.032
USB Bus-Powered Devices							3.3	5
							TLV1117-33CDCY	5-V USB
USB to JTAG or UART	FT2232HL						130	130
EEPROM	AT93C46DY6-YH-T						2	2

⁽¹⁾ All current ratings are in mA.

9.3 Power-up Sequence

Figure 9-2 shows the power sequencing for the CSK carrier card.

Figure 9-2. Power-up Sequence



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