

Using the LMG3410-HB-EVM Half-Bridge and LMG34XX-BB-EVM Breakout Board EVM General TI High Voltage Evaluation User Safety Guidelines



WARNING

Always follow TI's set-up and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and the safety of those working around you. Contact TI's Product Information Center <http://support/ti.com> for further information.

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions may result in personal injury, property damage, or death due to electrical shock and/or burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise, and knowledge of electrical safety risks in development and application of high-voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments. If you are not suitably qualified, you should immediately stop from further use of the HV EVM.

- **Work Area Safety:**

- Maintain a clean and orderly work area .
- Qualified observer(s) must be present anytime circuits are energized.
- Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
- All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50 V_{RMS}/75 VDC must be electrically located within a protected Emergency Power Off (EPO) protected power strip.
- Use a stable and non-conductive work surface.
- Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.

- **Electrical Safety:**

As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.

- De-energize the TI HV EVM and all its inputs, outputs, and electrical loads before performing any electrical or other diagnostic measurements. Confirm that TI HV EVM power has been safely de-energized.
- With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
- When EVM readiness is complete, energize the EVM as intended.

WARNING: While the EVM is energized, never touch the EVM or its electrical circuits as they could be at high voltages capable of causing electrical shock hazard.

- **Personal Safety:**
 - Wear personal protective equipment, for example, latex gloves and/or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.
- **Limitation for Safe Use:**
 - EVMs are not to be used as all or part of a production unit.

Safety and Precautions

The EVM is designed for professionals who have received the appropriate technical training, and is designed to operate from an AC power supply or a high-voltage DC supply. Please read this user guide and the safety-related documents that come with the EVM package before operating this EVM.

CAUTION



Do not leave the EVM powered when unattended.

WARNING



Hot surface! Contact may cause burns. Do not touch!

WARNING



High Voltage! Electric shock is possible when connecting board to live wire. Board should be handled with care by a professional.

For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

Using the LMG3410-HB-EVM Half-Bridge and LMG34XX-BB-EVM Breakout Board EVM

The LMG3410-HB-EVM features two LMG3410 600V/12A GaN power transistors with integrated drivers that are configured in a half bridge with all the required bias circuit and logic/power level shifting. Essential power stage and gate driving high frequency current loops are fully enclosed on the board to minimize parasitic inductances, reducing voltage overshoots and improving performance. The LMG3410-HB-EVM is configured to have a socket style external connection for easy interface with external power stages to run the LMG3410 in various applications.

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Trademarks

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1 Description

The LMG3410-HB-EVM operates as a daughter card as part of a larger custom designed system or with the LMG34XX-BB-EVM breakout motherboard.

1.1 LMG3410-HB-EVM

The LMG3410-HB-EVM configures two LMG3410 GaN FETs in a half bridge. All the bias and level shifting components are included, allowing low side referenced signals to control both FETs. High frequency bypass capacitors are included on the power stage in an optimized layout to minimize parasitic inductance and reduce voltage overshoot.

There are 6 logic pins on the FET card

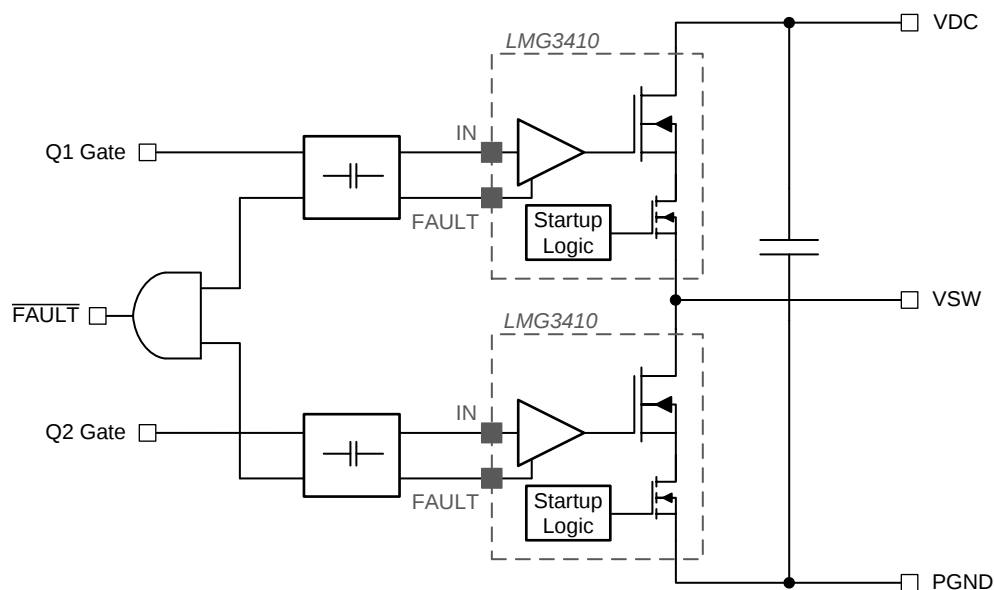
Table 1. Logic Pin Function Description

Pin	Description
AGND	Logic and bias power ground return pin. Functionally isolated from PGND.
12V	Auxiliary power input for when the LMG3410-HB-EVM is configured in bootstrap mode. Pin is not used when configured in isolated power mode.
5V	Auxiliary power input for the LMG3410-HB-EVM. Used to power logic isolators. Used as input bias power of LMG3410 devices when configured in isolated power mode.
$\overline{\text{FAULT}}$	Logic AND output from $\overline{\text{FAULT}}$ signal from LMG3410. Pin is either pulled to AGND or 5V.
Q2 Gate	AGND referenced logic gate signal input for bottom LMG3410. Compatible with both 3.3V and 5V logic.
Q1 Gate	AGND referenced logic gate signal input for top LMG3410. Compatible with both 3.3V and 5V logic.

There are 3 power pins on the FET card.

Table 2. Power Pin Function Description

Pin	Description
VSW	Switch node of the half bridge
VDC	Input DC voltage of the half bridge
PGND	Power ground of the half bridge. Functionally isolated from AGND.



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Figure 1. Simplified LMG3410-HB-EVM Schematic

CAUTION

High-voltage levels are present on the evaluation module whenever it is energized. Proper precautions must be taken when working with the EVM.

1.1.1 FAULT

The $\overline{\text{FAULT}}$ pin of LMG3410-HB-EVM is active low when an under voltage lockout on an auxiliary voltage rail, over temperature or overcurrent even occurs on the LMG3410. The $\overline{\text{FAULT}}$ signal for both LMG3410 devices are level shifted to AGND, where they are logic AND connected to the $\overline{\text{FAULT}}$ pin.

CAUTION

Please do NOT ignore $\overline{\text{FAULT}}$ signal when using LMG3410-HB-EVM. Turn off both top and bottom devices, if any device is generating $\overline{\text{FAULT}}$ signal. The device under fault condition may operate in undesired 3rd-quadrant mode and may be over heated and damaged due to the high source-drain voltage drop if the other device is still switching.

1.1.2 Power Pins

While there are some power stage bypass capacitors on the LMG3410-HB-EVM from VDC to PGND to minimize voltage overshoot during switching, more bulk capacitance is required to hold up the DC voltage during operation. It is highly recommended to minimize, and ideally prevent, any overlap and parasitic capacitance from VSW to VDC, PGND and any logic pins. The two grounds PGND and AGND are functionally isolated from each other on the LMG3410-HB-EVM.

1.1.3 Bootstrap Mode

The LMG3410-HB-EVM card can be modified to operate in bootstrap mode, where the 12V bias voltage is used to power both LMG3410 devices. This can be achieved by removing U3, U4 and R2, and placing a 20 Ω resistor on R1, a 0 Ω resistor on R18 and a 600V SOD-123 diode on D1, such as Micro Commercial Components UFM15PL-TP. Do NOT power up the LMG3410-HB-EVM when R1, R2, R18, D1, U3 and U4 are all populated.

1.1.4 Heatsink

Heatsink is installed to help with heat dissipation of the LMG3410. Exposed copper pads that are attached to the die attach pad (DAP) of both the high and low side devices are provided for a low thermal impedance point to a heatsink. The two copper pads have high voltage potential difference between them so an electrically isolative thermal interface material (TIM) is required. Bergquist BP100-0.005-00-1112 double sided adhesive tape TIM and Cool Innovations 3-101004U heatsink are recommended.

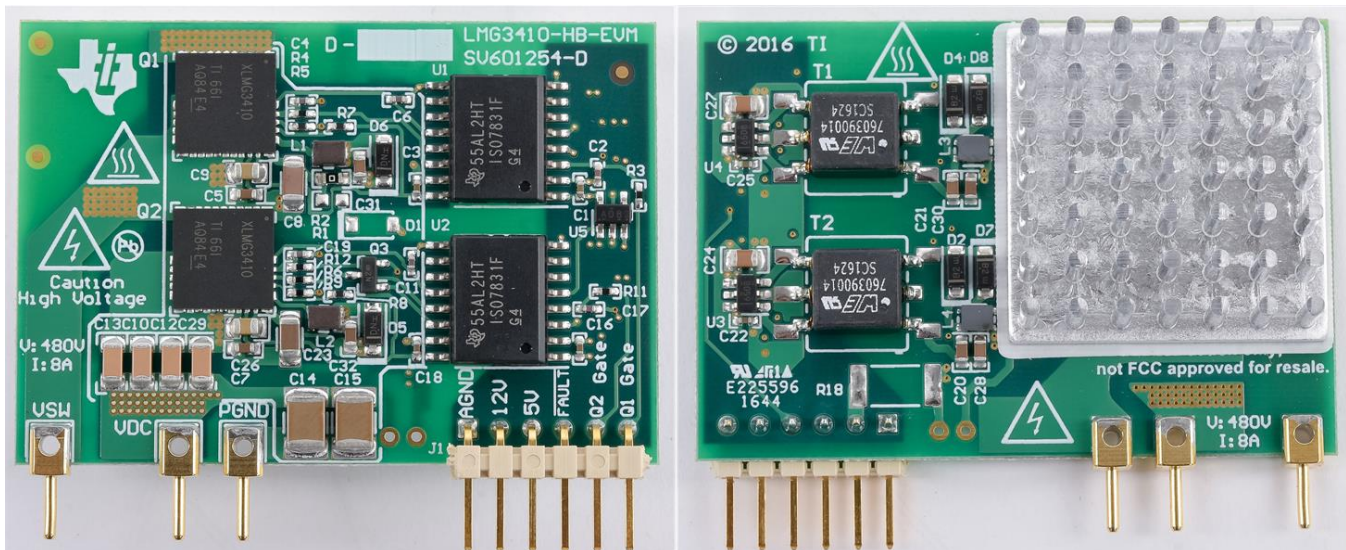


Figure 2. Front and Back Side Photos of LMG3410-HB-EVM

1.2 LMG34XX-BB-EVM

To allow for quick operation the LMG34XX-BB-EVM is available to interface with the LMG3410-HB-EVM. This mother board is designed to operate the LMG3410 as a synchronous open loop buck converter. Easy probe locations are provided for measurement of logic and power stage voltages.

1.2.1 Bias Supply

The motherboard requires one 12V bias supply. A linear drop off regulator steps the voltage down to a tightly regulated 5V for logic and auxiliary power of the LMG3410 when the LMG3410-HB-EVM is configured in isolated power mode. When the LMG3410-HB-EVM is configured in bootstrap mode the 12V input is used to power the two LMG3410 devices.

1.2.2 Logic PWM Input

The LMG34XX-BB-EVM supports a single PWM, with complimentary signal and corresponding dead time generated on board. A 0 V to 5 V magnitude input square wave is required. The complementary PWM generation circuit creates 50 ns of dead time between both transitions of the PWM signals.

1.2.3 Fault Protection

There is an option to disable PWM input to the FET card in the event of a fault signal from the LMG3410-HB-EVM. When the FAULT Protect jumper is placed in the EN mode PWM is disabled when either LMG3410 has an active fault. This disable is not latching, so when the fault clears PWM immediately resumes. If FAULT Protect mode is not desired it can be disabled by placing the jumper in the DIS position. The FAULT LED will still illuminate when either LMG3410 has an active fault, regardless of the position of FAULT Protect jumper.

1.3 Typical Applications

The LMG3410-HB-EVM is designed for use in AC/DC, DC/DC and DC/AC applications

- Totem-Pole PFC converters
- Phase-Shifted Full Bridge or LLC Converter
- Buck converter such as the LMG34XX-BB-EVM

1.4 Features

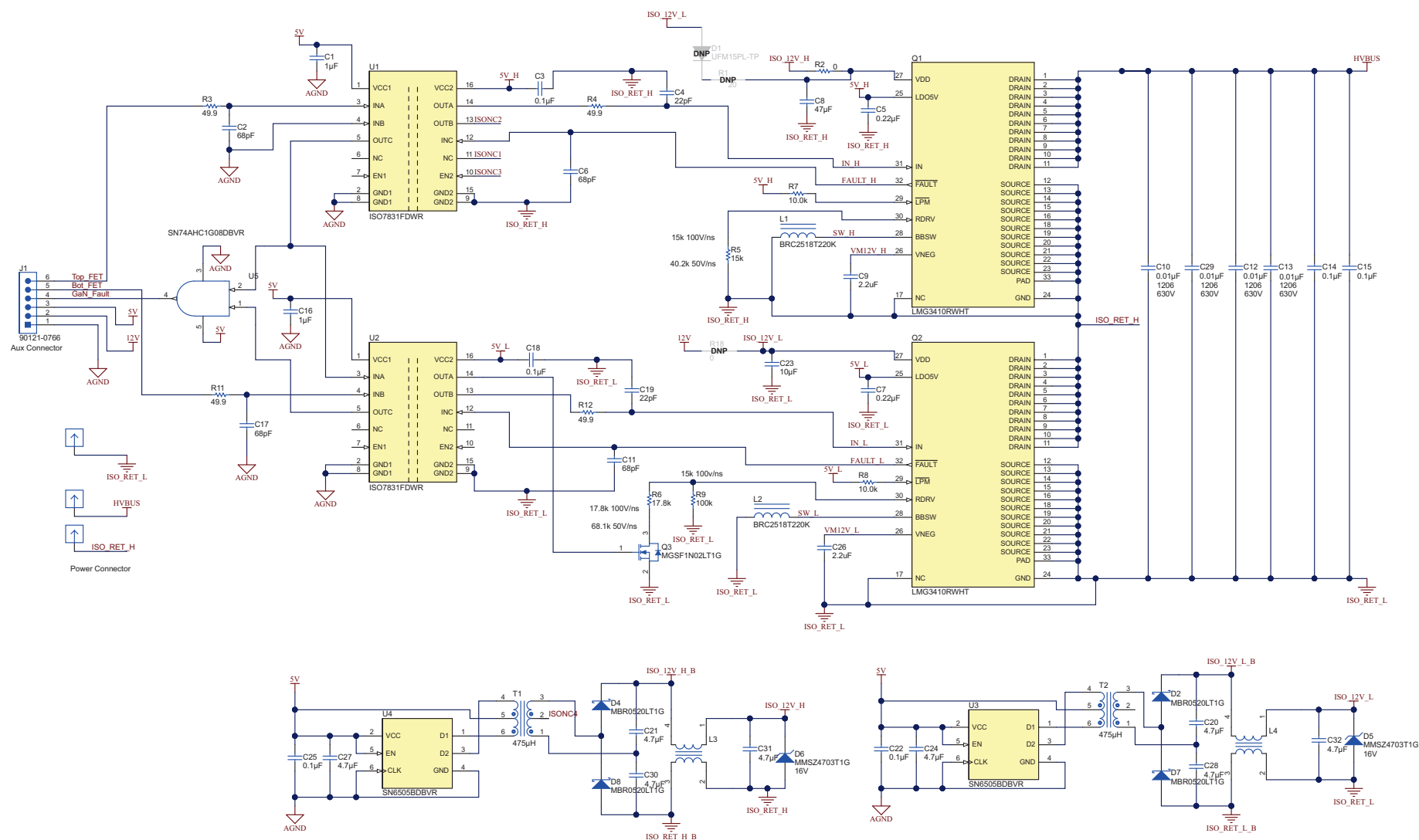
The LMG3410-HB-EVM has the following features and specifications:

- Two options to bias the LMG3410, isolated power or from bootstrap diode
- Over temperature, overcurrent, and under voltage lockout protection with FAULT indication that is level shifted to an AGND referenced signal
- Gate logic input support of either 3.3V or 5V logic
- Maximum recommended operating voltage of 480V and absolute maximum voltage of 600V

The LMG34XX-BB-EVM has the following features and specifications:

- Requires only a single 12V bias supply
- Requires only a single 0V to 5V PWM input to generate gate drive signal
- PWM disable in the event of a fault from the LMG3410-HB-EVM
- Maximum recommended operating voltage of 480V and absolute maximum voltage of 600V
- Maximum recommended operating inductor current of 8A

2 Schematic



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Figure 3. LMG3410-HB-EVM Schematic

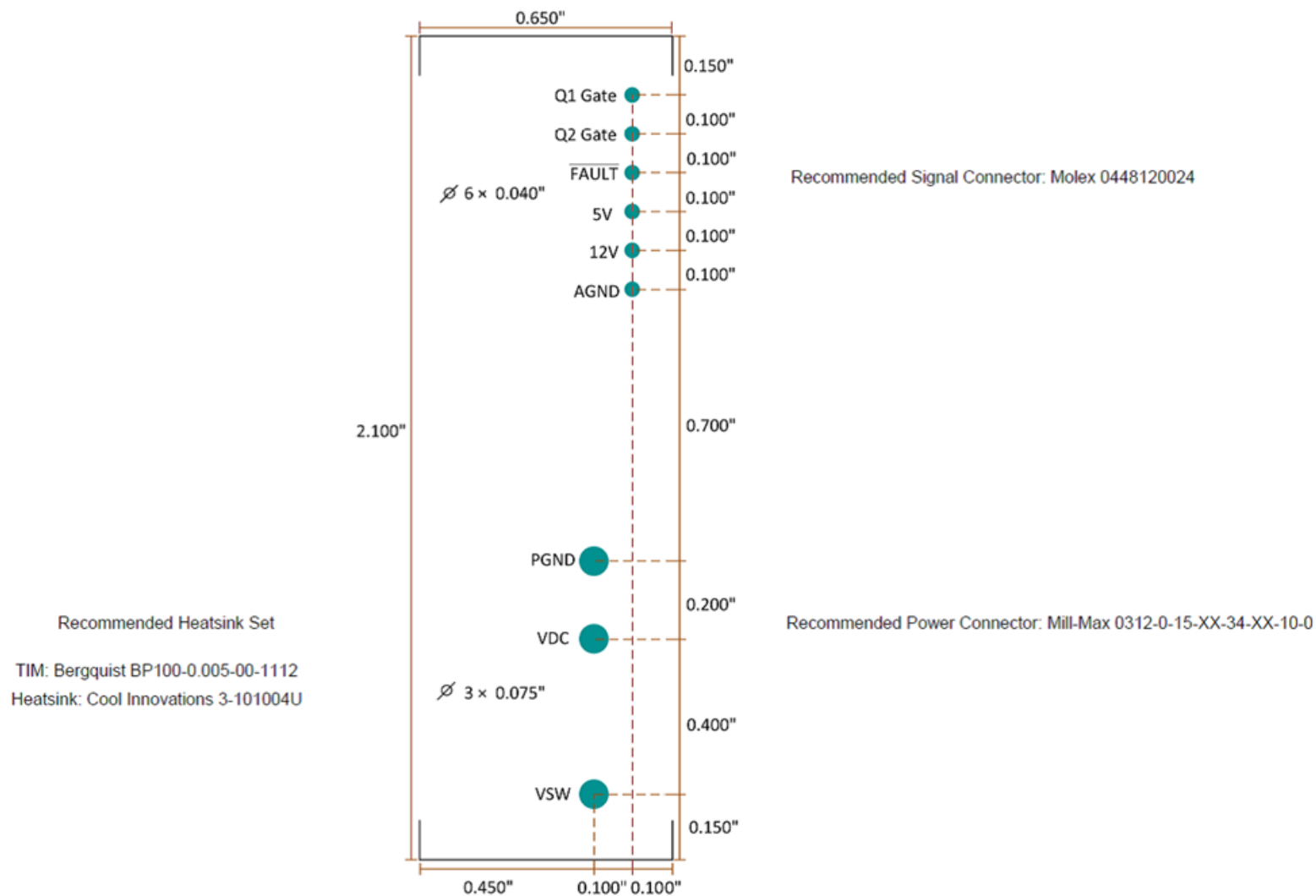
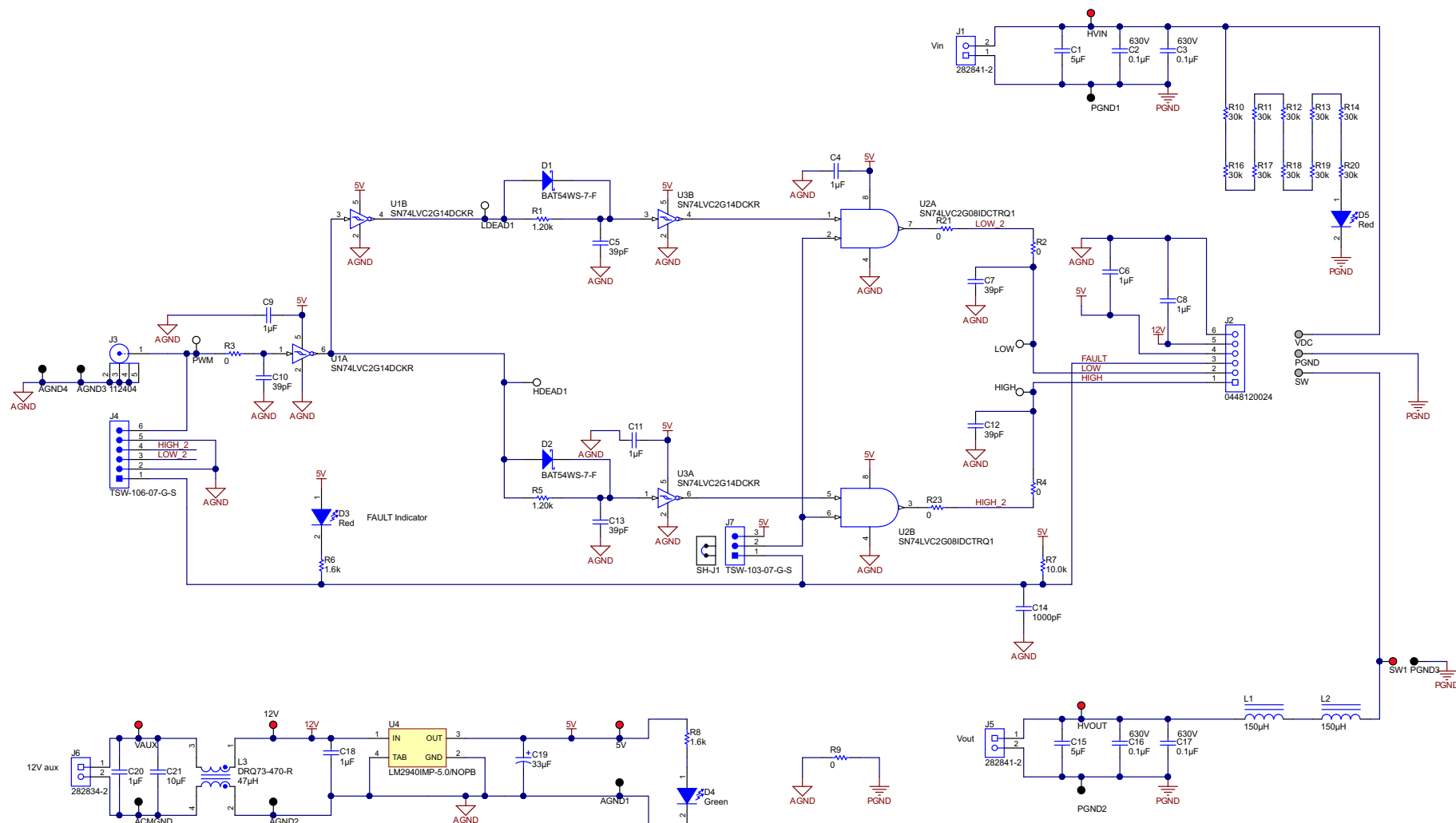


Figure 4. Recommended Footprint for LMG3410-HB-EVM

TI HV Synchronous Buck Motherboard



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Figure 5. LMG34XX-BB-EVM Schematic

3 Test Setup

3.1 Test Equipment

DC Voltage Source: Capable of supplying the input of the EVM up to 480 V

DC Bias Source: Capable of 12 V output at up to 0.7 A

Function Generator: Capable of 0 V to 5 V square wave output with adjustable duty cycle and frequency in desired operating range. It is recommended to operate the LMG3410-HB-EVM and LMG34XX-BB-EVM with a switching frequency between 50 kHz to 200 kHz.

Oscilloscope: Capable of at least 200 MHz operation. A 1 GHz or greater oscilloscope and probes with short ground springs are recommended for accurate measurements.

DC Multimeter(s): Capable of 600 V measurement, suitable for determining operation and efficiency (if desired).

DC Load: Capable of 600 V operation at up to 8 A in current-mode operation.

Fan: 200 LFM minimum airflow is recommended

3.2 Recommended Test Setup

The LMG3410-HB-EVM connects to the LMG34XX-BB-EVM as [Figure 6](#) shows.

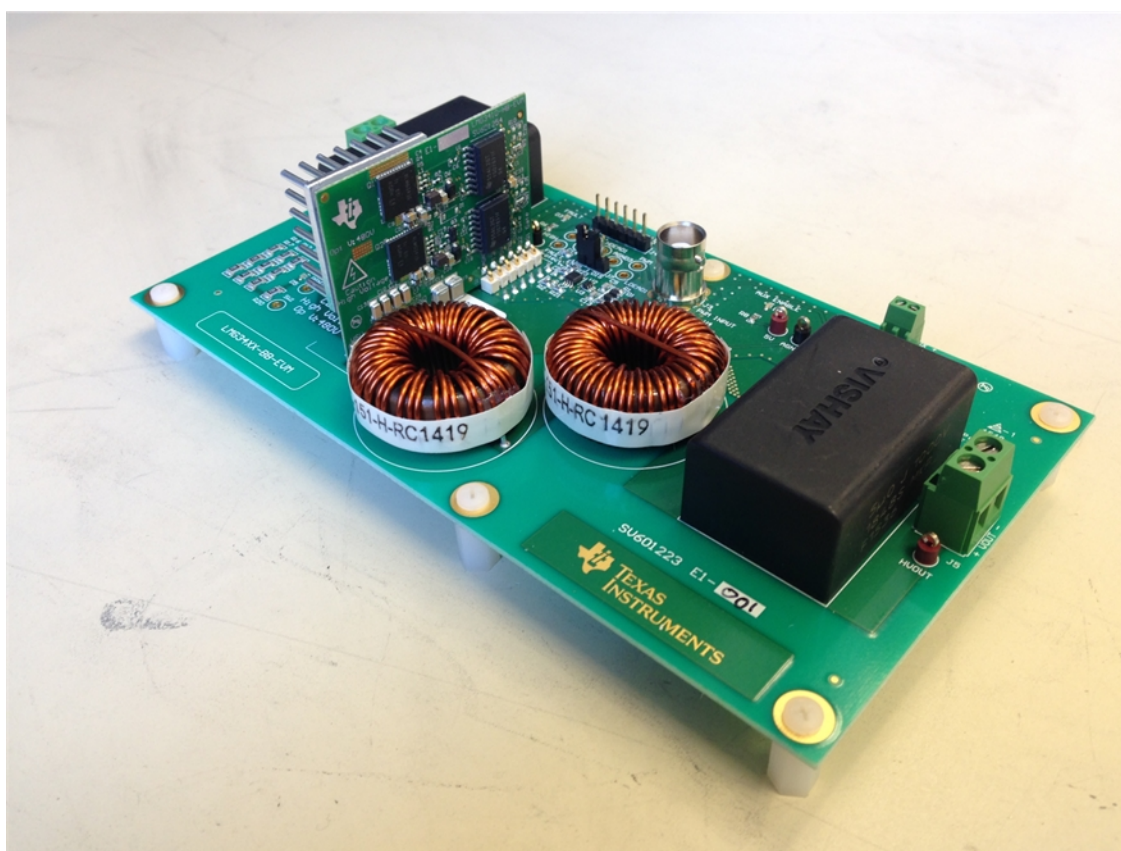


Figure 6. LMG3410-HB-EVM Connected with LMG34XX-BB-EVM

The LMG34XX-BB-EVM power and probe connection points are shown in [Figure 7](#).

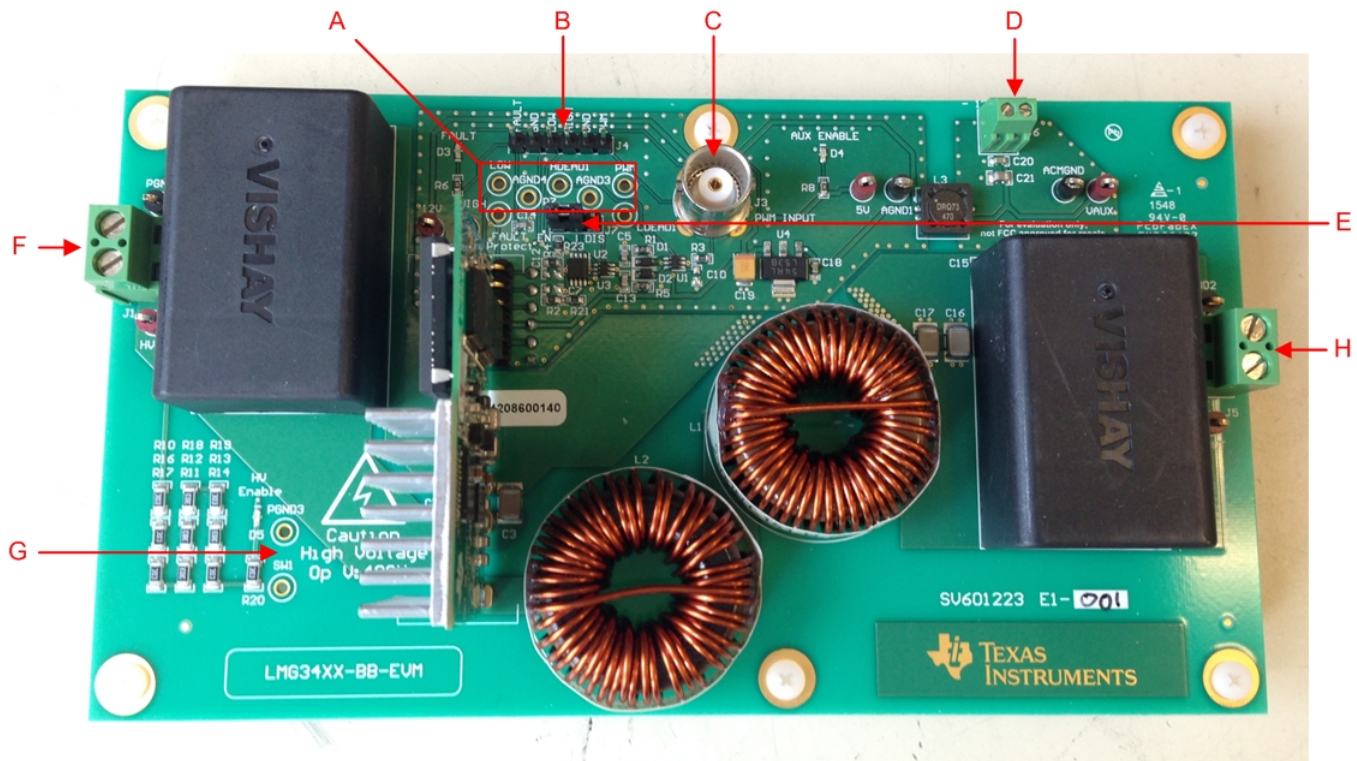


Figure 7. Recommended Connection Points

PCB Notes:

- Probe points for gate drive logic
- 100 mil header for PWM input, PWM signals to LMG3410-HB-EVM and FAULT output
- BNC connector for PWM input
- 12V bias supply input
- FAULT Protection option header
- Power stage high voltage input
- Probe point for power stage switch node
- Power stage high voltage output

WARNING

There are very high voltages present on the EVM. Some components reach temperatures above 50°C. Precautions must be taken when handling the board.

3.3 List of Test Points

Key test points on this EVM have been designed for use with oscilloscope probes with short ground springs. Using the short ground spring instead of the alligator ground lead will minimize measurement error and produce a cleaner signal with the fast switching GaN devices used on this EVM. The data shown in this user guide has been obtained using such a measurement method.

Table 3. Test Point Functional Description

NAME	DESCRIPTION
VAUX	12 V bias input connection before filter
ACMGND	Ground for 12 V bias input before filter
5V	5 V bias
AGND1	Analog ground for logic
PWM	Single input PWM signal
LDEAD1	Low side PWM signal before dead time generation
AGND3	Analog ground for logic
HDEAD1	High side PWM signal before dead time generation
AGND4	Analog ground for logic
LOW	Low side PWM signal with dead time
HIGH	High side PWM signal with dead time
AGND2	Analog ground for logic
12V	12 V bias after filter
PGND1	Power ground
HVIN	DC input voltage
PGND2	Power ground
HVOUT	DC output voltage
PGND3	Power ground
SW1	Switch node voltage

3.4 List of Terminals

Table 4. List of Terminals

TERMINAL	NAME	DESCRIPTION
J1	VIN	Input DC voltage input
J5	VOUT	Output DC voltage output
J6	12V AUX	12 V bias voltage input
J3	PWM INPUT	Single 0 V to 5 V PWM input for gate
J4	LOGIC	Header to connect PWM, FAULT logic
J2	HB Card PIN	Connector to interface LMG3410-HB-EVM board

4 Test Procedure

4.1 Setup

The following procedure is recommended to set up the LMG34XX-BB-EVM with the LMG3410-HB-EVM:

- Connect LMG3410-HB-EVM to LMG34XX-BB-EVM
- Connect oscilloscope or multimeter probes to desired test points as shown in A or G
- Connect the 12 V bias supply, load to the output, and input supply to the input
- Connect the function generator to either the BNC connector PWM input at C or 100 mil header connector input at pin 6 (PWM) and pin 5 (GND) at B.
- Enable an external fan to direct airflow across the heatsink attached to the LMG3410-HB-EVM

4.2 Startup and Operating Procedure

The following procedure is recommended to enable the LMG34XX-BB-EVM with the LMG3410-HB-EVM:

1. Power up the 12 V bias supply. Ensure the top right green “Aux Enable” LED is illuminated.
2. Enable PWM on the function generator
3. Power up high voltage input supply. Ensure the red “HV Enable” LED is illuminated when the input supply is above 20 V.

WARNING

Do NOT turn on device at absolute maximum voltage. It is recommended to start at voltages at or below 480 V, and then increase the input voltage slowly while monitoring V_{SW} to insure the peak voltage does not exceed the absolute maximum rating of 600 V.

4.3 Shutdown Procedure

1. Turn off input supply then PWM. Wait until red “HV Enable” LED turns off.
2. Disable 12 V bias supply

4.4 Additional Operation Notes

- Fault protection on the LMG34XX-BB-EVM is not latching, so if a fault clears and the LMG34XX-BB-EVM is still operational PWM will resume.

5 Typical Characteristics

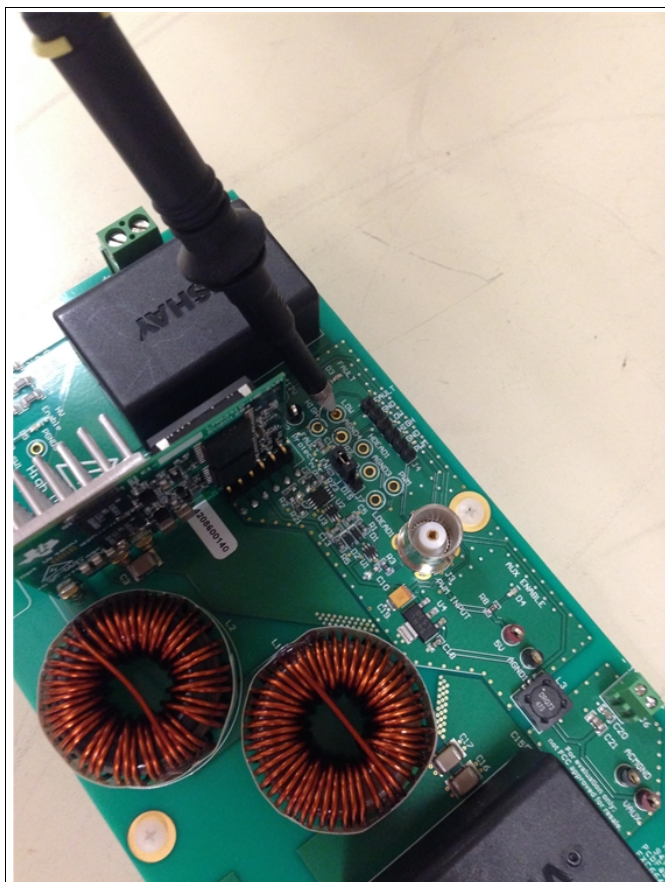


Figure 8. Recommended Probe Connection for Logic Signals

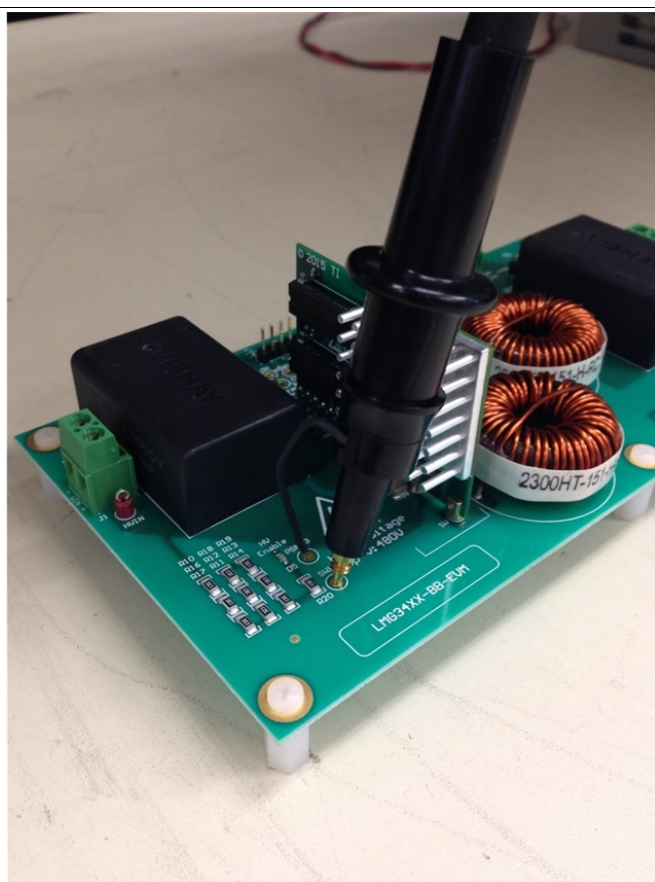


Figure 9. Recommended Probe Connection for High Voltage Switch Node

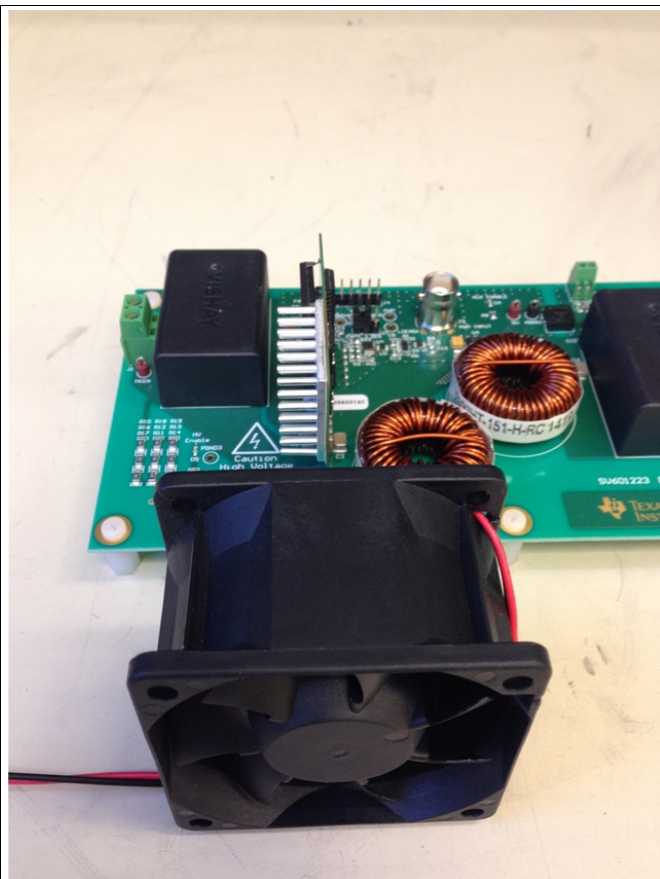


Figure 10. Recommended Configuration for Heatsink and Fan

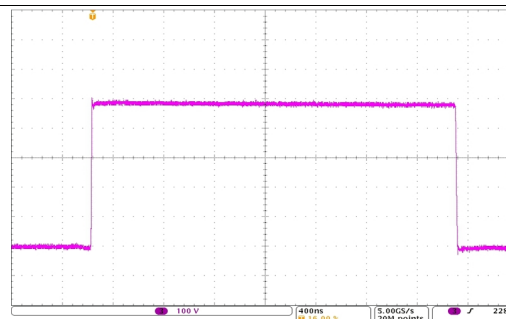


Figure 11. Switching Waveforms with 480V input, 100kHz, 30% duty cycle, 6A output

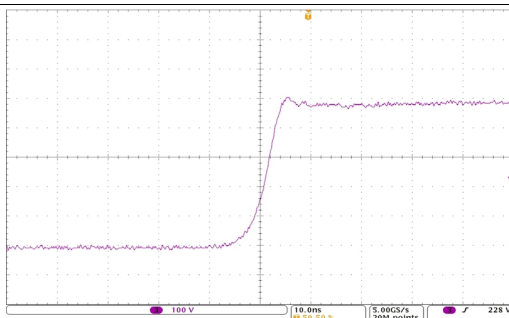


Figure 12. Low to High Transition Waveform with 480V input, 100kHz, 30% duty cycle, 6A output

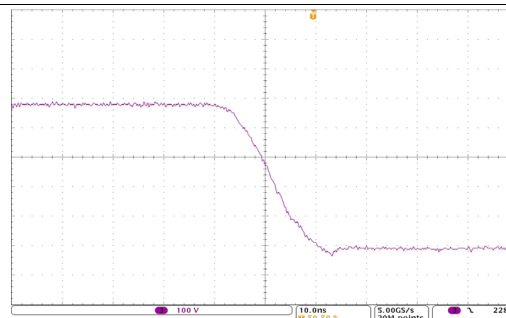


Figure 13. High to Low Transition Waveform with 480V input, 100kHz, 30% duty cycle, 6A output

6 EVM Assembly Drawing and PCB Layout

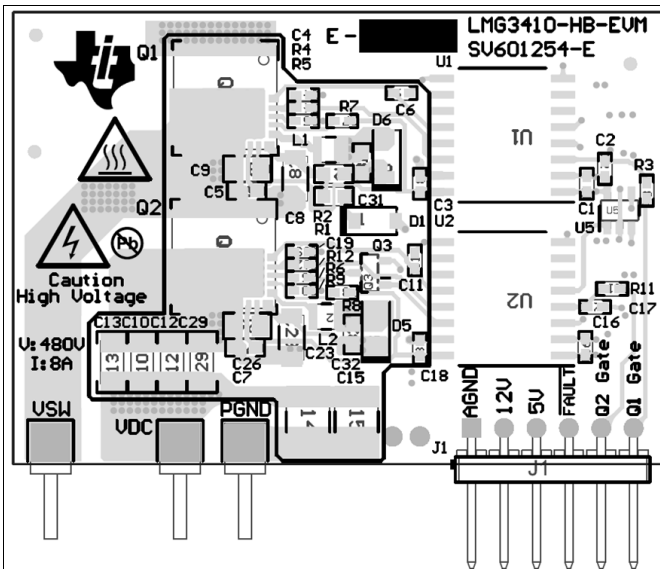


Figure 14. LMG3410-HB-EVM Top Layer and Components

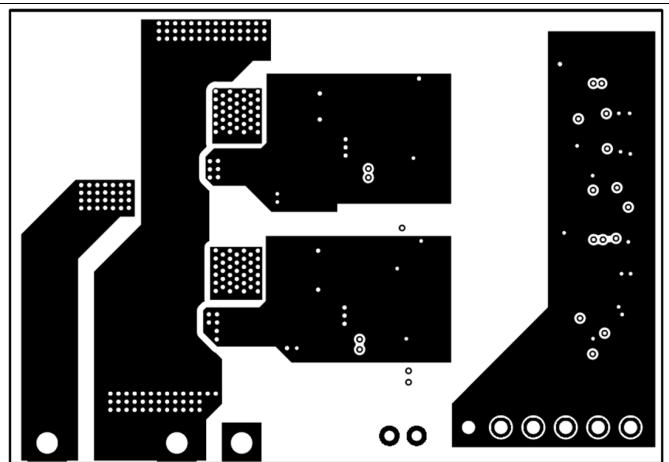


Figure 15. LMG3410-HB-EVM Inner Copper Layer 1

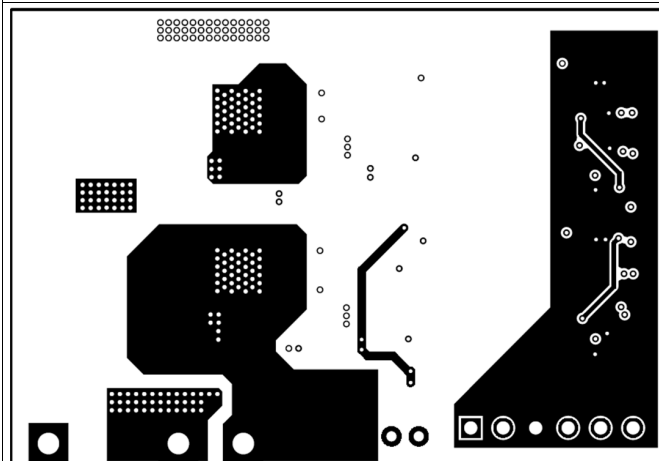


Figure 16. LMG3410-HB-EVM Inner Copper Layer 2

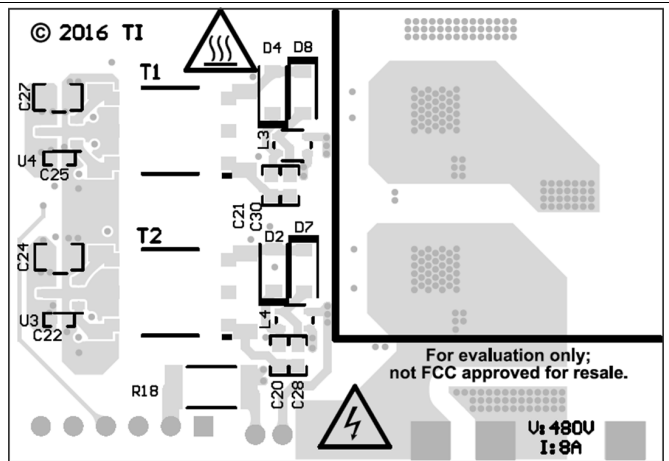


Figure 17. LMG3410-HB-EVM Bottom Layer and Components

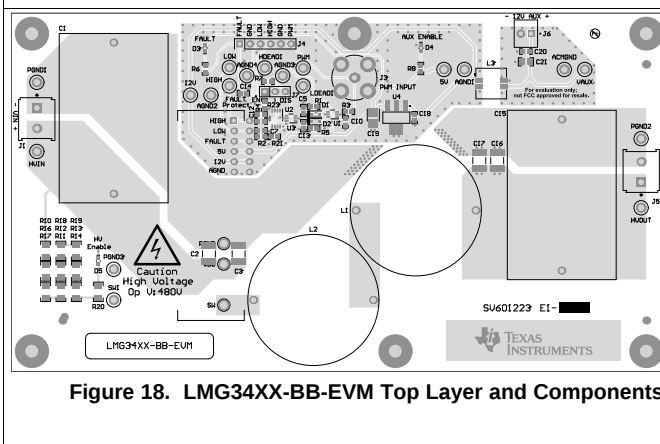


Figure 18. LMG34XX-BB-EVM Top Layer and Components

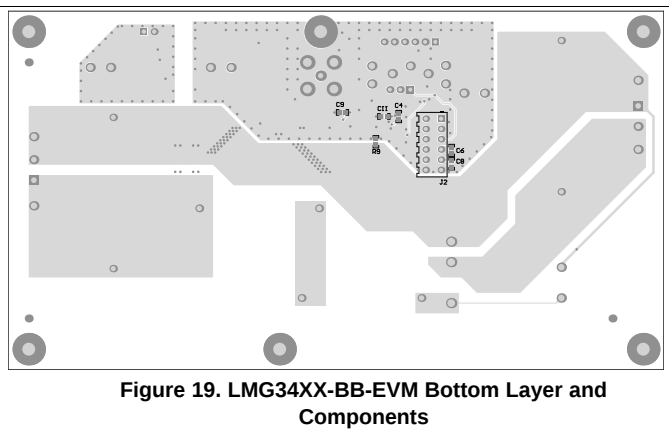


Figure 19. LMG34XX-BB-EVM Bottom Layer and Components

7 Bill of Materials

Table 5. LMG3410-HB-EVM List of Materials

Qty	Designator	Description	Part Number	Manufacturer
2	C1, C16	CAP, CERM, 1 μ F, 16 V, +/- 10%, X5R, 0402	EMK105BJ105KVHF	Taiyo Yuden
4	C2, C6, C11, C17	CAP, CERM, 68 pF, 50 V, +/- 5%, C0G/NP0, 0402	GRM1555C1H680JA01D	MuRata
4	C3, C18, C22, C25	CAP, CERM, 0.1 μ F, 50 V, +/- 10%, X7R, 0402	C1005X7R1H104K050BB	TDK
2	C4, C19	CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, 0402	C1005C0G1H220J050BA	TDK
2	C5, C7	CAP, CERM, 0.22 μ F, 50 V, +/- 10%, X7R, 0603	C1608X7R1H224K080AB	TDK
1	C8	CAP, CERM, 47 μ F, 25 V, +/- 20%, X5R, 1206_190	C3216X5R1E476M160AC	TDK
2	C9, C26	CAP, CERM, 2.2 μ F, 25V, +/-10%, X7R, 0805	GRM21BR71E225KA73L	MuRata
4	C10, C12, C13, C29	CAP, CERM, 0.01 μ F, 630V, +/-10%, X7R, 1206	GRM31BR72J103KW01L	MuRata
2	C14, C15	CAP, CERM, 0.1 μ F, 1000 V, +/- 10%, X7R, 1812	C1812W104KDRCTU	Kemet
6	C20, C21, C28, C30, C31, C32	CAP, CERM, 4.7 μ F, 35 V, +/- 10%, X5R, 0603	GRM188R6YA475KE15D	MuRata
1	C23	CAP, CERM, 10 μ F, 25 V, +/- 10%, X7R, 1206_190	C1206C106K3RACTU	Kemet
2	C24, C27	CAP, CERM, 4.7 μ F, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	GCM21BR71C475KA73K	MuRata
4	D2, D4, D7, D8	Diode, Schottky, 20 V, 0.5 A, SOD-123	MBR0520LT1G	ON Semiconductor
2	D5, D6	Diode, Zener, 16 V, 500 mW, SOD-123	MMSZ4703T1G	ON Semiconductor
1	HS1	'Cool Innovations Heat sink 1.00"x1.00"	3-101004U	Cool Innovations
1	J1	Header, 2.54mm, 6x1, Gold, R/A, TH	90121-0766	Molex
2	L1, L2	Inductor, Wirewound, 22 μ H, 0.49 A, 0.56 ohm, SMD	BRC2518T220K	Taiyo Yuden
2	L3, L4	Coupled inductor, 0.2 A, 0.45 ohm, SMD	ACM2520-601-2P-T002	TDK
2	Q1, Q2	600-V 12-A Single Channel GaN Power Stage, RWH0032A (VQFN-32)	LMG3410RWHT	Texas Instruments
1	Q3	MOSFET, N-CH, 20 V, 0.75 A, SOT-23	MGSF1N02LT1G	ON Semiconductor
1	R2	RES, 0, 5%, 0.1 W, 0603	CRCW06030000Z0EA	Vishay-Dale
4	R3, R4, R11, R12	RES, 49.9, 1%, 0.063 W, 0402	RC0402FR-0749R9L	Yageo America
1	R5	RES, 15 k, 5%, 0.063 W, 0402	CRCW040215K0JNED	Vishay-Dale
1	R6	RES, 17.8 k, 1%, 0.063 W, 0402	CRCW040217K8FKED	Vishay-Dale
2	R7, R8	RES, 10.0 k, 1%, 0.1 W, 0402	ERJ-2RKF1002X	Panasonic
1	R9	RES, 100 k, 1%, 0.063 W, 0402	RC1005F104CS	Samsung Electro-Mechanics
2	T1, T2	Transformer, 475 μ H, SMT	760390014	Würth Elektronik
1	TIM1	'Bergquist double sided thermal tape	'TI-Bond Ply100 0.005"/.127mm(1).cu-27.0mm by 27.0mm	Bergquist
3	TP1, TP2, TP3	Edge-Mount Pin, Gold	3620-1-32-15-00-00-08-0	Mill-Max
2	U1, U2	High-Performance, 8000 VPK Reinforced Triple Digital Isolator, DW0016B	ISO7831FDWR	Texas Instruments
2	U3, U4	Low-Noise 1 A, 420 kHz Transformer Driver, DBV0006A (SOT-6)	SN6505BDBVR	Texas Instruments
1	U5	Single 2-Input Positive-AND Gate, DBV0005A	SN74AHC1G08DBVR	Texas Instruments

Table 6. LMG34XX-BB-EVM List of Materials

Qty	Designator	Description	Part Number	Manufacturer
5	5V, 12V, HVIN, HVOUT, VAUX	Test Point, Compact, Red, TH	5005	Keystone
5	ACMGND, AGND1, AGND2, PGND1, PGND2	Test Point, Compact, Black, TH	5006	Keystone
2	C1, C15	CAP, Film, 5 μ F, 1000 V, +/- 5%, 0.016 ohm, TH	MKP1848S55010JP2C	Vishay-Components
4	C2, C3, C16, C17	CAP, CERM, 0.1 μ F, 630V, +/-10%, X7R, 1812	GRM43DR72J104KW01L	MuRata
5	C4, C6, C8, C9, C11	CAP, CERM, 1 μ F, 25 V, +/- 10%, X7R, 0603	C1608X7R1E105K080AB	TDK
2	C5, C13	CAP, CERM, 39 pF, 50 V, +/- 5%, COG/NPO, 0603	C1608C0G1H390J	TDK
1	C14	CAP, CERM, 1000 pF, 25 V, +/- 5%, COG/NPO, 0603	GRM1885C1E102JA01D	MuRata
2	C18, C20	CAP, CERM, 1 μ F, 25 V, +/- 10%, X7R, 0603	GRM188R71E105KA12D	MuRata
1	C19	CAP, TA, 33 μ F, 16 V, +/- 10%, 0.35 ohm, SMD	TPSB336K016R0350	AVX
1	C21	CAP, CERM, 10 μ F, 25 V, +/- 10%, X5R, 0805	GRM219R61E106KA12D	MuRata
2	D1, D2	Diode, Schottky, 30 V, 0.2 A, SOD-323	BAT54WS-7-F	Diodes Inc.
2	D3, D5	LED, Red, SMD	LS L29K-G1J2-1-Z	OSRAM
1	D4	LED, Green, SMD	LG L29K-G2J1-24-Z	OSRAM
6	H1, H2, H3, H4, H9, H10	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH	B and F Fastener Supply
6	H5, H6, H7, H8, H11, H12	Standoff, Hex, 0.5"L #4-40 Nylon	1902C	Keystone
2	J1, J5	Terminal Block, 2x1, 5.08mm, TH	282841-2	TE Connectivity
1	J2	Receptacle, 2.54mm, 6x1, Gold, TH	448120024	Molex
1	J3	Connector, TH, BNC	112404	Amphenol Connex
1	J4	Header, 100mil, 6x1, Gold, TH	TSW-106-07-G-S	Samtec
1	J6	Terminal Block, 2x1, 2.54mm, TH	282834-2	TE Connectivity
1	J7	Header, 100mil, 3x1, Gold, TH	TSW-103-07-G-S	Samtec
2	L1, L2	Inductor, Toroid, 150 μ H, 7.5 A, 0.05 ohm, TH	2300HT-151-H-RC	Bourns
1	L3	Coupled inductor, 47 μ H, 1.14 A, 0.241 ohm, +/- 20%, SMD	DRQ73-470-R	Cooper Bussman
3	PGND, SW, VDC	Pin Receptacle, .032-.046" .075" Dia, Gold, TH	0312-0-15-15-34-27-10-0	Mill-Max
2	R1, R5	RES, 1.20 k, 1%, 0.1 W, 0603	RC0603FR-071K2L	Yageo America
6	R2, R3, R4, R9, R21, R23	RES, 0, 5%, 0.1 W, 0603	CRCW06030000Z0EA	Vishay-Dale
2	R6, R8	RES, 1.6 k, 5%, 0.1 W, 0603	CRCW06031K60JNEA	Vishay-Dale
1	R7	RES, 10.0 k, 1%, 0.1 W, 0603	ERJ-3EKF1002V	Panasonic
10	R10, R11, R12, R13, R14, R16, R17, R18, R19, R20	RES, 30 k, 5%, 0.25 W, 1206	CRCW120630K0JNEA	Vishay-Dale
1	SH-J1	Shunt, 100mil, Gold plated, Black	969102-0000-DA	3M
2	U1, U3	Dual Schmitt-Trigger Inverter, DCK0006A	SN74LVC2G14DCKR	Texas Instruments
1	U2	DUAL 2-INPUT POSITIVE-AND GATE, DCT0008A	SN74LVC2G08IDCTRQ1	Texas Instruments
1	U4	1A Low Dropout Regulator, 4-pin SOT-223, Pb-Free	LM2940IMP-5.0/NOPB	Texas Instruments

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2016) to A Revision	Page
• Changed Figure 1, Updated Fault connection in schematics	4
• Changed Section 1.1.1, Updated Fault connection description	5
• Changed Section 1.1.4, Updated Heatsink description	6
• Changed Figure 2, Updated Front and Back Side Photos of LMG3410-HB-EVM.....	6
• Changed Figure 3 and 4	8
• Changed figures 14, 15, 16 and 17	17
• Changed Table 5, Updated LMG3410-HB-EVM List of Materials	18

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- 3 **Regulatory Notices:**

- 3.1 **United States**

- 3.1.1 **Notice applicable to EVMs not FCC-Approved:**

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

- 3.1.2 **For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:**

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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