

TLV225x-Q1, TLV225xA-Q1
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER OPERATIONAL AMPLIFIERS

SGLS192B – OCTOBER 2003 – REVISED APRIL 2008

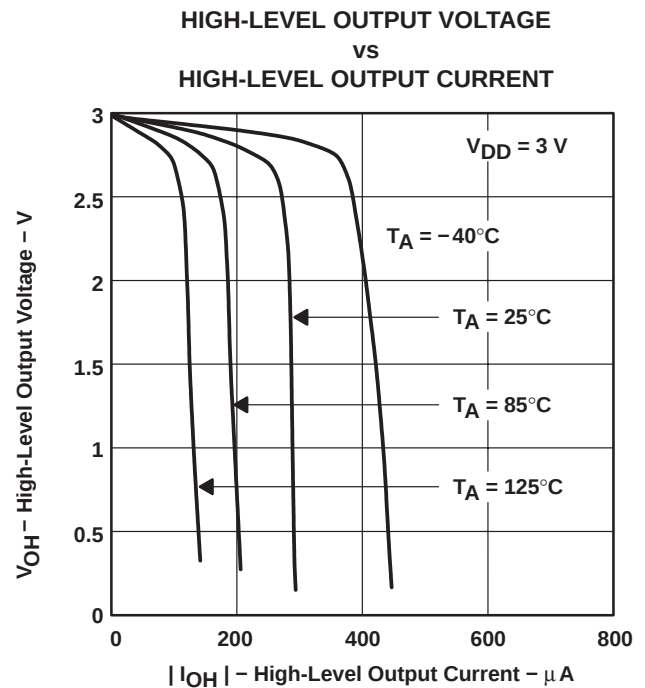
- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 150 V (TLV2252/52A) and 100 V (TLV2254/54A) Using Machine Model (C = 200 pF, R = 0)
- Output Swing Includes Both Supply Rails
- Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Very Low Power . . . 34 μA Per Channel Typ
- Common-Mode Input Voltage Range Includes Negative Rail
- Low Input Offset Voltage
850 μV Max at T_A = 25°C
- Wide Supply Voltage Range
2.7 V to 16 V
- Macromodel Included

description

The TLV2252 and TLV2254 are dual and quad low-voltage operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLV225x family consumes only 34 μA of supply current per channel. This micropower operation makes them good choices for battery-powered applications. This family is fully characterized at 3 V and 5 V and is optimized for low-voltage applications. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. The TLV225x has a noise level of 19 nV/√Hz at 1kHz, four times lower than competitive micropower solutions.

The TLV225x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV225xA family is available and has a maximum input offset voltage of 850 μV.

The TLV2252/4 also make great upgrades to the TLV2322/4 in standard designs. They offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442 devices. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ORDERING INFORMATION†

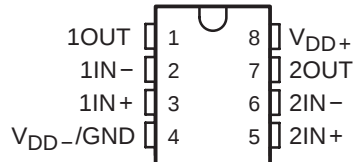
T _A	V _{IO} max AT 25°C	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	850 µV	SOIC (D)	Tape and reel	TLV2252AQDRQ1	2252AQ
		TSSOP (PW)	Tape and reel	TLV2252AQPWRQ1§	
	1500 µV	SOIC (D)	Tape and reel	TLV2252QDRQ1	2252Q1
		TSSOP (PW)	Tape and reel	TLV2252QPWRQ1§	
–40°C to 125°C	850 µV	SOIC (D)	Tape and reel	TLV2254AQDRQ1	TLV2254AQ1
		TSSOP (PW)	Tape and reel	TLV2254AQPWRQ1§	
	1500 µV	SOIC (D)	Tape and reel	TLV2254QDRQ1	TLV2254Q1
		TSSOP (PW)	Tape and reel	TLV2254QPWRQ1§	

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

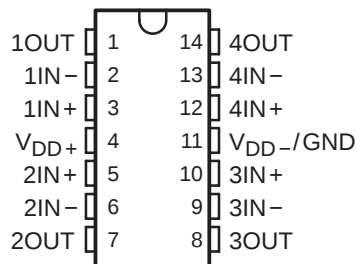
‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

§ Product preview

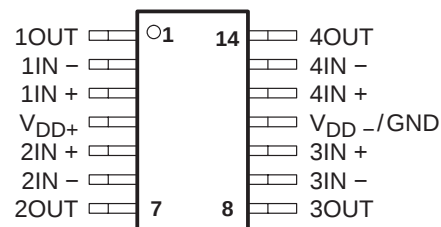
TLV2252, TLV2252A
D OR PW PACKAGE
(TOP VIEW)



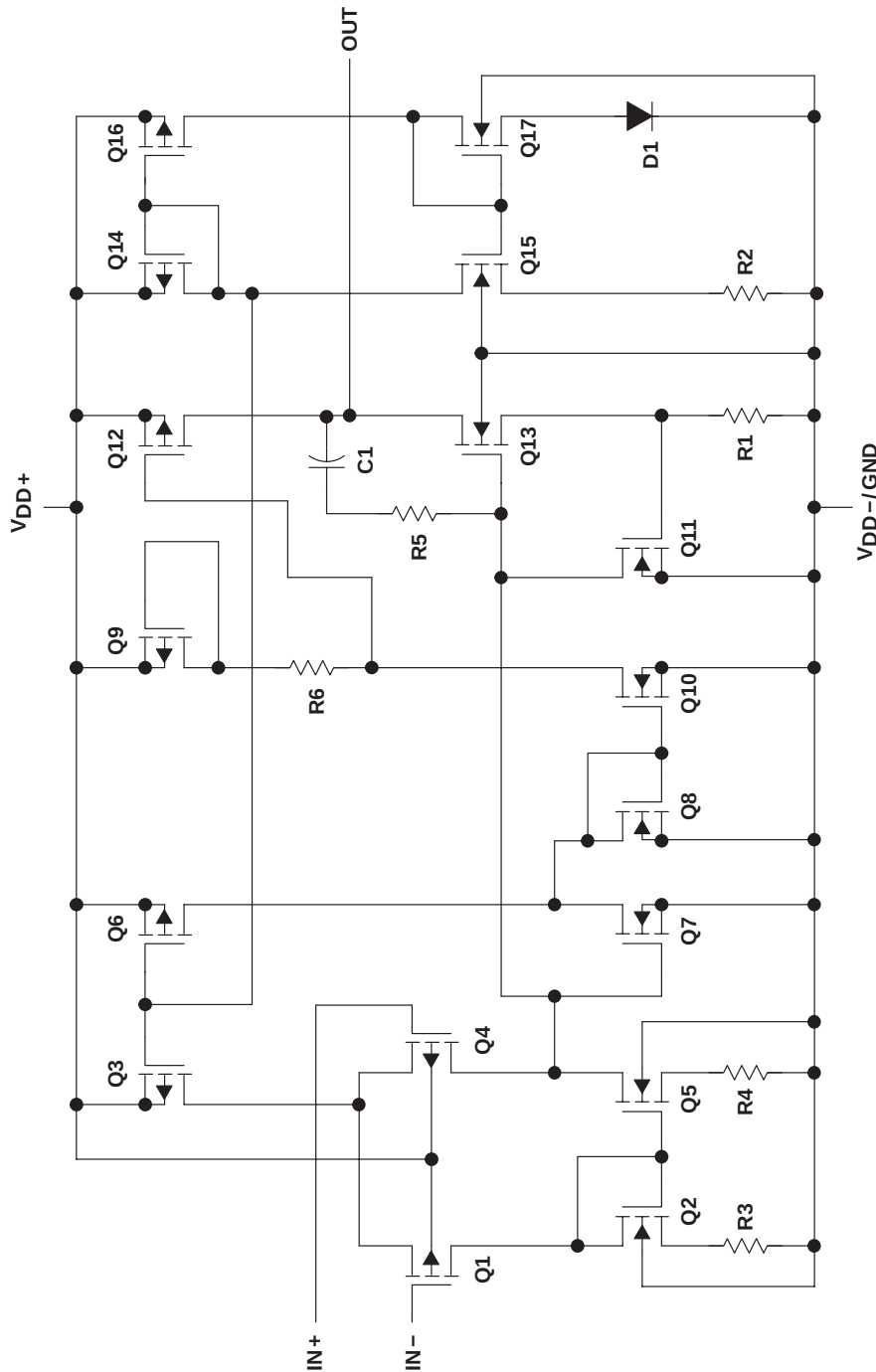
TLV2254, TLV2254A
D PACKAGE
(TOP VIEW)



TLV2254, TLV2254A
PW PACKAGE
(TOP VIEW)



equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLV2252	TLV2254
Transistors	38	76
Resistors	30	56
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	16 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1)	$V_{DD} - 0.3$ V to $V_{DD} +$
Input current, I_I (each input)	± 5 mA
Output current, I_O	± 50 mA
Total current into $V_{DD} +$	± 50 mA
Total current out of $V_{DD} -$	± 50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : Q Suffix	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and PW packages	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to $V_{DD} -$.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below $V_{DD} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D-8	725 mW	5.8 mW/°C	377 mW	145 mW
D-14	950 mW	7.6 mW/°C	494 mW	190 mW
PW-8	525 mW	4.2 mW/°C	273 mW	105 mW
PW-14	700 mW	5.6 mW/°C	364 mW	140 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD} (see Note 1)	2.7	16	V
Input voltage range, V_I	$V_{DD} -$	$V_{DD} + 1.3$	V
Common-mode input voltage, V_{IC}	$V_{DD} -$	$V_{DD} + 1.3$	V
Operating free-air temperature, T_A	-40	125	°C

NOTE 1: All voltage values, except differential voltages, are with respect to $V_{DD} -$.

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TLV2252-Q1 electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLV2252-Q1		TLV2252A-Q1		UNIT
					MIN	TYP	MAX	MIN	
V _{IO}	Input offset voltage	V _{DD±} = ±1.5 V, V _{IC} = 0, V _O = 0, R _S = 50 Ω		25°C	200	1500	200	850	μV
	Full range			1750		1000			
α _{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C	0.5		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.003		0.003		μV/mo
I _{IO}	Input offset current			25°C	0.5	60	0.5	60	pA
				125°C	1000		1000		
I _{IB}	Input bias current			25°C	1	60	1	60	pA
				125°C	1000		1000		
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω, V _{IO} ≤5 mV	25°C	0 to 2	−0.3 to 2.2	0 to 2	−0.3 to 2.2	V	
			Full range	0 to 1.7		0 to 1.7			
V _{OH}	High-level output voltage	I _{OH} = −20 μA	25°C	2.98		2.98		V	
		I _{OH} = −75 μA	25°C	2.9		2.9			
			Full range	2.8		2.8			
		I _{OH} = −150 μA	25°C	2.8		2.8			
V _{OL}	Low-level output voltage	V _{IC} = 1.5 V, I _{OL} = 50 μA	25°C	10		10		mV	
		V _{IC} = 1.5 V, I _{OL} = 500 μA	25°C	100	150	100	150		
			Full range	165		165			
		V _{IC} = 1.5 V, I _{OL} = 1 mA	25°C	200	300	200	300		
			Full range	300		300			
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 1.5 V, V _O = 1 V to 2 V	R _L = 100 kΩ [‡]	25°C	100	250	100	250	V/mV
				Full range	10		10		
			R _L = 1 MΩ [‡]	25°C	800		800		
r _{i(d)}	Differential input resistance			25°C	10 ¹²		10 ¹²		Ω
r _{i(c)}	Common-mode input resistance			25°C	10 ¹²		10 ¹²		Ω
c _{i(c)}	Common-mode input capacitance	f = 10 kHz		25°C	8		8		pF
z _O	Closed-loop output impedance	f = 25 kHz,	A _V = 10	25°C	220		220		Ω
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 1.7 V, V _O = 1.5 V, R _S = 50 Ω		25°C	65	75	65	77	dB
				Full range	60		60		
k _{SVR}	Supply voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 2.7 V to 8 V, V _{IC} = V _{DD} /2, No load		25°C	80	95	80	100	dB
				Full range	80		80		
I _{DD}	Supply current	V _O = 1.5 V, No load		25°C	68	125	68	125	μA
				Full range	150		150		

† Full range is -40°C to 125°C for Q level part.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLV2252-Q1 operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV2252-Q1			TLV2252A-Q1			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 0.8\text{ V to }1.4\text{ V}, R_L = 100\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C	0.07	0.1		0.07	0.1		V/ μs
		Full range	0.05			0.05			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		35			35		nV/ $\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C		19			19		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		0.6			0.6		μV
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.1			1.1		
I_n Equivalent input noise current		25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
Gain-bandwidth product	$f = 1\text{ kHz}, R_L = 50\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C		0.187			0.187		MHz
B_{OM} Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}, R_L = 50\text{ k}\Omega^\ddagger, A_V = 1, C_L = 100\text{ pF}^\ddagger$	25°C		60			60		kHz
ϕ_m Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C		63°			63°		
Gain margin		25°C		15			15		dB

† Full range is -40°C to 125°C for Q level part.

‡ Referenced to 1.5 V



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TLV2252-Q1 electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLV2252-Q1			TLV2252A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{DD±} = ±2.5 V, V _{IC} = 0, V _O = 0, R _S = 50 Ω		25°C	200	1500		200	850	μV	
	Full range						1750	1000			
αV _{IO}	Temperature coefficient of input offset voltage			25°C to 85°C	0.5			0.5			μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.003			0.003			μV/mo
I _{IO}	Input offset current			25°C	0.5	60		0.5	60	pA	
				125°C	1000			1000			
I _{IB}	Input bias current			25°C	1	60		1	60	pA	
				125°C	1000			1000			
V _{ICR}	Common-mode input voltage range	V _{IO} ≤ 5 mV, R _S = 50 Ω		25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2	V	
				Full range	0 to 3.5				0 to 3.5		
V _{OH}	High-level output voltage	I _{OH} = −20 μA		25°C	4.98			4.98			V
		I _{OH} = −75 μA		25°C	4.9	4.94		4.9	4.94		
				Full range	4.8			4.8			
		I _{OH} = −150 μA		25°C	4.8	4.88		4.8	4.88		
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 50 μA		25°C	0.01			0.01			V
		V _{IC} = 2.5 V, I _{OL} = 500 μA		25°C	0.09	0.15		0.09	0.15		
				Full range	0.15			0.15			
		V _{IC} = 2.5 V, I _{OL} = 1 mA		25°C	0.2	0.3		0.2	0.3		
				Full range	0.3			0.3			
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V	R _L = 100 kΩ [‡]	25°C	100	350		100	350	V/mV	
				Full range	10			10			
			R _L = 1 MΩ [‡]	25°C	1700			1700			
r _{i(d)}	Differential input resistance			25°C	10 ¹²			10 ¹²			Ω
r _{i(c)}	Common-mode input resistance			25°C	10 ¹²			10 ¹²			Ω
c _{i(c)}	Common-mode input capacitance	f = 10 kHz		25°C	8			8			pF
z _o	Closed-loop output impedance	f = 25 kHz,	A _V = 10	25°C	200			200			Ω
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 2.7 V, V _O = 2.5 V, R _S = 50 Ω		25°C	70	83		70	83	dB	
				Full range	70			70			
k _{SVR}	Supply voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 4.4 V to 8 V, V _{IC} = V _{DD} /2, No load		25°C	80	95		80	95	dB	
				Full range	80			80			

† Full range is -40°C to 125°C for Q level part.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLV2252-Q1 electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2252-Q1			TLV2252A-Q1			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C		70	125		70	125	μA
		Full range			150			150	

† Full range is -40°C to 125°C for Q level part.

TLV2252-Q1 operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLV2252-Q1			TLV2252A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 1.25 V to 2.75 V, R _L = 100 kΩ [‡] , C _L = 100 pF [‡]		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	36			36			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.7			0.7			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 20 kHz, R _L = 50 kΩ [‡]	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
Gain-bandwidth product		f = 50 kHz, C _L = 100 pF [‡]	R _L = 50 kΩ [‡] ,	25°C	0.2			0.2			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 50 kΩ [‡] ,	A _V = 1, C _L = 100 pF [‡]	25°C	30			30			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ [‡] ,	C _L = 100 pF [‡]	25°C	63°			63°			
Gain margin				25°C	15			15			dB

† Full range is -40°C to 125°C for Q level part.

‡ Referenced to 2.5 V



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TLV2254-Q1 electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2254-Q1			TLV2254A-Q1			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} \pm \pm 1.5\text{ V}, V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C	200	1500		200	850		μV
		Full range		1750			1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		125°C		1000			1000		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		125°C		1000			1000		
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	0 to 2	-0.3 to 2.2		0 to 2	-0.3 to 2.2		V
		Full range	0 to 1.7			0 to 1.7			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		2.98			2.98		V
	$I_{OH} = -75\ \mu\text{A}$	25°C		2.9			2.9		
		Full range		2.8			2.8		
	$I_{OH} = -150\ \mu\text{A}$	25°C		2.8			2.8		
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V}, I_{OL} = 50\ \mu\text{A}$	25°C		10			10		mV
	$V_{IC} = 1.5\text{ V}, I_{OL} = 500\ \mu\text{A}$	25°C		100	150		100	150	
		Full range			165			165	
	$V_{IC} = 1.5\text{ V}, I_{OL} = 1\text{ mA}$	25°C		200	300		200	300	
		Full range			300			300	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 1.5\text{ V}, V_O = 1\text{ V to }2\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C	100	225		100	225	V/mV
			Full range	10			10		
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C		800			800	
$r_{i(d)}$ Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}, A_V = 10$	25°C		220			220		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }1.7\text{ V}, V_O = 1.5\text{ V}, R_S = 50\ \Omega$	25°C	65	75		65	77		dB
		Full range	60			60			
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to }8\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95		80	100		dB
		Full range	80			80			

† Full range is -40°C to 125°C for Q level part.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLV2254-Q1 electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2254-Q1			TLV2254A-Q1			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD} Supply current (four amplifiers)	$V_O = 1.5\text{ V}$, No load	25°C		135	250		135	250	μA
		Full range			300			300	

† Full range is -40°C to 125°C for Q level part.

TLV2254-Q1 operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2254-Q1			TLV2254A-Q1			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 0.5\text{ V}$ to 1.7 V , $R_L = 100\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C	0.07	0.1		0.07	0.1		$\text{V}/\mu\text{s}$
		Full range	0.05			0.05			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		35			35		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C		19			19		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz}$ to 1 Hz	25°C		0.6			0.6		μV
	$f = 0.1\text{ Hz}$ to 10 Hz	25°C		1.1			1.1		
I_n Equivalent input noise current		25°C		0.6			0.6		$\text{fA}/\sqrt{\text{Hz}}$
Gain-bandwidth product	$f = 1\text{ kHz}$, $R_L = 50\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		0.187			0.187		MHz
B_{OM} Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V}$, $A_V = 1$, $R_L = 50\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		60			60		kHz
ϕ_m Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		63°			63°		
Gain margin		25°C		15			15		dB

† Full range is -40°C to 125°C for Q level part.

‡ Referenced to 1.5 V

TLV2254-Q1 electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2254-Q1			TLV2254A-Q1			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} = \pm 2.5\text{ V}, V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C		200	1500		200	850	μV
		Full range			1750			1000	
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C		0.5			0.5		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.5	60		0.5	60	pA
		125°C			1000			1000	
I_{IB} Input bias current		25°C		1	60		1	60	pA
		125°C			1000			1000	
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}, R_S = 50\ \Omega$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		V
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.98			4.98		V
	$I_{OH} = -75\ \mu\text{A}$	25°C		4.9	4.94		4.9	4.94	
		Full range		4.8			4.8		
	$I_{OH} = -150\ \mu\text{A}$	25°C		4.8	4.88		4.8	4.88	
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}, I_{OL} = 50\ \mu\text{A}$	25°C		0.01			0.01		V
	$V_{IC} = 2.5\text{ V}, I_{OL} = 500\ \mu\text{A}$	25°C		0.09	0.15		0.09	0.15	
		Full range			0.15			0.15	
	$V_{IC} = 2.5\text{ V}, I_{OL} = 1\text{ mA}$	25°C		0.2	0.3		0.2	0.3	
		Full range			0.3			0.3	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}, V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C	100	350		100	350	V/mV
			Full range	10			10		
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C		1700			1700	
$r_{i(d)}$ Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}, A_V = 10$	25°C		200			200		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}, V_O = 2.5\text{ V}, R_S = 50\ \Omega$	25°C	70	83		70	83		dB
		Full range	70			70			
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95		80	95		dB
		Full range	80			80			

† Full range is -40°C to 125°C for Q level part.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLV2254-Q1 electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLV2254-Q1			TLV2254A-Q1			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load	25°C		140	250		140	250	μA
		Full range			300			300	

† Full range is -40°C to 125°C for Q level part.

TLV2254-Q1 operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLV2254-Q1			TLV2254A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 0.5 V to 3.5 V, R _L = 100 kΩ [‡] , C _L = 100 pF [‡]		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	36			36			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.7			0.7			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 20 kHz, R _L = 50 kΩ [‡]	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
	Gain-bandwidth product	f = 50 kHz, C _L = 100 pF [‡]	R _L = 50 kΩ [‡] ,	25°C	0.2			0.2			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 50 kΩ [‡] ,	A _V = 1, C _L = 100 pF [‡]	25°C	30			30			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ [‡] , C _L = 100 pF [‡]		25°C	63°			63°			
	Gain margin			25°C	15			15			dB

† Full range is -40°C to 125°C for Q level part.

‡ Referenced to 2.5 V



TYPICAL CHARACTERISTICS

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DISTRIBUTION OF TLV2252
INPUT OFFSET VOLTAGE

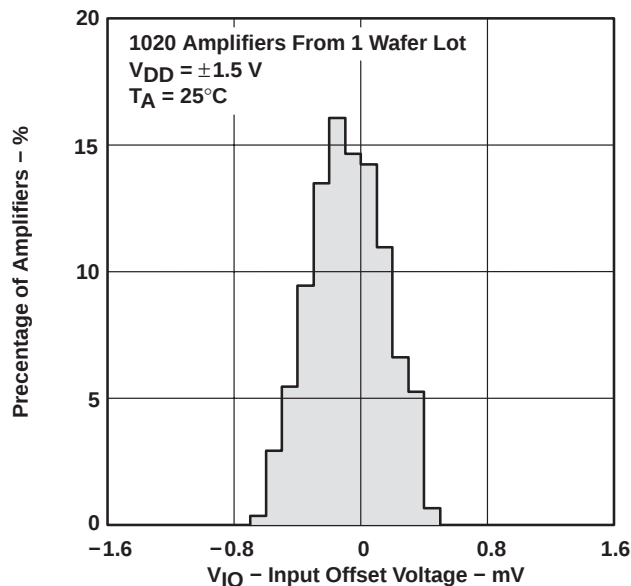


Figure 2

DISTRIBUTION OF TLV2252
INPUT OFFSET VOLTAGE

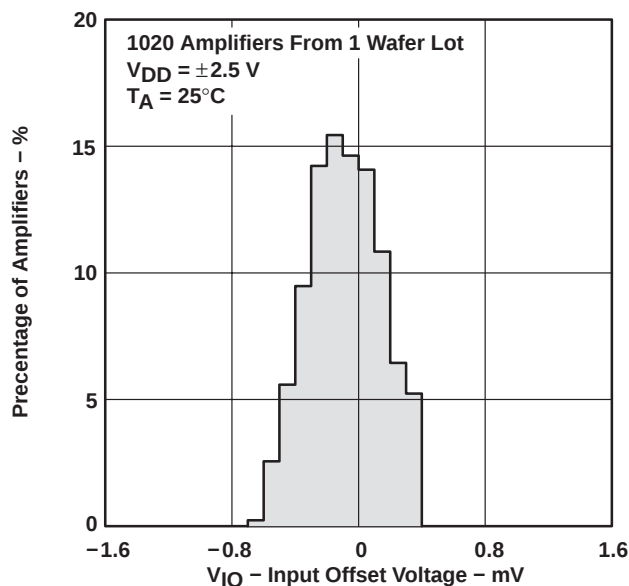


Figure 3

DISTRIBUTION OF TLV2254
INPUT OFFSET VOLTAGE

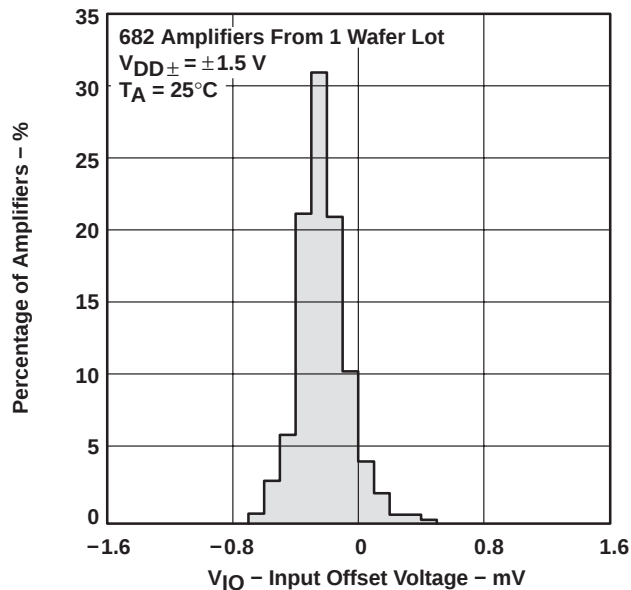


Figure 4

DISTRIBUTION OF TLV2254
INPUT OFFSET VOLTAGE

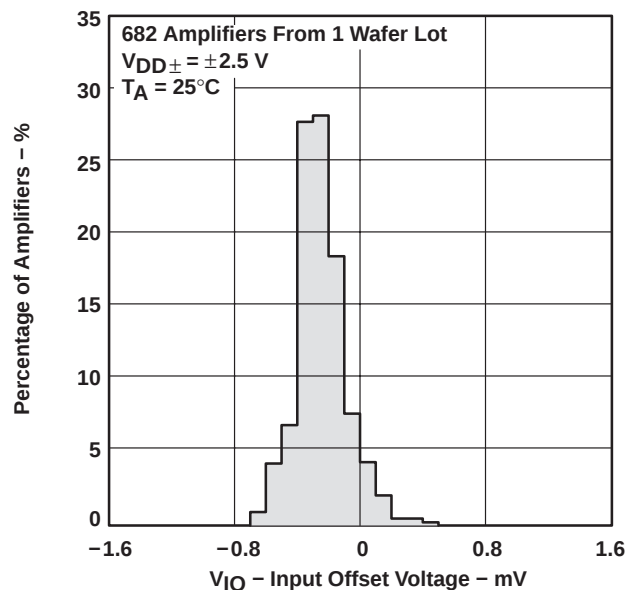


Figure 5

TYPICAL CHARACTERISTICS

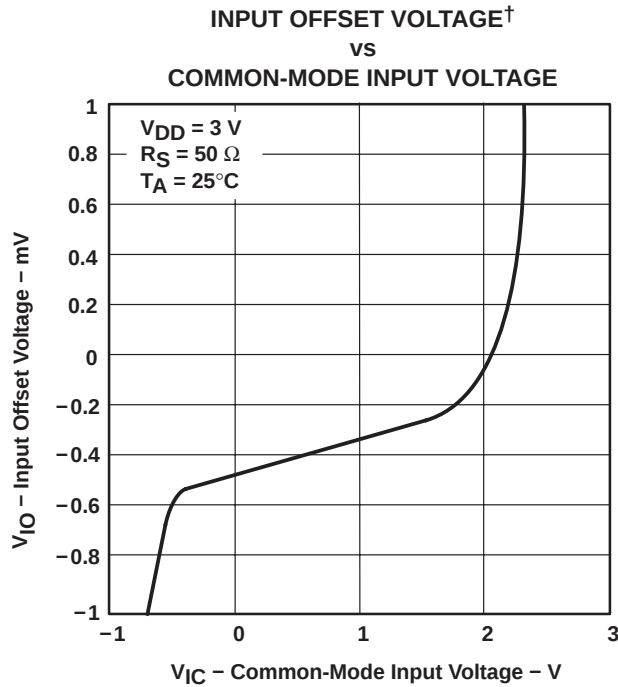


Figure 6

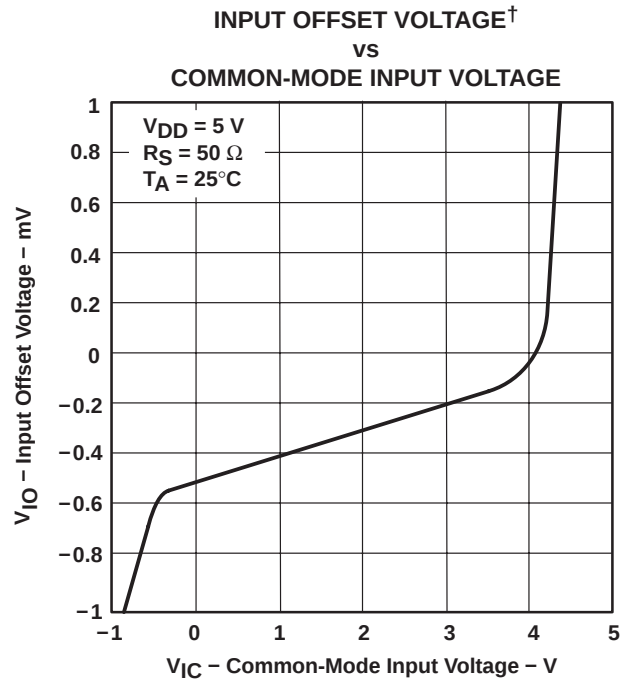


Figure 7

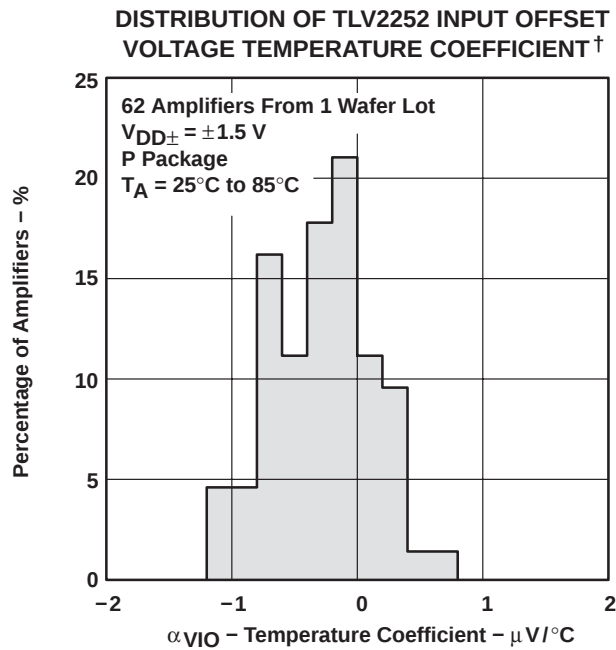


Figure 8

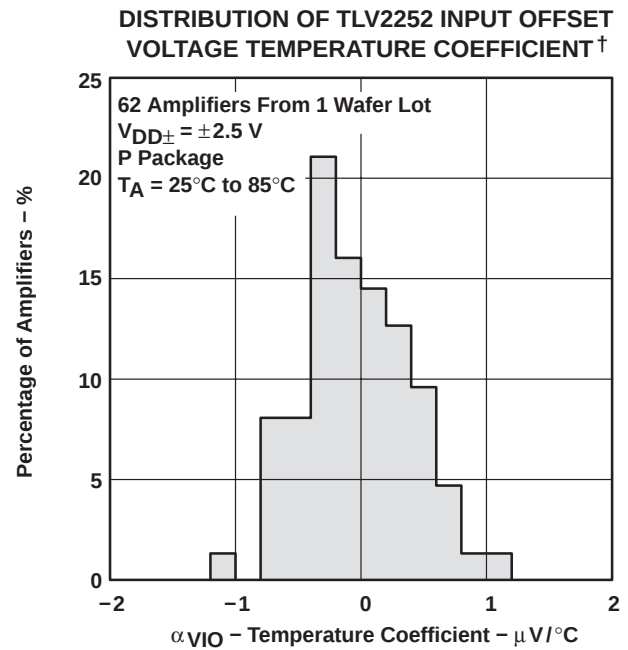


Figure 9

[†] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

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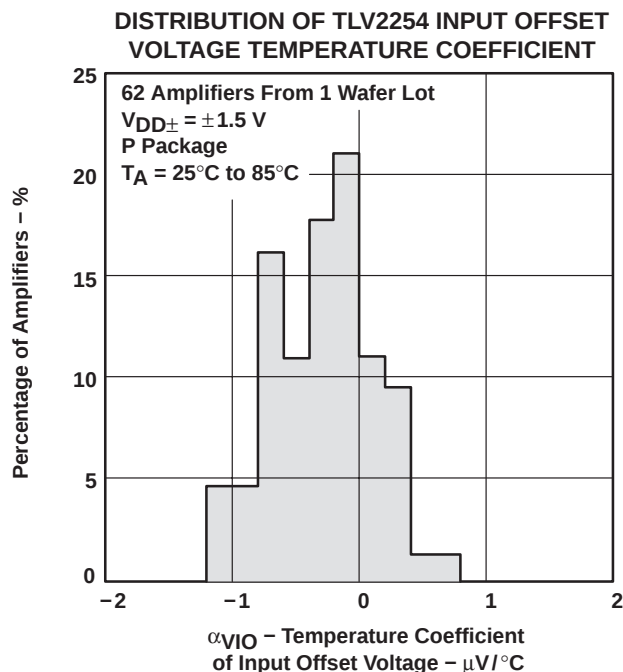


Figure 10

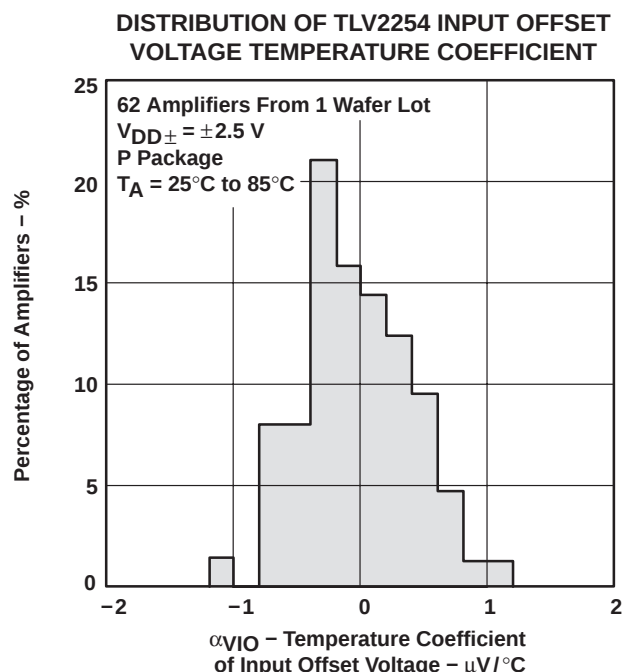


Figure 11

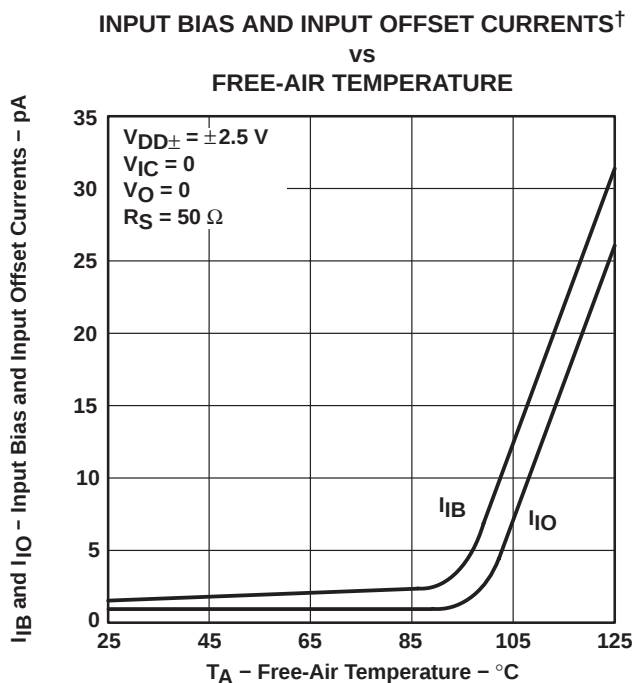


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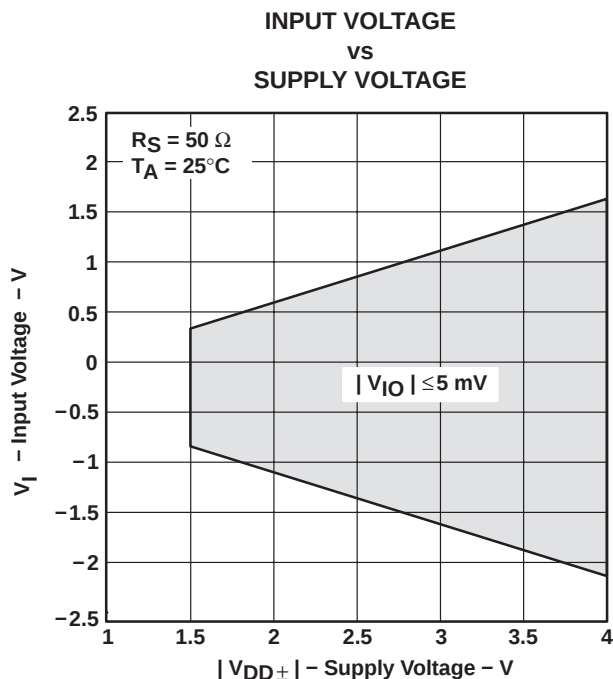
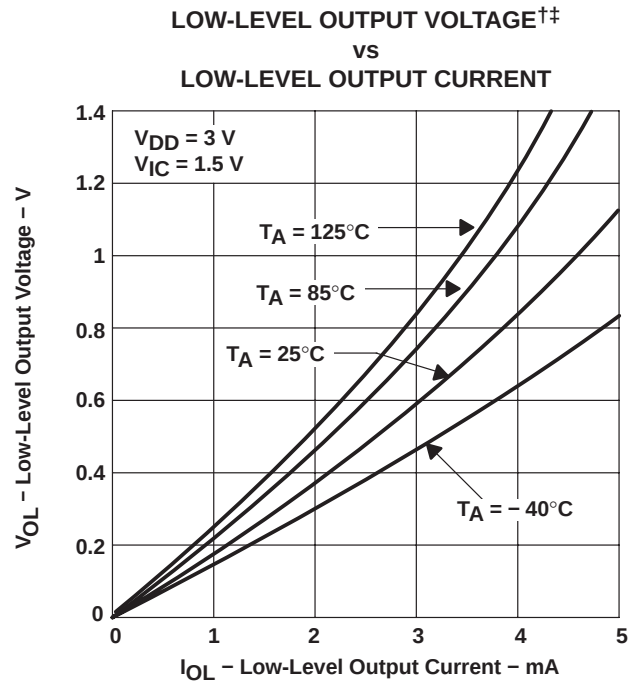
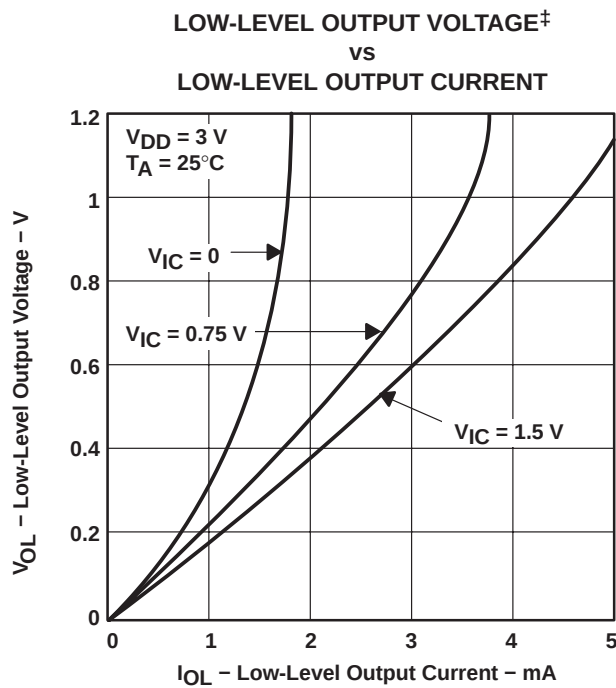
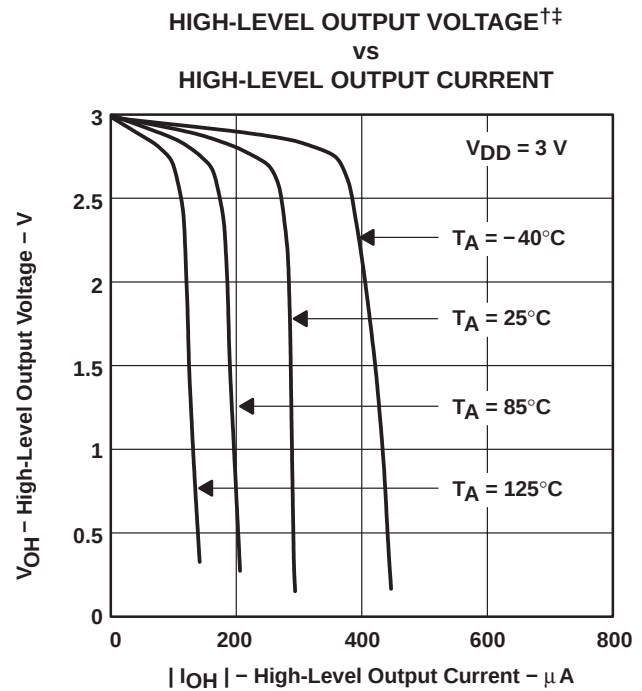
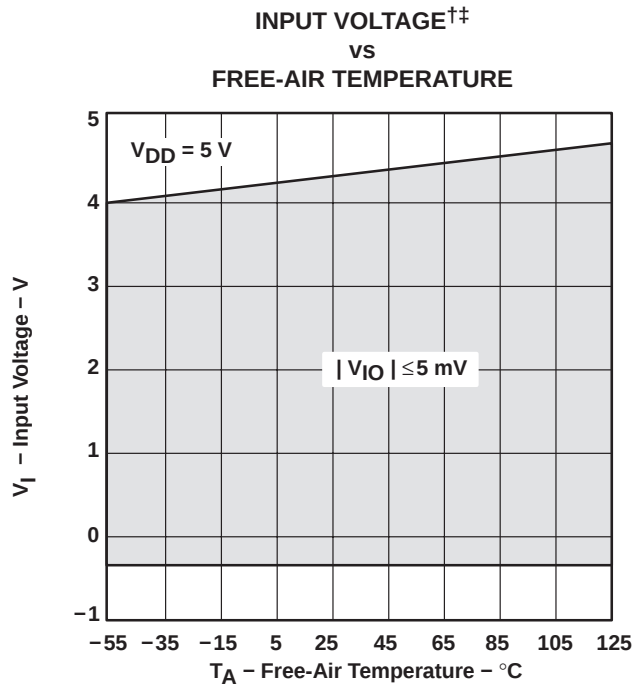


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

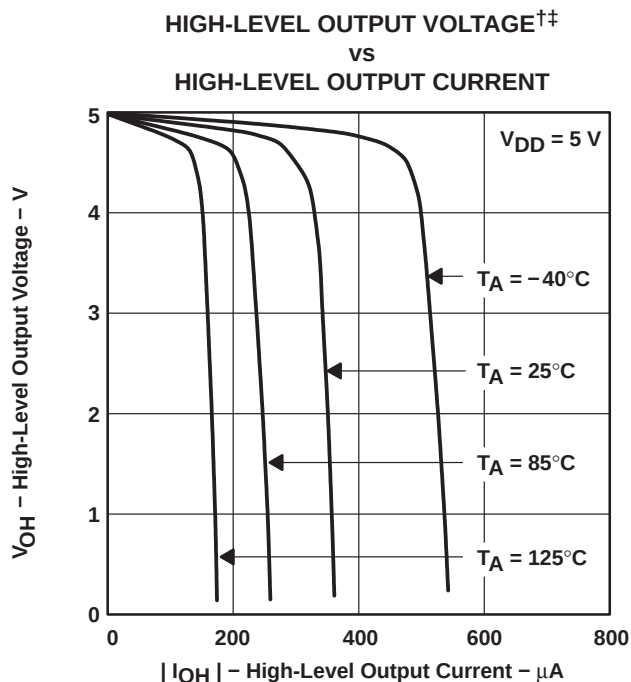


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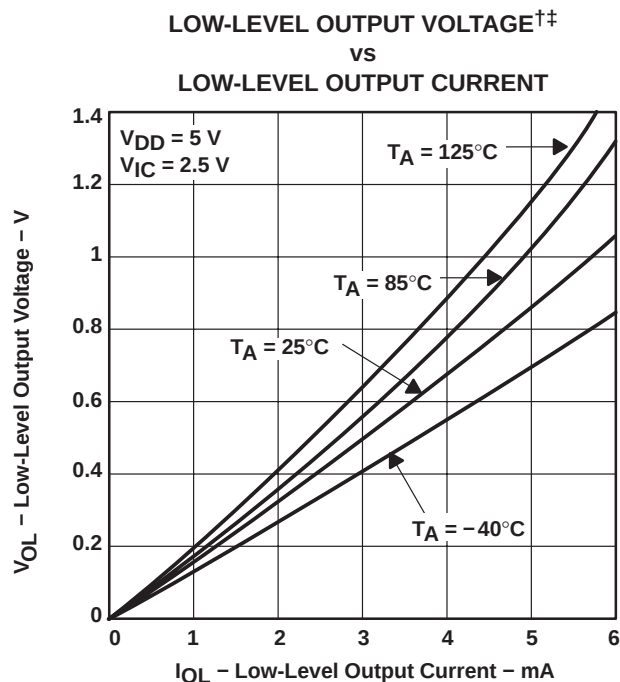


Figure 19

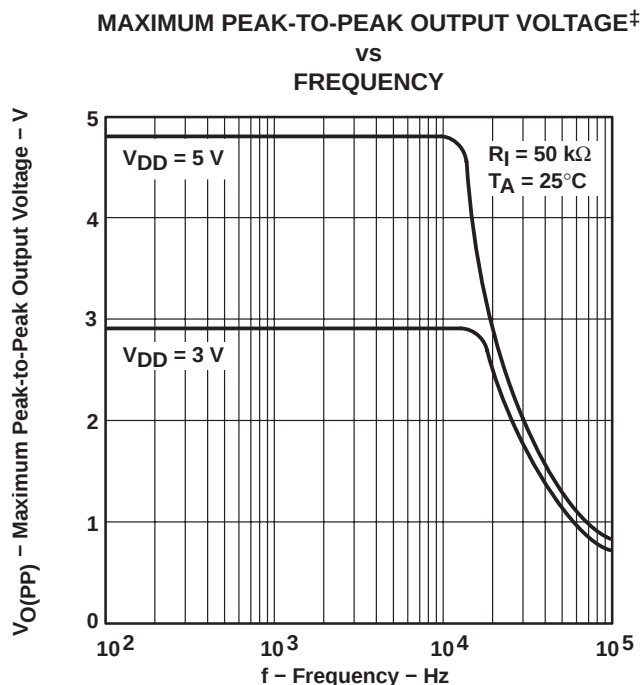


Figure 20

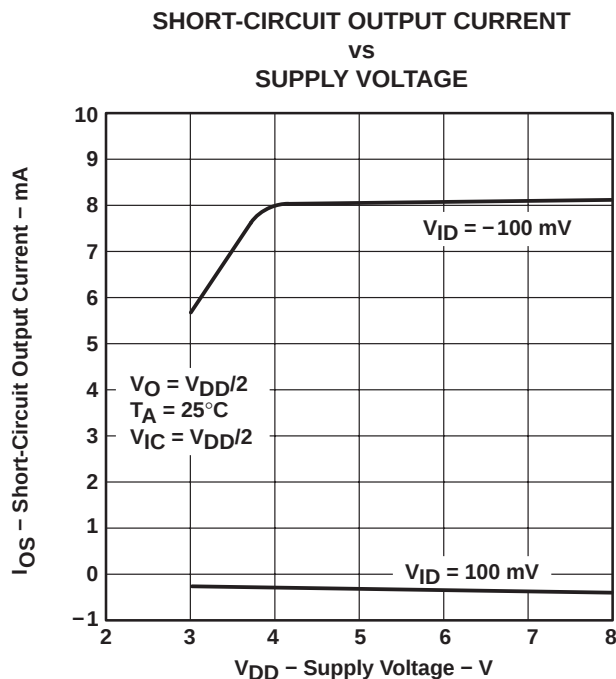
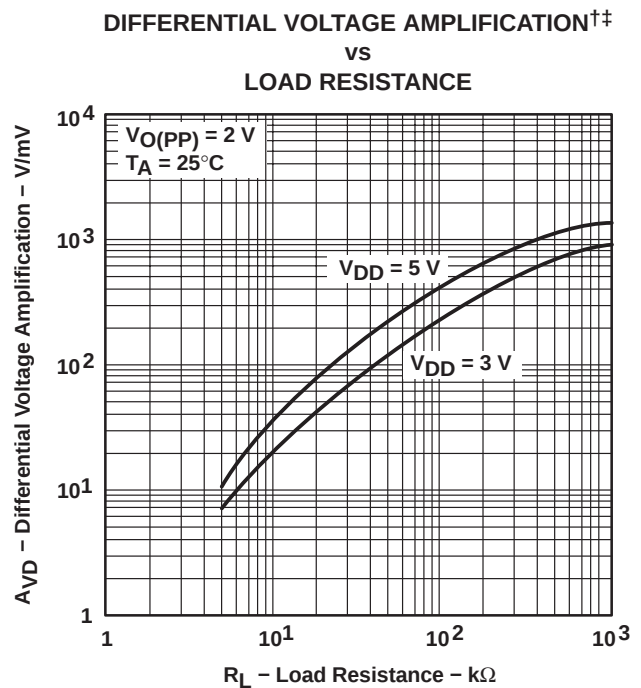
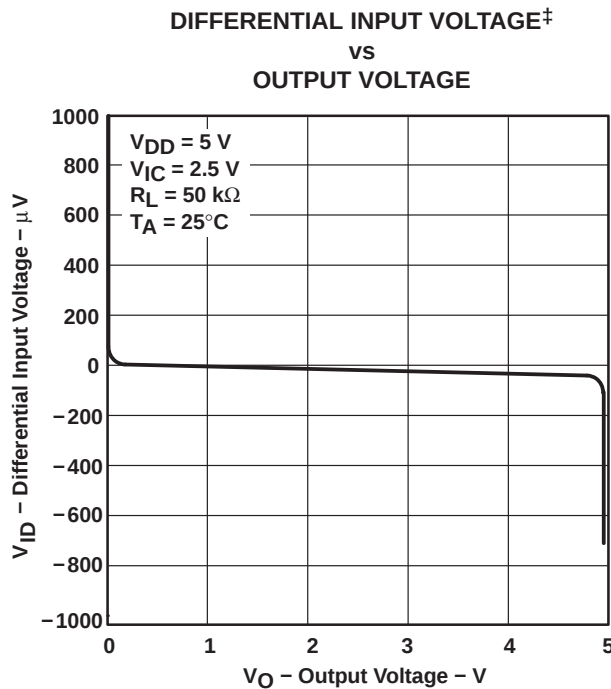
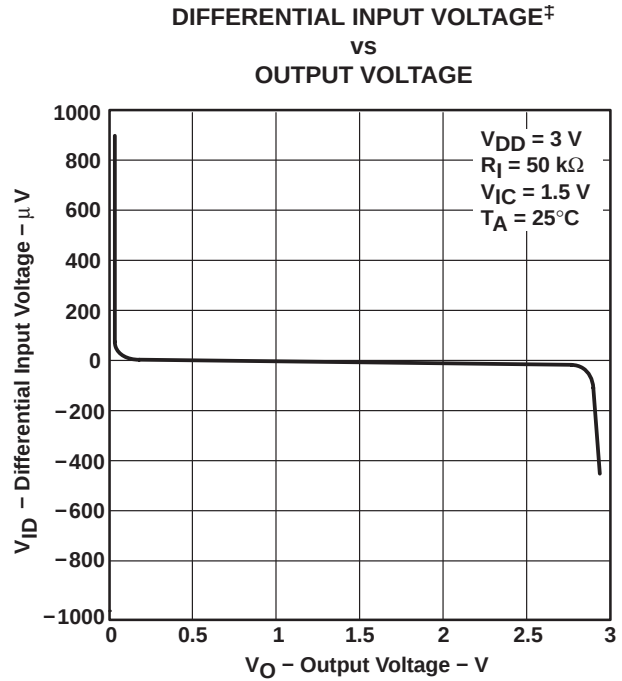
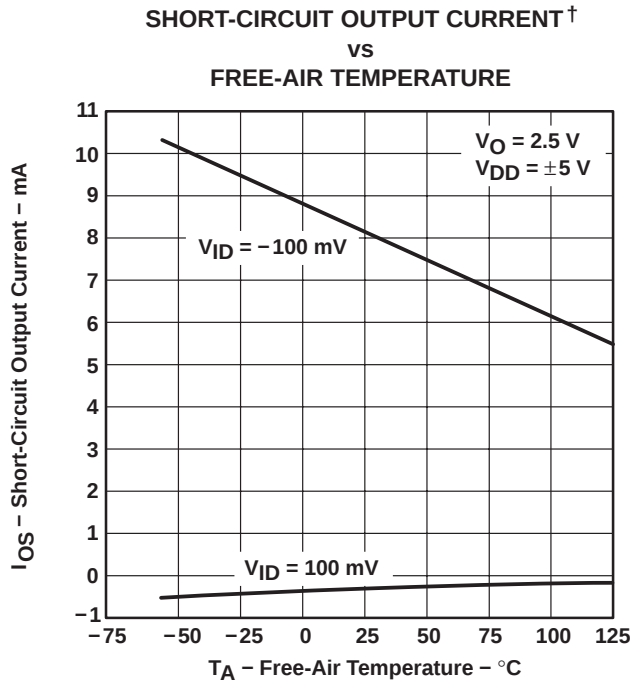


Figure 21

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE†
AMPLIFICATION AND PHASE MARGIN**

**VS
FREQUENCY**

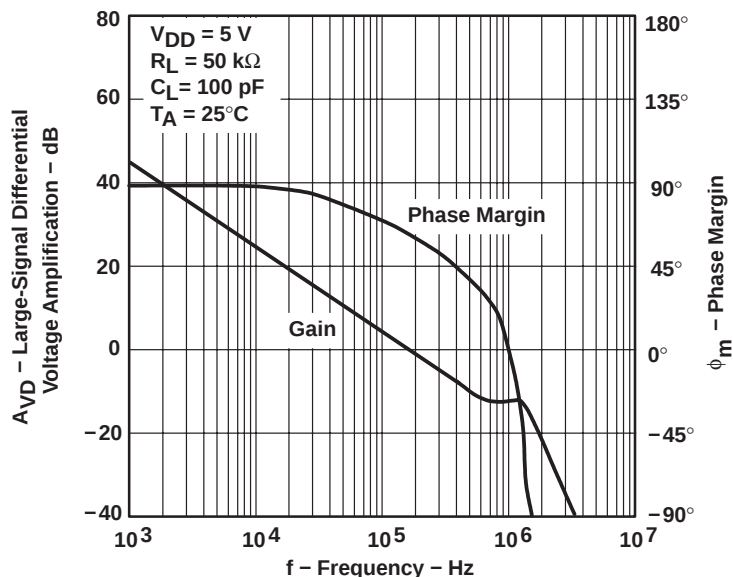


Figure 26

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE†
AMPLIFICATION AND PHASE MARGIN**

**VS
FREQUENCY**

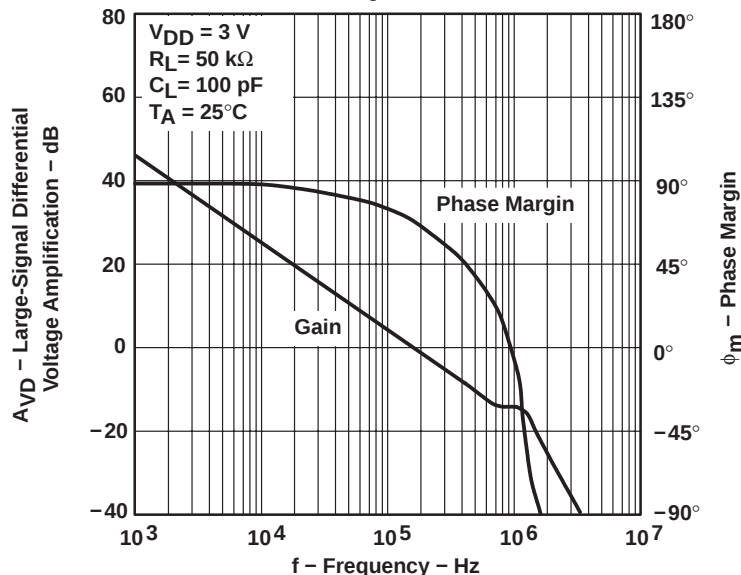


Figure 27

† For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

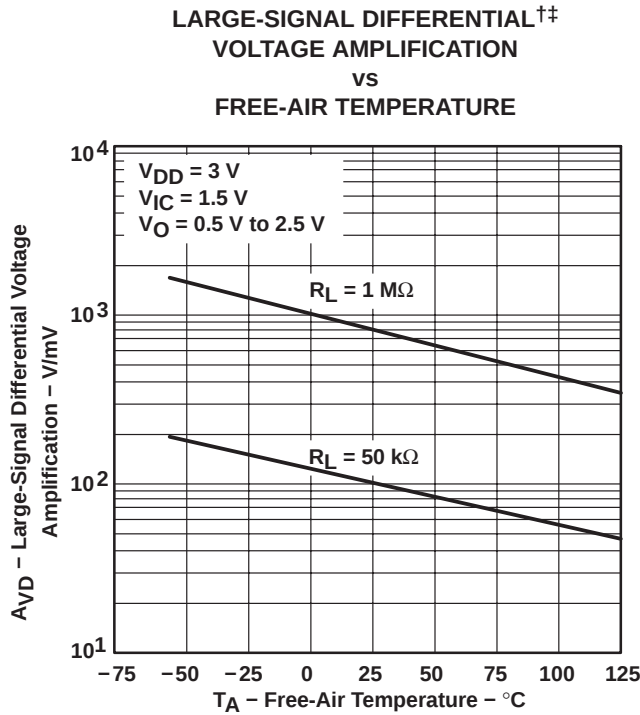


Figure 28

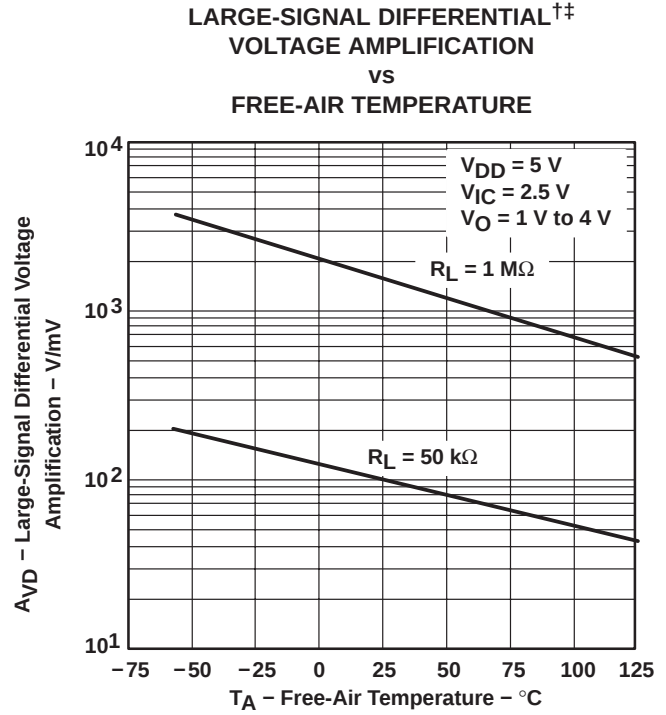


Figure 29

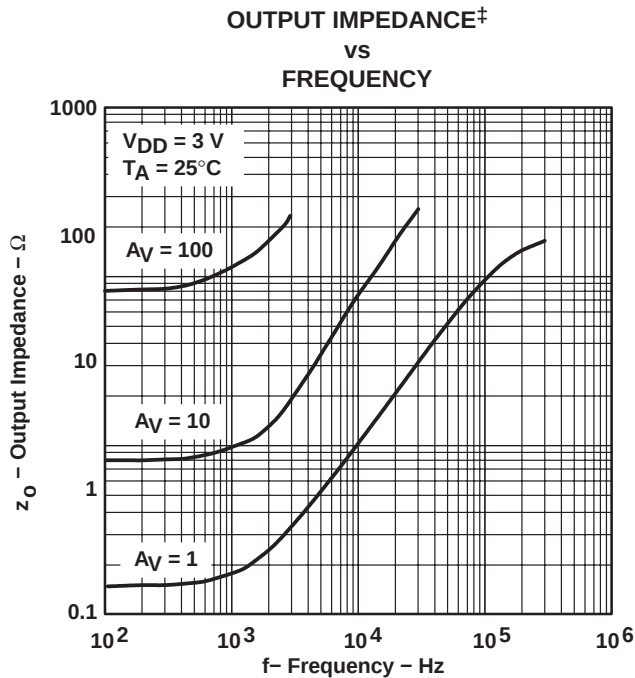


Figure 30

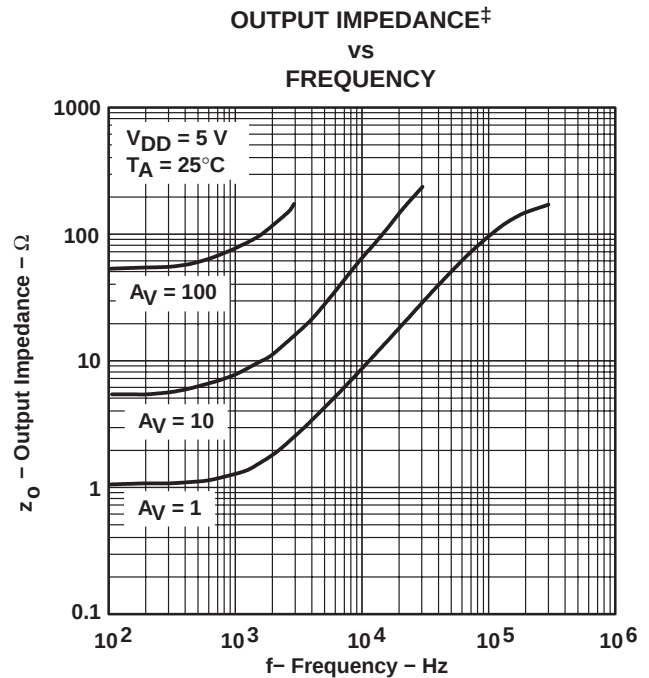


Figure 31

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

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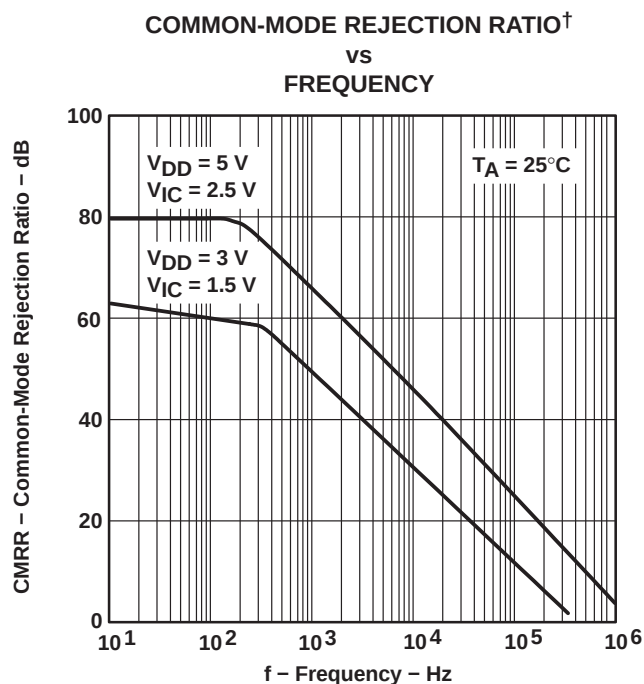


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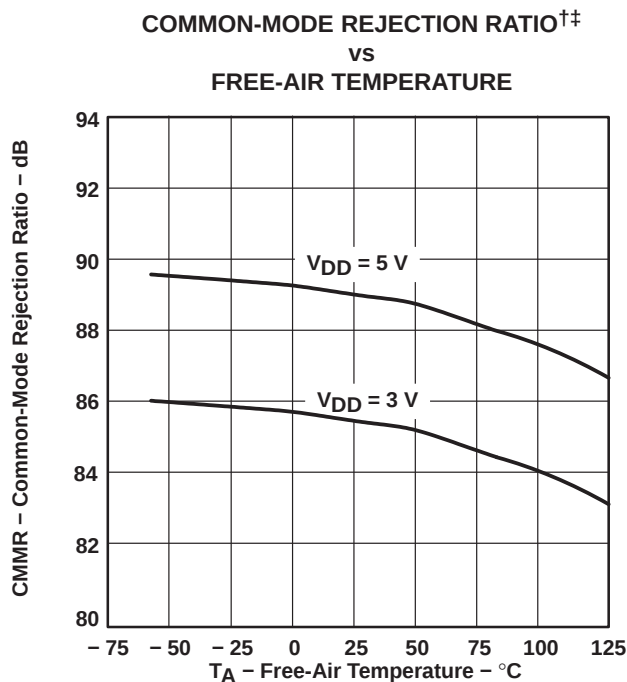


Figure 33

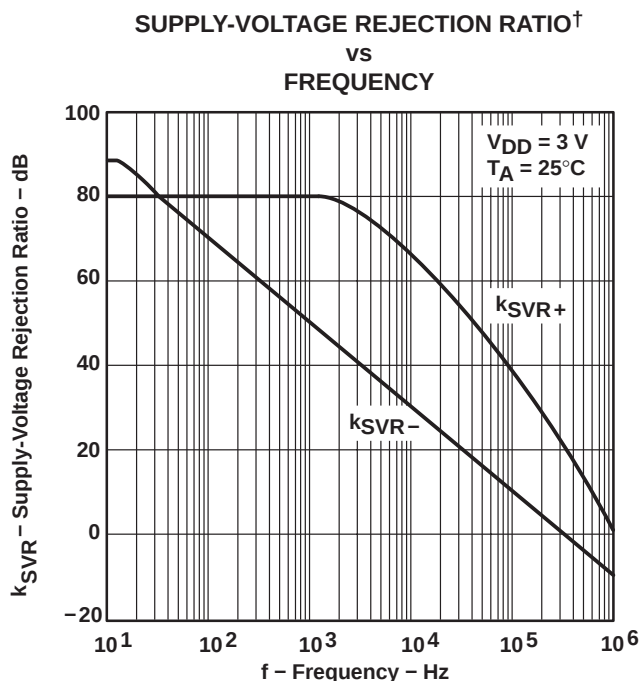


Figure 34

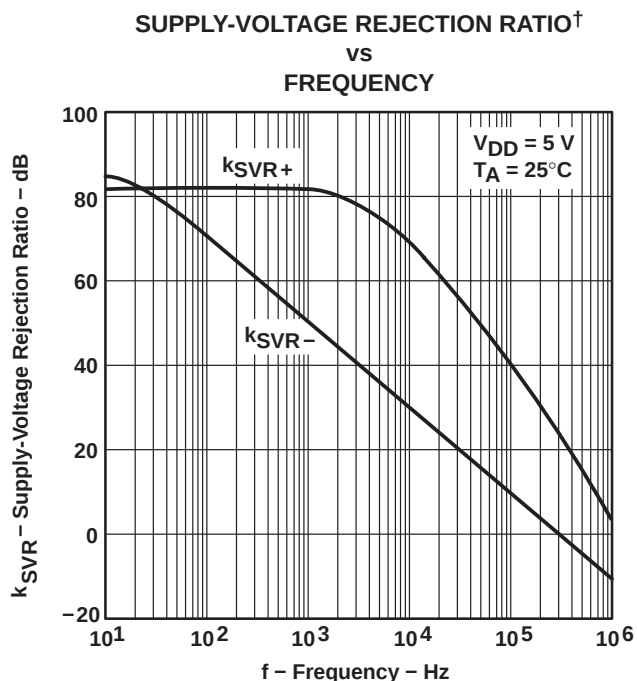


Figure 35

[†] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

[‡] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

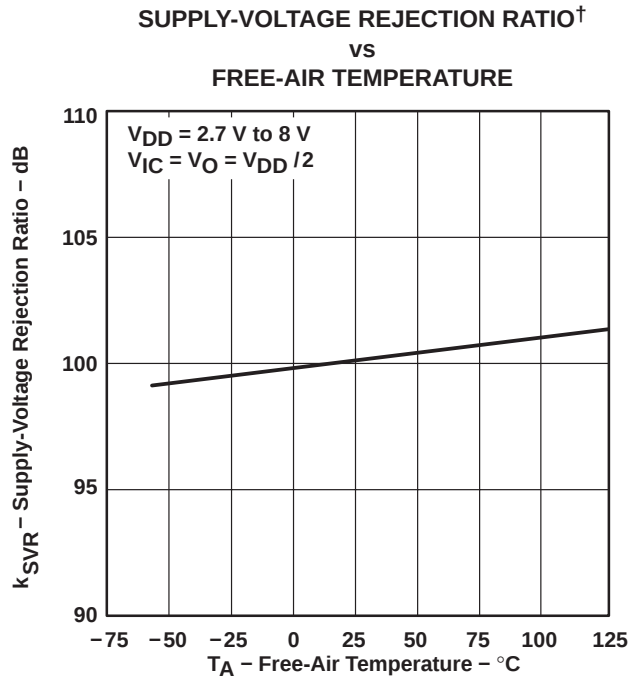


Figure 36

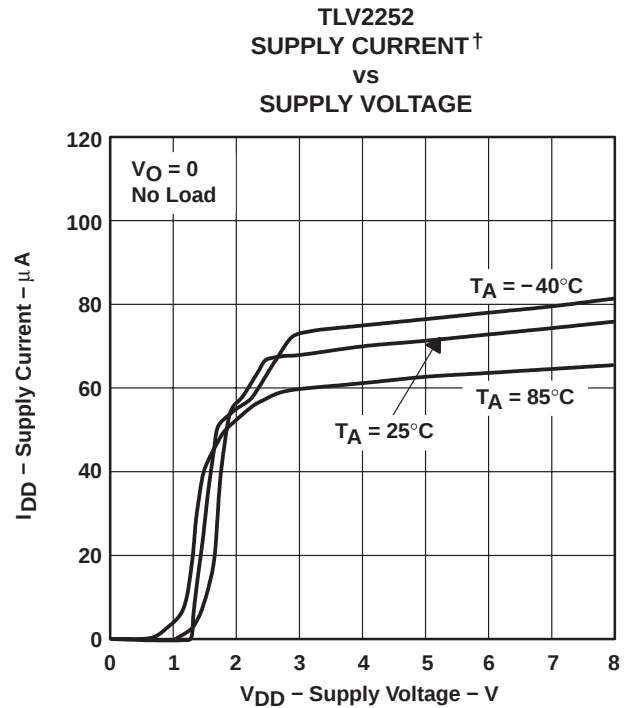


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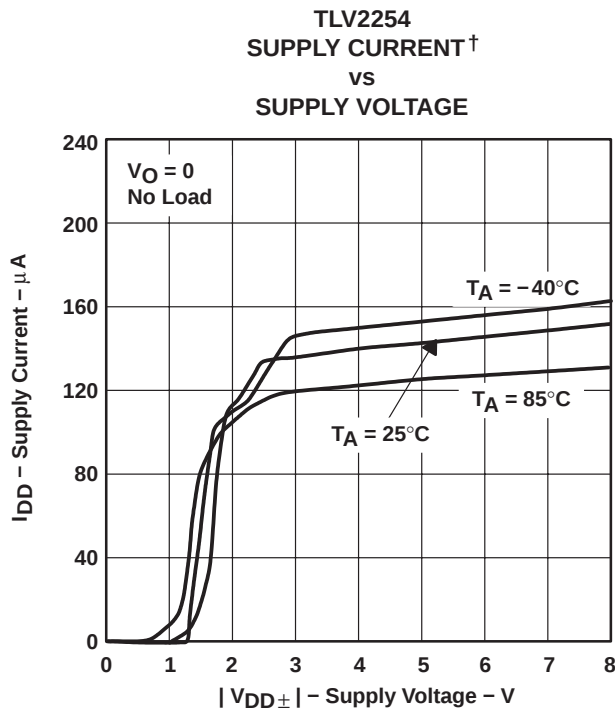


Figure 38

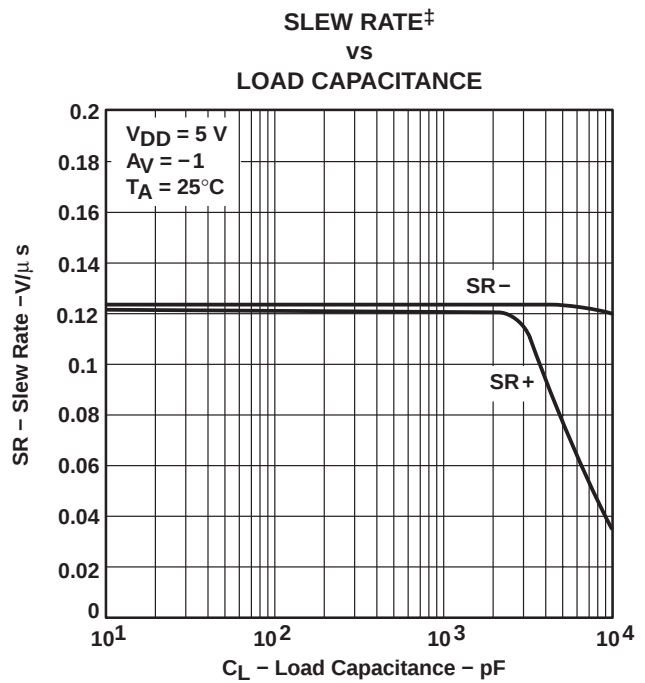


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For all curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 \text{ V}$, all loads are referenced to 1.5 V.

TLV225x-Q1, TLV225xA-Q1

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TYPICAL CHARACTERISTICS

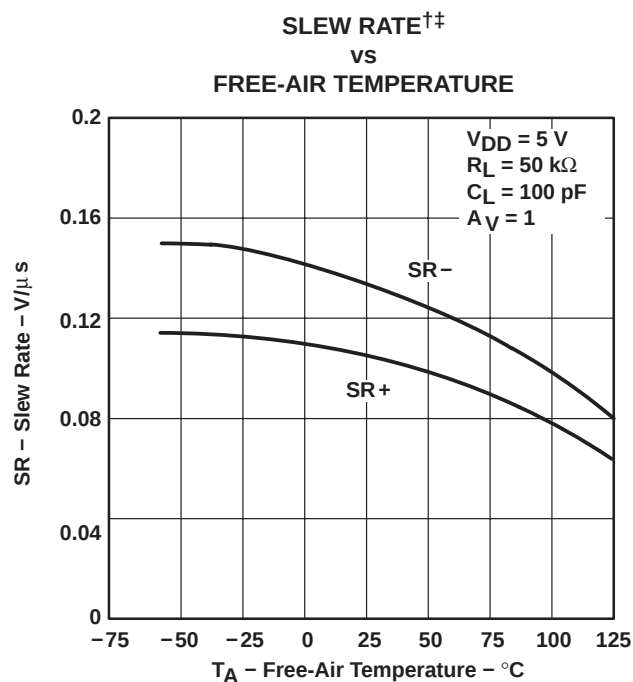


Figure 40

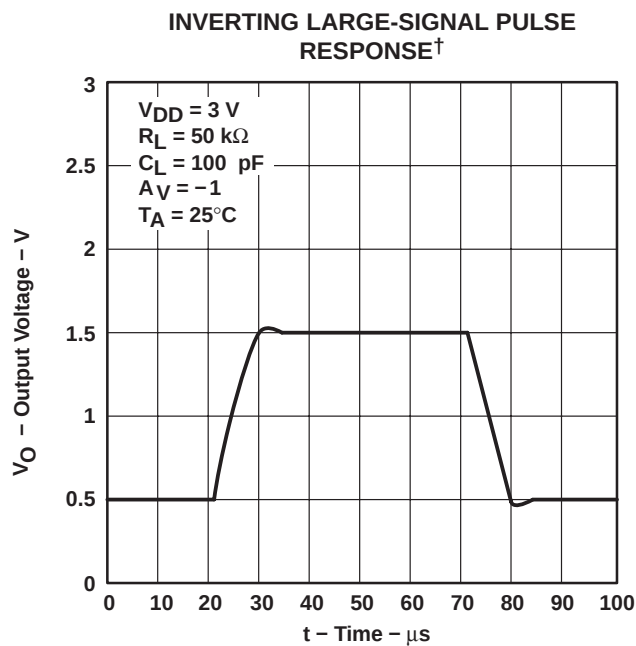


Figure 41

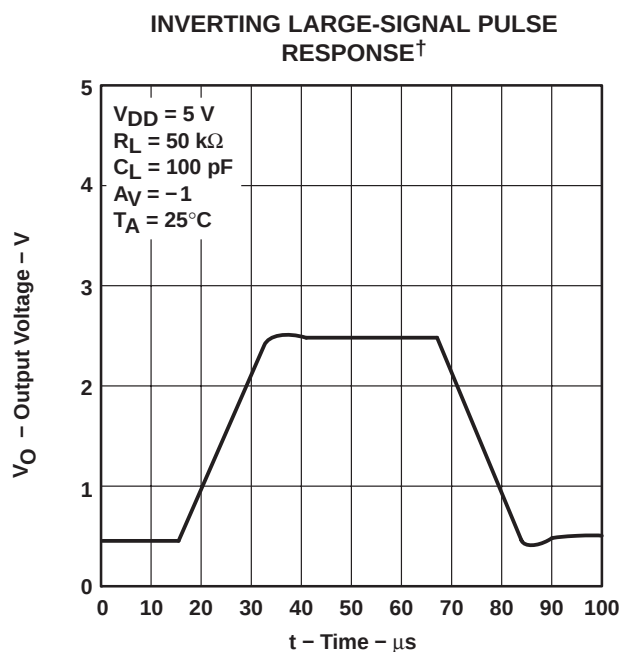


Figure 42

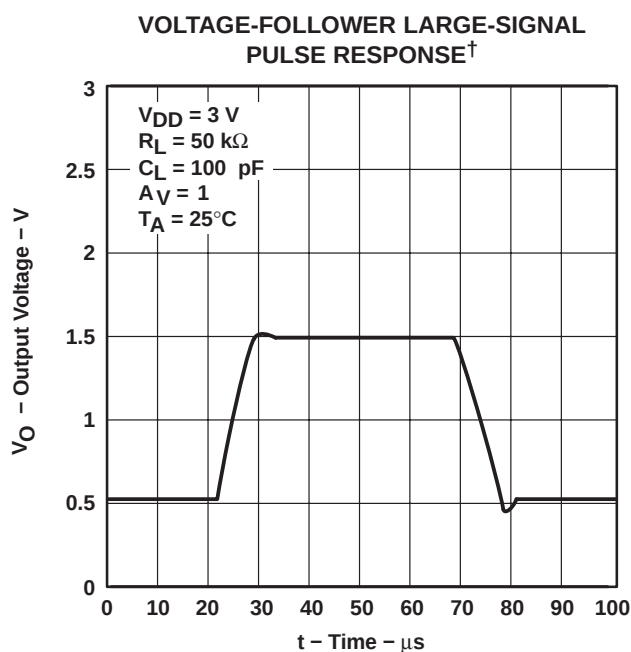


Figure 43

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

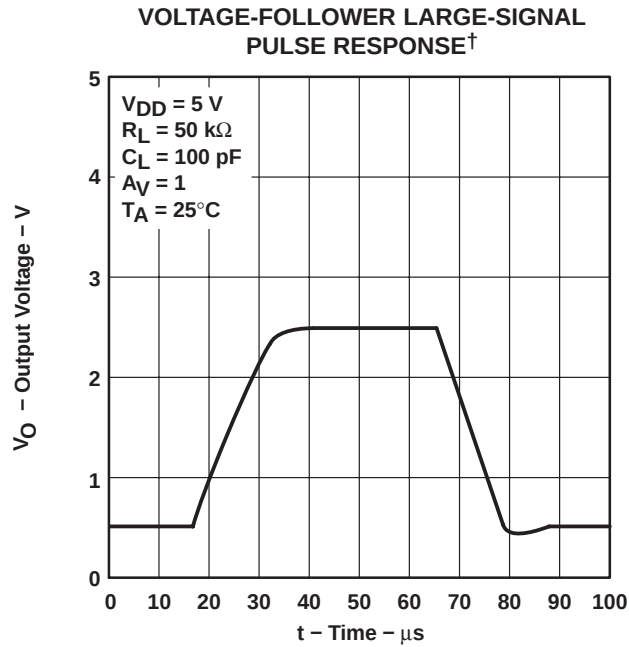


Figure 44

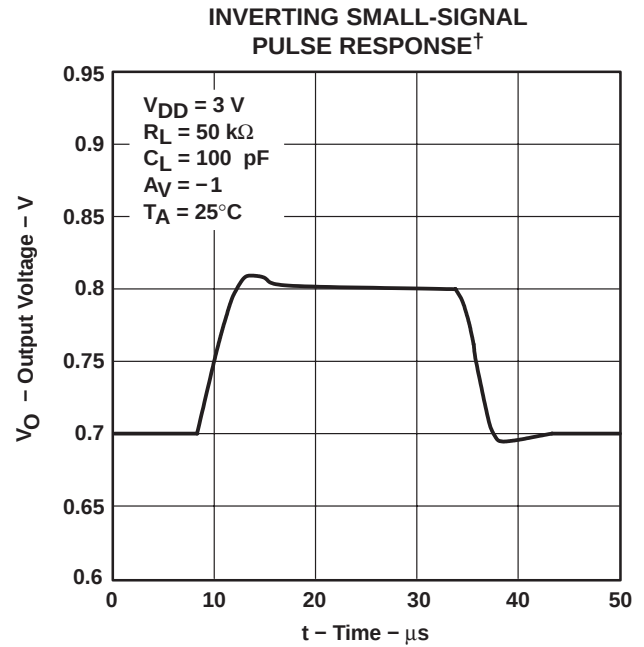


Figure 45

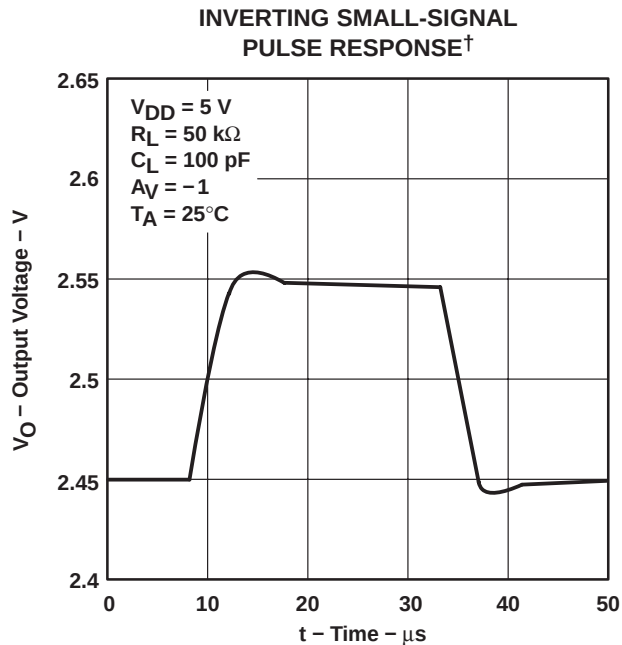


Figure 46

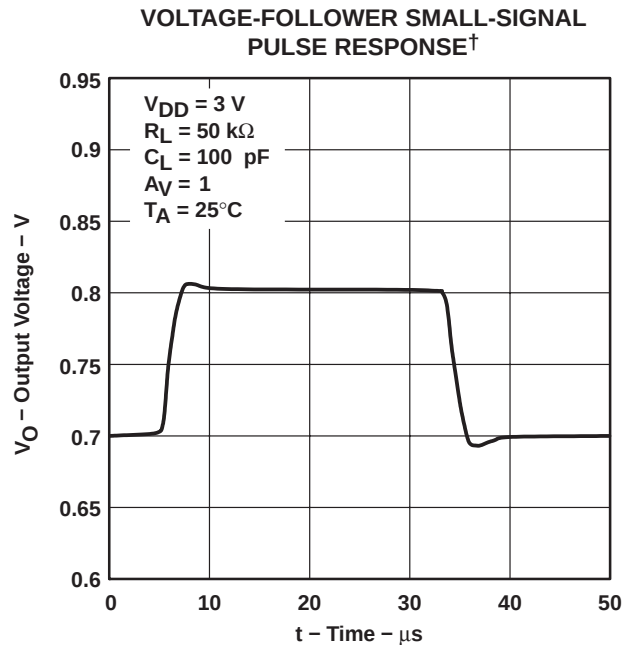


Figure 47

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

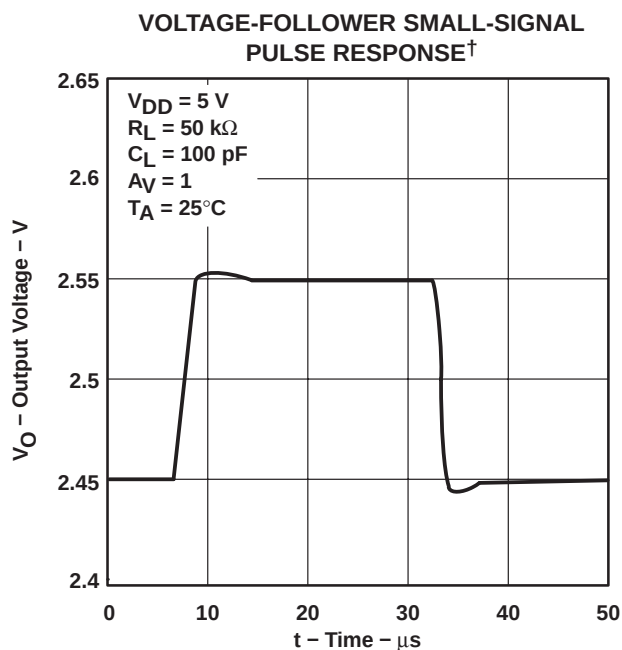


Figure 48

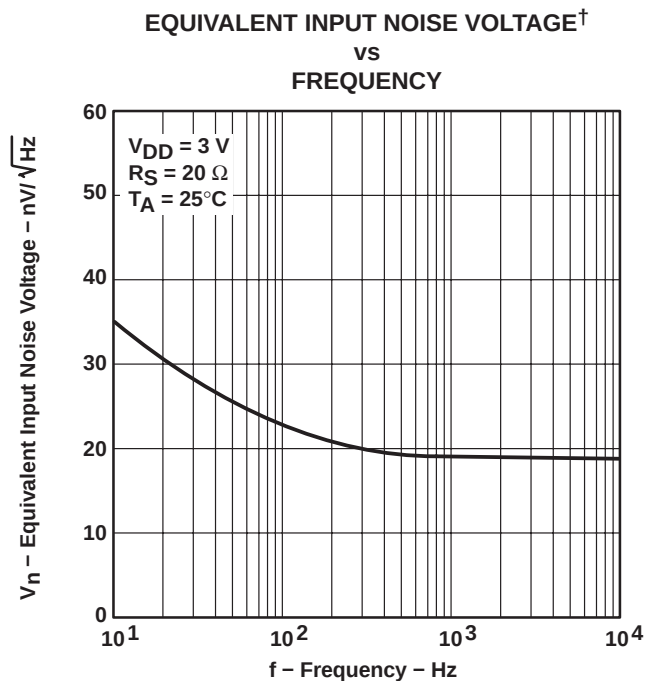


Figure 49

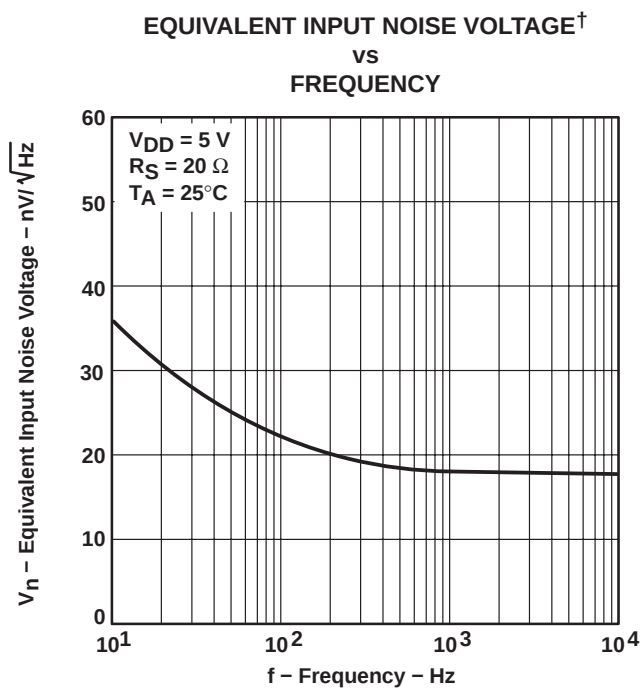


Figure 50

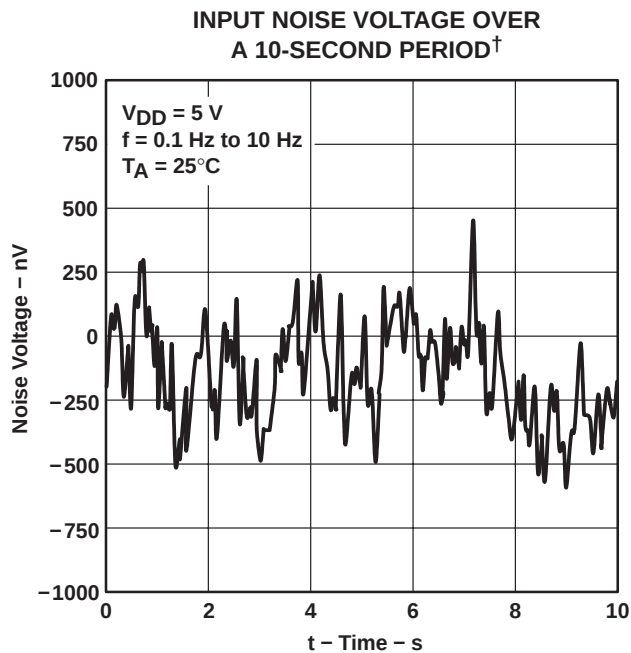


Figure 51

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

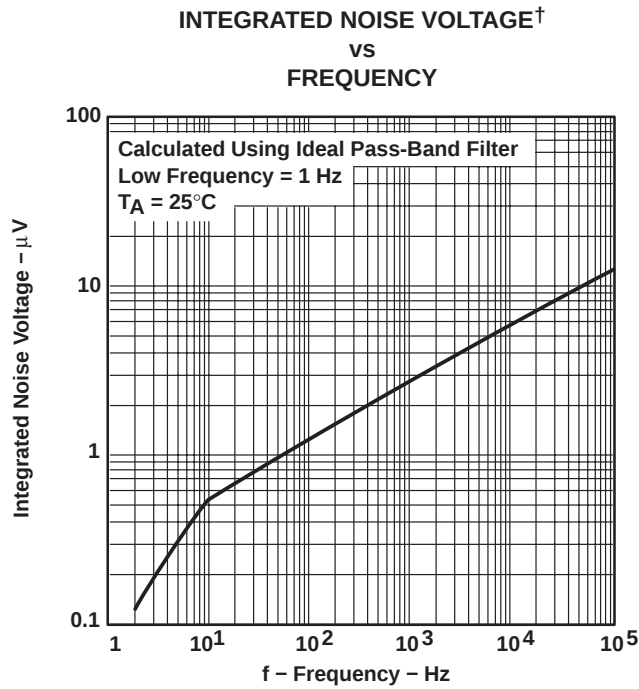


Figure 52

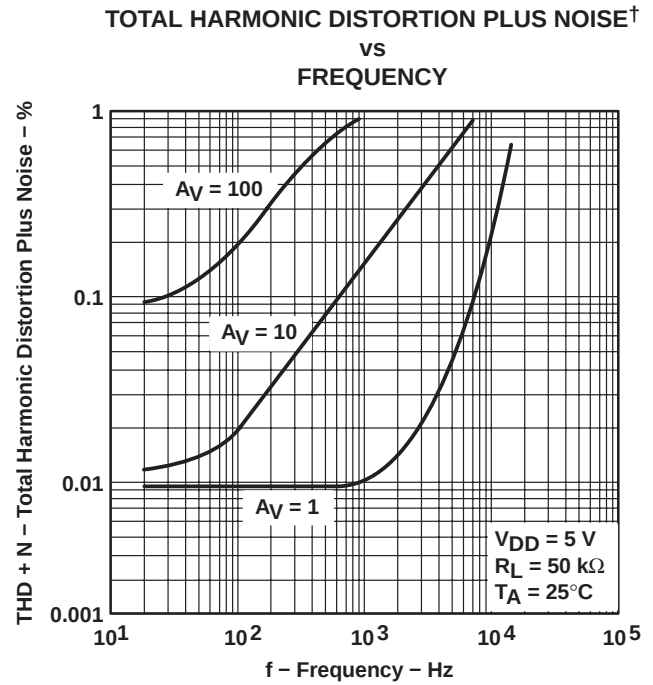


Figure 53

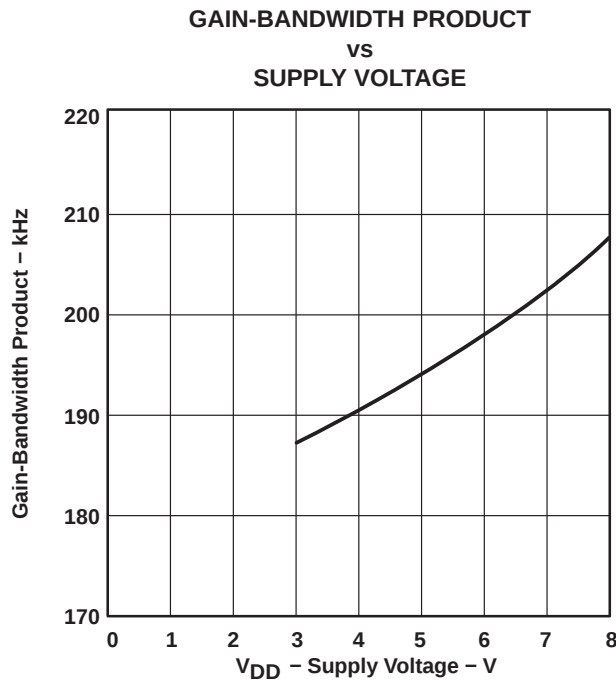


Figure 54

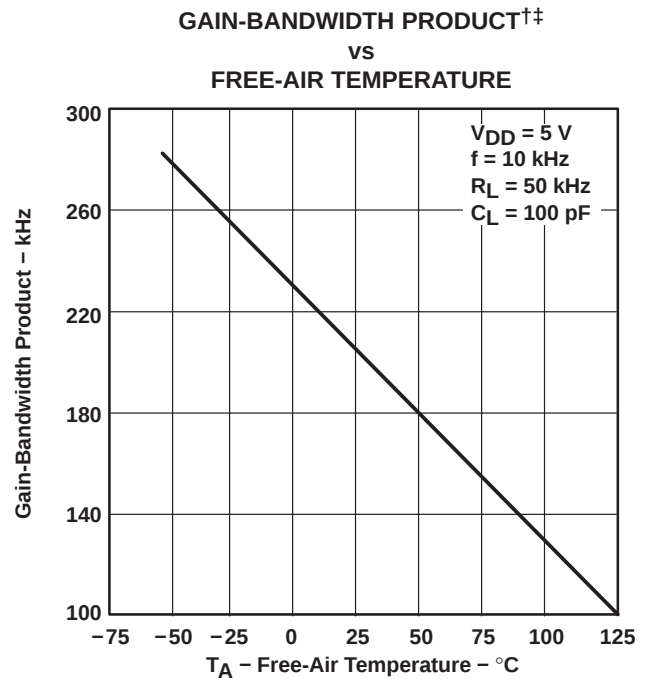


Figure 55

[†] For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

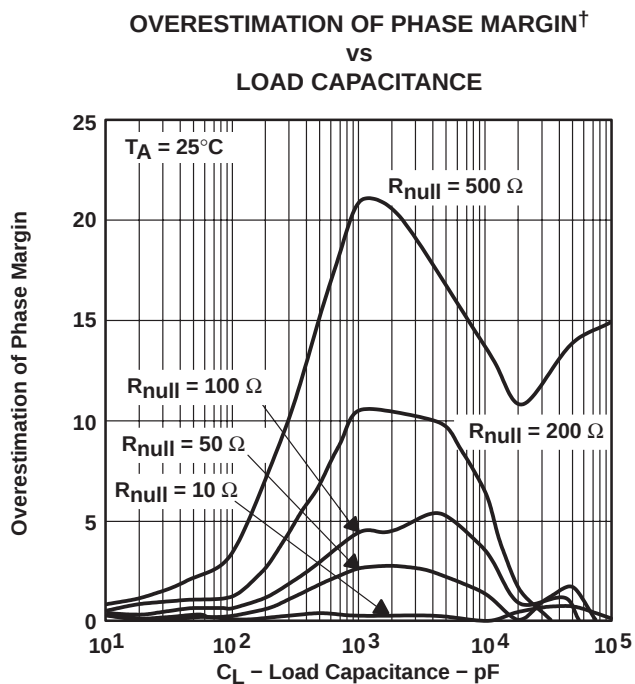
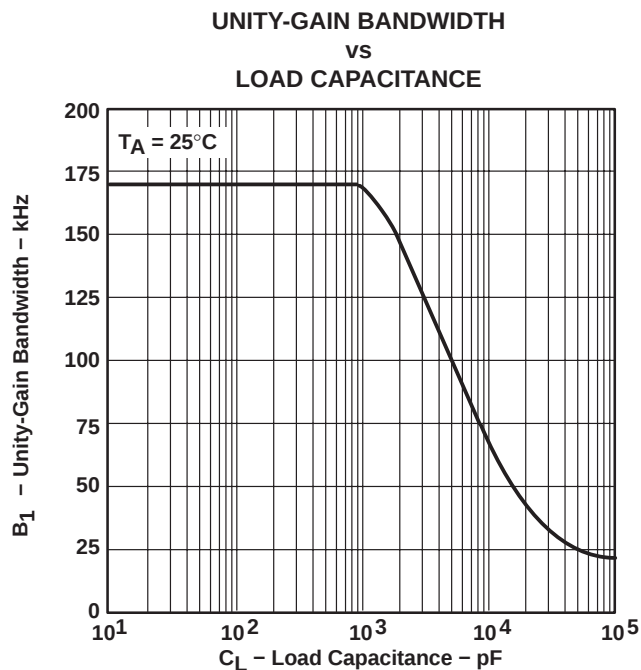
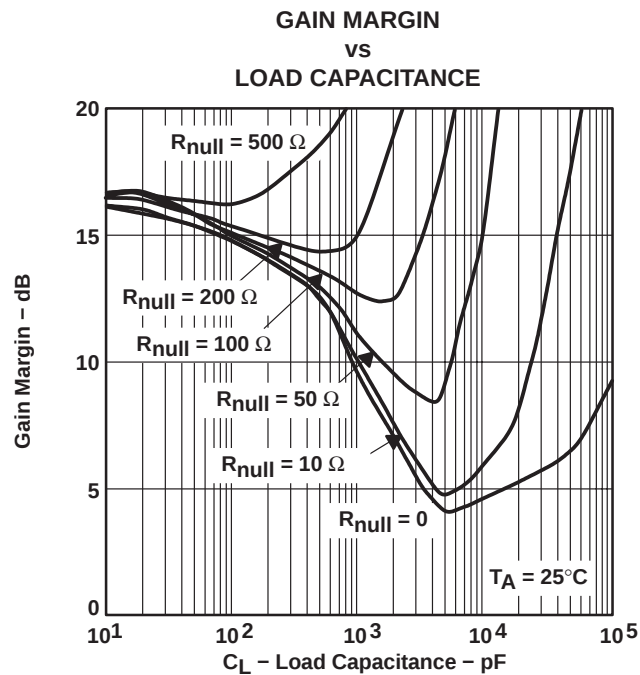
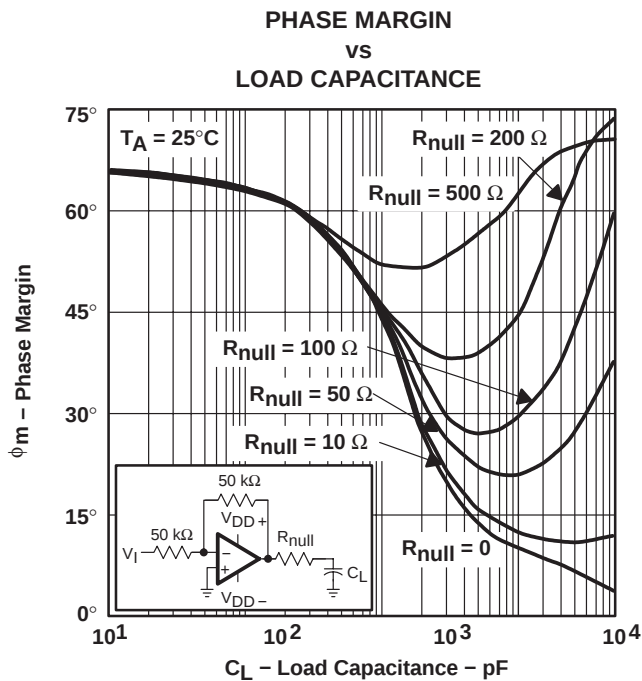
TLV225x-Q1, TLV225xA-Q1

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TYPICAL CHARACTERISTICS



† For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

driving large capacitive loads

The TLV2252 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 56 and Figure 57 illustrate its ability to drive loads up to 1000 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 60) improves the gain and phase margins when driving large capacitive loads. Figure 55 and Figure 56 show the effects of adding series resistances of 10 Ω , 50 Ω , 100 Ω , 200 Ω , and 500 Ω . The addition of this series resistor has two effects: the first adds a zero to the transfer function and the second reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1} \left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L \right) \quad (1)$$

Where :

$\Delta\phi_{m1}$ = improvement in phase margin

UGBW = unity-gain bandwidth frequency

R_{null} = output series resistance

C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 58). To use equation 1, UGBW must be approximated from Figure 58.

Using equation 1 alone overestimates the improvement in phase margin as illustrated in Figure 59. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin.

Using Figure 60, with equation 1 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

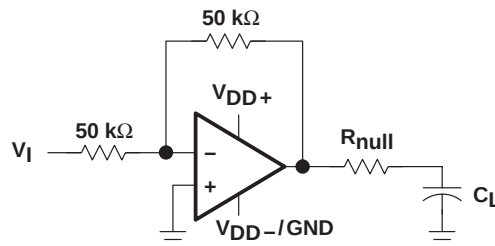


Figure 60. Series-Resistance Circuit

TLV225x-Q1, TLV225xA-Q1

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APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 61 are generated using the TLV2252 typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

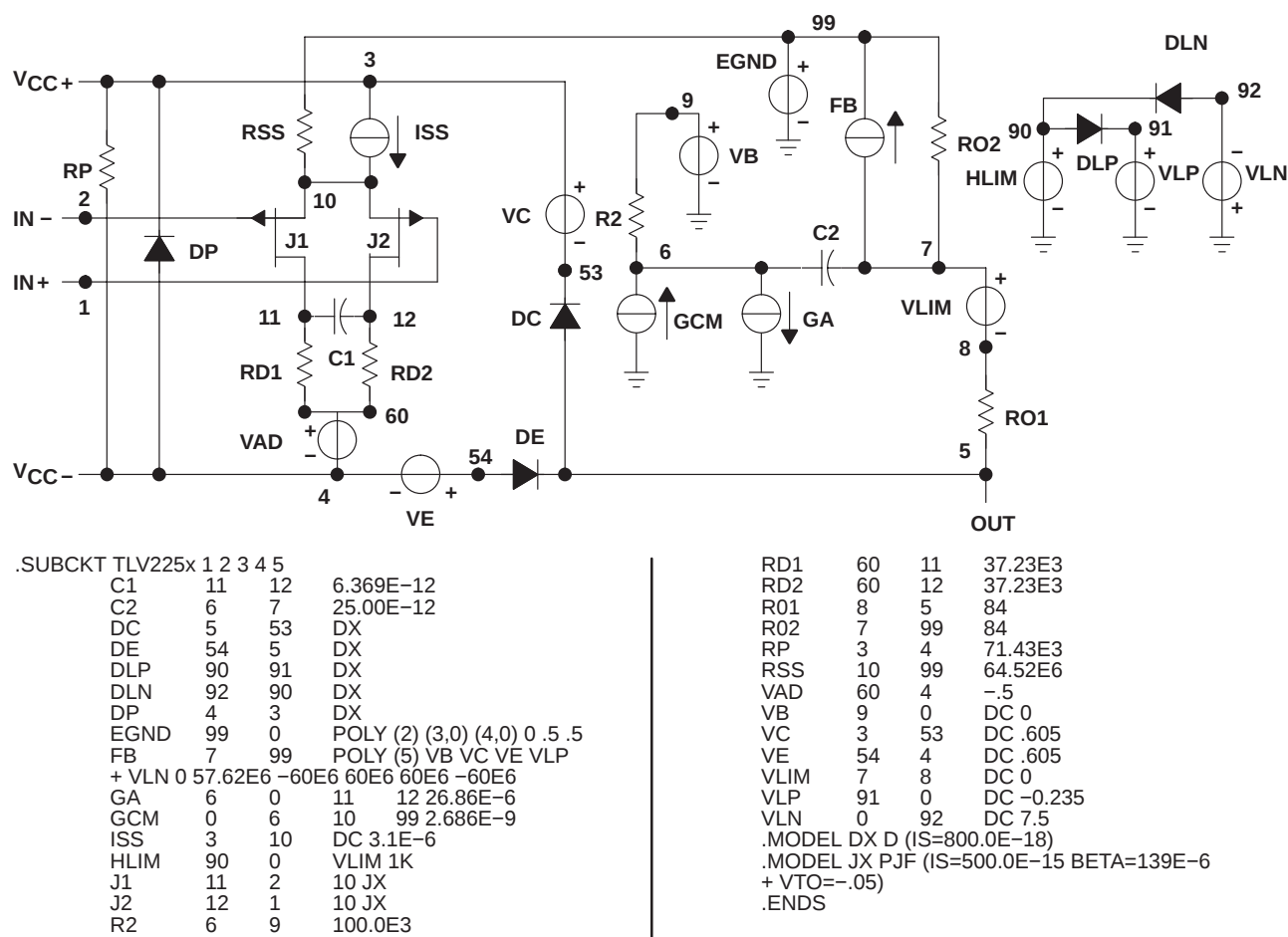


Figure 61. Boyle Macromodel and Subcircuit

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POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2252AQDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2252AQ	Samples
TLV2252AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2252AQ	Samples
TLV2252QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2252Q1	Samples
TLV2252QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2252Q1	Samples
TLV2254AQDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2254AQ1	Samples
TLV2254AQDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2254AQ1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV2252-Q1, TLV2252A-Q1, TLV2254A-Q1 :

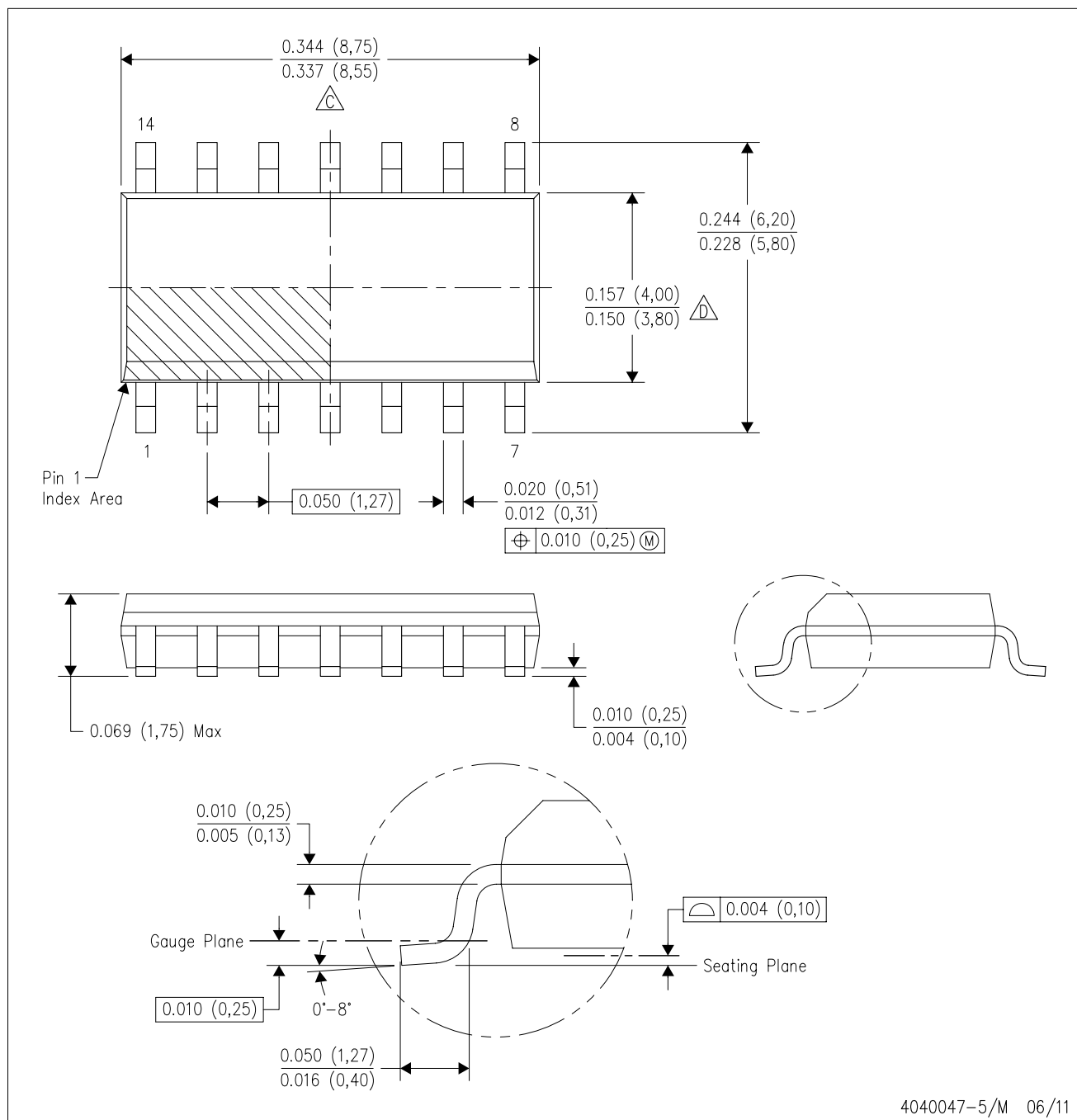
- Catalog: [TLV2252](#), [TLV2252A](#), [TLV2254A](#)
- Enhanced Product: [TLV2252A-EP](#), [TLV2254A-EP](#)
- Military: [TLV2252M](#), [TLV2252AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

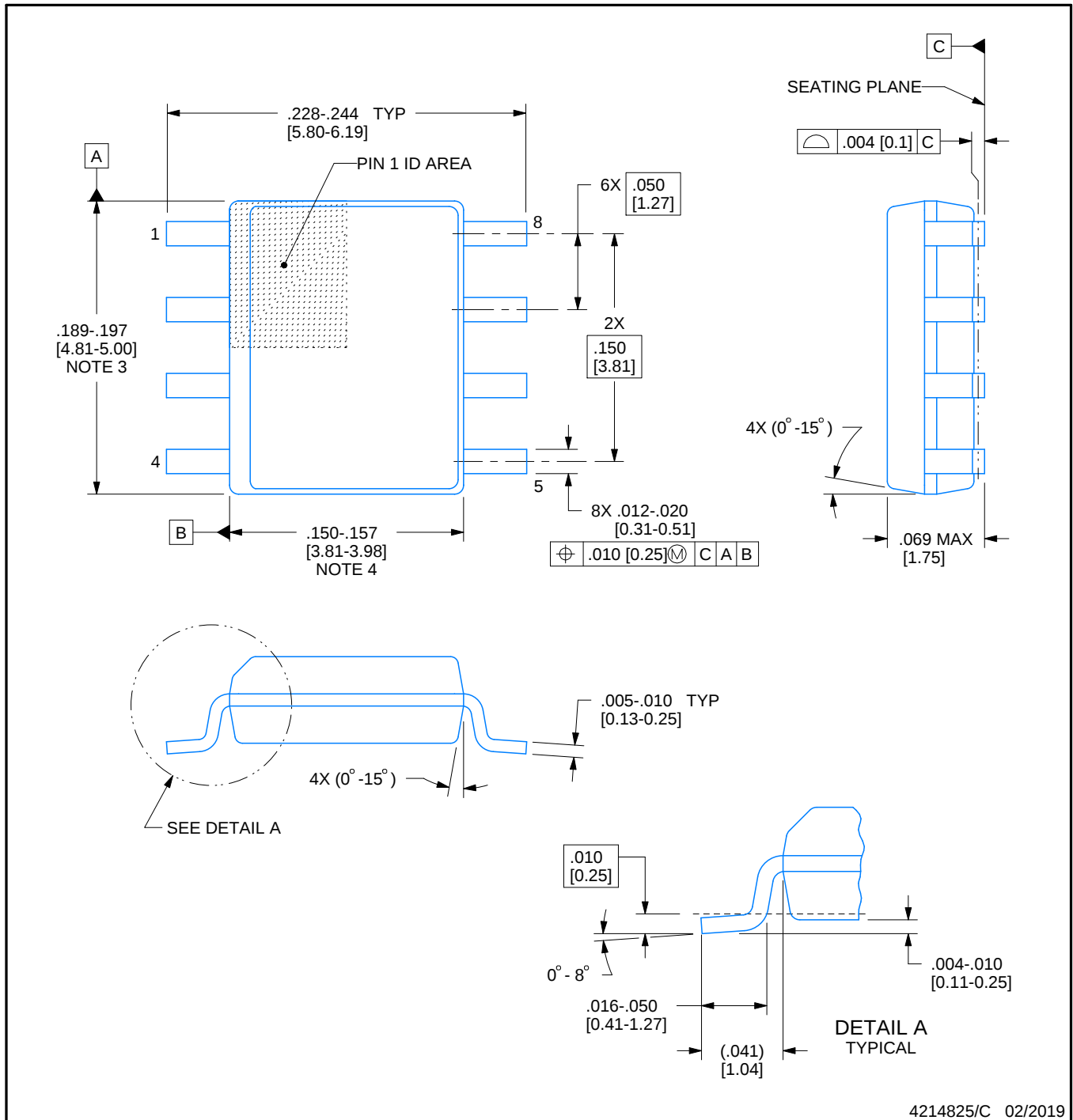


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

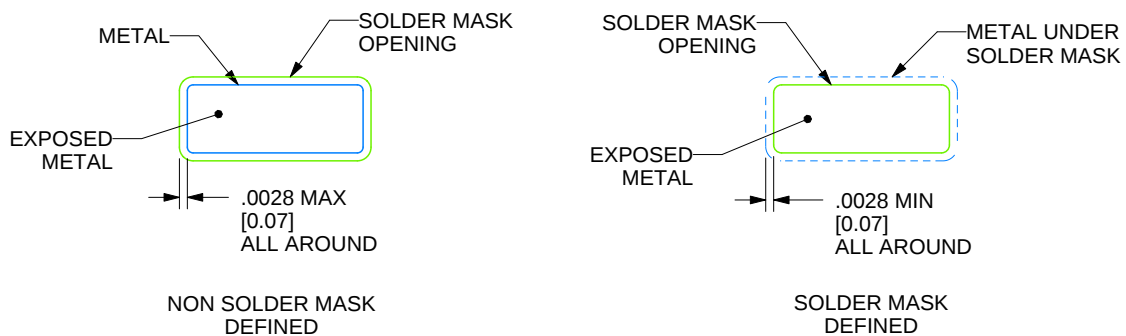
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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