N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD16409Q3

FEATURES

- **Ultra Low Q_g and Q_{gd}**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 3.3mm x 3.3mm Plastic Package**

APPLICATIONS

- **Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems**
- **Optimized for Control FET Applications**

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	25		V
Q_g	Gate Charge Total (4.5V)	4		nC
Q_{gd}	Gate Charge Gate to Drain	1		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V	9.5	mΩ
		V_{GS} = 10V	6.2	mΩ
V_{th}	Threshold Voltage	2		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16409Q3	SON 3.3 × 3.3 Plastic Package	13-inch reel	2500	Tape and Reel

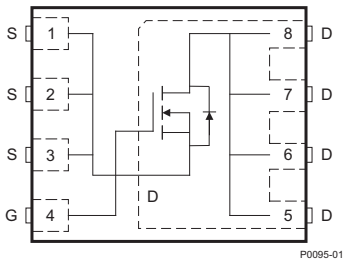
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+16 / –12	V
I_D	Continuous Drain Current, T_C = 25°C	60	A
	Continuous Drain Current(1)	15	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	90	A
P_D	Power Dissipation(1)	2.6	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 38A, L = 0.1mH, R_G = 25Ω	72	mJ

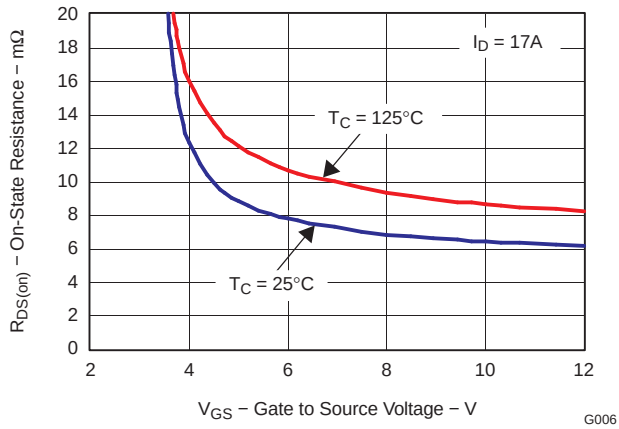
(1) $R_{\theta JA}$ = 47°C/W on 1in^2 Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width ≤300μs, duty cycle ≤2%

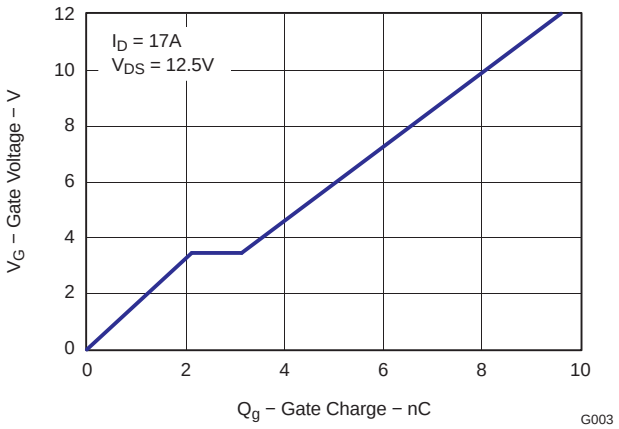
Top View



$R_{DS(ON)}$ vs V_{GS}



Gate Charge



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250µA	25			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 20V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = +16/-12V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1.7	2	2.3	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V, I_D = 17A		9.5	12.4	mΩ
		V_{GS} = 10V, I_D = 17A		6.2	8.2	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_D = 17A		38		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 12.5V , f = 1MHz		600	800	pF
C_{OSS}	Output Capacitance			480	635	pF
C_{RSS}	Reverse Transfer Capacitance			40	55	pF
R_g	Series Gate Resistance			0.9	1.8	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 12.5V, I_D = 17A		4	5.6	nC
Q_{gd}	Gate Charge Gate to Drain			1		nC
Q_{gs}	Gate Charge Gate to Source			2.1		nC
Qg(th)	Gate Charge at Vth			1.1		nC
Q_{OSS}	Output Charge	V_{DS} = 12.9V, V_{GS} = 0V		9.1		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 17A, R_G = 2Ω		6.5		ns
t_r	Rise Time			10.6		ns
$t_{d(off)}$	Turn Off Delay Time			6.3		ns
t_f	Fall Time			3.4		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = 17A, V_{GS} = 0V		0.85	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 12.9V, I_F = 17A, di/dt = 300A/µs		13.8		nC
t_{rr}	Reverse Recovery Time	V_{DD} = 12.9V, I_F = 17A, di/dt = 300A/µs		17.5		ns

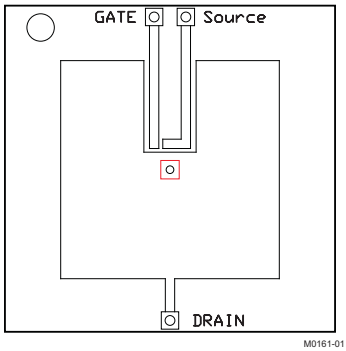
THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

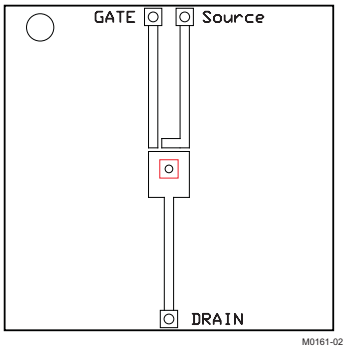
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			3.5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1) (2)			59	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch square 2 oz. Cu pad on a 1.5 × 1.5 in 0.06 inch thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 Material with 1 $inch^2$ of 2 oz. Cu.

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Max $R_{\theta JA}$ = 59°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Max $R_{\theta JA}$ = 157°C/W when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

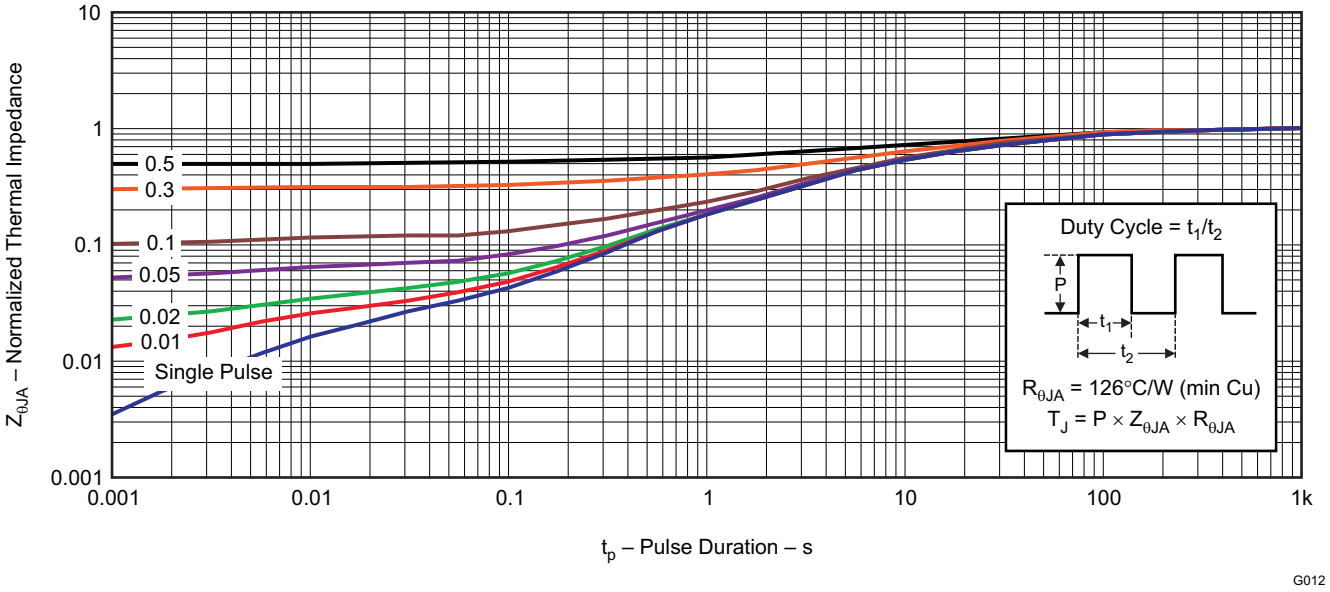


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

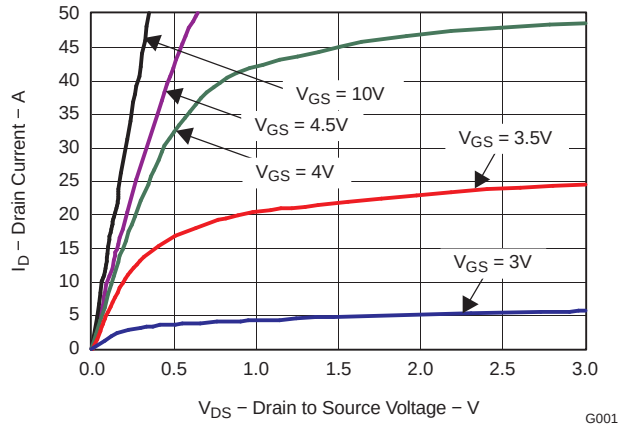


Figure 2. Saturation Characteristics

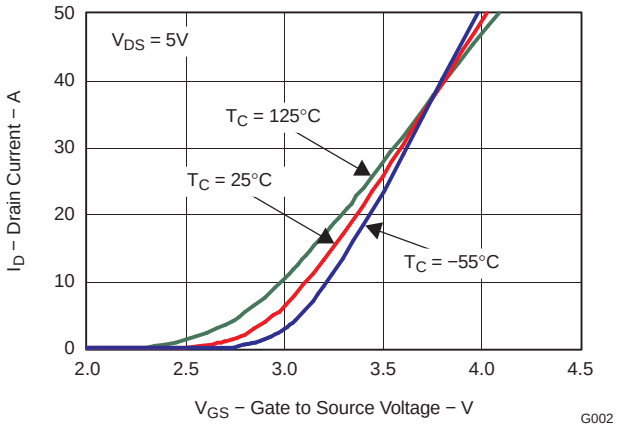


Figure 3. Transfer Characteristics

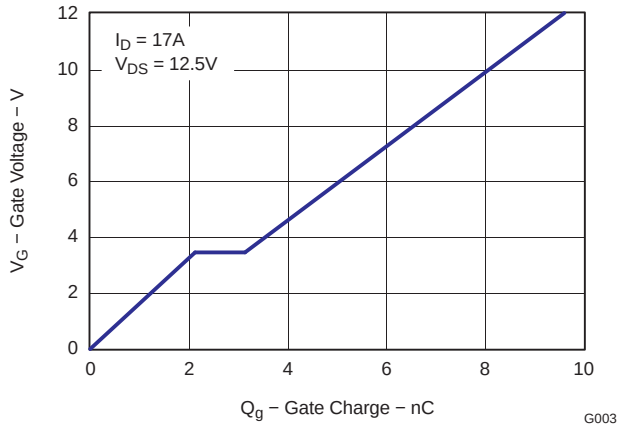


Figure 4. Gate Charge

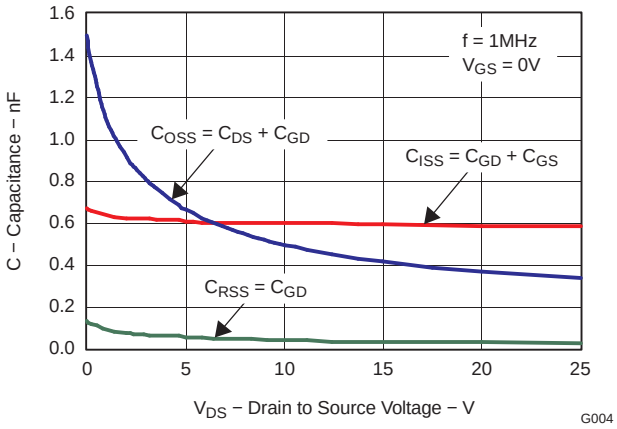


Figure 5. Capacitance

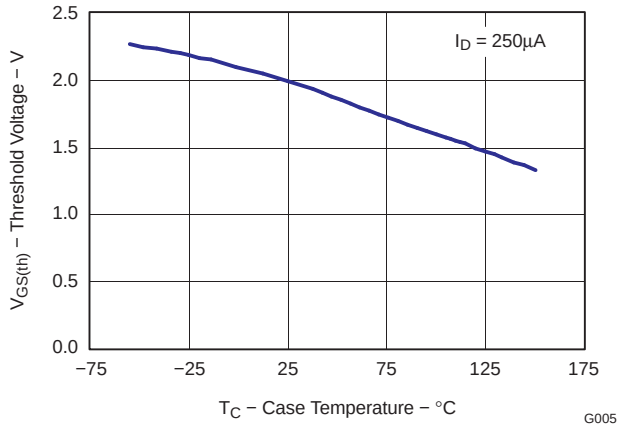


Figure 6. Threshold Voltage vs. Temperature

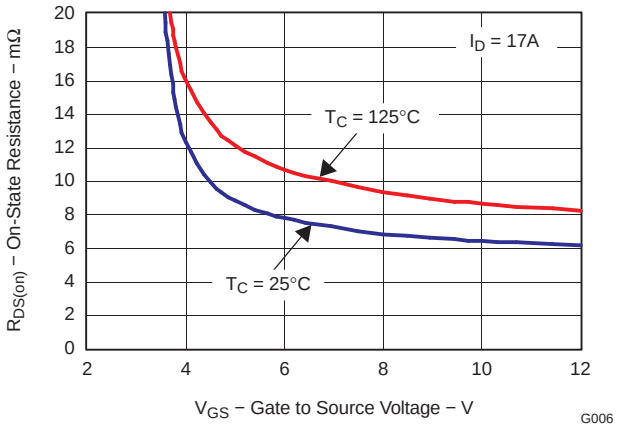


Figure 7. On Resistance vs. Gate Voltage

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TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

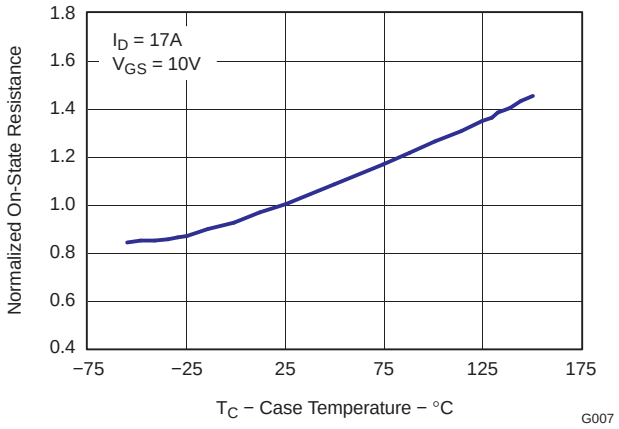


Figure 8. Normalized On Resistance vs. Temperature

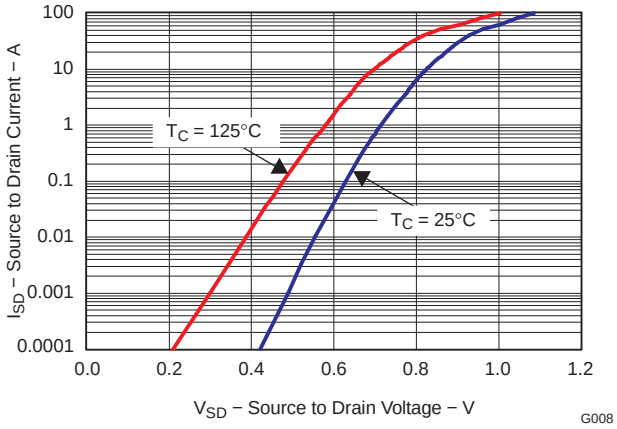


Figure 9. Typical Diode Forward Voltage

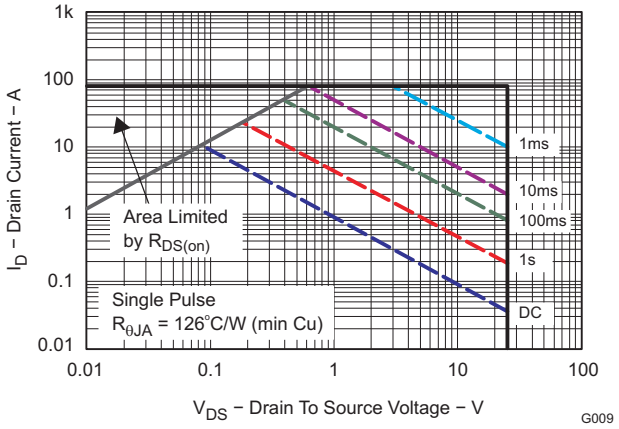


Figure 10. Maximum Safe Operating Area

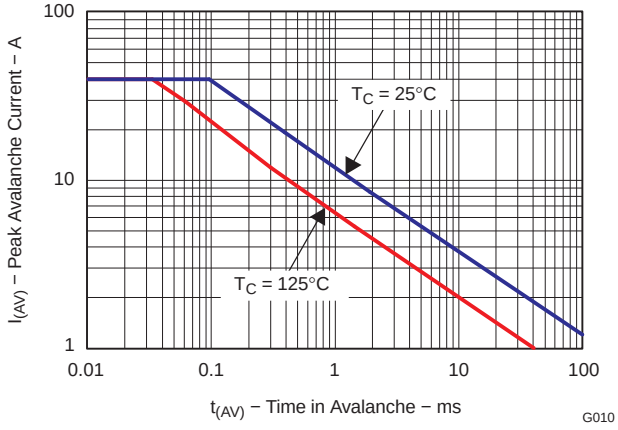


Figure 11. Single Pulse Unclamped Inductive Switching

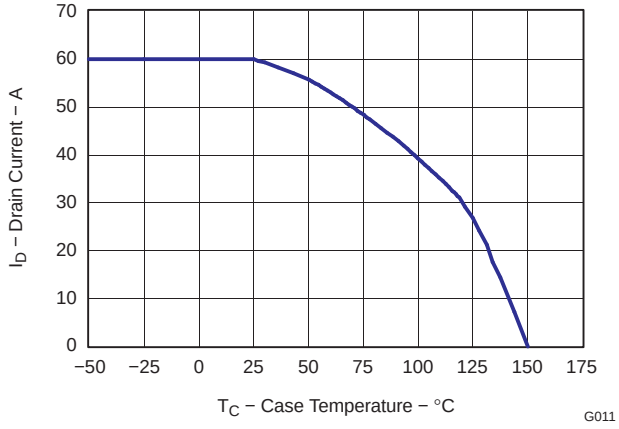
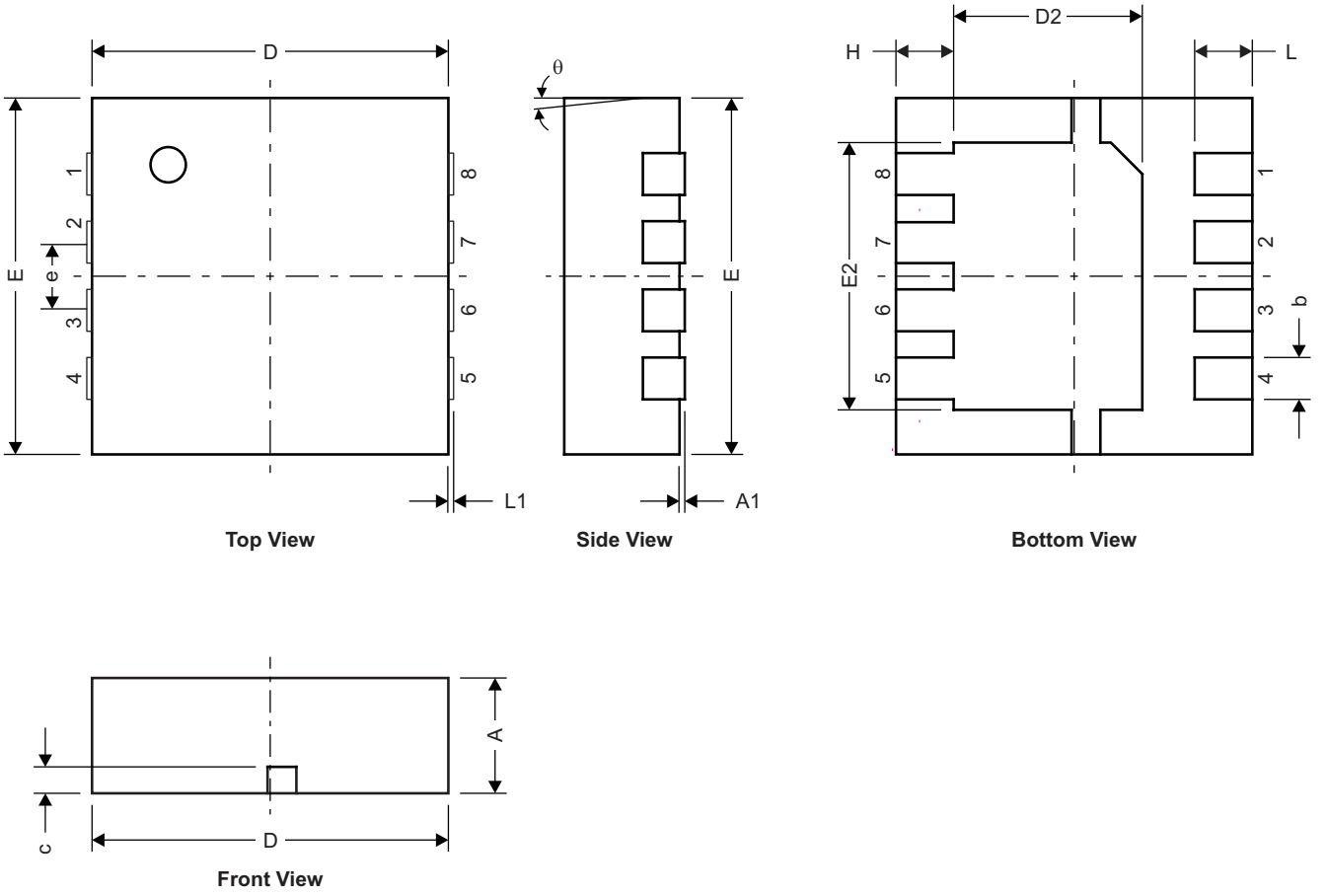


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

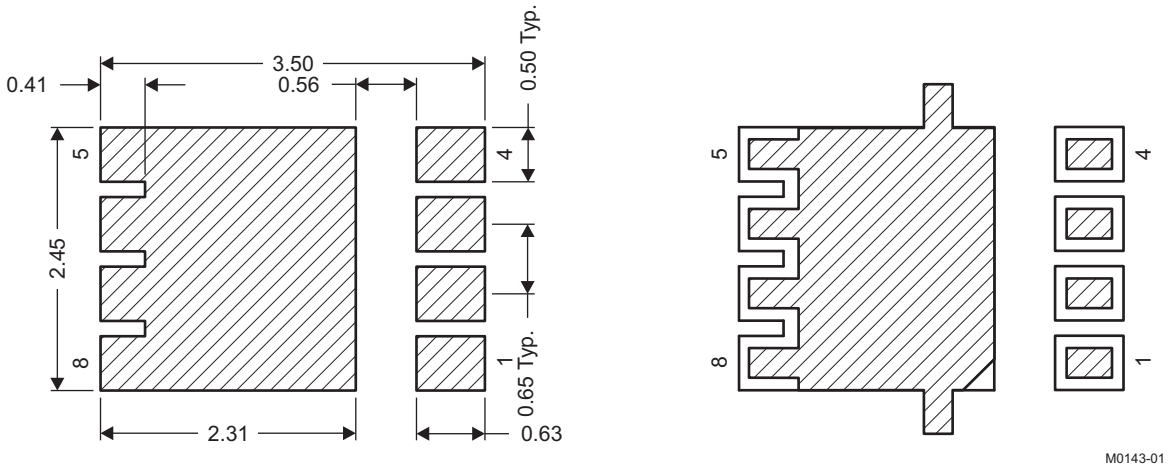
Q3 Package Dimensions



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D1	–	–	–	–	–	–
D2	1.650	1.750	1.800	0.065	0.069	0.071
E	3.200	3.300	3.400	0.126	0.130	0.134
E1	–	–	–	–	–	–
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	–	–	–	–	–	–
θ	–	–	–	–	–	–

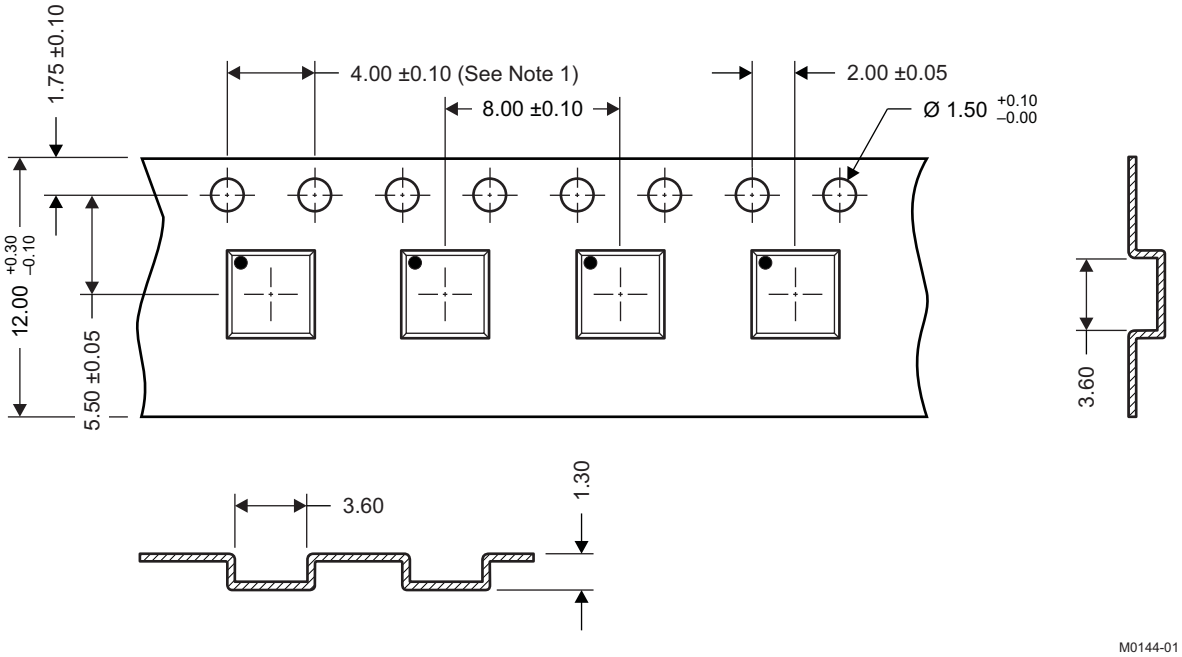
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Recommended PCB Land Pattern



For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q3 Tape and Reel Information



Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
3. Material:black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness: 0.30 ±0.05mm
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

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REVISION HISTORY

Changes from Original (August 2009) to Revision A	Page
• Deleted the Package Marking Information section	7

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16409Q3	ACTIVE	VSON-CLIP	DQG	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-55 to 150	CSD16409	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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