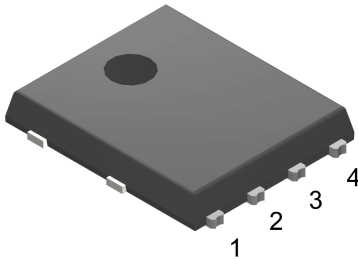
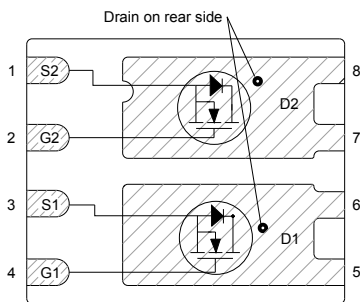


Automotive-grade N-channel 60 V, 24 mΩ typ., 10 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 double island package



**PowerFLAT™ 5x6
double island**



NG14G22D1D2RSS13S21

Product status

STL38DN6F7AG

Device summary

Order code	STL38DN6F7AG
Marking	38DN6F7
Package	PowerFLAT™ 5x6 double island
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STL38DN6F7AG	60 V	27 mΩ	10 A

- AEC-Q101 qualified
- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	10	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	10	A
$I_{DM}^{(2)(1)}$	Drain current (pulsed)	40	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	57.7	W
I_{AV}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	10	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 40\text{ V}$)	50	mJ
T_{stg}	Storage temperature range	-55 to 175	$^\circ\text{C}$
T_J	Operation junction temperature range		

1. Drain current is limited by package, the current capability of the silicon is 33 A at 25 $^\circ\text{C}$ and 23 A at 100 $^\circ\text{C}$.

2. Pulse width limited by safe operating area

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.6	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	32	

1. When mounted on FR-4 board of 1 inch², 2oz Cu, $t < 10\text{ s}$

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	60			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 60\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 60\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			100	μA
I_{GSS}	Gate-body leakage current	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 5\text{ A}$		24	27	m Ω

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	380	-	pF
C_{oss}	Output capacitance		-	320	-	pF
C_{rss}	Reverse transfer capacitance		-	7.9	-	pF
Q_g	Total gate charge	$V_{DD} = 30\text{ V}$, $I_D = 10\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	7.9	-	nC
Q_{gs}	Gate-source charge		-	2.9	-	nC
Q_{gd}	Gate-drain charge		-	2.4	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$, $I_D = 5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	12	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	16	-	ns
t_f	Fall time		-	5	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} ⁽¹⁾	Forward on voltage	$I_{SD} = 10\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.3	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	$I_{SD} = 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	21.5		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 48\text{ V}$	-	8.5		nC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	0.8		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

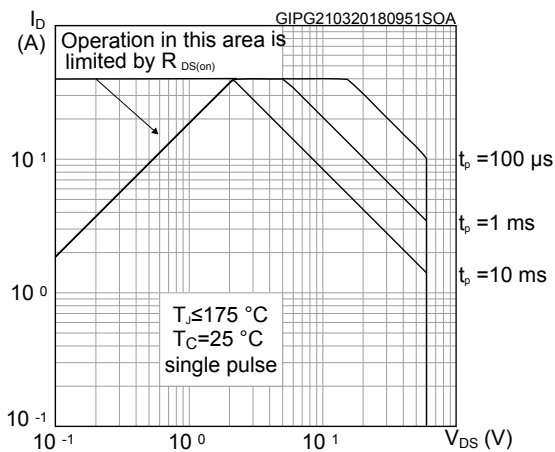
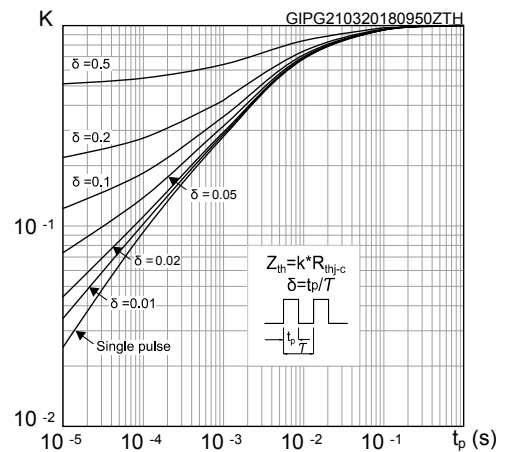
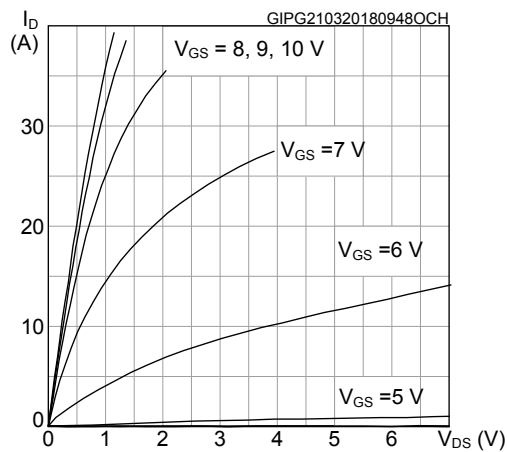
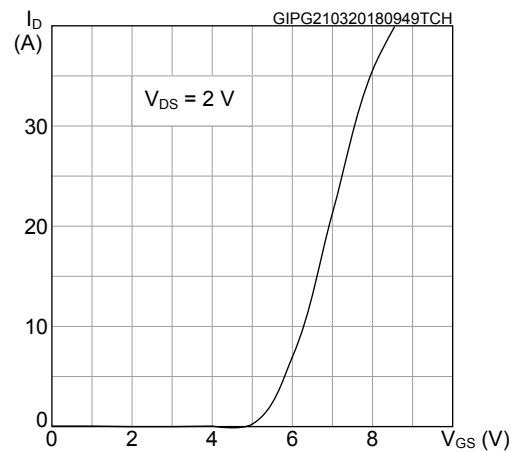
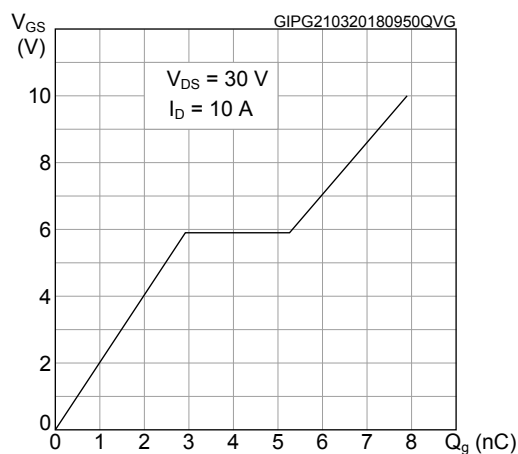
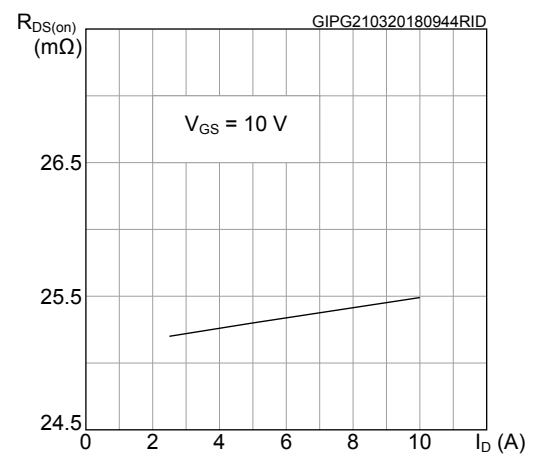
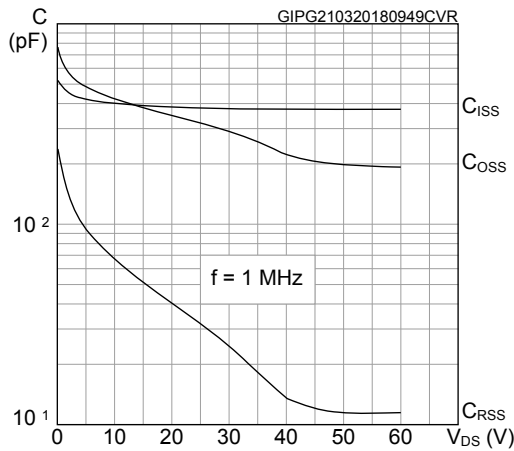
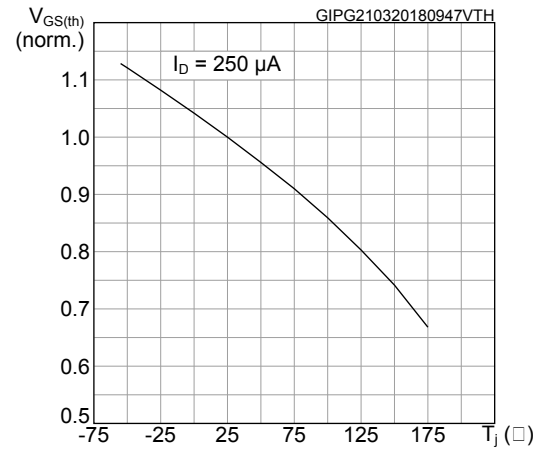
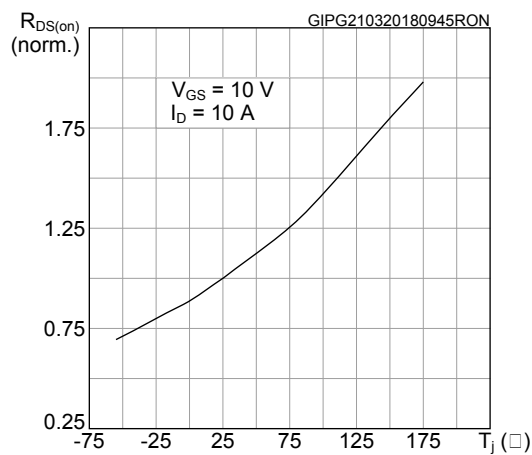
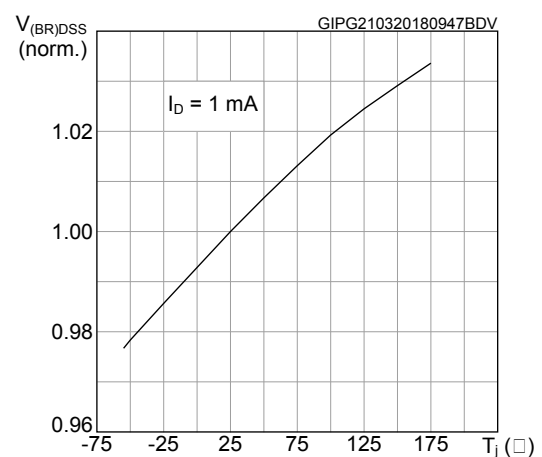
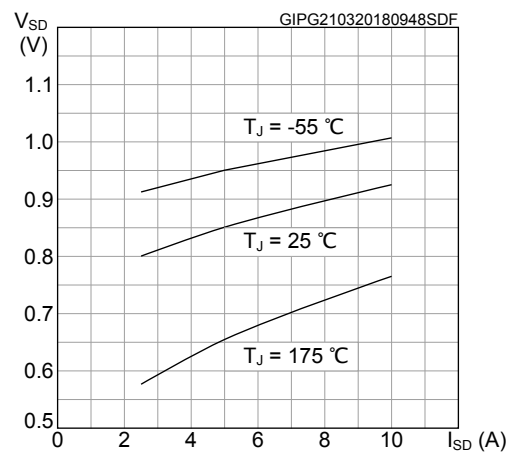
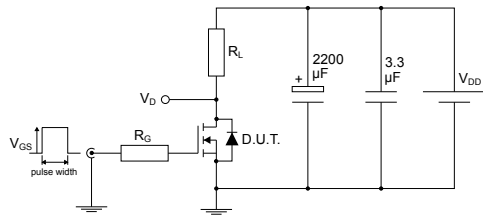
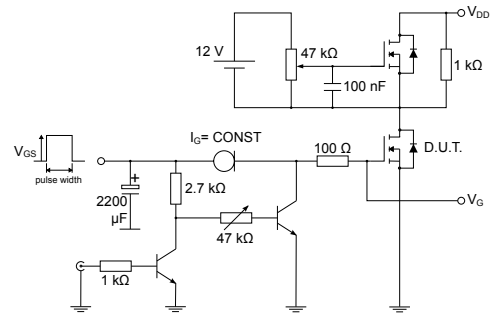
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Gate charge vs gate-source voltage

Figure 6. Static drain-source on-resistance


Figure 7. Capacitance variations

Figure 8. Normalized gate threshold voltage vs temperature

Figure 9. Normalized on-resistance vs temperature

Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

Figure 11. Source- drain diode forward characteristics


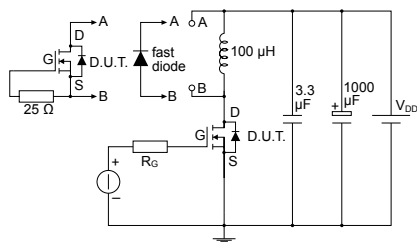
3 Test circuits

Figure 12. Test circuit for resistive load switching times


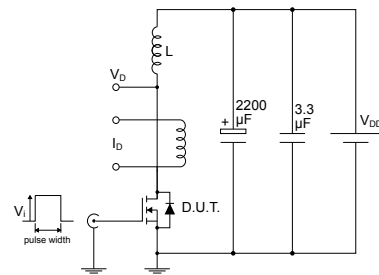
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Figure 13. Test circuit for gate charge behavior


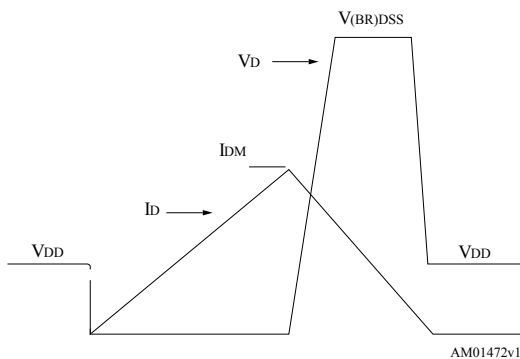
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Figure 14. Test circuit for inductive load switching and diode recovery times


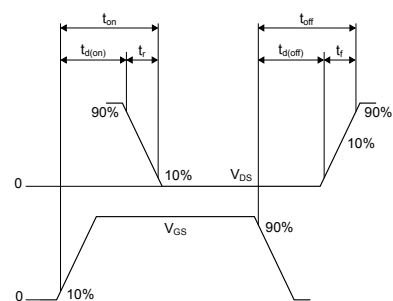
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Figure 15. Unclamped inductive load test circuit


AM01471v1

Figure 16. Unclamped inductive waveform


AM01472v1

Figure 17. Switching time waveform


AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 double island WF type R package information

Figure 18. PowerFLAT™ 5x6 double island WF type R package outline

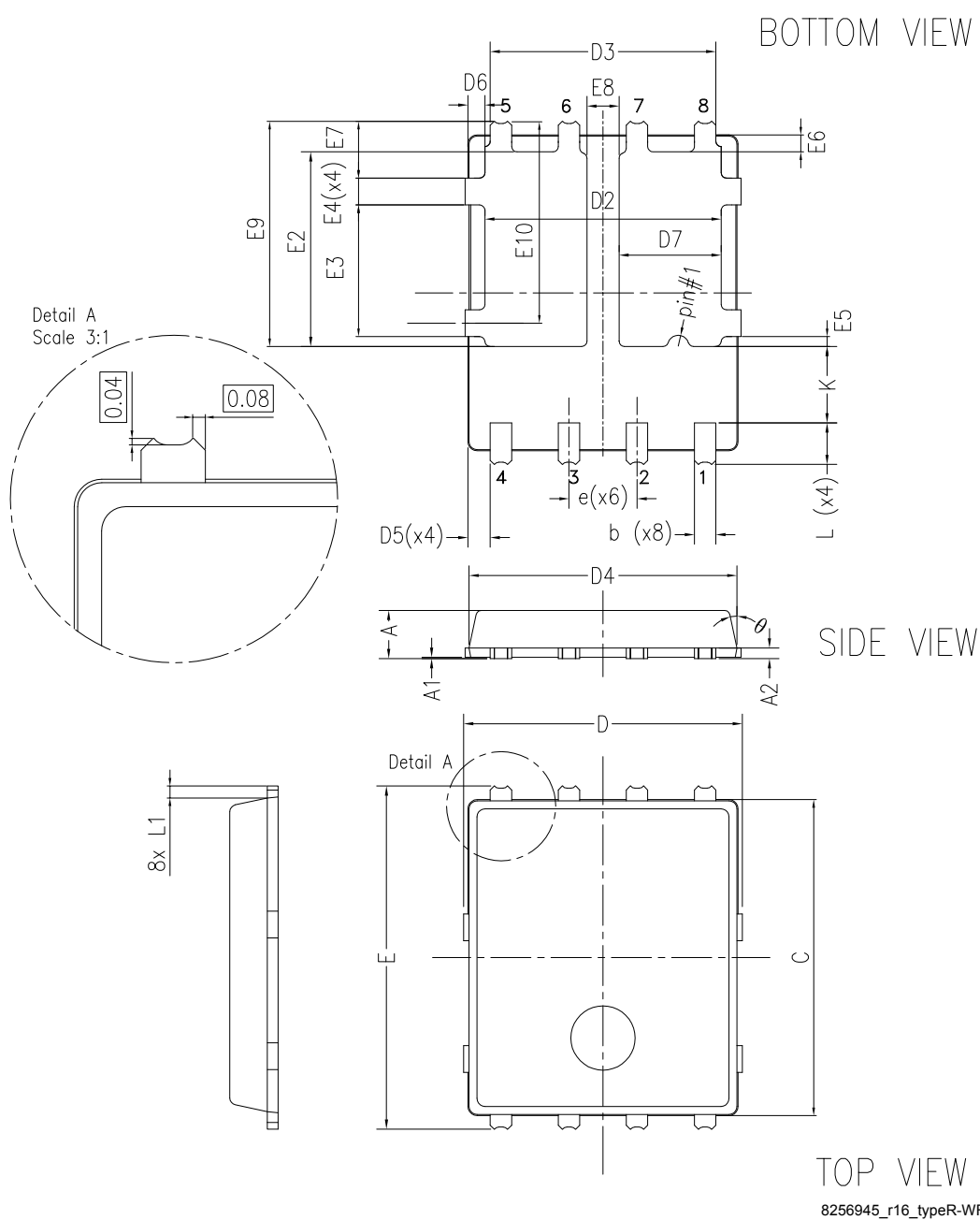
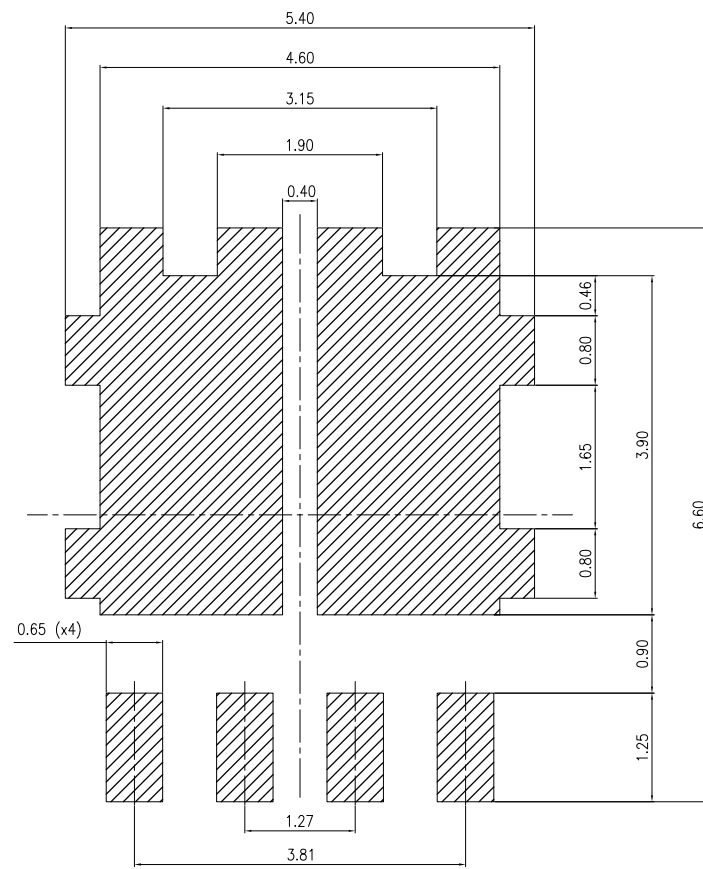


Table 7. PowerFLAT™ 5x6 double island WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
D7	1.68		1.98
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E8	0.55		0.75
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
θ	0°		12°

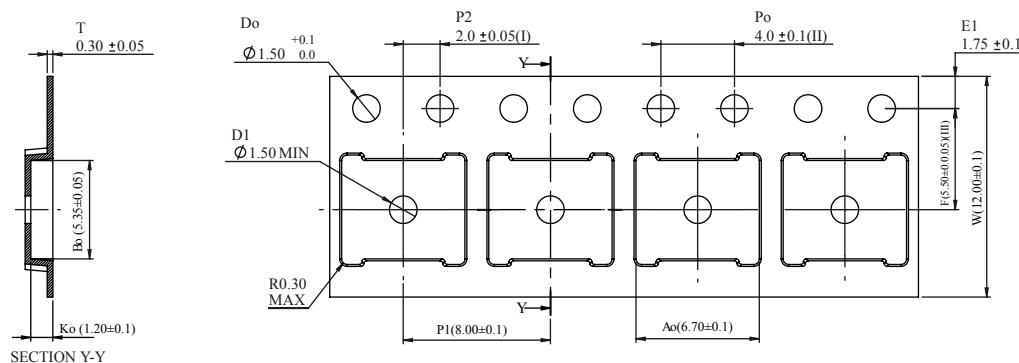
Figure 19. PowerFLAT™ 5x6 double island recommended footprint (dimensions are in mm)



8256945_FP_std_R16

4.2 PowerFLAT™ 5x6 WF packing information

Figure 20. PowerFLAT™ 5x6 WF tape (dimensions are in mm)



- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
- (III) Measured from centreline of sprocket hole to centreline of pocket.

Base and bulk quantity 3000 pcs

8234350_TapeWF_rev_C

Figure 21. PowerFLAT™ 5x6 package orientation in carrier tape

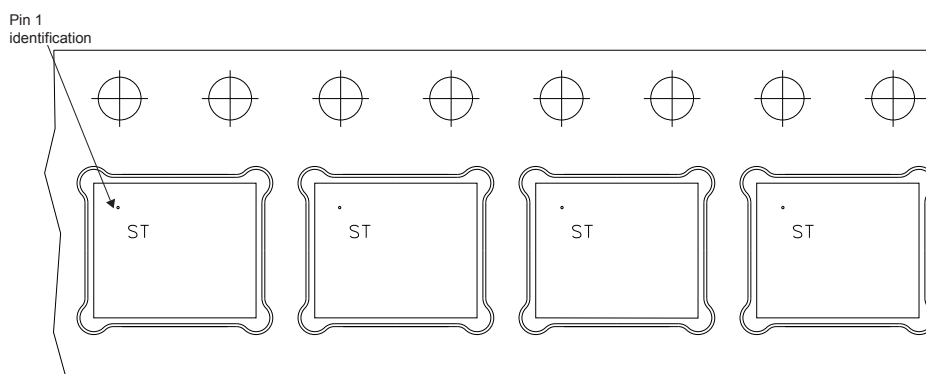
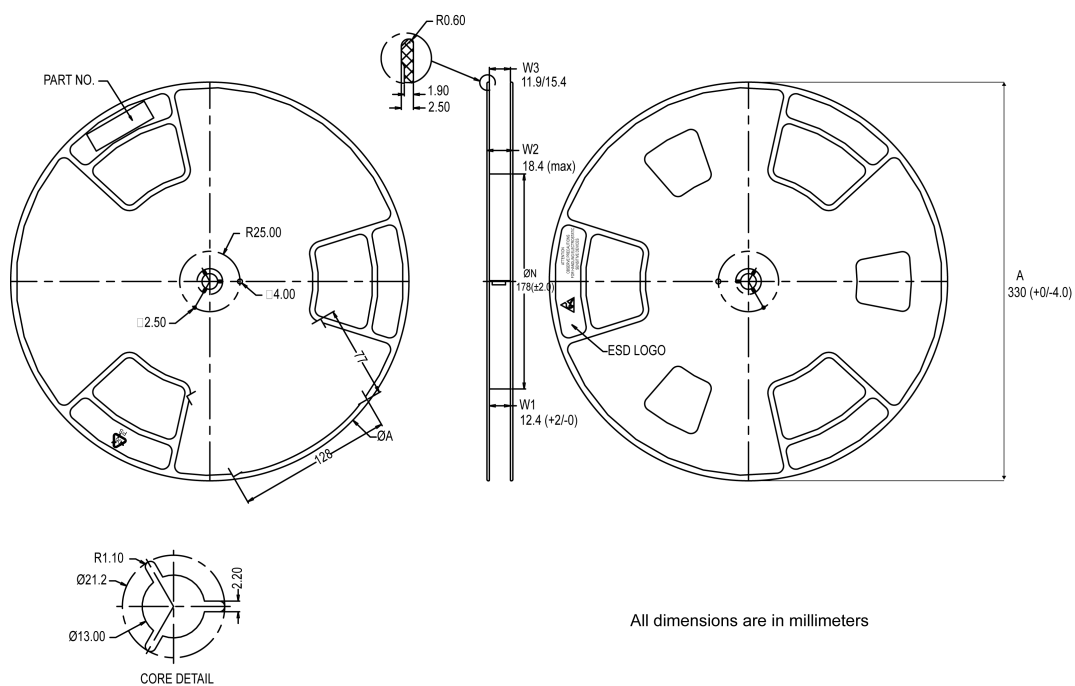


Figure 22. PowerFLAT™ 5x6 reel (dimensions are in mm)



8234350_Reel_rev_C

Revision history

Table 8. Document revision history

Date	Revision	Changes
21-Mar-2018	1	Initial release. The document status is production data.

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