

## CSD13385F5 12-V N-Channel FemtoFET™ MOSFET

### 1 Features

- Low On Resistance
- Low  $Q_g$  and  $Q_{gd}$
- Ultra-Small Footprint
  - 1.53 mm × 0.77 mm
- Low Profile
  - 0.35-mm Height
- Integrated ESD Protection Diode
  - Rated > 4-kV HBM
  - Rated > 2-kV CDM
- Lead and Halogen Free
- RoHS Compliant

### 2 Applications

- Optimized for Industrial Load Switch Applications
- Optimized for General Purpose Switching Applications

### 3 Description

This 12-V, 15-m $\Omega$ , N-Channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing a significant reduction in footprint size.

### Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	12	V
$Q_g$	Gate Charge Total (4.5 V)	3.9	nC
$Q_{gd}$	Gate Charge Gate-to-Drain	0.39	nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 1.8\text{ V}$	26
		$V_{GS} = 2.5\text{ V}$	18
		$V_{GS} = 4.5\text{ V}$	15
$V_{GS(th)}$	Threshold Voltage	0.8	V

### Device Information<sup>(1)</sup>

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD13385F5	3000	7-Inch Reel	Femto 1.53-mm × 0.77-mm SMD Lead Less	Tape and Reel
CSD13385F5T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Absolute Maximum Ratings

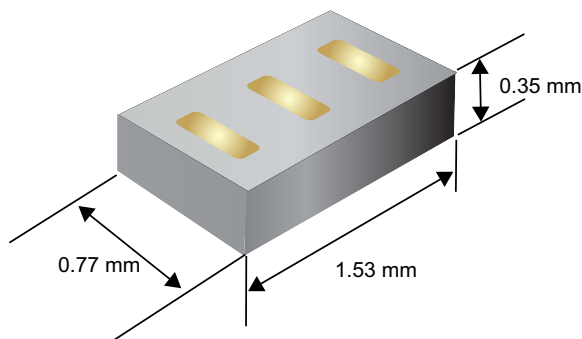
$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	12	V
$V_{GS}$	Gate-to-Source Voltage	8	V
$I_D$	Continuous Drain Current <sup>(1)</sup>	4.3	A
	Continuous Drain Current <sup>(2)</sup>	7.1	
$I_{DM}$	Pulsed Drain Current <sup>(1)(3)</sup>	41	A
$P_D$	Power Dissipation <sup>(1)</sup>	0.5	W
	Power Dissipation <sup>(2)</sup>	1.4	
$V_{(ESD)}$	Human-Body Model (HBM)	4	kV
	Charged-Device Model (CDM)	2	
$T_J$ , $T_{stg}$	Operating Junction, Storage Temperature	–55 to 150	$^\circ\text{C}$

(1) Min Cu, typical  $R_{\theta JA} = 245^\circ\text{C}/\text{W}$ .

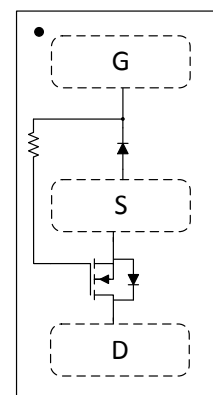
(2) Max Cu, typical  $R_{\theta JA} = 90^\circ\text{C}/\text{W}$ .

(3) Pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$ .

Typical Part Dimensions



Top View



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## 4 Revision History

### Changes from Original (October 2016) to Revision A

**Page**

- |  |          |
|--|----------|
| • Changed $I_{DSS}$ and $I_{GSS}$ unit value from $\mu A$ to nA in the <i>Electrical Characteristics</i> table. .... | <b>3</b> |
|--|----------|

## 5 Specifications

### 5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	12			V
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 9.6\text{ V}$			50	nA
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 8\text{ V}$			25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	0.5	0.8	1.2	V
$R_{DS(on)}$	Drain-to-source on resistance	$V_{GS} = 1.8\text{ V}, I_{DS} = 0.1\text{ A}$		26	50	m $\Omega$
		$V_{GS} = 2.5\text{ V}, I_{DS} = 0.9\text{ A}$		18	23	
		$V_{GS} = 4.5\text{ V}, I_{DS} = 0.9\text{ A}$		15	19	
$g_{fs}$	Transconductance	$V_{DS} = 1.2\text{ V}, I_{DS} = 0.9\text{ A}$		11.3		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 6\text{ V}, f = 1\text{ MHz}$		519	674	pF
$C_{oss}$	Output capacitance			305	396	pF
$C_{rss}$	Reverse transfer capacitance			29	38	pF
$R_G$	Series gate resistance			20		$\Omega$
$Q_g$	Gate charge total (4.5 V)	$V_{DS} = 6\text{ V}, I_{DS} = 0.9\text{ A}$		3.9	5.0	nC
$Q_{gd}$	Gate charge gate-to-drain			0.39		nC
$Q_{gs}$	Gate charge gate-to-source			0.74		nC
$Q_{g(th)}$	Gate charge at $V_{th}$			0.46		nC
$Q_{oss}$	Output charge	$V_{DS} = 6\text{ V}, V_{GS} = 0\text{ V}$		2.5		nC
$t_{d(on)}$	Turnon delay time	$V_{DS} = 6\text{ V}, V_{GS} = 4.5\text{ V}, I_{DS} = 0.9\text{ A}, R_G = 2\ \Omega$		7		ns
$t_r$	Rise time			10		ns
$t_{d(off)}$	Turnoff delay time			33		ns
$t_f$	Fall time			10		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode forward voltage	$I_{SD} = 0.9\text{ A}, V_{GS} = 0\text{ V}$		0.67	1.0	V

### 5.2 Thermal Information

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>		90		$^\circ\text{C/W}$
	Junction-to-ambient thermal resistance <sup>(2)</sup>		245		

(1) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

### 5.3 Typical MOSFET Characteristics

T<sub>A</sub> = 25°C (unless otherwise stated)

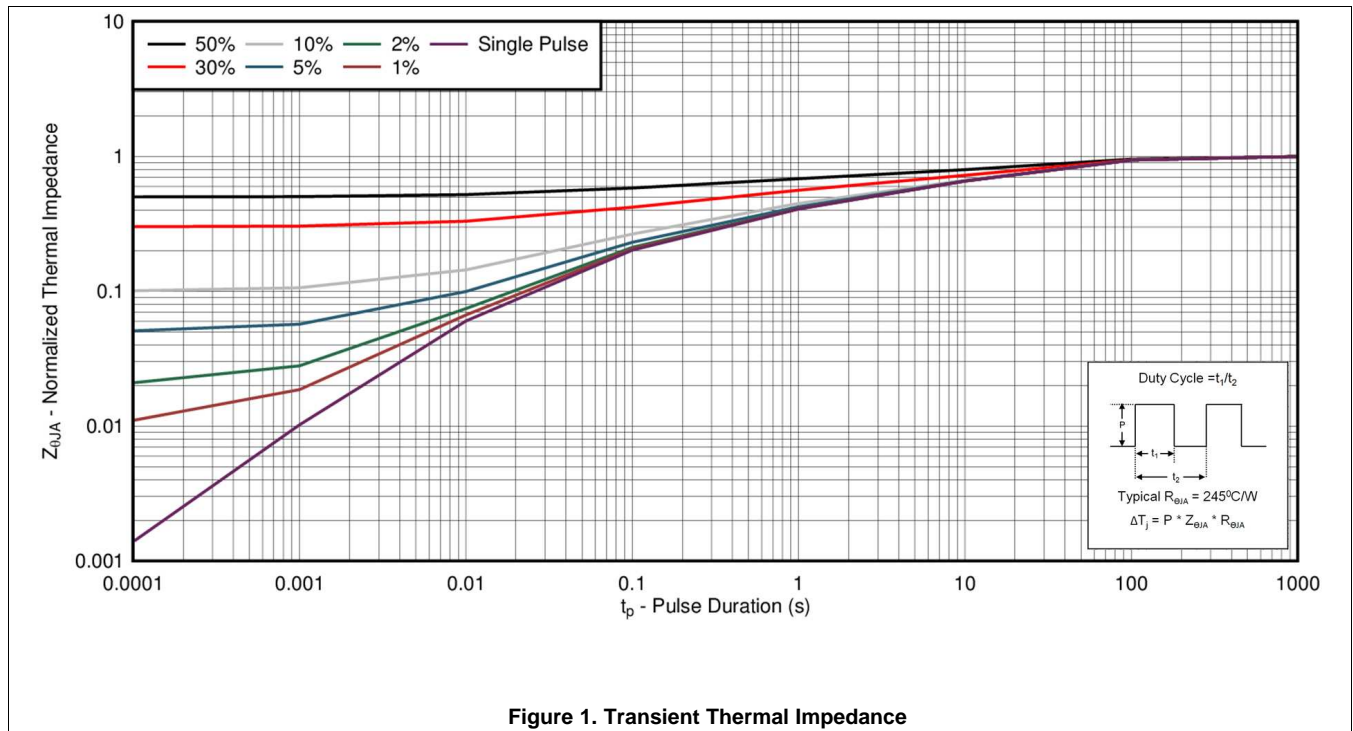


Figure 1. Transient Thermal Impedance

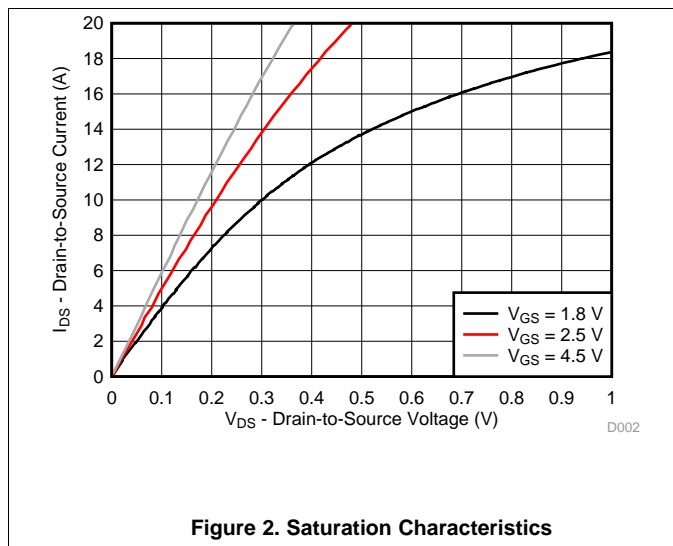


Figure 2. Saturation Characteristics

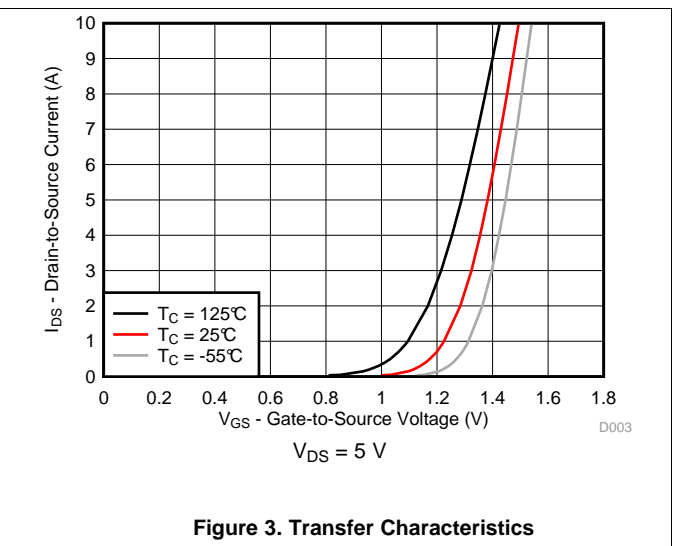


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

T<sub>A</sub> = 25°C (unless otherwise stated)

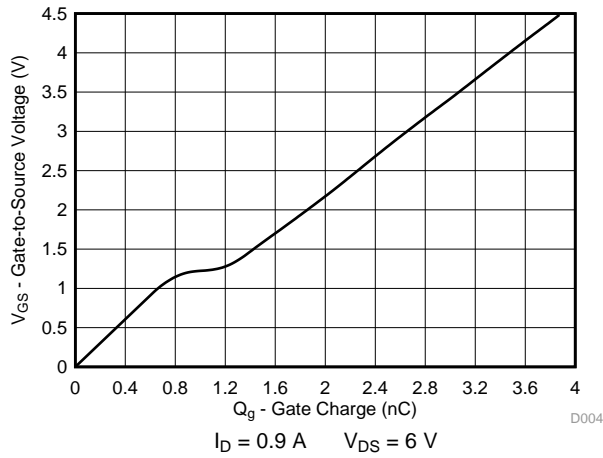


Figure 4. Gate Charge

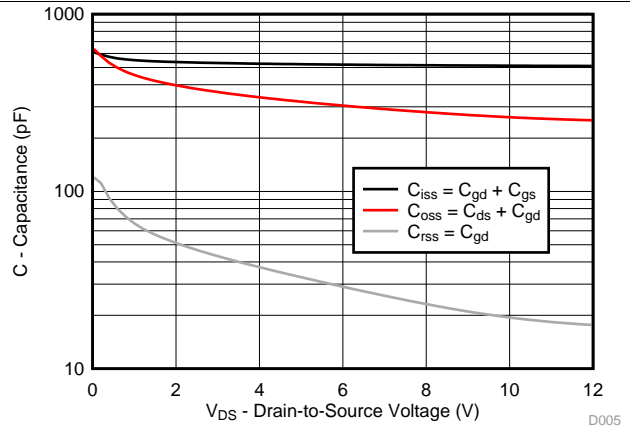


Figure 5. Capacitance

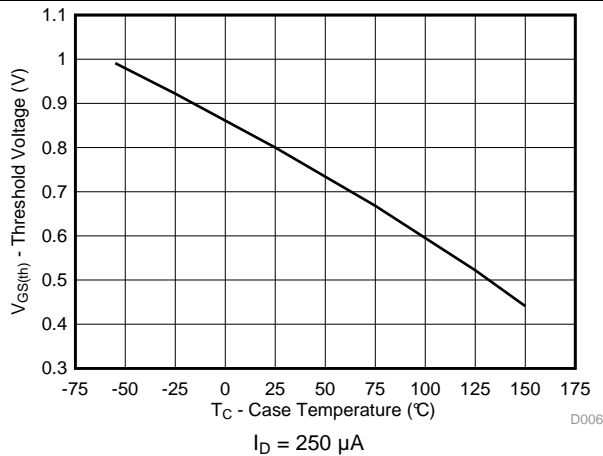


Figure 6. Threshold Voltage vs Temperature

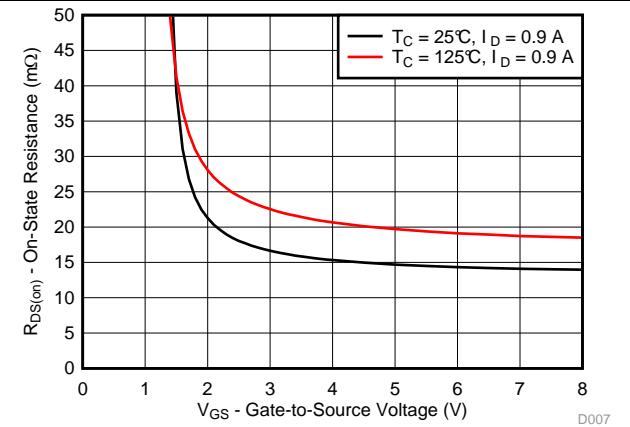


Figure 7. On-State Resistance vs Gate-to-Source Voltage

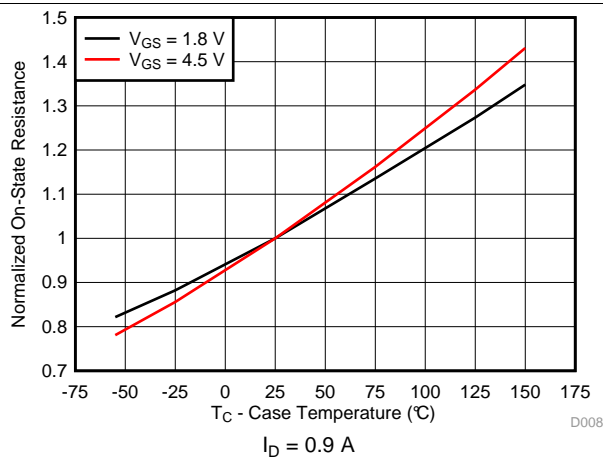


Figure 8. Normalized On-State Resistance vs Temperature

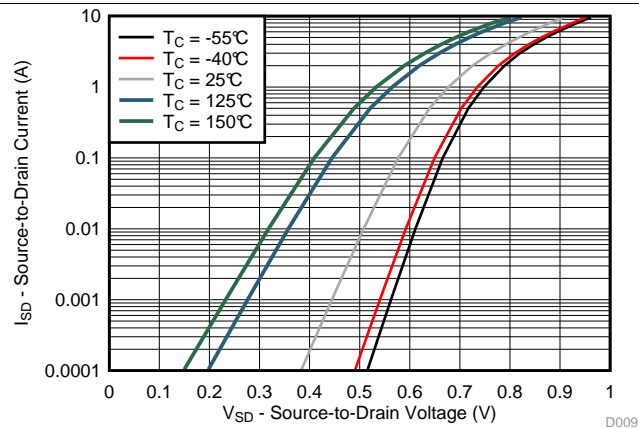
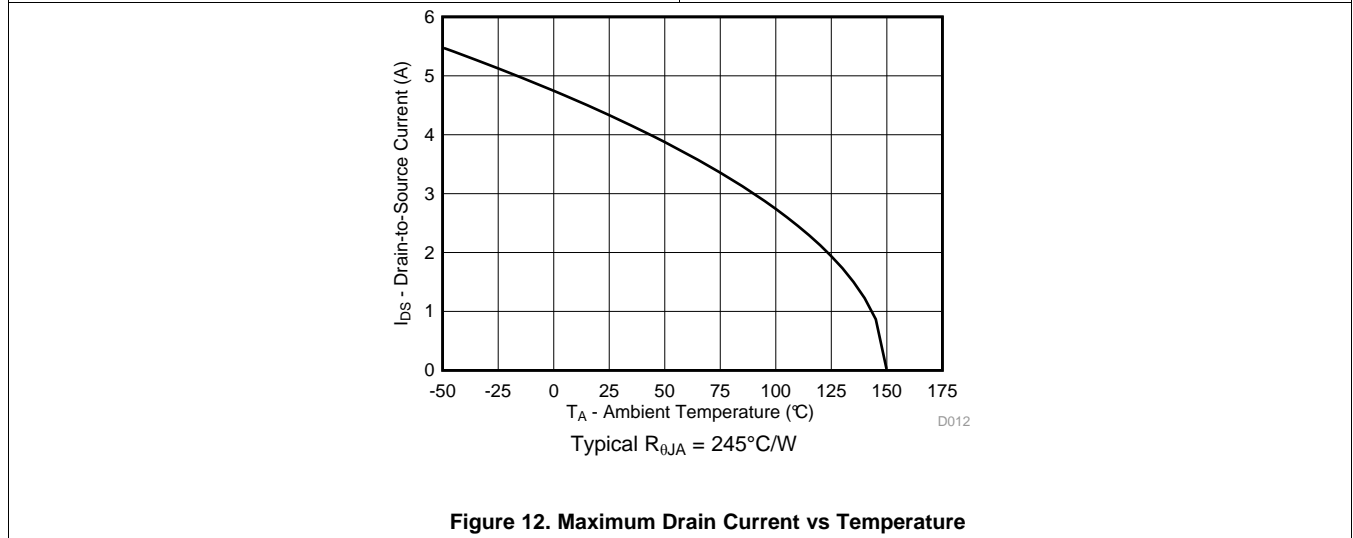
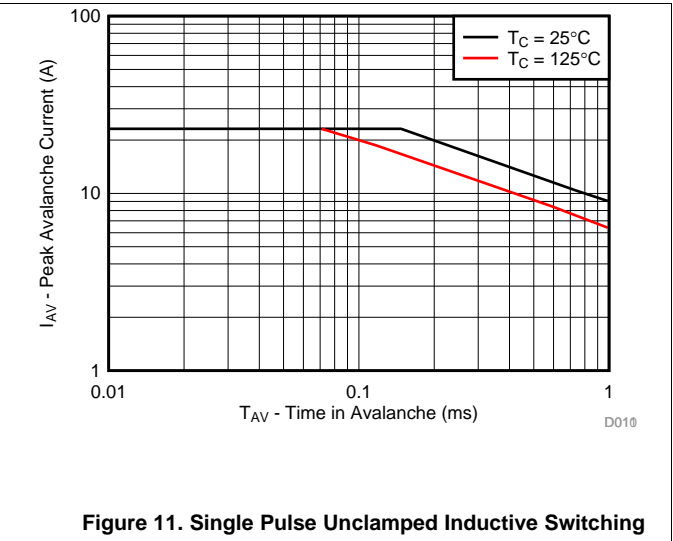
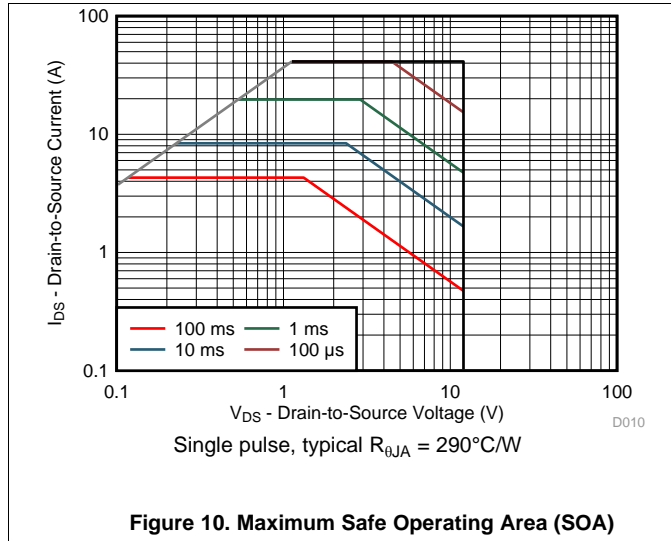


Figure 9. Typical Diode Forward Voltage

**Typical MOSFET Characteristics (continued)**

$T_A = 25^\circ\text{C}$  (unless otherwise stated)



## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 6.3 Trademarks

FemtoFET, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.5 Glossary

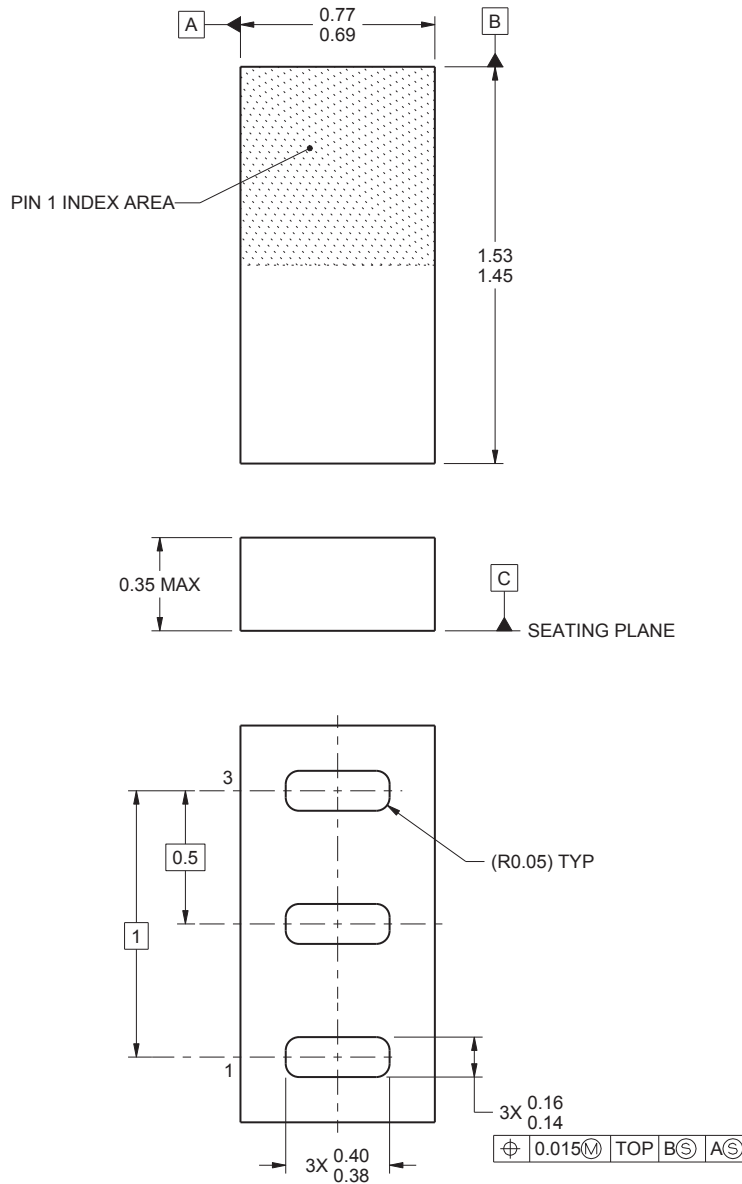
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Mechanical Dimensions

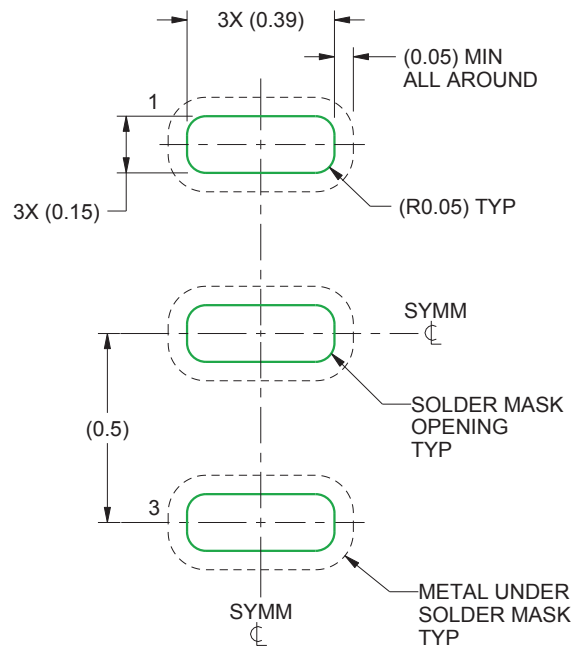


- (1) All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- (2) This drawing is subject to change without notice.
- (3) This package is a PB-free solder land design.

**Table 1. Pin Configuration**

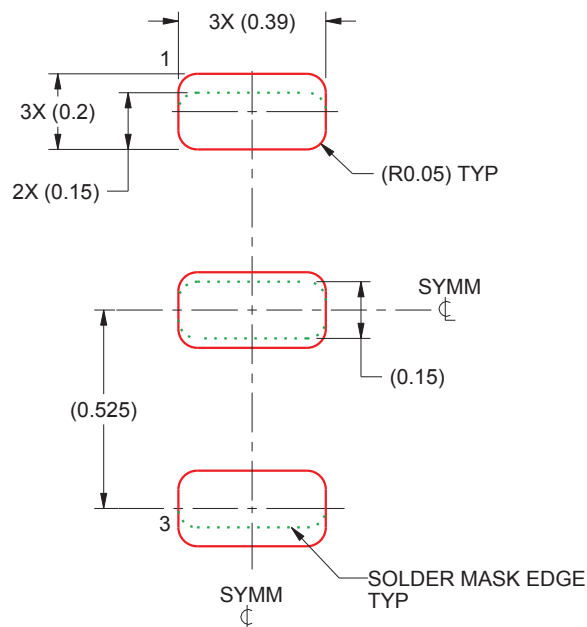
POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

## 7.2 Recommended Minimum PCB Layout



(1) All dimensions are in millimeters.

## 7.3 Recommended Stencil Pattern



(1) All dimensions are in millimeters.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13385F5	ACTIVE	PICOSTAR	YJK	3	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	4V	<a href="#">Samples</a>
CSD13385F5T	ACTIVE	PICOSTAR	YJK	3	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	4V	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13385F5	PICOST AR	YJK	3	3000	178.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD13385F5	PICOST AR	YJK	3	3000	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD13385F5T	PICOST AR	YJK	3	250	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD13385F5T	PICOST AR	YJK	3	250	178.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13385F5	PICOSTAR	YJK	3	3000	220.0	220.0	35.0
CSD13385F5	PICOSTAR	YJK	3	3000	182.0	182.0	20.0
CSD13385F5T	PICOSTAR	YJK	3	250	182.0	182.0	20.0
CSD13385F5T	PICOSTAR	YJK	3	250	220.0	220.0	35.0

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