CSD95378BQ5M Synchronous Buck NexFET™ Smart Power Stage

1 Features

- 60-A Continuous Operating Current Capability
- 93.4% System Efficiency at 30 A
- Low-Power Loss of 2.8 W at 30 A
- High-Frequency Operation (up to 1.25 MHz)
- Diode Emulation Mode With FCCM
- Temperature Compensated Bi-Directional Current Sense
- Analog Temperature Output (400 mV at 0°C)
- Fault Monitoring
  - High-Side Short, Overcurrent, and Overtemperature Protection
- 3.3-V and 5-V PWM Signal Compatible
- Tri-State PWM Input
- Integrated Bootstrap Diode
- Optimized Dead Time for Shoot-Through Protection
- High-Density SON 5-mm × 6-mm Footprint
- Ultra-Low-Inductance Package
- System Optimized PCB Footprint
- RoHS Compliant – Lead-Free Terminal Plating
- Halogen Free

2 Applications

- Multiphase Synchronous Buck Converters
  - High-Frequency Applications
  - High-Current, Low-Duty-Cycle Applications
- POL DC-DC Converters
- Memory and Graphic Cards
- Desktop and Server VR11.x / VR12.x V-core and Memory Synchronous Converters

3 Description

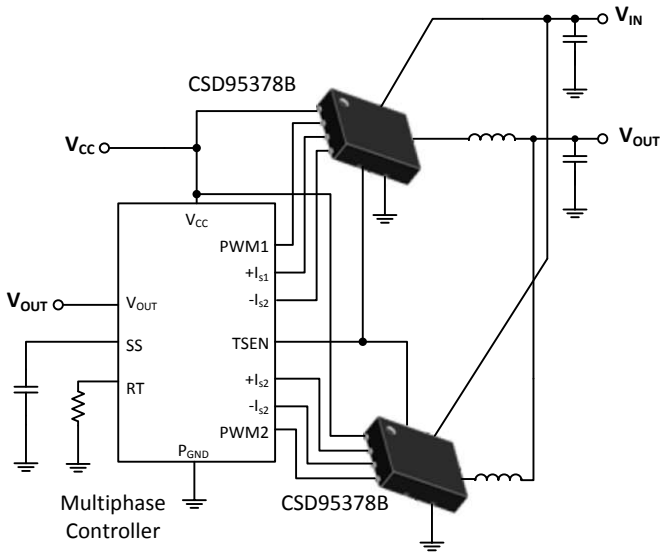
The CSD95378BQ5M NexFET™ smart power stage is a highly optimized design for use in a high-power, high-density synchronous buck converter. This product integrates the driver IC and power MOSFETs to complete the power stage switching function. This combination produces high-current, high-efficiency, and high speed switching capability in a small 5-mm × 6-mm outline package. It also integrates the accurate current sensing and temperature sensing functionality to simplify system design and improve accuracy. In addition, the PCB footprint is optimized to help reduce design time and simplify the completion of the overall system design.

Device Information(1)

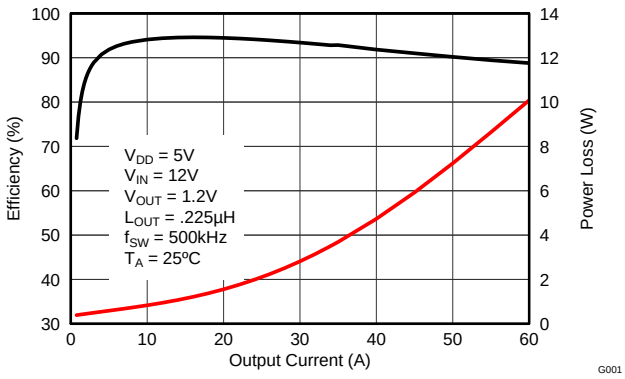
DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD95378BQ5M	13-Inch Reel	2500	SON 5.00-mm × 6.00-mm Package	Tape and Reel
CSD95378BQ5MT	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Diagram



Typical Power Stage Efficiency and Power Loss



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision A (July 2014) to Revision B **Page**

- Updated the CSD95378B parts in the *Application Schematic* ... 5
- Added the *Receiving Notification of Documentation Updates* and *Community Resources* sections in *Device and Documentation Support* ... 6

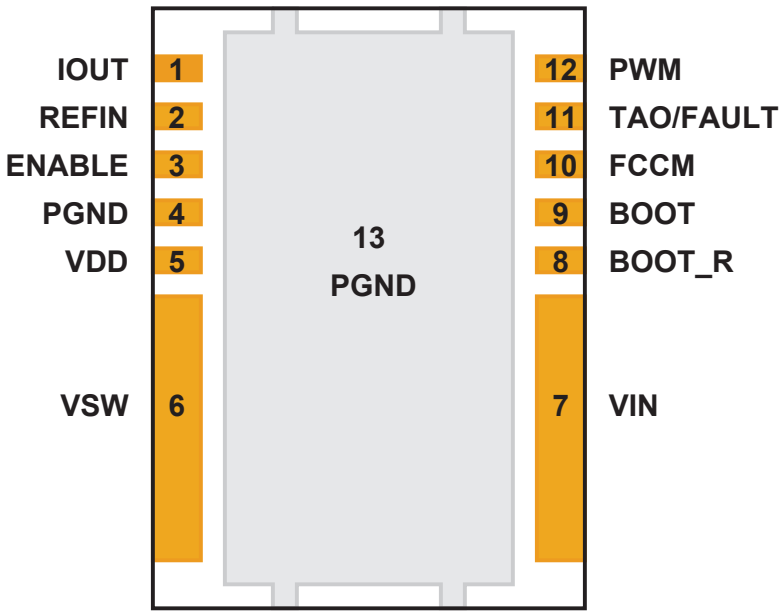
Changes from Original (April 2014) to Revision A **Page**

- Updated the controller IC in the *Application Schematic* to the TPS40428 ... 5

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5 Pin Configuration and Functions

13-Pin SON
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
BOOT	9	Bootstrap capacitor connection. Connect a minimum of 0.1-µF, 16-V, X7R ceramic capacitor from BOOT to BOOT_R pins. The bootstrap capacitor provides the charge to turn on the control FET. The bootstrap diode is integrated.
BOOT_R	8	Return path for HS gate driver, connected to V_{SW} internally.
ENABLE	3	Enables device operation. If ENABLE = logic HIGH, turns on device. If ENABLE = logic LOW, the device is turned off and both MOSFET gates are actively pulled low. An internal 100-kΩ pulldown resistor will pull the ENABLE pin LOW if left floating.
FCCM	10	This pin enables the Diode Emulation function. When this pin is held LOW, Diode Emulation Mode is enabled for sync FET. When FCCM is HIGH, the device is operated in Forced Continuous Conduction Mode. An internal 5-µA current source will pull the FCCM pin to 3.3 V if left floating.
IOUT	1	Output of current sensing amplifier. V(IOUT) – V(REFIN) is proportional to the phase current.
P_{GND}	4	Power ground, connected directly to pin 13.
P_{GND}	13	Power ground.
PWM	12	Pulse width modulated tri-state input from external controller. Logic LOW sets control FET gate low and sync FET gate high. Logic HIGH sets control FET gate high and sync FET gate low. Open or Hi-Z sets both MOSFET gates low if greater than the tri-state shutdown hold-off time (t_{3HT}).
REFIN	2	External reference voltage input for current sensing amplifier.
TAO/ FAULT	11	Temperature analog output. Reports a voltage proportional to the die temperature. An ORing diode is integrated in the IC. When used in multiphase application, a single wire can be used to connect the TAO pins of all the ICs. Only the highest temperature will be reported. TAO will be pulled up to 3.3 V if thermal shutdown occurs. TAO should be bypassed to P_{GND} with a 1-nF, 16-V, X7R ceramic capacitor.
V_{DD}	5	Supply voltage to gate driver and internal circuitry.
V_{IN}	7	Input voltage pin. Connect input capacitors close to this pin.
V_{SW}	6	Phase node connecting the HS MOSFET source and LS MOSFET drain - pin connection to the output inductor.

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6 Specifications

6.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN} to P_{GND}	–0.3	25	V
V_{IN} to V_{SW}	–0.3	25	V
V_{IN} to V_{SW} (10 ns)	–7	27	V
V_{SW} to P_{GND}	–0.3	20	V
V_{SW} to P_{GND} (10 ns)	–7	23	V
V_{DD} to P_{GND}	–0.3	7	V
ENABLE, PWM, FCCM. TAO, IOUT, REFIN to P_{GND}	–0.3	V_{DD} + 0.3 V	V
BOOT to BOOT_R(2)	–0.3	V_{DD} + 0.3 V	V
Power dissipation, P_D		12	W
Operating junction temperature, T_J	–55	150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Should not exceed 7 V.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	–2000	2000	V
		Charged-device model (CDM)	–500	500	

6.3 Recommended Operating Conditions

T_A = 25°C (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Gate drive voltage		4.5	5.5	V
V_{IN}	Input supply voltage(1)			16	V
V_{OUT}	Output voltage			5.5	V
I_{OUT}	Continuous output current	V_{IN} = 12 V, V_{DD} = 5 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz, L_{OUT} = 0.225 µH(2)		60	
I_{OUT-PK}	Peak output current(3)			90	A
f_{SW}	Switching frequency	C_{BST} = 0.1 µF (min)		1250	kHz
	On-time duty cycle	f_{SW} = 1 MHz		85%	
	Minimum PWM on time		40		ns
	Operating temperature		–40	125	°C

(1) Operating at high V_{IN} can create excessive AC voltage overshoots on the switch node (V_{SW}) during MOSFET switching transients. For reliable operation, the switch node (V_{SW}) to ground voltage must remain at or below the *Absolute Maximum Ratings*.
(2) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(3) System conditions as defined in Note 1. Peak output current is applied for t_p = 50 µs.

6.4 Thermal Information

T_A = 25°C (unless otherwise noted)

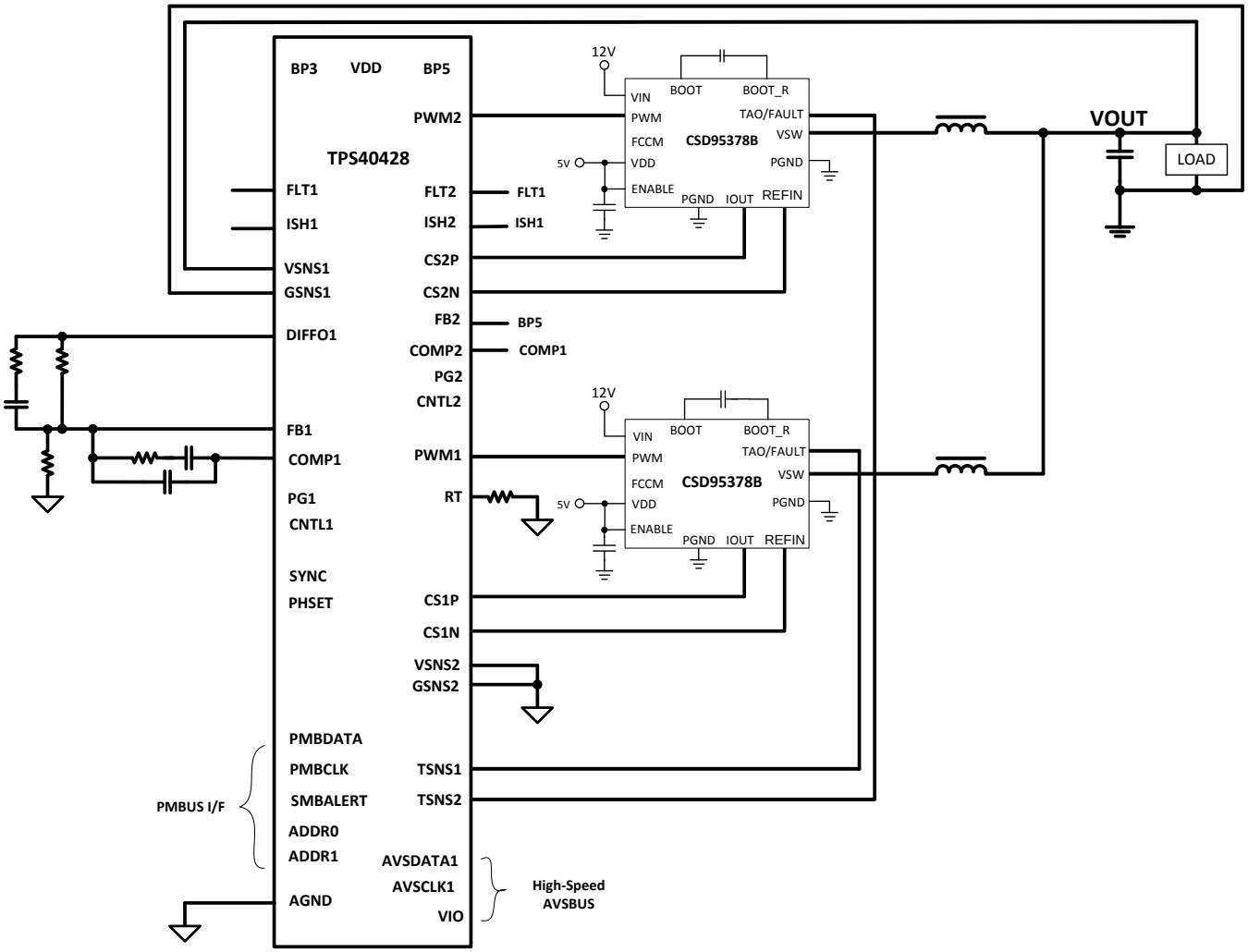
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case (top-of-package) thermal resistance(1)			15	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(2)			1.5	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45 -cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in, 0.06-in (1.52-mm) thick FR4 board.
(2) $R_{\theta JB}$ value based on hottest board temperature within 1 mm of the package.

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7 Application Schematic

7.1 Typical Application



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8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.3 Trademarks

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8.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.5 Glossary

SLYZ022 — *TI Glossary*.

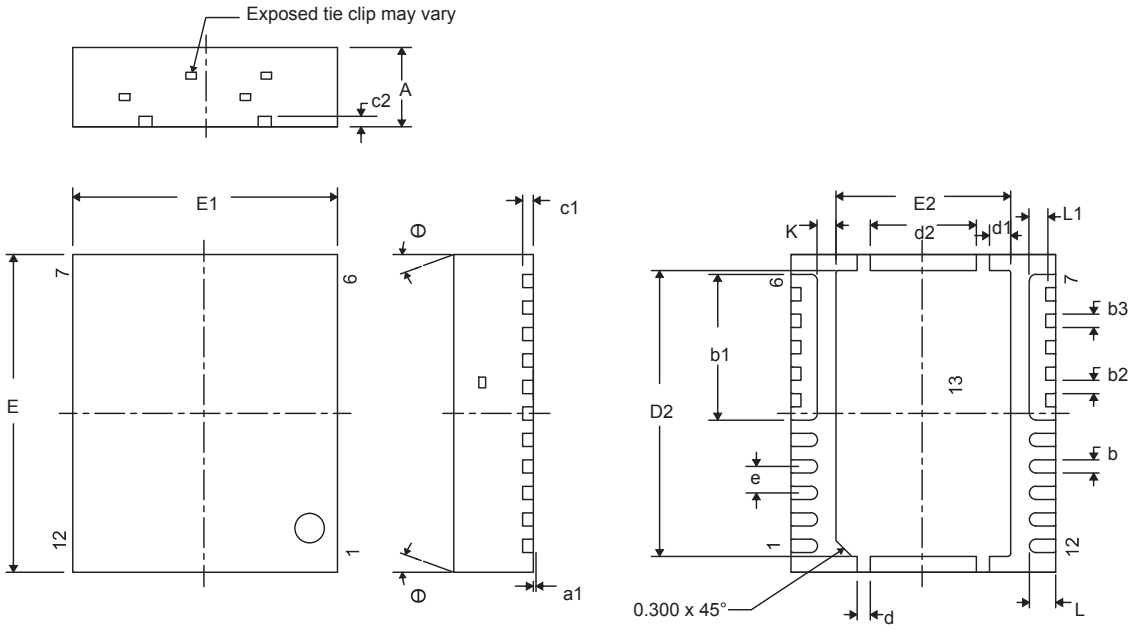
This glossary lists and explains terms, acronyms, and definitions.

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9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

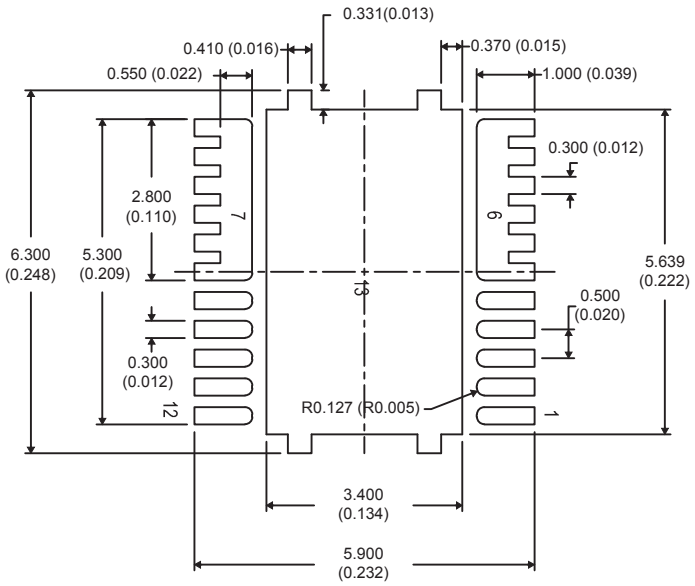
9.1 Mechanical Drawing



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.400	1.450	1.500	0.057	0.059	0.061
a1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.200	0.250	0.320	0.008	0.010	0.013
b1		2.750 TYP			0.108 TYP	
b2	0.200	0.250	0.320	0.008	0.010	0.013
b3		0.250 TYP			0.010 TYP	
c1	0.150	0.200	0.250	0.006	0.008	0.010
c2	0.200	0.250	0.300	0.008	0.010	0.012
D2	5.300	5.400	5.500	0.209	0.213	0.217
d	0.200	0.250	0.300	0.008	0.010	0.012
d1	0.350	0.400	0.450	0.014	0.016	0.018
d2	1.900	2.000	2.100	0.075	0.079	0.083
E	5.900	6.000	6.100	0.232	0.236	0.240
E1	4.900	5.000	5.100	0.193	0.197	0.201
E2	3.200	3.300	3.400	0.126	0.130	0.134
e		0.500 TYP			0.020 TYP	
K		0.350 TYP			0.014 TYP	
L	0.400	0.500	0.600	0.016	0.020	0.024
L1	0.210	0.310	0.410	0.008	0.012	0.016
θ	0.00	—	—	0.00	—	—

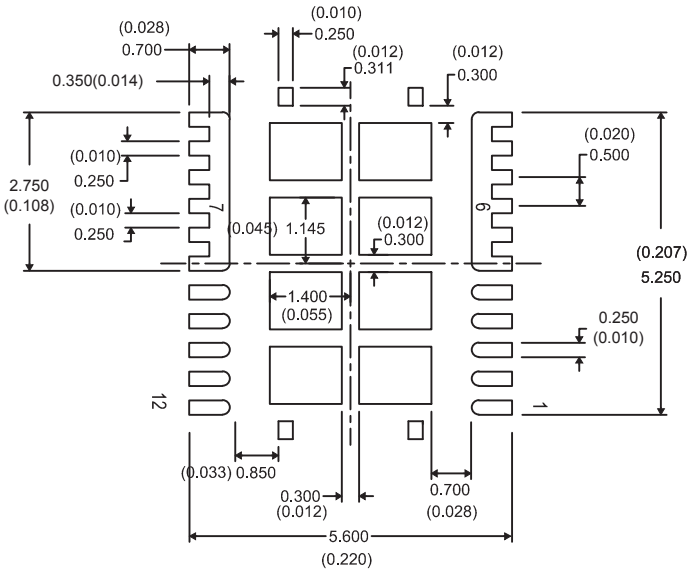
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9.2 Recommended PCB Land Pattern



1. Dimensions are in mm (in).

9.3 Recommended Stencil Opening



1. Dimensions are in mm (in).
2. Stencil thickness is 100 µm.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD95378BQ5M	ACTIVE	LSON-CLIP	DQP	12	2500	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 150	95378BM	Samples
CSD95378BQ5MT	ACTIVE	LSON-CLIP	DQP	12	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 150	95378BM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

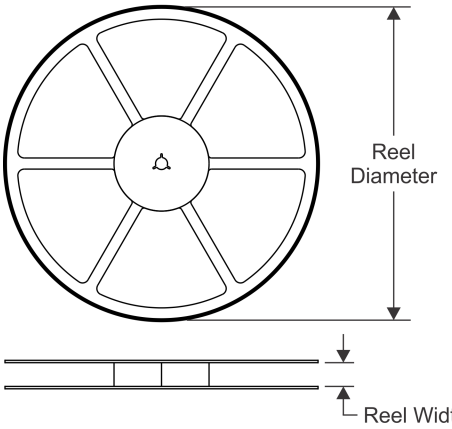
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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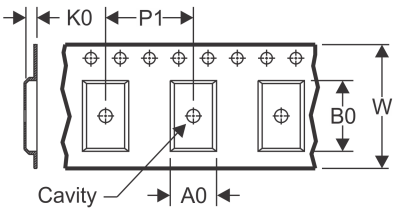
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

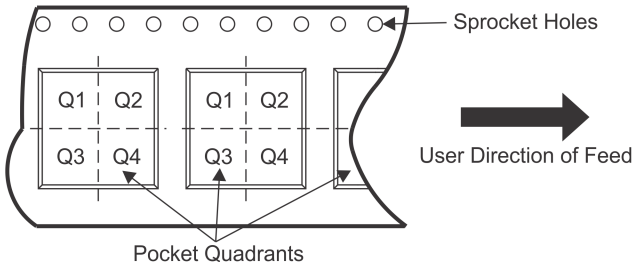


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

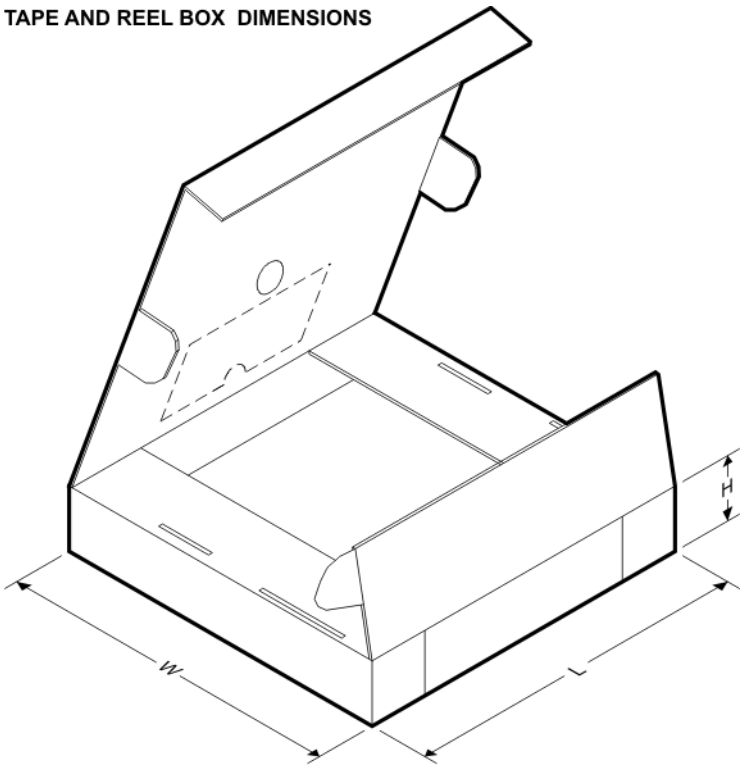
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD95378BQ5M	LSON-CLIP	DQP	12	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1
CSD95378BQ5MT	LSON-CLIP	DQP	12	250	180.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD95378BQ5M	LSON-CLIP	DQP	12	2500	367.0	367.0	35.0
CSD95378BQ5MT	LSON-CLIP	DQP	12	250	210.0	185.0	35.0

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