LTC4332
SPI Extender Over Rugged Differential Link

DESCRIPTION

Demonstration circuit 2799A uses the LTC®4332 to extend a SPI interface with 3 slave devices to up to 1200m (150m with a 500kHz SCK as factory configured). The DC2799A is designed to be compatible with the popular Pmod interface to allow for easy evaluation with the many master and slave devices in this ecosystem.

The LTC4332 is a 2MHz SPI bus extender designed for operation in high noise industrial environments. The SPI bus is extended over two twisted pairs by ±60V fault protected differential transceivers. The LTC4332's extended 25V common mode voltage range allows it to bridge across different ground potentials.

The DC2799A's local side interfaces with the host SPI master as 4 different SPI slave devices. These slave devices support SPI modes (0,0) or (1,1) where (CPOL, CPHA). Three of the slave devices are associated with the remote side devices ($\overline{SS1}$, $\overline{SS2}$, $\overline{SS3}$) and the fourth device ($\overline{SSC}$) is used to configure the DC2799A's LTC4332 SPI extenders. The DC2799A's remote side interface implements a SPI master with 3 different slave selects. The remote side master supports all four SPI modes and a unique mode may be associated to each slave select.

By default, the remote SPI modes are all mode (0,0). The remote side SPI modes are configured by writing to the local side LTC4332 using the $\overline{SSC}$ slave device.

The LTC4332 data sheet gives a complete description of the part, its operation and application information. The data sheet should be referred to when reading this demo manual. The LTC4332 is available in a 20-lead QFN package and three temperature grades (commercial 0°C to 70°C, industrial –40°C to 85°C, and high temperature –40°C to 125°C).

Design files for this circuit board are available.

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DC2799A CONNECTION DIAGRAM

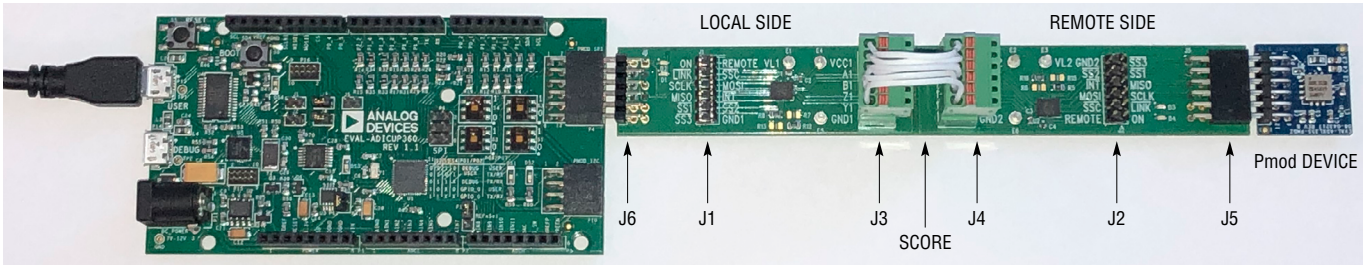


Figure 1. DC2799A

QUICK START PROCEDURE

Demonstration circuit 2799A is easy to set up to evaluate the performance of the LTC4332 using the Pmod system. Refer to Figure 1 for proper equipment setup and follow the procedure below:

1. Connect the DC2799A's male connector J6 to the Pmod host.
2. Confirm the Pmod device's expanded SPI alternate signal pins are compatible with the DC2799A. Make any necessary modifications to the Pmode device and/or DC2799A. See PMOD Interface section for more details.
3. Connect the DC2799A's female connector J5 to the Pmod peripheral.
4. Connect the jumper wires between J3 and J4.
5. Update the host's peripheral interface code if the peripheral(s) use a SPI mode other than (0,0) or the host reads data from the peripheral. See SPI Network Considerations section for more details.
6. Energize the Pmod host and execute the peripheral's code.

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Pmod Interface

The Pmod interface is a popular interface for embedded system development which specifies a standardized electromechanical interface for connecting low frequency, low I/O count peripheral modules to controller boards and covers many different protocols. The DC2799A is compatible with the Digilent Pmod Interface Type 2A (expanded SPI) version 1.2.0 and implements a modified version of the alternate signal definition as shown in Figure 2. *Note that the pin numbering for this connector follows the Pmod specification and is different from the standard connector numbering.*

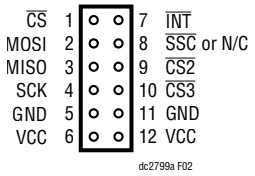


Figure 2. J5, J6 Pmod Connector Pinout

NOTE: The DC2799A does not support the RESET function on pin 8. Instead, it uses this pin on J6 as a select pin ($\overline{SSC}$) to allow the Pmod host to communicate with the local-side LTC4332 device. The remote side host connector J5 leaves pin 8 open circuited.

The $\overline{INT}$ signal (pin 7) provides an interrupt signal from remote slaves to the Pmod host when the SPI bus is idle. On the remote side, pin 7 is an input with a 4.7k pull-up resistor. Open drain outputs from the remote slave devices can signal the Pmod host by pulling this pin low. On the local side, pin 7 is an open-drain output with a 4.7k pull-up resistor. The local side $\overline{INT}$ output will reflect the state of the remote side $\overline{INT}$ input pin. $\overline{INT}$ may change asynchronously with respect to the slave select framing or SCK.

Only one local side slave select ($\overline{SS1}$ ($\overline{CS}$), $\overline{SS2}$ ($\overline{CS2}$), $\overline{SS3}$ ($\overline{CS3}$) or $\overline{SSC}$) may be asserted at a time. The remote side $\overline{SS2}$ ($\overline{CS2}$) and $\overline{SS3}$ ($\overline{CS3}$) are outputs which follow the local side states. The local side slave selects have a weak pull-up and may be left open circuited if not used. In this situation, the corresponding remote side slave selects will be driven high.

NOTE: Some Pmod devices use pins 7-10 as general-purpose IO (GPIO) pins. Depending on the function of these GPIO pins, the DC2799A may or many not be compatible with these Pmod devices. In some cases, the Pmod device can be modified to be compatible. For example, in an DAC Pmod, bringing one of the GPIO pins low after the SPI transaction, might trigger the loading of DAC data; however, if this pin is held low, then the DAC data may

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be loaded with the rising edge of the slave select. In this situation, disconnecting this pin from the DC2799A and then wiring it low on the Pmod device would allow the device to function with the DC2799A.

The DC2799A's Pmod interface uses a standard 100 mil spaced, 25 mil square, 12 pin, right-angle, pin-header style connectors. The DC2799A's local side has a male connector to connect as a Pmod peripheral module with a Pmod host board. The DC2799A's remote side has a female connector and acts as a remote Pmod host to the remote peripheral.

Separable Local and Remote Sides

The DC2799A comes as a single printed circuit board with the local and remote side circuits located on either side of a score. Breaking this score will allow the circuits to be physically separated. Note that the scored edges are sharp after separation and they should be deburred before handling.

Pin Header Connections

Except for the speed setting pins, all control and I/O pins for the two LTC4332 extenders are available on 100 mil center pin headers J1 or J2. See Figure 3.

The ON pins (pin 1) are pulled to their associated VL via 1k resistors and may be externally pulled down to disable the associated LTC4332.

The remote pins (pin 2) are configured via 1k resistors with the local/Pmod peripheral side set as local (pull down) and the remote/Pmod host side set as remote (pull-up). The local/remote configuration can be reversed by externally driving these pins the other way.

The LTC4332's internal slave device select, $\overline{SSC}$, is available on pin 4 of the pin header. Use this slave select when communicating with the LTC4332.

The status of the extender link is available on pin 3 and indicated by the link LEDs D1 and D3.

The presence of a supply voltage (and ON being pulled high) is available on pin 1 and indicated by LEDs D2 and D4.

The remaining pins on the header are the SPI interface pins. In addition to the MOSI/MISO/SCK, there are 3 slave device select pins and an interrupt pin which allows a slave to send an interrupt to the host.

The pin out for the headers J1 or J2 is as follows:

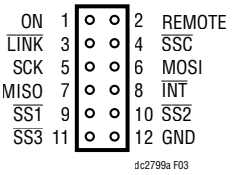


Figure 3. J1, J2 Pin Header Pinout

Local – Remote Link Connection

The DC2799A uses pluggable terminal blocks to allow the use of different cable types as well as access to VCC and GND for incorporating modified bias or protective networks into the differential bus link and/or separating the power and ground connections between the local and remote sides.

When replacing the short jumper wires between the terminal block pins, connect pin 1 to pin 1, etc. The field bus link between the local and remote sides is full-duplex and so A connects to Y and B connects to Z.

The DC2799A includes biasing networks which consist of 619Ω pull-up and pull-down resistors and 120Ω terminating resistors and these values should be acceptable for most nonisolated applications. The pull-up / down resistors are located at the transmitter/driver side of the field bus while the terminating resistors are located at the receiver. This allows the bus pull-up/down voltages to be consistent with the driver voltage and so increases the common mode voltage range between the local and remote sides. Using the pluggable terminal blocks, additional parallel resistors may be easily added to reduce the biasing network's effective resistor values or add a bus protective network if needed.

The link speed is factory set for a maximum SCK frequency of 500kHz but may be adjusted by inserting or removing resistors to configure for different speed settings. Make

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sure that the local and remote sides have the same speed configuration. Refer to the DC2799A schematic to identify the proper pull-up and down resistors and see the LTC4332 data sheet for more details on setting the link speed.

Similar to other field buses such as RS-485, there is an inverse relationship between the link extension distance and SPI bus speed. For more details on link speeds and maximum link distance, see the Link Speed table in the LTC4332 data sheet.

SPI Network Consideration

The SPI protocol supports four unique timing configurations defined by the SCK polarity (CPOL) and clock phase (CPHA) summarized in Table 1. Example waveforms for the different modes are shown in Figure 4.

Table 1. SPI Mode

CPOL	CPHA	SCK IDLE	DATA CAPTURED	DATA LAUNCHED
0	0	Low	Rising SCK	Falling SCK
0	1	Low	Falling SCK	Rising SCK
1	0	High	Falling SCK	Rising SCK
1	1	High	Rising SCK	Falling SCK

The DC2799A SPI extender can be inserted into an existing 8-bit word SPI mode (0,0) network with minimal impact. Write accesses to remove slave devices are software transparent; however, read accesses from remote slave devices incur a one-word latency and so require a compensating adjustment to the host software. In most cases, simply performing a dummy SPI read at the start of each read transaction is enough.

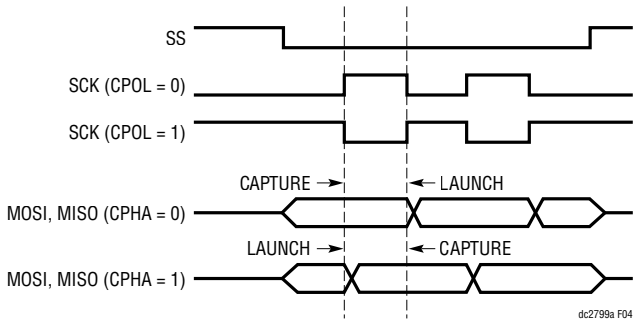


Figure 4. SPI Mode Waveform

When using the DC2799A with SPI modes other than (0,0) and/or an 8-bit word size, modifications to the host code will be required. These modifications will potentially include modifying the host's SPI mode as well configuring the LTC4332's configuration registers with the proper slave device mode and word sizes.

The DC2799A's local side supports either SPI mode (0,0) or (1,1). The host software will need to be configured to operate in one of these two modes. If a remote side device operates with a different SPI mode, the DC2799A may be configured to automatically convert between the configured remote mode and mode (0,0) or (1,1).

On the remote side, the DC2799A supports all SPI modes and allows different modes to be associated for each of the three remote side slaves. All remote side SPI modes are (0,0) by default. The SPI mode associated with each slave select is configured in the LTC4332's CONFIG register, address 0x00h. This register is accessed by reading from or writing to the local side LTC4332 using the $\overline{SSC}$ slave select which is available on the local side as pin 8 on J6 or pin 4 on J1. See the LTC4332 data sheet for details on the LTC4332's registers, including the register definition for CONFIG.

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Note that when reading from the local side LTC4332 using $\overline{SSC}$, there is no latency in the readback data and therefore the dummy read is not required.

The local side LTC4332's internal slave device uses 8-bit words; however, the DC2799A can allow remote device word sizes of any value within the range 8 ≤ WORD_LENGTH ≤ 32 by writing the desired remote size word length into the configuration register WORD_LENGTH, address 0x05h. The readback data from the remote side is delayed by WORD_LENGTH SCK's. Note that WORD_LENGTH is applied to all remote side devices. If the remote side devices have different word sizes, then WORD_LENGTH will need to be updated each time a remote device with a different word size is accessed. See the LTC4332 data sheet for additional details on the LTC4332's registers.

Supply Connections

The DC2799A is factory configured to operate the local and remote sides from the Pmod V_{CC} supply; however, turrets are provided to allow external supplies to be connected.

The DC2799A is factory configured to have the logic and transceiver supplies connected via the zero ohm resistors R1 and R2. Removing these resistors and providing external supplies allows the DC2799A to translate across different voltage domains for the logic and/or transceiver supplies. See the LTC4332 data sheet for details on the supply voltage ranges.

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