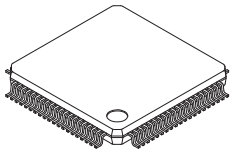
LC75886PW

1/4, 1/3-Duty LCD Driver with Key Input Function

ON Semiconductor®

www.onsemi.com



SQFP80 12x12 / SQFP80

Overview

The LC75886PW is 1/4 duty and 1/3 duty LCD display driver that can directly drive up to 224 segments and can control up to 5 general-purpose output ports. This product also incorporates a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wiring.

Features

- Key input function for up to 30 keys (A key scan is performed only when a key is pressed.)
- 1/4 duty 1/3 bias and 1/3 duty 1/3 bias drive schemes can be controlled from serial data.
- Capable of driving up to 224 segments using 1/4 duty and up to 171 segments using 1/3 duty.
- Switching between key scan output and segment output can be controlled from serial data.
- The key scan operation enabled/disabled state can be controlled from serial data.
- Switching between segment output port and general-purpose output port can be controlled from serial data.
- Switching between general-purpose output port, clock output port, and segment output port can be controlled from serial data.
  (Up to 5 general-purpose output ports and up to one clock output port)
- Serial data I/O supports CCB* format communication with the system controller. (Support 3.3 V and 5 V operation)
- Sleep mode and all segments off functions that are controlled from serial data.
- The frame frequency of the common and segment output waveforms can be controlled from serial data.
- Switching between RC oscillator operating mode and external clock operationg mode can be controlled from serial data.
- Direct display of display data without the use of a decoder provides high generality.
- Provision of an on-chip voltage-detection type reset circuit prevents incorrect displays.
- $\overline{\text{RES}}$ pin provided for forcibly initializing the IC internal circuits.

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 36 of this data sheet.

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July 2017 - Rev. 1

Publication Order Number :
LC75886PW/D

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	−0.3 to +7.0	V
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{RES}$	−0.3 to +7.0	V
	$V_{IN}2$	OSC, TEST, $V_{DD}1$, $V_{DD}2$, KI1 to KI5	−0.3 to V_{DD}+0.3	
Output voltage	$V_{OUT}1$	DO	−0.3 to +7.0	V
	$V_{OUT}2$	OSC, S1 to S57, COM1 to COM4, KS1 to KS6, P1 to P5	−0.3 to V_{DD}+0.3	
Output current	$I_{OUT}1$	S1 to S57	300	μA
	$I_{OUT}2$	COM1 to COM4	3	mA
	$I_{OUT}3$	KS1 to KS6	1	
	$I_{OUT}4$	P1 to P5	5	
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−55 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Ranges at Ta = −40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5		6.0	V
Input voltage	$V_{DD}1$	$V_{DD}1$		2/3V_{DD}	V_{DD}	V
	$V_{DD}2$	$V_{DD}2$		1/3V_{DD}	V_{DD}	
Input high level voltage	$V_{IH}1$	CE, CL, DI, $\overline{RES}$	0.4V_{DD}		6.0	V
	$V_{IH}2$	KI1 to KI5	0.6V_{DD}		V_{DD}	
	$V_{IH}3$	OSC: External clock operating mode	0.4V_{DD}		V_{DD}	
Input low level voltage	$V_{IL}1$	CE, CL, DI, $\overline{RES}$	0		0.2V_{DD}	V
	$V_{IL}2$	KI1 to KI5	0		0.2V_{DD}	
	$V_{IL}3$	OSC: External clock operating mode	0		0.2V_{DD}	
Recommended external resistor for RC oscillation	R_{OSC}	OSC: RC oscillation operating mode		39		kΩ
Recommended external capacitor for RC oscillation	C_{OSC}	OSC: RC oscillation operating mode		1000		pF
Guaranteed range of RC oscillation	f_{OSC}	OSC: RC oscillation operating mode	19	38	76	kHz
External clock operating frequency	f_{CK}	OSC: External clock operating mode [Figure4]	10	38	76	kHz
External clock duty cycle	D_{CK}	OSC: External clock operating mode [Figure4]	30	50	70	%
Data setup time	t_{ds}	CL, DI [Figure2], [Figure3]	160			ns
Data hold time	t_{dh}	CL, DI [Figure2], [Figure3]	160			ns
CE wait time	t_{cp}	CE, CL [Figure2], [Figure3]	160			ns
CE setup time	t_{cs}	CE, CL [Figure2], [Figure3]	160			ns
CE hold time	t_{ch}	CE, CL [Figure2], [Figure3]	160			ns
High level clock pulse width	$t_{\phi H}$	CL [Figure2], [Figure3]	160			ns
Low level clock pulse width	$t_{\phi L}$	CL [Figure2], [Figure3]	160			ns
Rise time	t_r	CE, CL, DI [Figure2], [Figure3]		160		ns
Fall time	t_f	CE, CL, DI [Figure2], [Figure3]		160		ns
DO output deley time	t_{dc}	DO R_{PU} = 4.7 kΩ C_L = 10 pF *1 [Figure2], [Figure3]			1.5	μs
DO rise time	t_{dr}	DO R_{PU} = 4.7 kΩ C_L = 10 pF *1 [Figure2], [Figure3]			1.5	μs

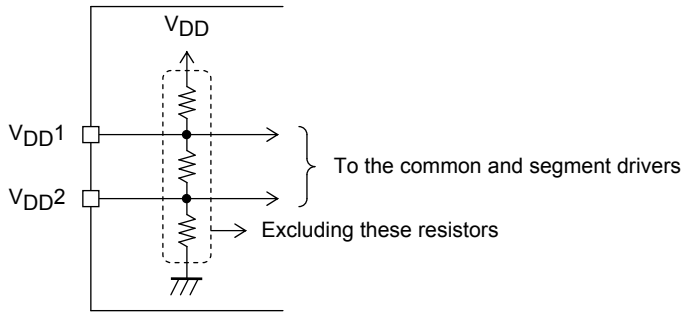
Note: *1 Since the DO pin is an open-drain output, these times depend on the values of the pull-up resistor R_{PU} and the load capacitance C_L.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Hysteresis	V_H1	CE, CL, DI, $\overline{RES}$			$0.03V_{DD}$		V
	V_H2	KI1 to KI5			$0.1V_{DD}$		
Power-down detection voltage	V_{DET}			2.0	2.3	2.6	V
Input high level current	$I_{IH}1$	CE, CL, DI, $\overline{RES}$	V_I = 6.0 V			5.0	μA
	$I_{IH}2$	OSC	$V_I = V_{DD}$: External clock operating mode			5.0	
Input low level current	$I_{IL}1$	CE, CL, DI, $\overline{RES}$	V_I = 0 V	−5.0			μA
	$I_{IL}2$	OSC	V_I = 0 V : External clock operating mode	−5.0			
Input floating voltage	V_{IF}	KI1 to KI5				$0.05V_{DD}$	V
Pull-down resistance	RPD	KI1 to KI5	V_{DD} = 5.0 V	50	100	250	kΩ
Output off leakage current	I_{OFFH}	DO	V_O = 6.0 V			6.0	μA
Output high level voltage	$V_{OH}1$	KS1 to KS6	I_O = −500 μA	V_{DD}−1.0	V_{DD}−0.5	V_{DD}−0.2	V
	$V_{OH}2$	P1 to P5	I_O = −1 mA	V_{DD}−0.9			
	$V_{OH}3$	S1 to S57	I_O = −20 μA	V_{DD}−0.9			
	$V_{OH}4$	COM1 to COM4	I_O = −100 μA	V_{DD}−0.9			
Output low level voltage	$V_{OL}1$	KS1 to KS6	I_O = 25 μA	0.2	0.5	1.5	V
	$V_{OL}2$	P1 to P5	I_O = 1 mA			0.9	
	$V_{OL}3$	S1 to S57	I_O = 20 μA			0.9	
	$V_{OL}4$	COM1 to COM4	I_O = 100 μA			0.9	
	$V_{OL}5$	DO	I_O = 1 mA		0.1	0.3	
Output middle level voltage *2	$V_{MID}1$	S1 to S57	1/3 bias I_O = ±20 μA	$2/3V_{DD}$ −0.9		$2/3V_{DD}$ +0.9	V
	$V_{MID}2$	S1 to S57	1/3 bias I_O = ±20 μA	$1/3V_{DD}$ −0.9		$1/3V_{DD}$ +0.9	
	$V_{MID}3$	COM1 to COM4	1/3 bias I_O = ±100 μA	$2/3V_{DD}$ −0.9		$2/3V_{DD}$ +0.9	
	$V_{MID}4$	COM1 to COM4	1/3 bias I_O = ±100 μA	$1/3V_{DD}$ −0.9		$1/3V_{DD}$ +0.9	
Oscillator frequency	f_{OSC}	OSC	R_{OSC} = 39 kΩ, C_{OSC} = 1000 pF RC oscillation operating mode	30.4	38	45.6	kHz
Current drain	$I_{DD}1$	V_{DD}	Sleep mode			100	μA
	$I_{DD}2$	V_{DD}	V_{DD} = 6.0 V, Output open, RC oscillation operating mode, f_{OSC} = 38 kHz		450	900	
	$I_{DD}3$	V_{DD}	V_{DD} = 6.0 V, Output open, External clock operating mode, f_{CK} = 38 kHz, $V_{IH}3 = 0.5V_{DD}$, $V_{IL}3 = 0.1V_{DD}$		550	1100	

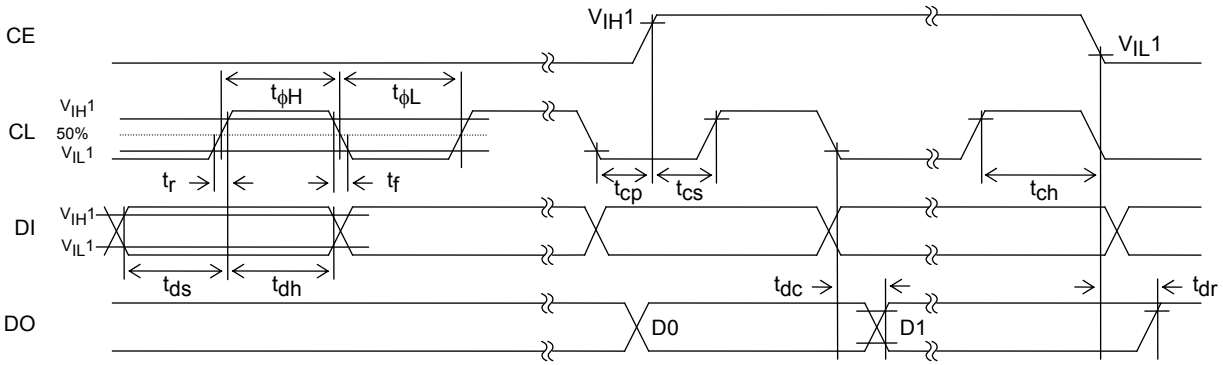
Note: *2. Excluding the bias voltage generation divider resistor built into the $V_{DD}1$ and $V_{DD}2$. (See [Figure 1])



[Figure 1]

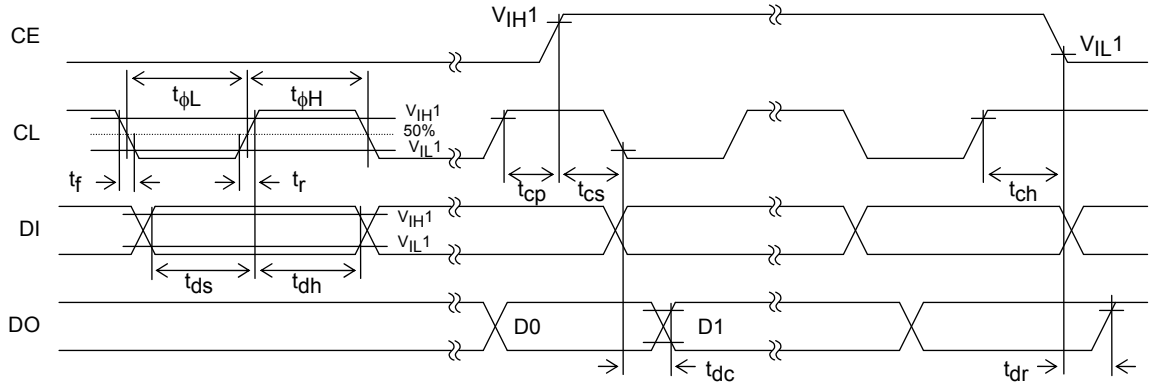
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. When CL is stopped at the low level



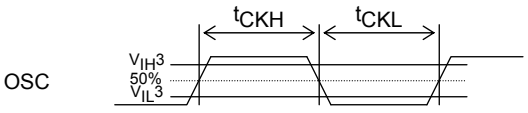
[Figure 2]

2. When CL is stopped at the high level



[Figure 3]

3. OSC pin clock timing in external clock operating mode



[Figure 4]

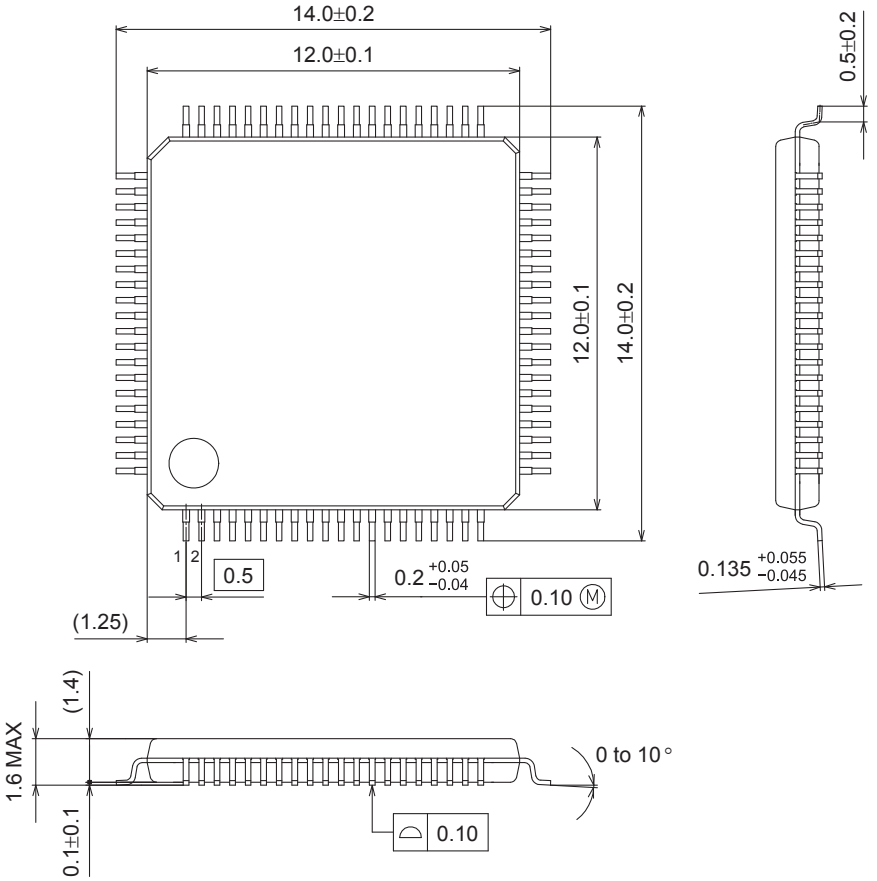
$$f_{CK} = \frac{1}{t_{CKH} + t_{CKL}} \quad [kHz]$$

$$D_{CK} = \frac{t_{CKH}}{t_{CKH} + t_{CKL}} \times 100[\%]$$

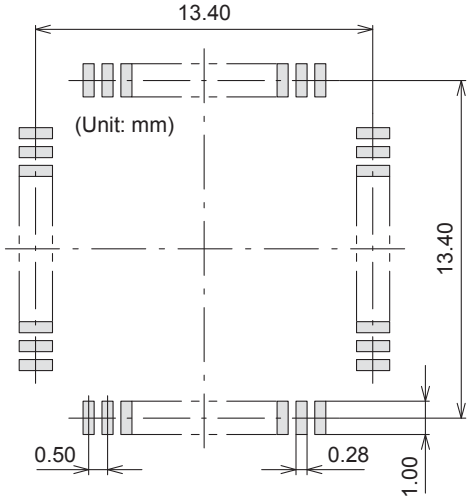
Package Dimensions

unit : mm

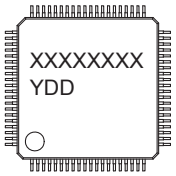
SPQFP80 12x12 / SQFP80
CASE 131AL
ISSUE A



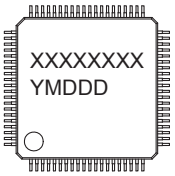
SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
DD = Additional Traceability Data



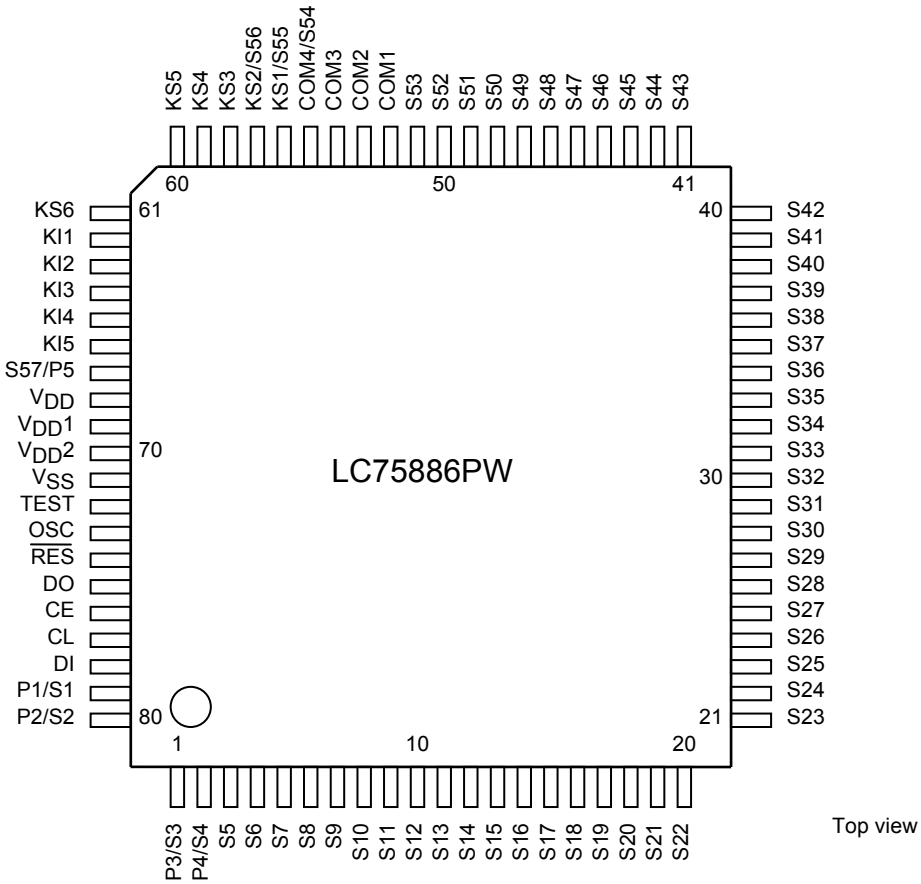
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “ ▪ ”, may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

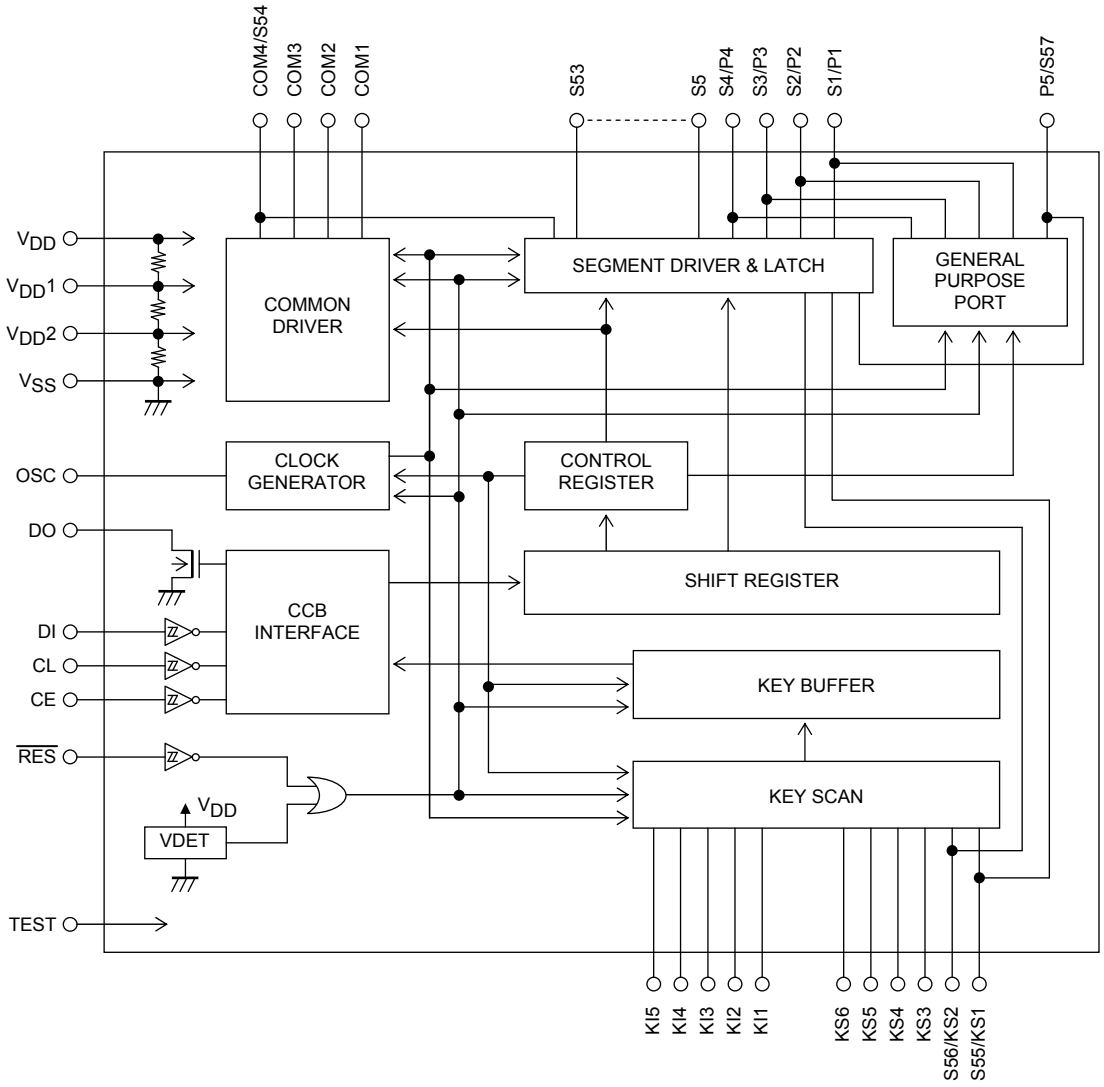
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin Assignment



Top view

Block Diagram



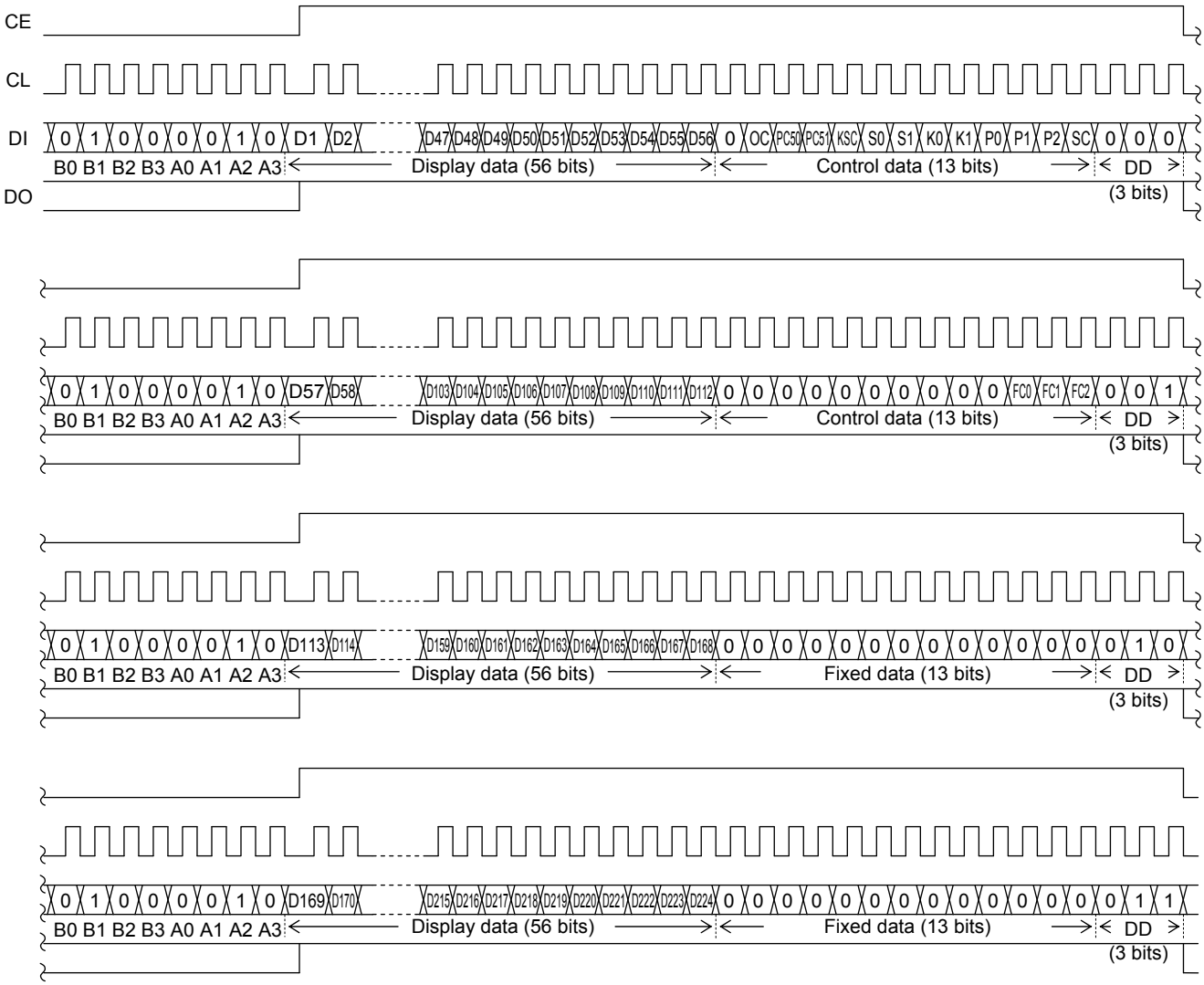
Pin Functions

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S1/P1 to S4/P4 S5 to S53	79,80,1,2 3 to 51	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S4/P4 pins can be used as general-purpose output ports under serial data control.	-	O	OPEN
COM1 to COM3 COM4/S54	52 to 54 55	Common driver outputs. The frame frequency is f_O[Hz]. The COM4/S54 pin can be used as a segment output in 1/3 duty.	-	O	OPEN
KS1/S55 KS2/S56 KS3 to KS6	56 57 58 to 61	Key scan outputs. Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S55 and KS2/S56 pins can be used as segment outputs when so specified by the control data.	-	O	OPEN
KI1 to KI5	62 to 66	Key scan inputs. These pins have built-in pull-down resistors.	H	I	GND
P5/S57	67	General-purpose output port. This pin can be used as clock output port or segment output port under serial data control.	-	O	OPEN
OSC	73	Oscillator connections. An oscillator circuit is formed by connecting an external resistor and capacitor at this pin. This pin can also be used as the external clock input pin if the external clock operating mode is selected with the control data.	-	I/O	V_{DD}
CE CL DI DO	76 77 78 75	Serial data interface connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor. CE: Chip enable CL: Synchronization clock DI: Transfer data DO: Output data	H ↑ - -	I I I O	GND GND GND OPEN
$\overline{RES}$	74	Reset signal input • $\overline{RES}$=Low ···· Display off - S1/P1 to S4/P4, KS1/S55, KS2/S56=Low (These pins are forcibly set to the segment output port function and fixed at the low level.) - S5 to S53=Low - COM1 to COM3=Low - COM4/S54=Low (This pin is forcibly set to the common output function and fixed at the low level.) - P5/S57=Low (This pin is forcibly set to the general-purpose output port function and fixed at the low level.) - KS3 to KS6=Low - Key scanning disabled - All the key data is reset to low. - OSC="Z"(High impedance) - RC oscillation stopped - Inhibits external clock input • $\overline{RES}$=High ··· Display on - General-purpose output port state setting is enabled - Key scanning is enabled. - RC oscillation enabled (RC oscilltator operating mode) - Enables external clock input (external clock operating mode) However, serial data can be transferred when the $\overline{RES}$ pin is low	L	I	V_{DD}
TEST	72	This pin must be connected to ground.	-	I	-
$V_{DD}1$	69	Used to apply the LCD drive 2/3 bias voltage externally.	-	I	OPEN
$V_{DD}2$	70	Used to apply the LCD drive 1/3 bias voltage externally.	-	I	OPEN
V_{DD}	68	Power supply connections. Provide a voltage of between 4.5 to 6.0 V.	-	-	-
V_{SS}	71	Power supply connections. Connect to ground.	-	-	-

Serial Data Input

1. 1/4 duty

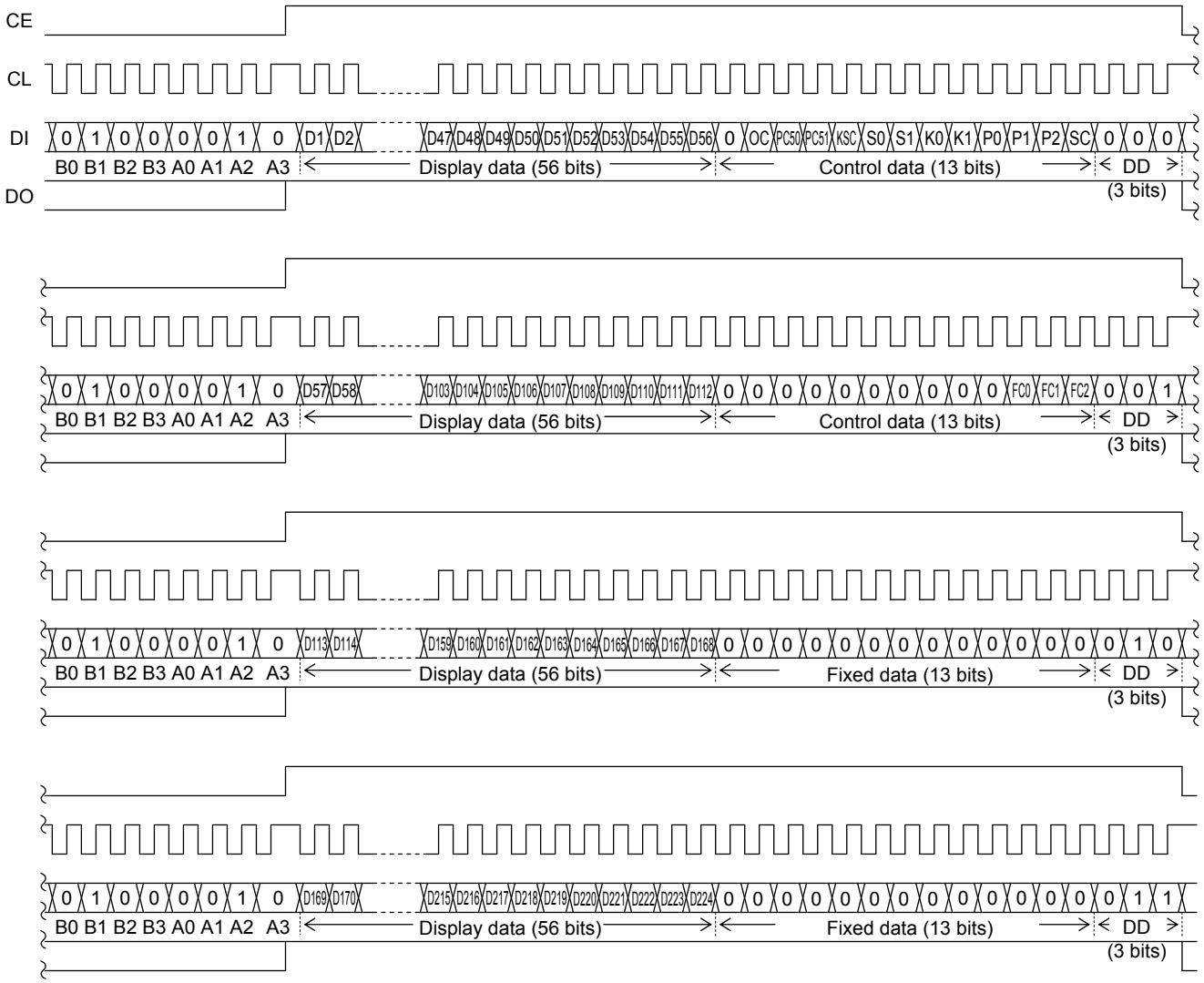
(1) When CL is stopped at the low level



Note: B0 to B3, A0 to A3 ····· CCB address

DD ····· Direction data

(2) When CL is stopped at the high level

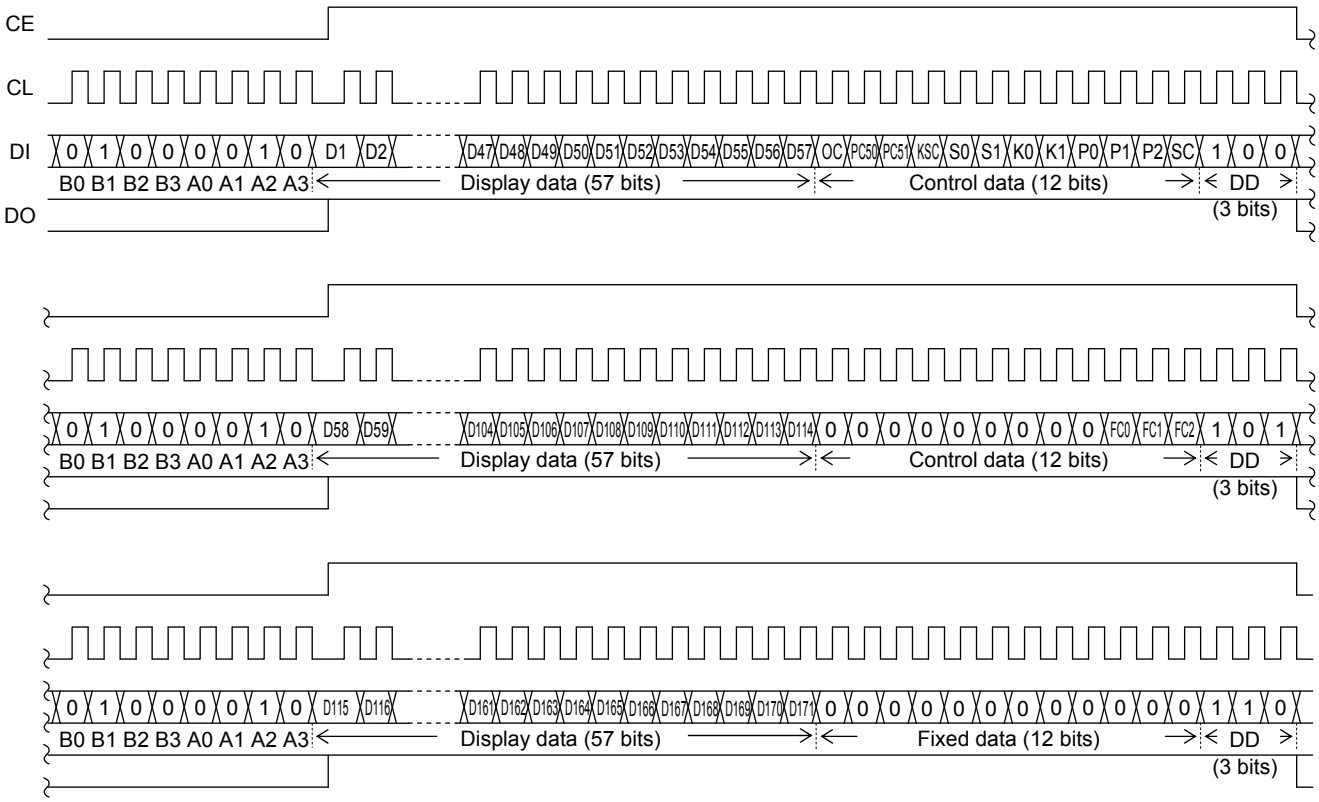


Note: B0 to B3, A0 to A3 ····· CCB address
DD ····· Direction data

- CCB address ····· "42H"
- D1 to D224 ····· Display data
- OC ····· RC oscillator operating mode/external clock operationg mode switching control data
- PC50, PC51 ····· General-purpose output port/clock output port/segment output port switching control data
- KSC ····· Key scan operation enabled/disabled state setting control data
- S0, S1 ····· Sleep control data
- K0, K1 ····· Key scan output/segment output switching control data
- P0 to P2 ····· Segment output port/general-purpose output port switching control data
- SC ····· Segment on/off control data
- FC0 to FC2 ····· Common and segment output waveform frame frequency control data

2. 1/3 duty

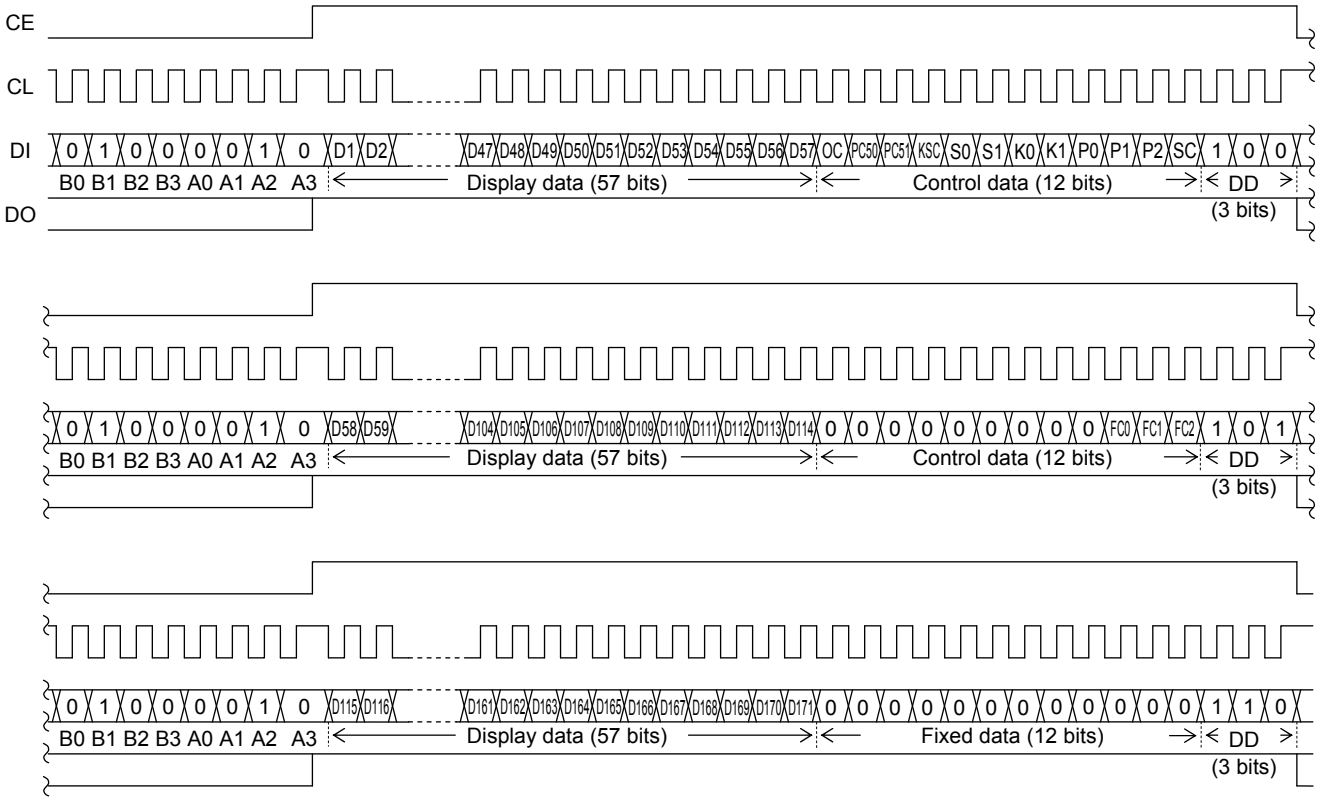
(1) When CL is stopped at the low level



Note: B0 to B3, A0 to A3 ·····CCB address

DD ·····Direction data

(2) When CL is stopped at the high level



Note: B0 to B3, A0 to A3 ····· CCB address
DD ····· Direction data

- CCB address ·····"42H"
- D1 to D171 ·····Display data
- OC ·····RC oscillator operating mode/external clock operationg mode switching control data
- PC50, PC51 ·····General-purpose output port/clock output port/segment output port switching control data
- KSC ·····Key scan operation enabled/disabled state setting control data
- S0, S1 ·····Sleep control data
- K0, K1 ·····Key scan output/segment output switching control data
- P0 to P2 ·····Segment output port/general-purpose output port switching control data
- SC ·····Segment on/off control data
- FC0 to FC2 ·····Common and segment output waveform frame frequency control data

Control Data Functions

1. OC … RC oscillator operating mode/external clock operating mode switching control data

This control data bit selects the OSC pin function (RC oscillator operating mode or external clock operating mode)

OC	OSC pin function
0	RC oscillator operating mode
1	External clock operating mode

Note: If RC oscillator operating mode is selected, connect an external resistor R_{OSC} and an external capacitor C_{OSC} to the OSC pin.

2. PC50, PC51 … General-purpose output port/clock output port/segment output port switching control data

These control data bits swithes the functions of the P5/S57 output pin between the general-purpose output port, the clock output port, and the segment output port.

Control data		The state of P5/S57 output pin
PC50	PC51	
0	0	General-purpose output port (P5) (”L” level output)
1	0	General-purpose output port (P5) (“H” level output)
0	1	Clock output port (P5) (Clock frequency is $f_{OSC}/2$ or $f_{CK}/2$)
1	1	Segment output port (S57)

Note: If the sleep mode is set, the P5/S57 output pin can not be used as the clock output port.

3. KSC … Key scan operation enabled/disabled state setting control data

This control data bit enables or disables key scan operation.

KSC	Key scan operating state
0	Key scan operation enabled (A key scan operation is performed if any key on the lines corresponding to KS1 to KS6 pin which is set high is pressed.)
1	Key scan operation disabled (No key scan operation is performed, even if any of the keys in the key matrix are pressed. If this state is set up, the key data is forcibly reset to 0 and the key data read request is also cleared. (DO is set high.))

4. S0, S1 … Sleep control data

These control data bits switch between normal mode and sleep mode, and set the states of the KS1 to KS6 key scan output during key scan standby.

Control data		Mode	OSC pin state (RC oscillator or acceptance of the external clock signal)	Segment output / Common output	Output pin states during key scan standby					
S0	S1				KS1	KS2	KS3	KS4	KS5	KS6
0	0	Normal	Operating	Operating	H	H	H	H	H	H
0	1	Sleep	Stopped	L	L	L	L	L	L	H
1	0	Sleep	Stopped	L	L	L	L	L	H	H
1	1	Sleep	Stopped	L	H	H	H	H	H	H

Note: This assumes that the KS1/S55 and KS2/S56 output pins are selected for key scan output.

5. K0, K1 … Key scan output/segment output switching control data

These control data bits switch the functions of the KS1/S55 and KS2/S56 output pins between the key scan output and the segment output.

Control data		Output pin state		Maximum number of input keys
K0	K1	KS1/S55	KS2/S56	
0	0	KS1	KS2	30
0	1	S55	KS2	25
1	X	S55	S56	20

Note: KSn (n=1 or 2): Key scan output
Sn (n=55 or 56): Segment output

X : don't care

6. P0 to P2 … Segment output port/general-purpose output port switching control data

These control data bits switch the functions of the S1/P1 to S4/P4 output pins between the segment output port and the general-purpose output port.

Control data			Output pin state			
P0	P1	P2	S1/P1	S2/P2	S3/P3	S4/P4
0	0	0	S1	S2	S3	S4
0	0	1	P1	S2	S3	S4
0	1	0	P1	P2	S3	S4
0	1	1	P1	P2	P3	S4
1	0	0	P1	P2	P3	P4

Note: Sn (n=1 to 4): Segment output port
Pn (n=1 to 4): General-purpose output port

The table below lists the correspondence between the display data and the output pins when these pins are selected to be general-purpose output ports.

Output pin	Correspondence display data	
	1/4 duty	1/3 duty
S1/P1	D1	D1
S2/P2	D5	D4
S3/P3	D9	D7
S4/P4	D13	D10

For example, if the circuit is operated in 1/4 duty and the S4/P4 output pin is selected to be a general-purpose output port, the S4/P4 output pin will output a high level when the display data D13 is 1, and will output a low level when D13 is 0.

7. SC … Segment on/off control data

This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

8. FC0 to FC2 … Common and segment output waveform frame frequency control data

These control data bits set the common and segment output waveform frequency.

Control data			Frame frequency f_O[Hz]
FC0	FC1	FC2	
1	1	0	$f_{OSC}/768$, $f_{CK}/768$
1	1	1	$f_{OSC}/576$, $f_{CK}/576$
0	0	0	$f_{OSC}/384$, $f_{CK}/384$
0	0	1	$f_{OSC}/288$, $f_{CK}/288$
0	1	0	$f_{OSC}/192$, $f_{CK}/192$

Display Data and Output Pin Correspondence

1. 1/4 duty

Output pin	COM1	COM2	COM3	COM4
S1/P1	D1	D2	D3	D4
S2/P2	D5	D6	D7	D8
S3/P3	D9	D10	D11	D12
S4/P4	D13	D14	D15	D16
S5	D17	D18	D19	D20
S6	D21	D22	D23	D24
S7	D25	D26	D27	D28
S8	D29	D30	D31	D32
S9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S25	D97	D98	D99	D100
S26	D101	D102	D103	D104
S27	D105	D106	D107	D108
S28	D109	D110	D111	D112

Output pin	COM1	COM2	COM3	COM4
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
S32	D125	D126	D127	D128
S33	D129	D130	D131	D132
S34	D133	D134	D135	D136
S35	D137	D138	D139	D140
S36	D141	D142	D143	D144
S37	D145	D146	D147	D148
S38	D149	D150	D151	D152
S39	D153	D154	D155	D156
S40	D157	D158	D159	D160
S41	D161	D162	D163	D164
S42	D165	D166	D167	D168
S43	D169	D170	D171	D172
S44	D173	D174	D175	D176
S45	D177	D178	D179	D180
S46	D181	D182	D183	D184
S47	D185	D186	D187	D188
S48	D189	D190	D191	D192
S49	D193	D194	D195	D196
S50	D197	D198	D199	D200
S51	D201	D202	D203	D204
S52	D205	D206	D207	D208
S53	D209	D210	D211	D212
KS1/S55	D213	D214	D215	D216
KS2/S56	D217	D218	D219	D220
P5/S57	D221	D222	D223	D224

Note: This is for the case where the S1/P1 to S4/P4, KS1/S55, KS2/S56, P5/S57 output pins are selected for use as segment outputs.

For example, the table below lists the segment output states for the S11 output pin.

Display data				Output pin state (S11)
D41	D42	D43	D44	
0	0	0	0	The LCD segments for COM1, COM2, COM3 and COM4 are off.
0	0	0	1	The LCD segment for COM4 is on.
0	0	1	0	The LCD segment for COM3 is on.
0	0	1	1	The LCD segments for COM3 and COM4 are on.
0	1	0	0	The LCD segment for COM2 is on.
0	1	0	1	The LCD segments for COM2 and COM4 are on.
0	1	1	0	The LCD segments for COM2 and COM3 are on.
0	1	1	1	The LCD segments for COM2, COM3 and COM4 are on.
1	0	0	0	The LCD segment for COM1 is on.
1	0	0	1	The LCD segments for COM1 and COM4 are on.
1	0	1	0	The LCD segments for COM1 and COM3 are on.
1	0	1	1	The LCD segments for COM1, COM3 and COM4 are on.
1	1	0	0	The LCD segments for COM1 and COM2 are on.
1	1	0	1	The LCD segments for COM1, COM2 and COM4 are on.
1	1	1	0	The LCD segments for COM1, COM2 and COM3 are on.
1	1	1	1	The LCD segments for COM1, COM2, COM3 and COM4 are on.

2. 1/3 duty

Output pin	COM1	COM2	COM3
S1/P1	D1	D2	D3
S2/P2	D4	D5	D6
S3/P3	D7	D8	D9
S4/P4	D10	D11	D12
S5	D13	D14	D15
S6	D16	D17	D18
S7	D19	D20	D21
S8	D22	D23	D24
S9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D86	D87
S30	D88	D89	D90

Output pin	COM1	COM2	COM3
S31	D91	D92	D93
S32	D94	D95	D96
S33	D97	D98	D99
S34	D100	D101	D102
S35	D103	D104	D105
S36	D106	D107	D108
S37	D109	D110	D111
S38	D112	D113	D114
S39	D115	D116	D117
S40	D118	D119	D120
S41	D121	D122	D123
S42	D124	D125	D126
S43	D127	D128	D129
S44	D130	D131	D132
S45	D133	D134	D135
S46	D136	D137	D138
S47	D139	D140	D141
S48	D142	D143	D144
S49	D145	D146	D147
S50	D148	D149	D150
S51	D151	D152	D153
S52	D154	D155	D156
S53	D157	D158	D159
COM4/S54	D160	D161	D162
KS1/S55	D163	D164	D165
KS2/S56	D166	D167	D168
P5/S57	D169	D170	D171

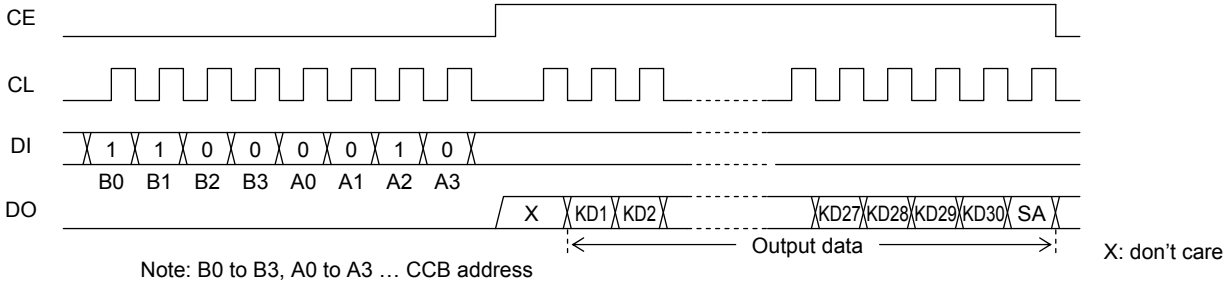
Note: This is for the case where the S1/P1 to S4/P4, COM4/S54, KS1/S55, KS2/S56, P5/S57 output pins are selected for use as segment outputs.

For example, the table below lists the segment output states for the S11 output pin.

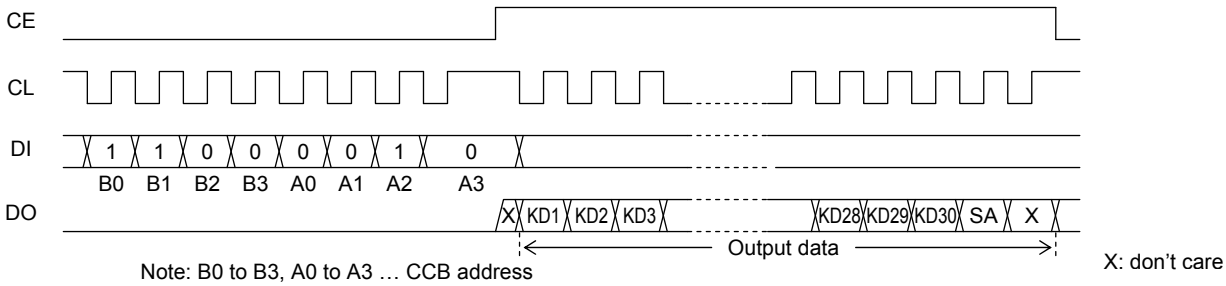
Display data			Output pin state (S11)
D31	D32	D33	
0	0	0	The LCD segments for COM1, COM2, and COM3 are off.
0	0	1	The LCD segment for COM3 is on.
0	1	0	The LCD segment for COM2 is on.
0	1	1	The LCD segments for COM2 and COM3 are on.
1	0	0	The LCD segment for COM1 is on.
1	0	1	The LCD segments for COM1 and COM3 are on.
1	1	0	The LCD segments for COM1 and COM2 are on.
1	1	1	The LCD segments for COM1, COM2 and COM3 are on.

Serial Data Output

1. When CL is stopped at the low level



2. When CL is stopped at the high level



- CCB address ···· "43H"
- KD1 to KD30 ··· Key data
- SA ·····Sleep acknowledge data

Note: <u>If a key data read operation is executed when DO is high (DO does not generate a key data read request output), the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.</u>

Output Data

1. KD1 to KD30 … Key data

When a key matrix of up to 30 keys is formed from the KS1 to KS6 output pins and KI1 to KI5 input pins and one of those keys is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

	KI1	KI2	KI3	KI4	KI5
KS1/S55	KD1	KD2	KD3	KD4	KD5
KS2/S56	KD6	KD7	KD8	KD9	KD10
KS3	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25
KS6	KD26	KD27	KD28	KD29	KD30

When the KS1/S55 and KS2/S56 output pins are selected to be segment outputs by control data bits K0 and K1 and a key matrix of up to 20 keys is formed using the KS3 to KS6 output pins and the KI1 to KI5 input pins, the KD1 to KD10 key data bits will be set to 0.

2. SA … Sleep acknowledge data

This output data bit is set to the state when the key was pressed. Also, while DO will be low in this case, if serial data is input and the mode is set (to normal or sleep mode) during this period, that mode will be set. SA will be 1 in sleep mode and 0 in normal mode.

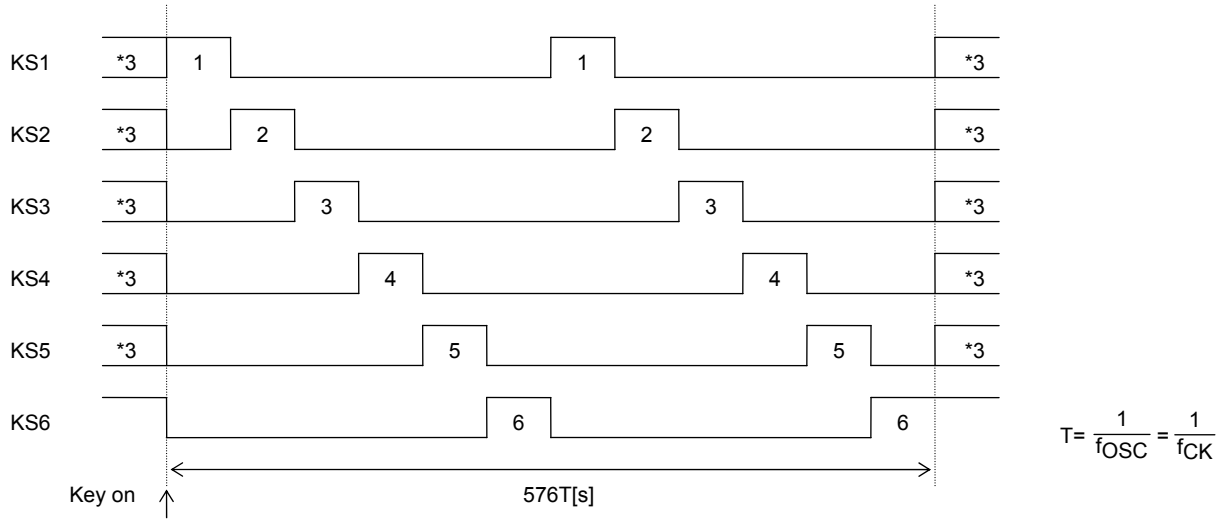
Sleep Mode Functions

Sleep mode is set up by setting S0 or S1 in the control data to 1. When sleep mode is set up, both the segment and common outputs will go to the low level. In RC oscillator operating mode (OC=0), the oscillator on the OSC pin will stop (although it will operate during key scan operations), and in exeternal clock operating mode (OC=1), acceptance of the external clock signal on the OSC pin will stop (although the clock signal will be accepted during key scan operations). Thus this mode reduces power consumption. However, the S1/P1 to S4/P4, P5/S57 output pins can be used as general-purpose output ports under control of the P0 to P2, PC50 and PC51 bits in the control data even in sleep mode (The P5/S57 output pin can not be used as clock output port). Sleep mode is cancelled by setting both S0 and S1 in control data to 0.

Key Scan Operation Functions

1. Key scan timing

   The key scan period is 288T[s]. To reliably determine the on/off state of the keys, the LC75886PW scans the keys twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request (a low level on DO) 615T[s] after starting a key scan. If the key data does not agree and a key was pressed at that point, it scans the keys again. Thus the LC75886PW cannot detect a key press shorter than 615T[s].



Note: *3. These are set to the high or low level by the S0 and S1 bits in the control data.
Key scan output signals are not output from pins that are set to the low level.

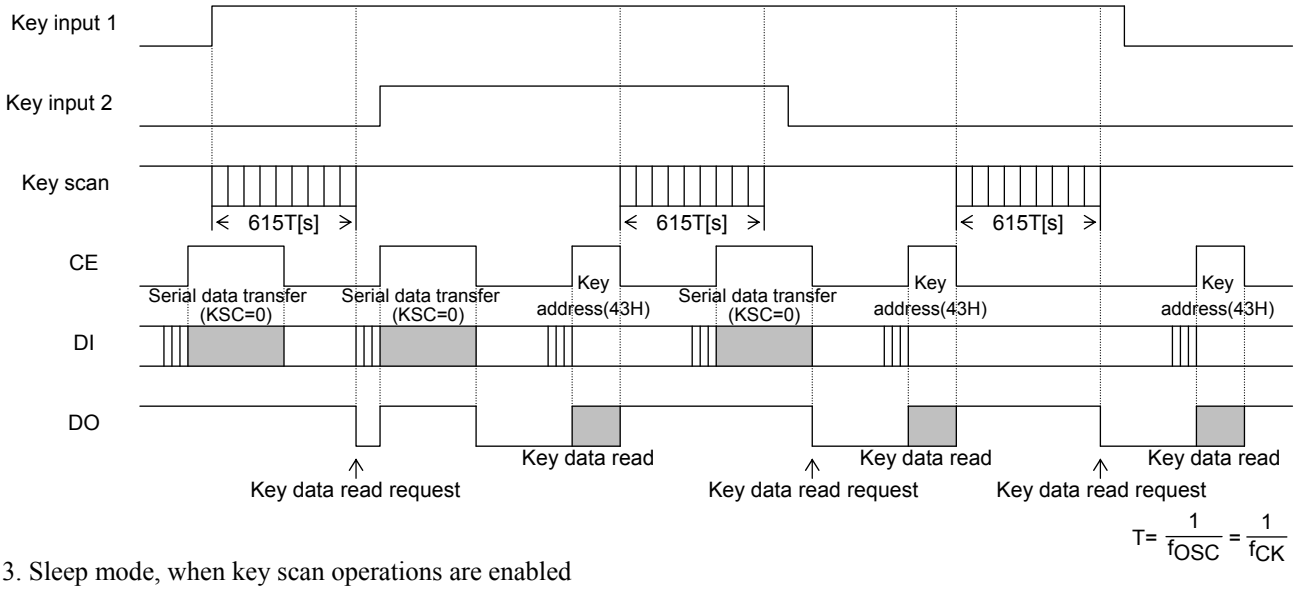
2. Normal mode, when key scan operations are enabled

(1) The KS1 to KS6 pins are set high. (See the description of the control data.)

(2) When a key is pressed, a key scan is started and the keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.

(3) If a key is pressed for longer than 615T[s] (Where $T=1/f_{OSC}$ or $T=1/f_{CK}$), the LC75886PW outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.

(4) After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75886PW performs another key scan. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 and 10 kΩ).



$$T=\frac{1}{f_{OSC}}=\frac{1}{f_{CK}}$$

3. Sleep mode, when key scan operations are enabled

(1) The KS1 to KS6 pins are set to high or low level by the S0 and S1 bits in the control data.
(See the description of the control data.)

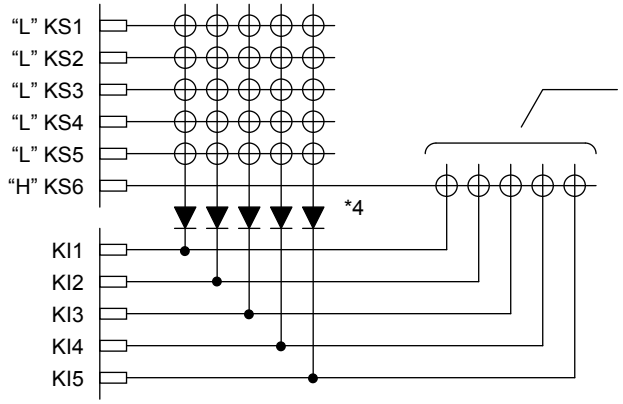
(2) If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, the oscillator on the OSC pins starts in RC oscillator operating mode (the IC starts accepting the external clock signal in external clock operating mode) and a key scan is performed. Keys are scanned until all keys are released.
Multiple key presses are recognized by determining whether multiple key data bits are set.

(3) If a key is pressed for longer than 615T[s] (Where $T=1/f_{OSC}$ or $T=1/f_{CK}$), the LC75886PW outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.

(4) After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75886PW performs another key scan. However, this does not clear sleep mode. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 and 10 kΩ).

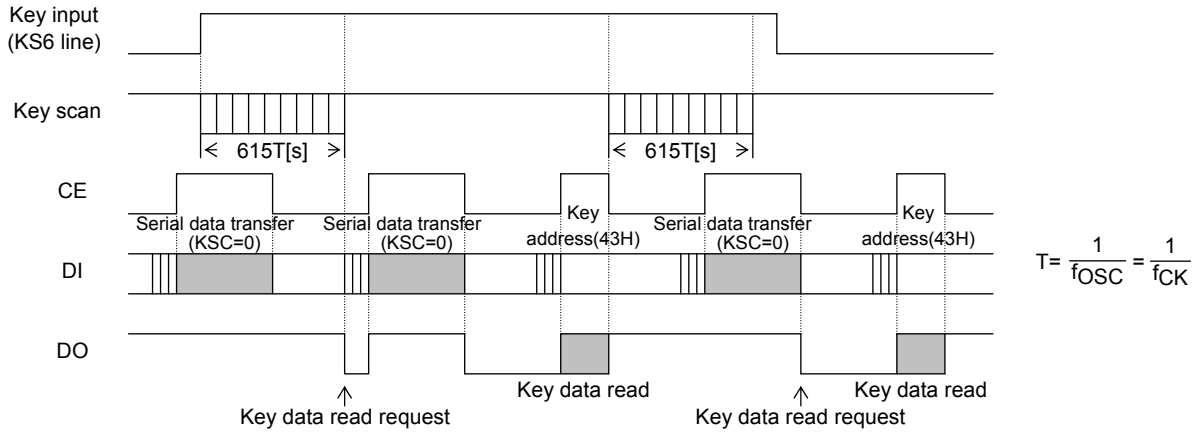
(5) Sleep mode key scan example

Example: S0=0, S1=1 (Sleep with only KS6 high)

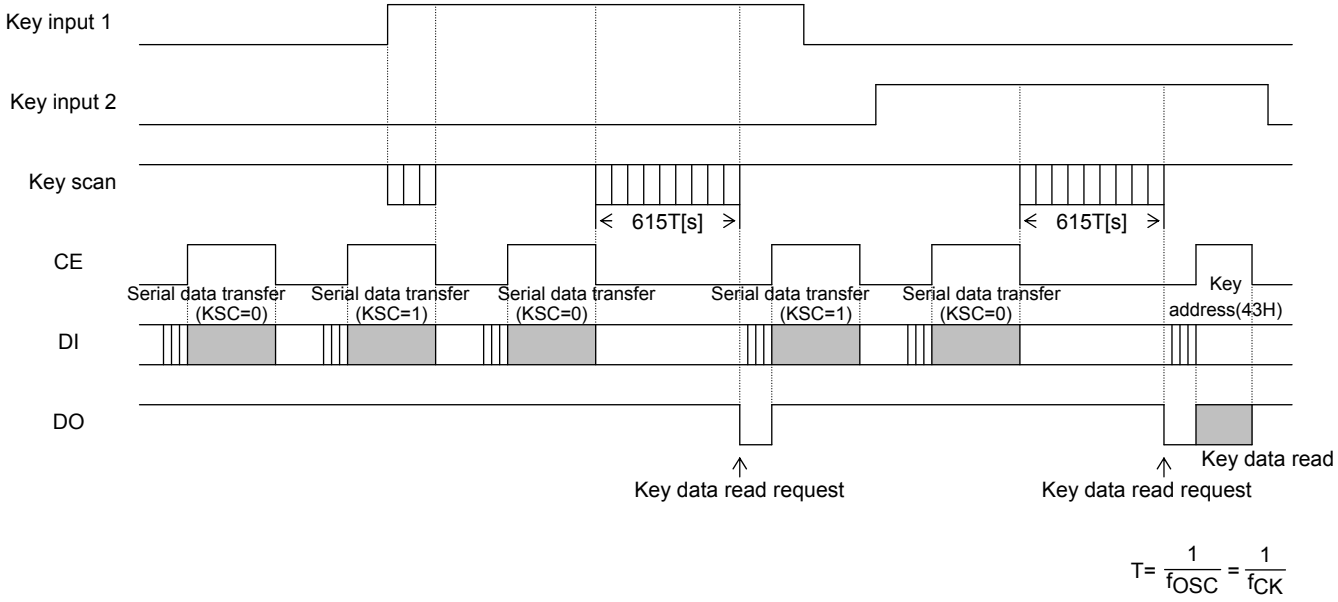


When any one of these keys is pressed, the oscillator on the OSC pins starts in RC oscillator operating mode (the IC starts accepting the external clock signal in external clock operating mode) and a key scan operation is performed.

Note: *4. These diodes are required to reliably recognize multiple key presses on the KS6 line when sleep mode state with only KS6 high, as in the above example. That is, these diodes prevent incorrect operations due to sneak currents in the KS6 key scan output signal when keys on the KS1 to KS5 lines are pressed at the same time.



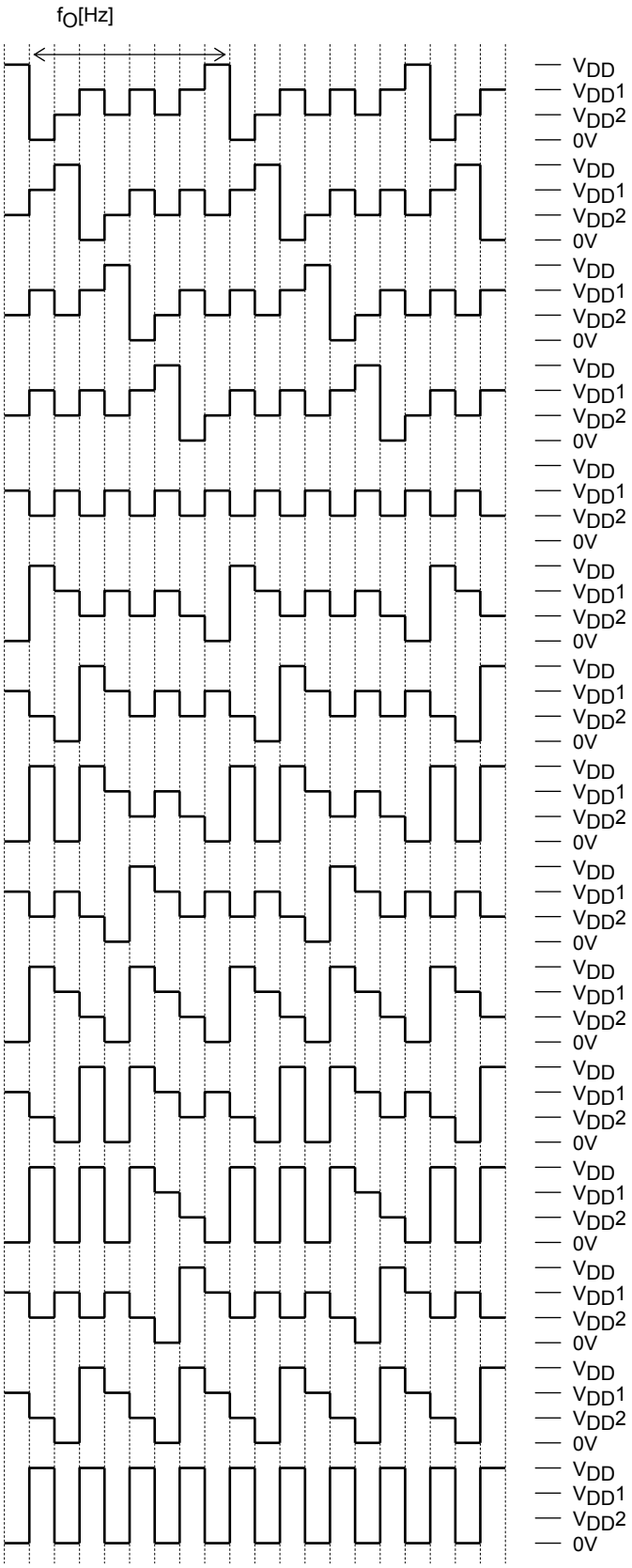
4. Normal/sleep mode, when key scan operations are disabled
(1) The KS1 to KS6 pins are set to high or low level by the S0 and S1 bits in the control data.
(2) No key scan operation is performed, whichever key is pressed.
(3) If the key scan disabled state (KSC=1 in the control data) is set during a key scan, the key scan is stopped.
(4) If the key scan disabled state (KSC=1 in the control data) is set when a key data read request (a low level on DO) is output to the controller, all the key data is set to 0 and the key data read request is cleared (DO is set high).
Note that DO, being an open-drain output, requires a pull-up resister (between 1 to 10 kΩ).
(5) The key scan disabled state is cleared by setting KSC in the control data to 0.



Multiple Key Presses

Although the LC75886PW is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KI1 to KI5 input pin lines, or multiple key presses on the KS1 to KS6 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed. Therefore, a diode must be inserted in series with each key. Applications that do not recognize multiple key presses of three or more keys should check the key data for three or more 1 bits and ignore such data.

1/4 Duty, 1/3 Bias Drive Technique



LCD driver output when all LCD segments corresponding to COM1, COM2, COM3, and COM4 are turned off.

LCD driver output when only LCD segments corresponding to COM1 are on.

LCD driver output when only LCD segments corresponding to COM2 are on.

LCD driver output when LCD segments corresponding to COM1 and COM2 are on.

LCD driver output when only LCD segments corresponding to COM3 are on.

LCD driver output when LCD segments corresponding to COM1 and COM3 are on.

LCD driver output when LCD segments corresponding to COM2 and COM3 are on.

LCD driver output when LCD segments corresponding to COM1, COM2, and COM3 are on.

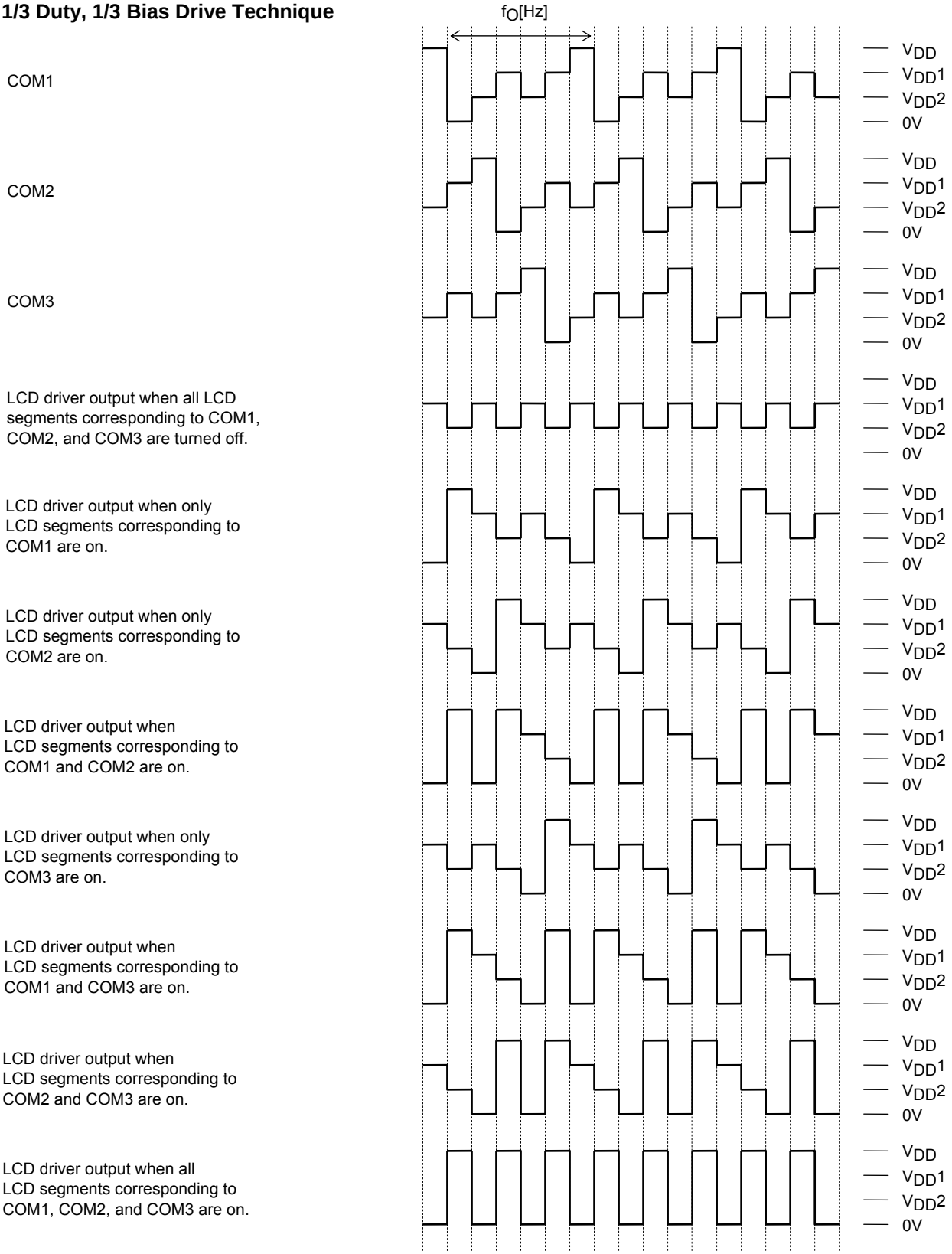
LCD driver output when only LCD segments corresponding to COM4 are on.

LCD driver output when LCD segments corresponding to COM2 and COM4 are on.

LCD driver output when all LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.

Control data			Common and segment output waveform frame frequency f_O[Hz]
FC0	FC1	FC2	
1	1	0	$f_{OSC}/768$, $f_{CK}/768$
1	1	1	$f_{OSC}/576$, $f_{CK}/576$
0	0	0	$f_{OSC}/384$, $f_{CK}/384$
0	0	1	$f_{OSC}/288$, $f_{CK}/288$
0	1	0	$f_{OSC}/192$, $f_{CK}/192$

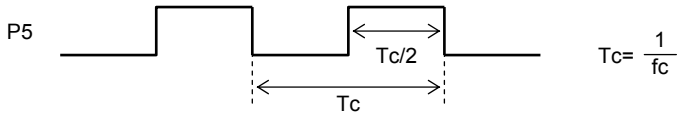
1/3 Duty, 1/3 Bias Drive Technique



Control data			Common and segment output waveform frame frequency f_O[Hz]
FC0	FC1	FC2	
1	1	0	$f_{OSC}/768$, $f_{CK}/768$
1	1	1	$f_{OSC}/576$, $f_{CK}/576$
0	0	0	$f_{OSC}/384$, $f_{CK}/384$
0	0	1	$f_{OSC}/288$, $f_{CK}/288$
0	1	0	$f_{OSC}/192$, $f_{CK}/192$

Clock Signal Output Waveform

Control data		The state of P5/S57 output pin
PC50	PC51	
0	1	Clock output port (P5) (Clock frequency is $f_{OSC}/2$ or $f_{CK}/2$)



Voltage Detection Type Reset Circuit (V_{DET})

This circuit generates an output signal and resets the system when power is first applied and when the voltage drops, i.e., when the power supply voltage is less than or equal to the power down detection voltage V_{DET}, which is 2.3 V, typical. To assure that this function operates reliably, a capacitor must be added to the power supply line so that the power supply voltage V_{DD} rise time when the power is first applied and the power supply voltage V_{DD} fall time when the voltage drops are both at least 1ms. (See Figure 5 and Figure 6.)

System Reset

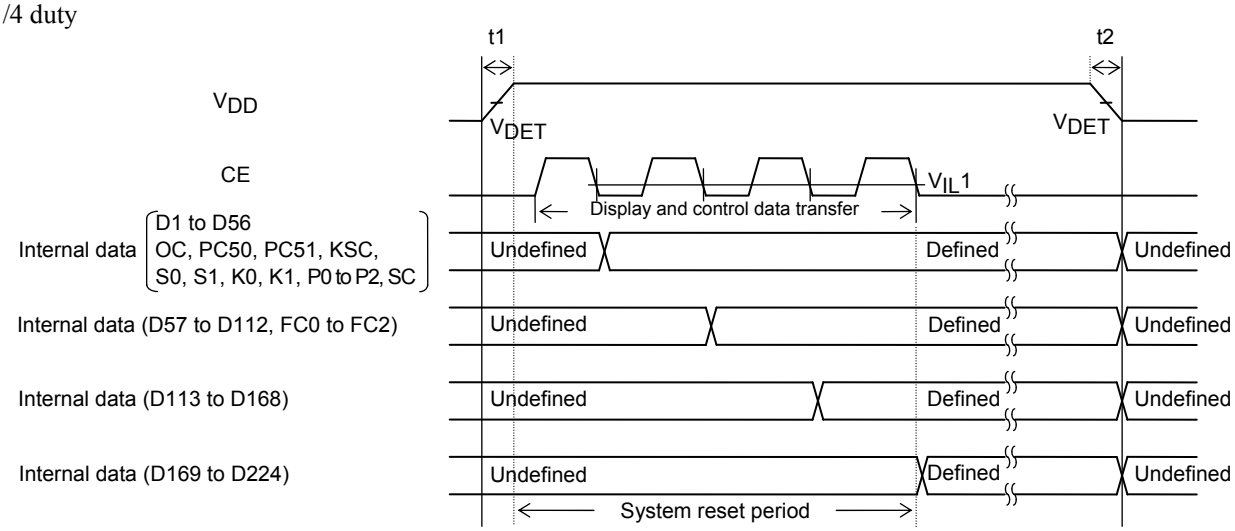
The LC75886PW supports the reset methods described below. When a system reset is applied, display is turned off, key scanning is stopped, all the key data is reset to low, and the general-purpose output ports are fixed at the low level (The S1/P1 to S4/P4 pins are forcibly set to the segment output port function and fixed at the low level. The P5/S57 pin is forcibly set to the general-purpose output port function and fixed at the low level). When the reset is cleared, display is turned on, key scanning is enabled and the general-purpose output ports state setting is enabled.

1. Reset methods

(1) Reset method by the voltage detection type reset circuit (V_{DET})

If at least 1ms is assured as the supply voltage V_{DD} rise time when power is applied, a system reset will be applied by the V_{DET} output signal when the supply voltage is brought up. If at least 1 ms is assured as the supply voltage V_{DD} fall time when power drops, a system reset will be applied in the same manner by the V_{DET} output signal when the supply voltage is lowered. Note that the reset is cleared at the point when all the serial data (1/4 duty: the display data D1 to D224 and the control data, 1/3 duty: the display data D1 to D171 and the control data) has been transferred, i.e., on the fall of the CE signal on the transfer of the last direction data, after all the direction data has been transferred. (See Figure 5 and Figure 6.)

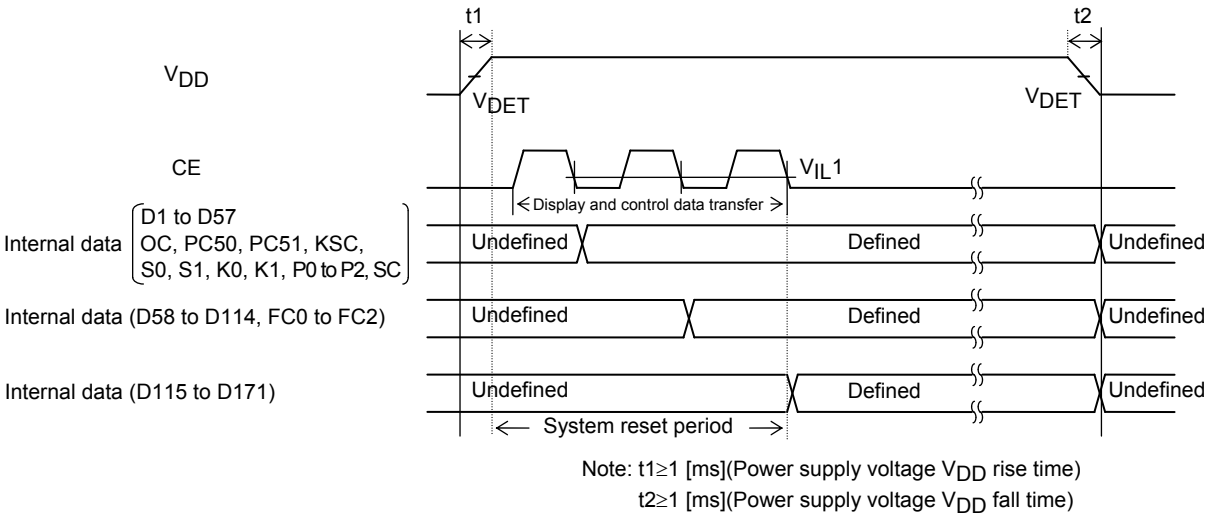
• 1/4 duty



Note: t1≥1 [ms](Power supply voltage V_{DD} rise time)
t2≥1 [ms](Power supply voltage V_{DD} fall time)

[Figure 5]

• 1/3 duty



[Figure 6]

(2) Reset method by the $\overline{RES}$ pin

When power is applied, a system reset is applied by setting the $\overline{RES}$ pin low level. The reset is cleared by setting the $\overline{RES}$ pin high level after all the serial data (1/4 duty: the display data D1 to D224 and the control data, 1/3 duty: the display data D1 to D171 and the control data) has been transferred.

In the allowable operating range (V_{DD} = 4.5 to 6.0 V), A reset is applied by setting the $\overline{RES}$ pin low level.
and the reset is cleared by setting the $\overline{RES}$ pin high level

2. Internal block states during the reset period

• CLOCK GENERATOR
A reset is applied and either the OSC pin oscillator is stopped or external clock reception is stopped

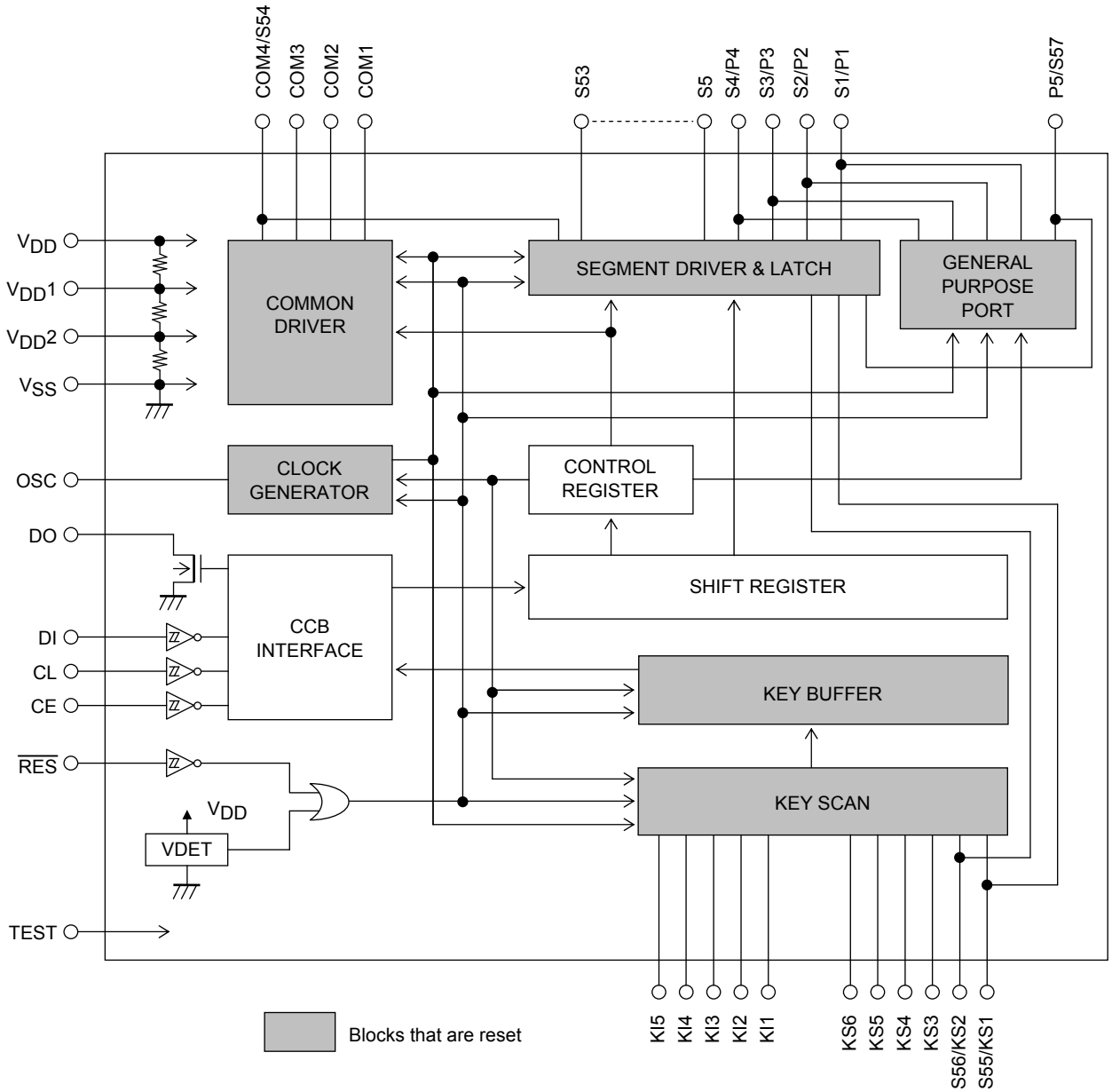
• COMMON DRIVER, SEGMENT DRIVER & LATCH
A reset is applied and the display is turned off. However, display data can be input to the latch circuit in this state.

• KEY SCAN
A reset is applied, the circuit is set to the initial state, and at the same time the key scan operation is disabled.

• KEY BUFFER
A reset is applied and all the key data is set to low.

• GENERAL PURPOSE PORT
A reset is applied, the circuit is set to the initial state.

• CCB INTERFACE, SHIFT REGISTER, CONTROL REGISTER
Since serial data transfer is possible, these circuits are not reset.


COM4/S54
COM3
COM2
COM1
S53
S5
S4/P4
S3/P3
S2/P2
S1/P1
P5/S57
VDD
VDD1
VDD2
VSS
COMMON DRIVER
SEGMENT DRIVER & LATCH
GENERAL PURPOSE PORT
OSC
CLOCK GENERATOR
CONTROL REGISTER
DO
SHIFT REGISTER
DI
CL
CE
CCB INTERFACE
KEY BUFFER
RES
KEY SCAN
VDD
VDET
TEST
KI5
KI4
KI3
KI2
KI1
KS6
KS5
KS4
KS3
S56/KS2
S55/KS1
Blocks that are reset

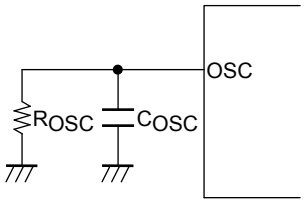
3. Pin states during the reset period

Pin	State during reset
S1/P1 to S4/P4	L *5
S5 to S53	L
COM1 to COM3	L
COM4/S54	L *6
KS1/S55, KS2/S56	L *5
KS3 to KS6	L *7
P5/S57	L *8
OSC	Z *9
DO	H *10

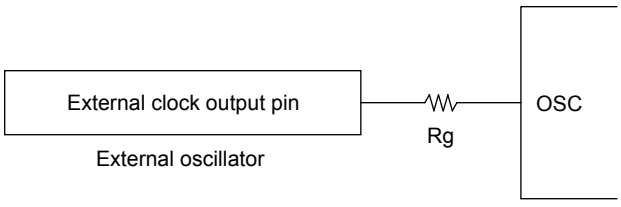
Note: *5. These output pins are forcibly set to the segment output function and held low.
*6. This output pin is forcibly set to the common output function and held low.
*7. These output pins are forcibly held fixed at the low level.
*8. This output pin is forcibly set to the general-purpose output port function and held low.
*9. This I/O pin is forcibly set to the high-impedance state.
*10.Since this output pin is an open-drain output, a pull-up resistor of between 1 and 10 kΩ is required. This pin remains high during the reset period even if a key data read operation is performed.

Notes on the OSC Pin Peripheral Circuit

1. RC oscillator operationg mode (Control data bit OC = 0)
When RC oscillator operationg mode is selected, an external resistor R_{OSC} and an external capacitor C_{OSC} must be connected between the OSC pin and GND.



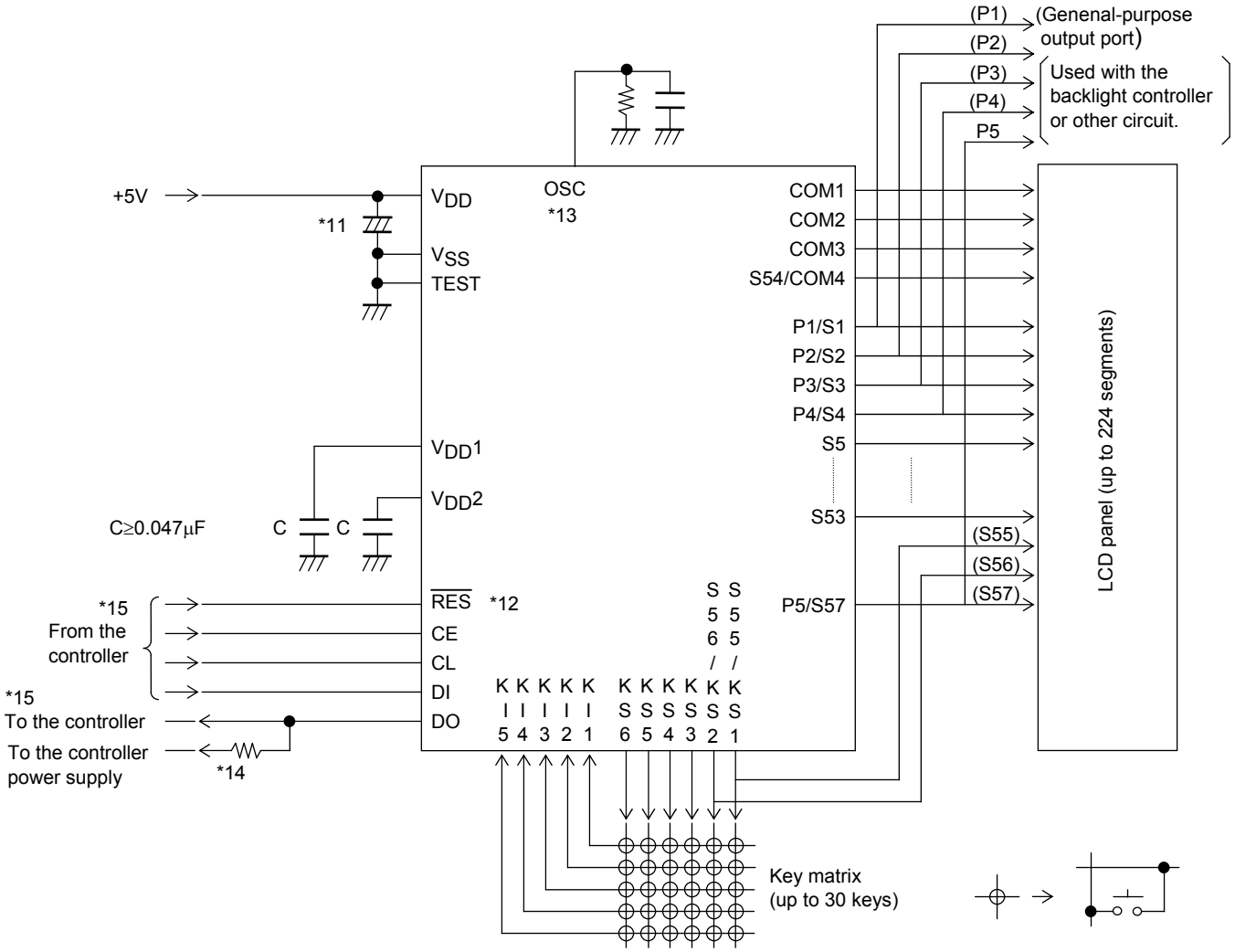
2. External clock operating mode (Control data bit OC = 1)
When selecting the external clock operating mode, connect a current protection resistor Rg (4.7 to 47 kΩ) between the OSC pin and the external clock output pin (external oscillator). Determine the value of the resistance according to the maximum allowable current value of the external clock output pin. Also make sure that the waveform of the external clock is not excessively distorted.



Note: Allowable current value at external clock output pin > $\frac{V_{DD}}{Rg}$

Sample Application Circuit 1

1/4 duty, 1/3 bias (for use with normal panels)



Note: *11. Add a capacitor to the power supply line so that the power supply voltage V_{DD} rise time when power is applied and the power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75886PW is reset by the V_{DET}.

*12. If the $\overline{RES}$ pin is not used for system reset, it must be connected to the power supply V_{DD}.

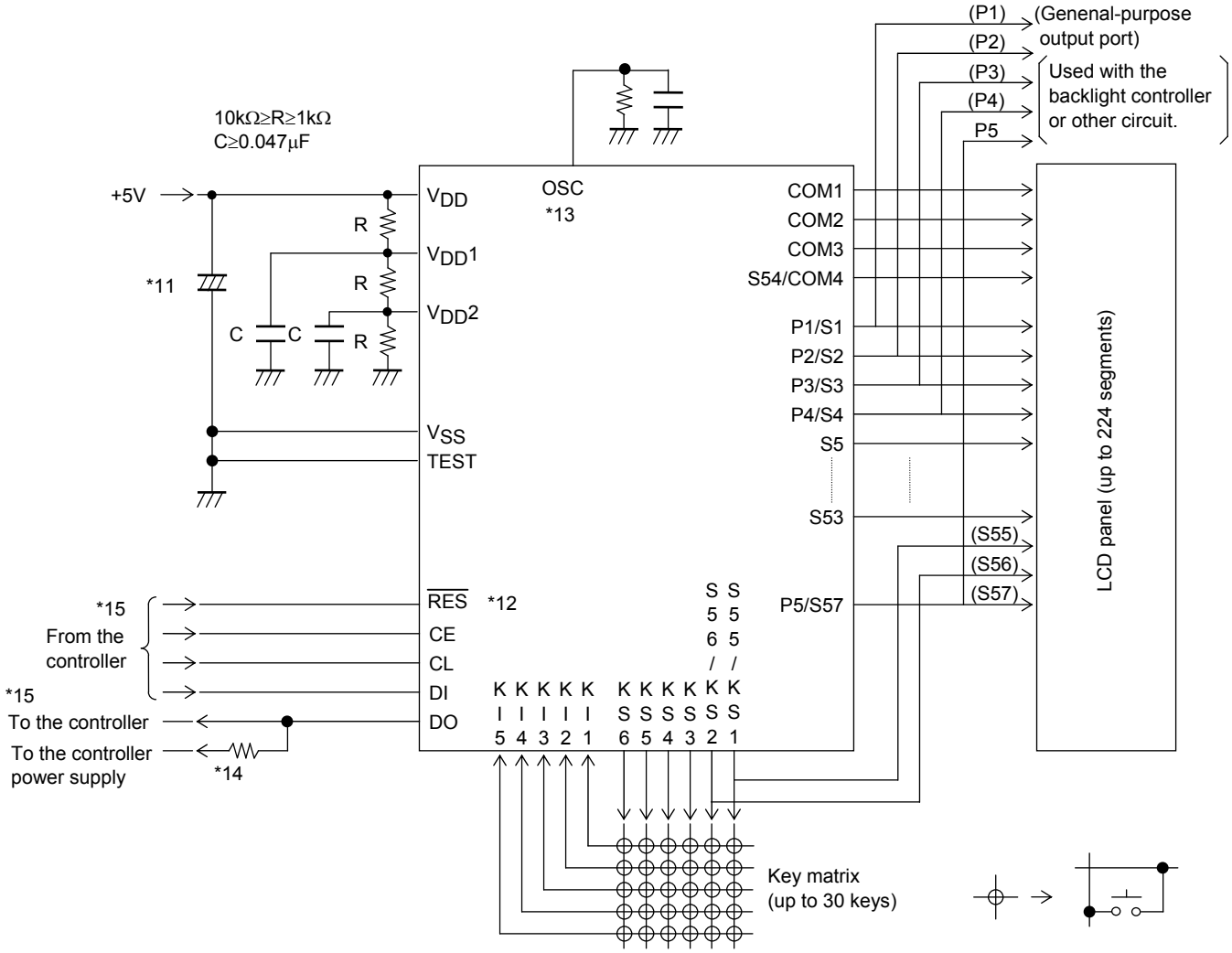
*13. When RC oscillator operating mode is used, the external resistor R_{OSC} and the external capacitor C_{OSC} must be connected between the OSC pin and GND, and when external clock operating mode is selected the current protection resistor Rg (4.7 to 47 kΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)

*14. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

*15. The pins to be connected to the controller (CE, CL, DI, DO, $\overline{RES}$) can handle 3.3 V or 5 V.

Sample Application Circuit 2

1/4 duty, 1/3bias (for use with large panels)



Note: *11. Add a capacitor to the power supply line so that the power supply voltage V_{DD} rise time when power is applied and the power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75886PW is reset by the V_{DET}.

*12. If the $\overline{RES}$ pin is not used for system reset, it must be connected to the power supply V_{DD}.

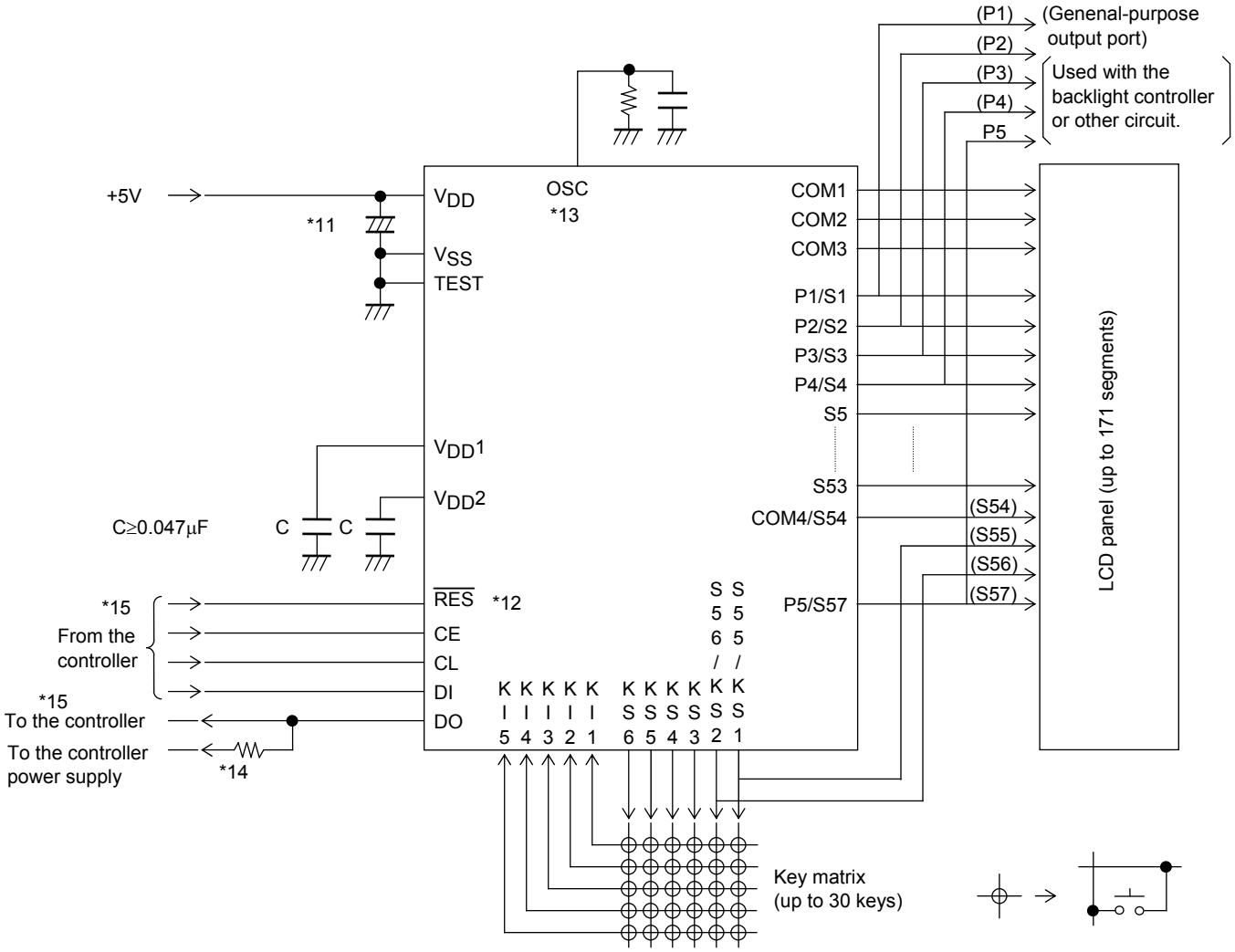
*13. When RC oscillator operating mode is used, the external resistor R_{OSC} and the external capacitor C_{OSC} must be connected between the OSC pin and GND, and when external clock operating mode is selected the current protection resistor Rg (4.7 to 47 kΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)

*14. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

*15. The pins to be connected to the controller (CE, CL, DI, DO, $\overline{RES}$) can handle 3.3 V or 5 V.

Sample Application Circuit 3

1/3 duty, 1/3 bias (for use with normal panels)



Note: *11. Add a capacitor to the power supply line so that the power supply voltage V_{DD} rise time when power is applied and the power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75886PW is reset by the V_{DET}.

*12. If the $\overline{RES}$ pin is not used for system reset, it must be connected to the power supply V_{DD}.

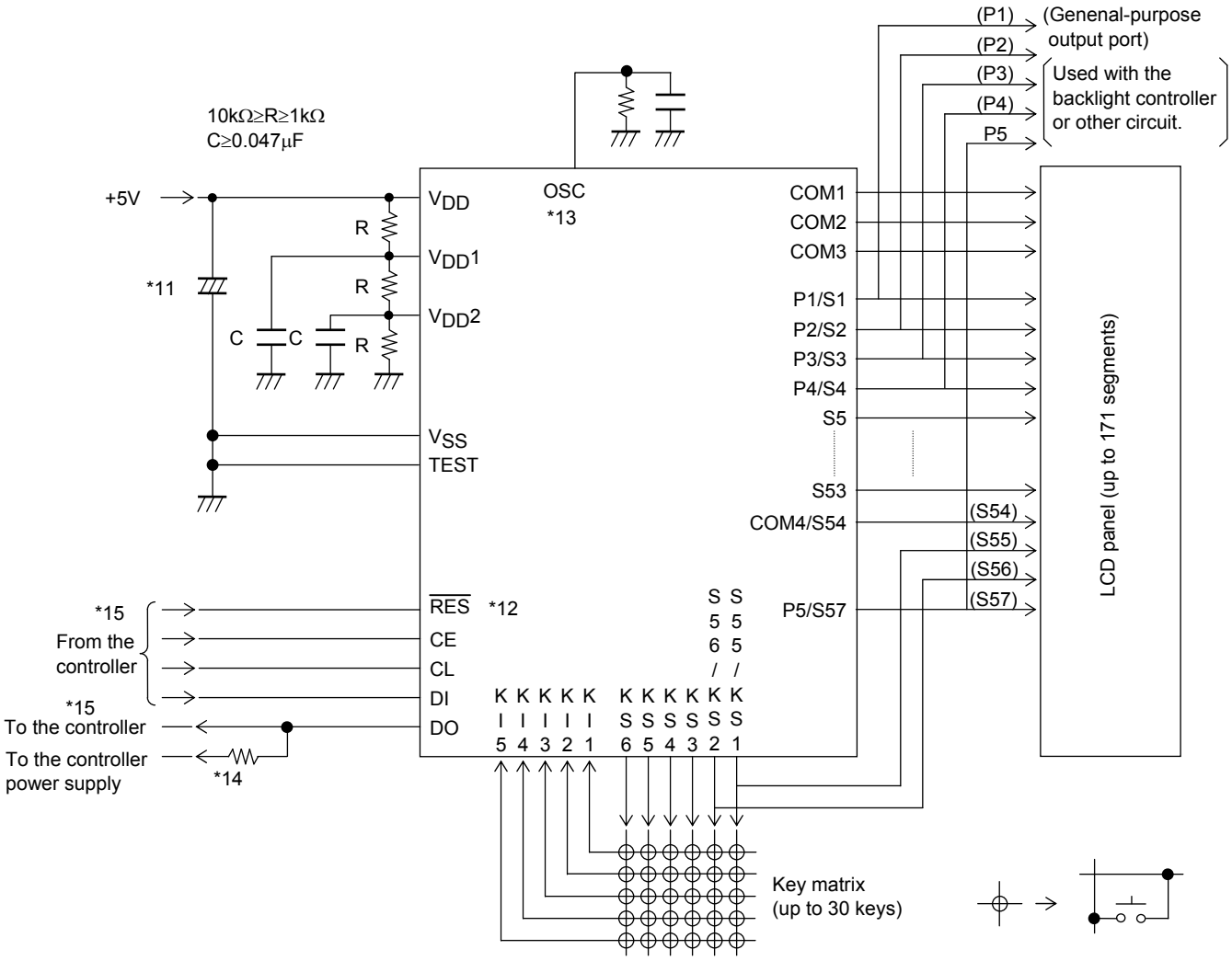
*13. When RC oscillator operating mode is used, the external resistor R_{OSC} and the external capacitor C_{OSC} must be connected between the OSC pin and GND, and when external clock operating mode is selected the current protection resistor Rg (4.7 to 47 kΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)

*14. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

*15. The pins to be connected to the controller (CE, CL, DI, DO, $\overline{RES}$) can handle 3.3 V or 5 V.

Sample Application Circuit 4

1/3 duty, 1/3bias (for use with large panels)



Note: *11. Add a capacitor to the power supply line so that the power supply voltage V_{DD} rise time when power is applied and the power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75886PW is reset by the V_{DET}.

*12. If the $\overline{RES}$ pin is not used for system reset, it must be connected to the power supply V_{DD}.

*13. When RC oscillator operating mode is used, the external resistor R_{OSC} and the external capacitor C_{OSC} must be connected between the OSC pin and GND, and when external clock operating mode is selected the current protection resistor Rg (4.7 to 47 kΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)

*14. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

*15. The pins to be connected to the controller (CE, CL, DI, DO, $\overline{RES}$) can handle 3.3 V or 5 V.

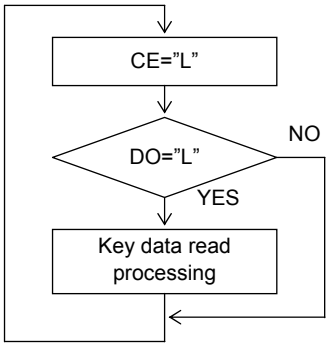
Notes on Transferring Display Data from The Controller

When using the LC75886PW in 1/4 duty, applications transfer the display data (D1 to D224) in four operations, and in 1/3 duty, they transfer the display data (D1 to D171) in three operations. In either case, applications should transfer all of the display data within 30 ms to maintain the quality of displayed image.

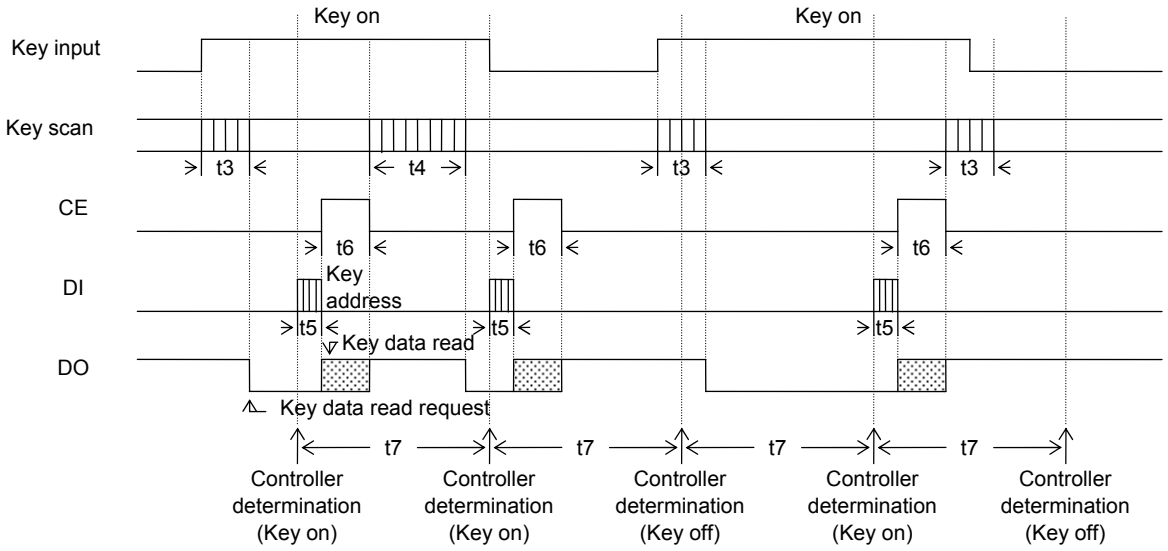
Notes on the Controller Key Data Read Techniques

1. Timer based key data acquisition

(1) Flowchart



(2) Timing chart



t3 ····· Key scan execution time when the key data agreed for two key scans. (615T[s])

t4 ····· Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (1230T[s])

t5 ····· Key address (43H) transfer time

t6 ····· Key data read time

$$T = \frac{1}{f_{OSC}} = \frac{1}{f_{CK}}$$

(3) Explanation

In this technique, the controller uses a timer to determine key on/off states and read the key data. The controller must check the DO state when CE is low every t7 period without fail. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation.

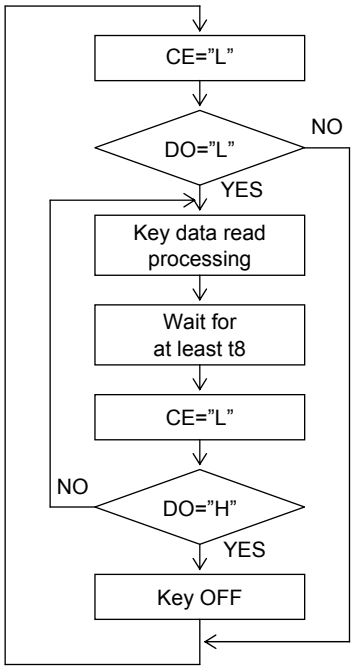
The period t7 in this technique must satisfy the following condition.

t7>t4+t5+t6

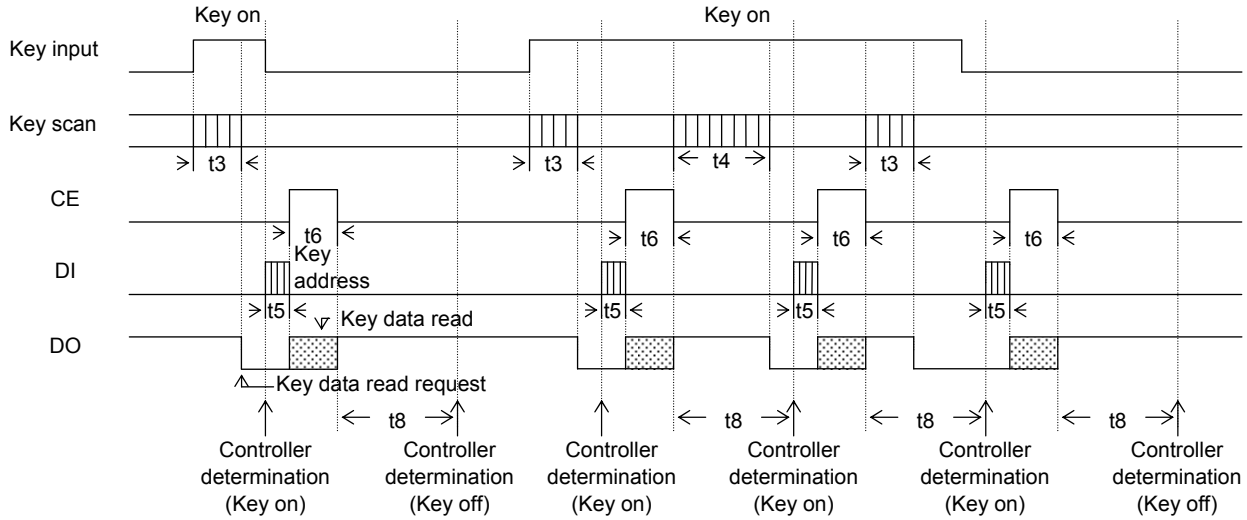
If a key data read operation is executed when DO is high (DO does not generate a key data read request output), the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

2. Interrupt based key data acquistion

(1) Flowchart



(2) Timing chart



t3 ····· Key scan execution time when the key data agreed for two key scans. (615T[s])

t4 ····· Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (1230T[s])

t5 ····· Key address (43H) transfer time

t6 ····· Key data read time

$$T = \frac{1}{f_{OSC}} = \frac{1}{f_{CK}}$$

(3) Explanation

In this technique, the controller uses interrupts to determine key on/off states and read the key data.

The controller must check the DO state when CE is low. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation. After that the next key on/off determination is performed after the time t8 has elapsed by checking the DO state when CE is low and reading the key data. The period t8 in this technique must satisfy the following condition.

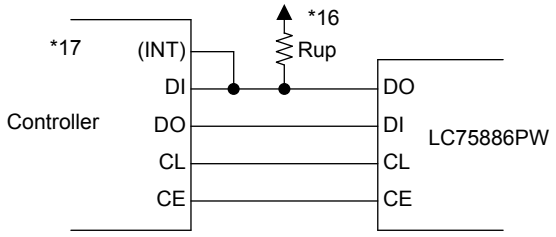
t8>t4

If a key data read operation is executed when DO is high (DO does not generate a key data read request output), the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

About Data Communication Method with The Controller

1. About data communication method of 4 line type CCB format

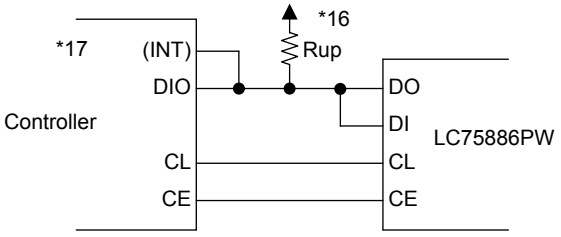
The 4 line type CCB format is the data communication method of before. The LC75886PW must connect to the controller as followings.



Note: *16. Connect the pull-up resistor Rup. Select a resistance (between 1 to 10kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.
*17. The (INT) pin is an input port for the key data read request signal (a low level on DO) detection.

2. About data communication method of 3 line type CCB format

The 3 line type CCB format is the data communication method that made a common use of the data input DI in the data output DO. The LC75886PW must connect to the controller as followings.

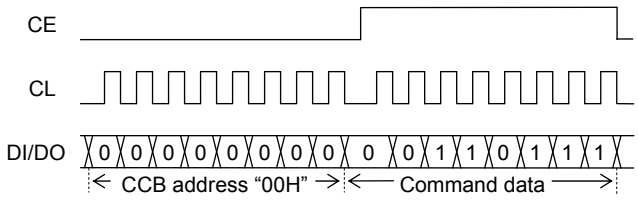


Note: *16. Connect the pull-up resistor Rup. Select a resistance (between 1 to 10kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.
*17. The (INT) pin is an input port for the key data read request signal (a low level on DO) detection.

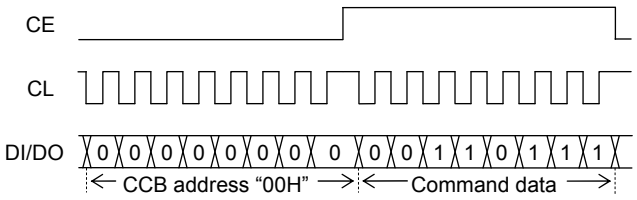
In this case, Applications must transfer the data communication start command before the serial data input (CCB address “42H”, display data and control data transfer) or serial data output (CCB address “43H” transfer, key data read) to avoid the collision of the data input signal DI and the data output signal DO.
Then applications must transfer the data communication stop command when the controller wants to detect the key data read request signal (a low level on DO) during a movement stop of the serial data input and the serial data output.

<1> Data communication start command

(1) When CL is stopped at the low level

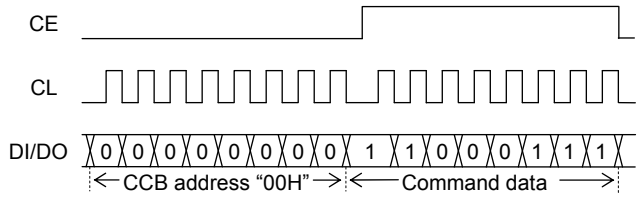


(2) When CL is stopped at the high level

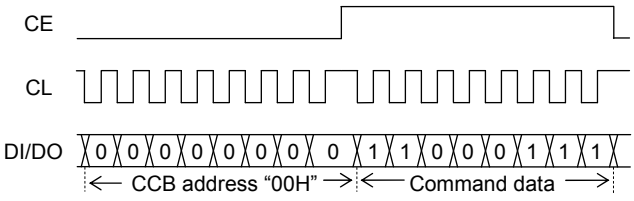


<2> Data communication stop command

(1) When CL is stopped at the low level

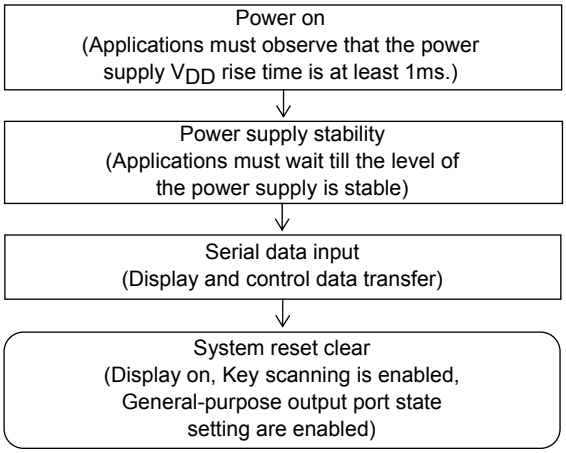


(2) When CL is stopped at the high level



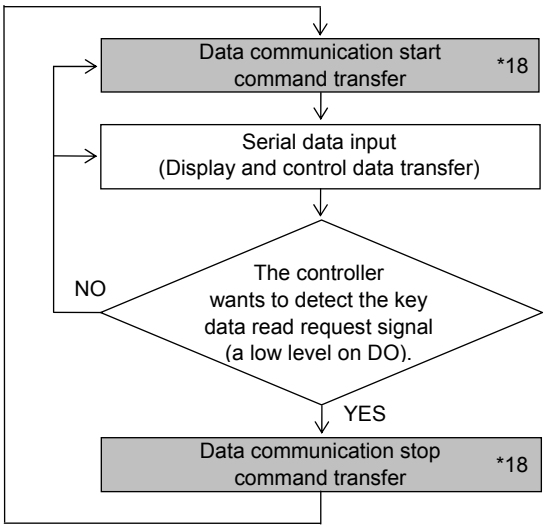
Data Communication Flowchart of 4 Line Type or 3 Line Type CCB Format

1. Flowchart of the initial setting when power is turned on.



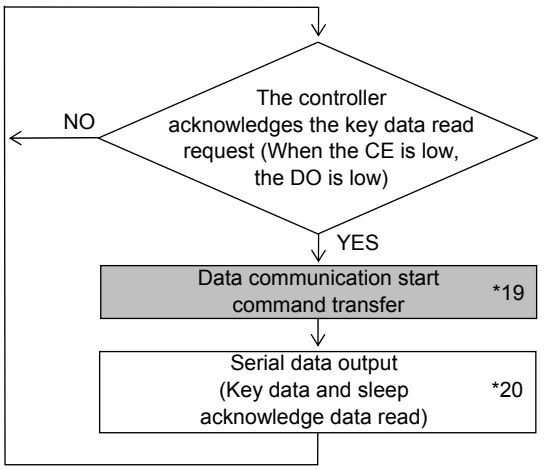
Note: The flowchart of initial setting when power is turned on is same regardless of the 4 line type or 3 line type CCB format.
Take explanation about "system reset" into account.

2. Flowchart of the serial data input



Note: *18. In the case of the 4 line type CCB format, the transfers of data communication start command and data communication stop command are unnecessary, and, in the case of the 3 line type CCB format, these transfers are necessary.

3. Flowchart of the serial data output

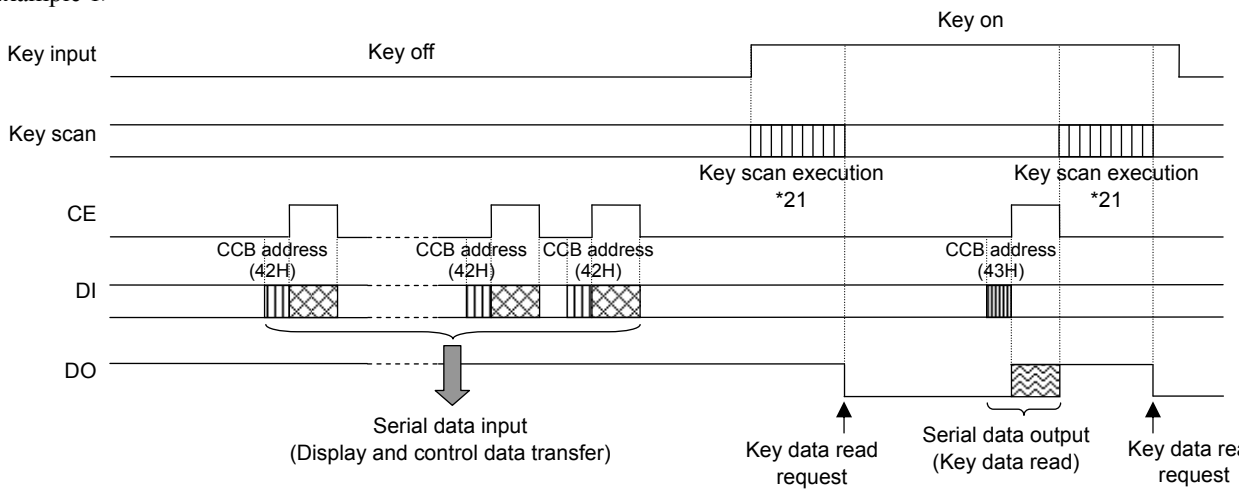


Note: *19. In the case of the 4 line type CCB format, the transfer of data communication start command is unnecessary, and, in the case of the 3 line type CCB format, the transfer is necessary.
*20. Because the serial data output has the role of the data communication stop command, it is not necessary to transfer the data communication stop command some other time.

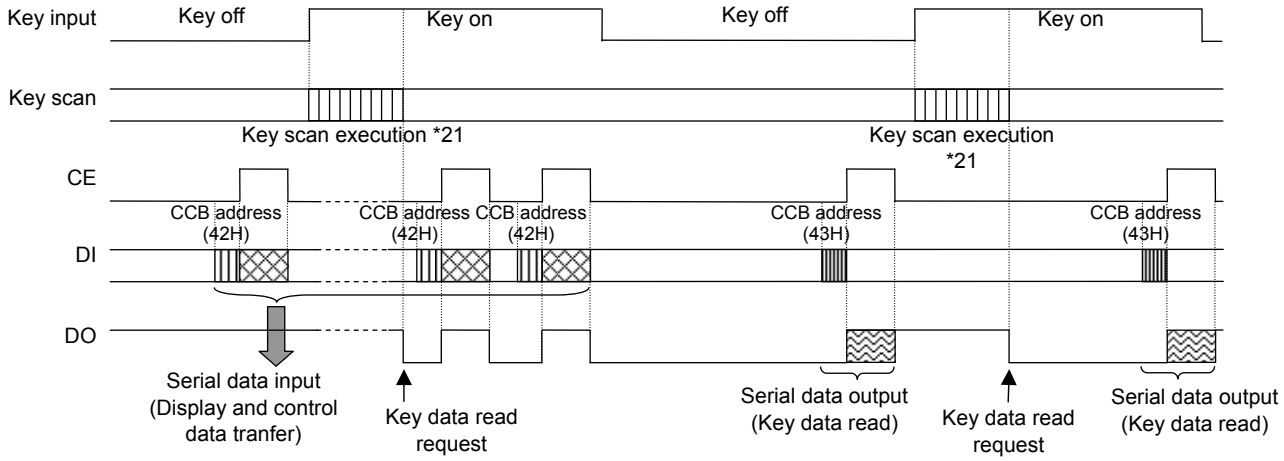
Timing Chart of 4 Line Type and 3 Line Type CCB Format

1. Timing chart of 4 line type CCB format

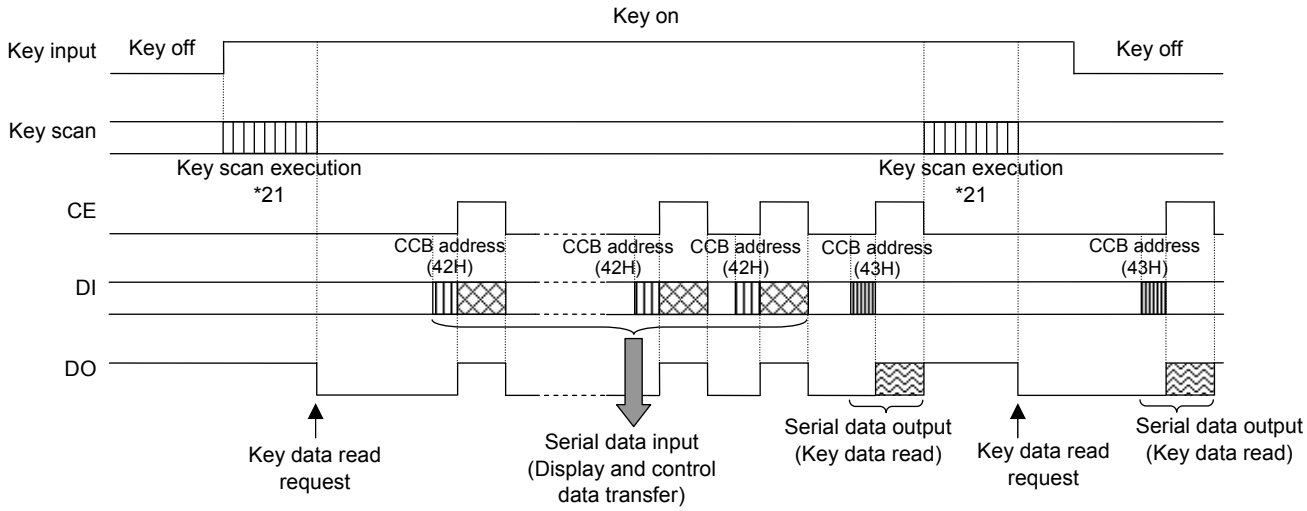
<Example 1>



<Example 2>



<Example 3>

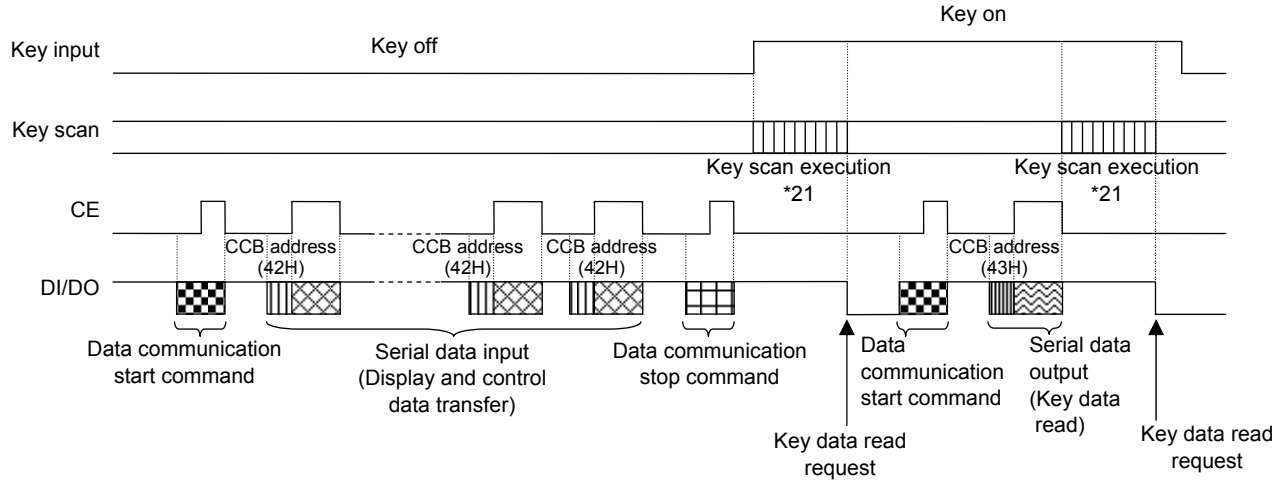


Note: *21. When the key data agrees for two key scans, the key scan execution time is 615T[s].
And, when the key data does not agree for two key scans and the key scan is executed again, the key scan execution time is 1230T[s].

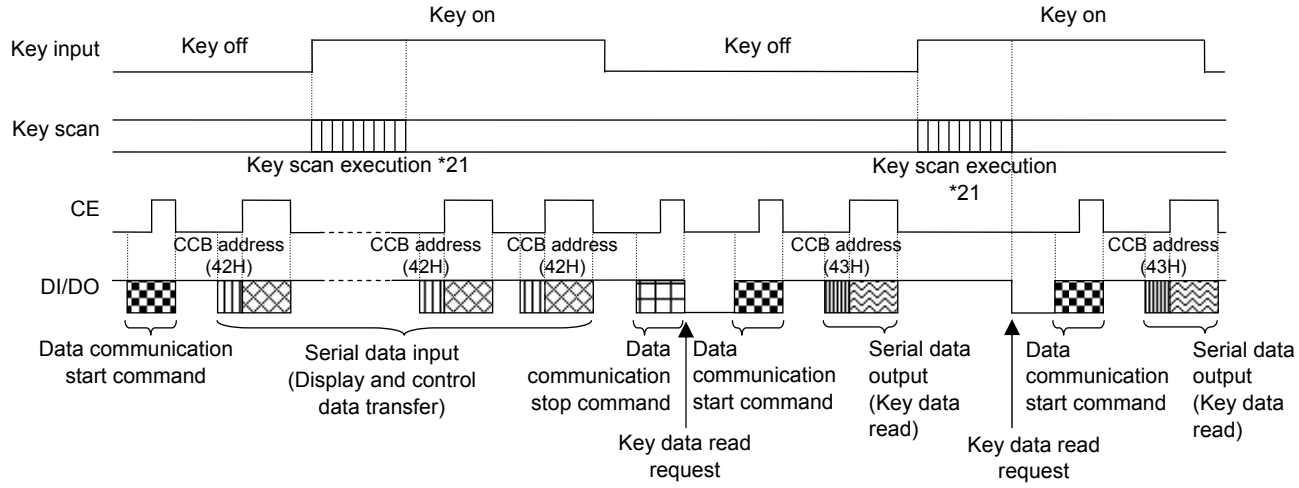
$$T = \frac{1}{f_{OSC}} = \frac{1}{f_{CK}}$$

2. Timing chart of 3 line type CCB format

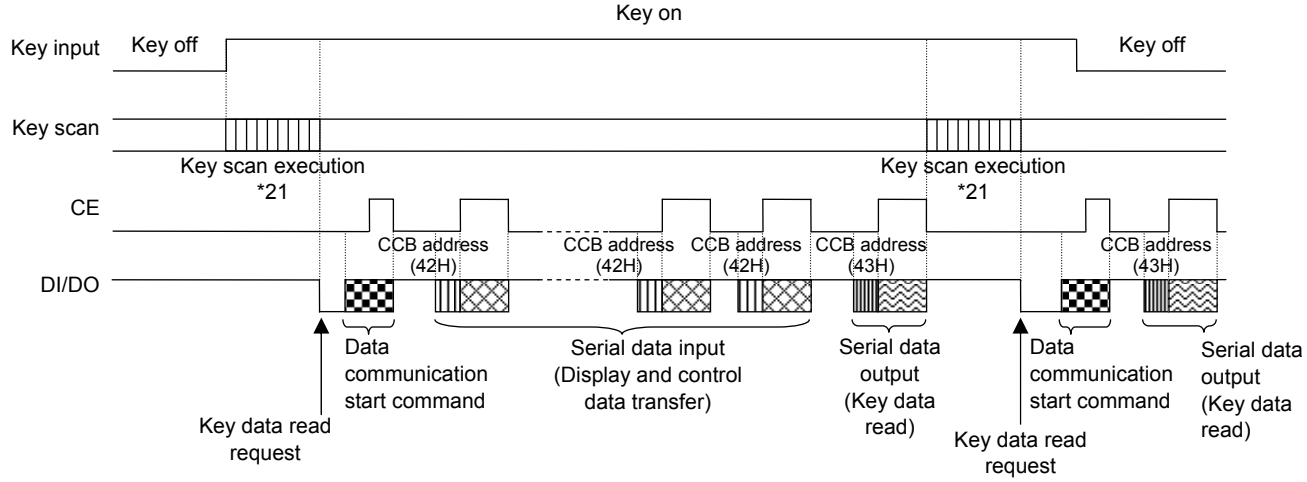
<Example 1>



<Example 2>



<Example 3>



Note: *21. When the key data agrees for two key scans, the key scan execution time is 615T[s].
And, when the key data does not agree for two key scans and the key scan is executed again, the key scan execution time is 1230T[s].

$$T = \frac{1}{f_{OSC}} = \frac{1}{f_{CK}}$$

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC75886PW-H	SQFP80 12x12 / SQFP80 (Pb-Free / Halogen Free)	300 / Tray Foam
LC75886PWH-H	SQFP80 12x12 / SQFP80 (Pb-Free / Halogen Free)	300 / Tray Foam

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