

2 MHz 650 mA Step Down Converter for RF Power Amplifiers in Tiny 8-pin WCSP Package

FEATURES

- High-Efficiency Step-Down Converter
- Output Current up to 650 mA
- V_{IN} Range From 2.5 to 6.0 V
- 2.0-MHz Fixed-Frequency Operation
- Clock Dithering (TPS62701)
- Dynamic Voltage Control With External Reference (1.3 V to 3.09 V)
- Fast Output-Voltage Settling (1.3 V to 3.09 V in 20 μ s)
- Soft Start
- Overload Protection
- Undervoltage Lockout
- Thermal Protection
- 8-Pin WCSP Package

APPLICATIONS

- Cell Phones, Smart Phones
- Battery-Powered RF Amplifier

DESCRIPTION

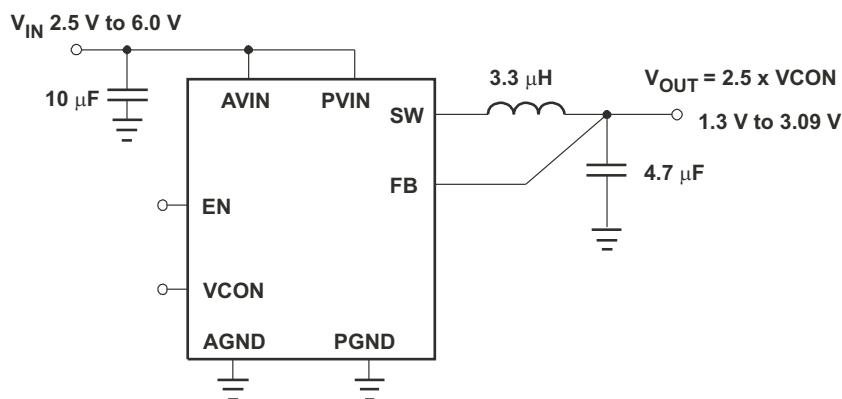
The TPS6270x device is a high-efficiency synchronous step-down DC-DC converter optimized for RF power-amplifier (PA) applications. It provides up to 650 mA of output current from a single Li-Ion cell.

The device converts input voltages from 2.5 to 6.0 V down to an output voltage set by an external analog reference voltage applied to the pin VCON. The output voltage follows the external reference by an internal gain of 2.5 within the limits of 1.3 V to 3.09 V. This scheme adjusts the output voltage of the DC/DC converter and therefore the output power of an RF-PA.

The TPS6270x operates in fixed-frequency PWM mode at a 2.0-MHz switching frequency to minimize RF interference. This converter operates with only three small external components; an input capacitor, inductor and output capacitor. The TPS62701 has in addition a built-in clock-dithering circuit to reduce RF noise.

The TPS6270x is available in a tiny 8 pin lead free WCSP package for smallest solution size.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

TA	PART NUMBER ⁽¹⁾	PACKAGE	ORDERING	PACKAGE MARKING
–30°C to 85°C	TPS62700	WCSP 8 pin	TPS62700YZF	CKL
	TPS62701		TPS62701YZF	CGJ

(1) The package is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		VALUE	UNIT
Input voltage range ⁽²⁾		–0.3 to 7	V
Voltage range at EN, VCON ⁽²⁾		–0.3 to $V_{IN} + 0.3$, ≤ 7	V
Voltage on SW ⁽²⁾		–0.3 to 7	V
Peak output current ⁽²⁾		internally limited	
ESD rating ⁽³⁾	HBM Human body model	2	kV
	Machine model	200	V
T _J	Maximum operating junction temperature	–40 to 150	°C
T _{stg}	Storage temperature range	–65 to 150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

DISSIPATION RATINGS^{(1) (2)}

PACKAGE	R _{θJA}	POWER RATING FOR T _A ≤ 25°C	DERATING FACTOR ABOVE T _A = 25°C
YZF	110°C/W	900 mW	9 mW/°C

- (1) Maximum power dissipation is a function of T_J(max), θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = [T_J(\text{max}) - T_A] / \theta_{JA}$.
- (2) This thermal data is measured with high-K board (4 layers board according to JESD51-7 JEDEC standard).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN} , AV _{IN} , PV _{IN}	Supply voltage	2.5		6	V
T _A	Operating ambient temperature	–40		85	°C
T _J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

$PV_{IN} = AV_{IN} = V_{IN} = 3.6\text{ V}$, $EN = AV_{IN}$, $T_A = T_J = -40^\circ\text{C}$ to 85°C typical values are at $T_A = 25^\circ\text{C}$ (unless otherwise noted), see parameter measurement information

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
AV _{IN} , PV _{IN}	Input voltage range	I _{OUT max} = 650 mA		2.5		6	V
I _{OUT}	Output current	V _{IN} 2.5 to 6 V				650	mA
I _Q	Operating quiescent current into AV _{IN}	V _{CON} = 1 V, FB = 0 V, V _{IN} = 3.6V, device not switching ⁽¹⁾			0.1	0.3	mA
I _{SD}	Shutdown current	EN = SW=V _{CON} = AGND, AV _{IN} = PV _{IN} = 3.6V			0.01	2	μA
ENABLE							
V _{IH}	High Level Input Voltage, EN			1.2		V _{IN}	V
V _{IL}	Low Level Input Voltage, EN			0		0.4	V
I _{IN}	Input bias Current, EN	EN = AV _{IN}			5	10	μA
CONTROL INPUT V _{CON}							
V _{VCON, MIN}	V _{CON} Threshold forcing V _{FB, MIN}	Falling V _{CON} signal		0.484	0.52	0.556	V
V _{VCON, MAX}	V _{CON} Threshold forcing V _{FB, MAX}	Rising V _{CON} signal		1.211	1.236	1.26	V
Z _{VCON}	V _{CON} Input resistance			100			kΩ
C _{VCON}	V _{CON} Input capacitance	V _{CON} = 1 V, f = 100 kHz				20	pF
I _{IN VCON}	V _{CON} Input current					10	μA
Gain	Internal Gain V _{OUT} /V _{CON}	0.556 V ≤ V _{CON} ≤ 1.208 V			2.5		
POWER SWITCH							
R _{DS(ON)}	High side MOSFET on-resistance	PV _{IN} = V _{GS} = 3.6 V	T _A = T _J = 25°C	100	140	230	mΩ
			T _A = T _J = −40°C to 85°C			270	
	Low-Side MOSFET on-resistance	PV _{IN} = V _{GS} = 3.6 V	T _A = T _J = 25°C	180	200	330	mΩ
			T _A = T _J = −40°C to 85°C			430	
I _{LIMF}	Forward current limit MOSFET high side and low side	PV _{IN} = 3.6 V		935	1100	1200	mA
OSCILLATOR							
f _{SW}	Oscillator frequency	3 V < V _{IN} < 5 V		1.7	2.0	2.3	MHz
FEEDBACK/OUTPUT							
V _{FB, MIN}	Minimum feedback voltage	V _{CON} = 0.4 V ⁽²⁾⁽³⁾		1.25	1.3	1.35	V
V _{FB}	Feedback voltage	V _{CON} = 1.1 V ⁽²⁾⁽³⁾		2.693	2.75	2.835	V
V _{FB, MAX}	Maximum feedback voltage	V _{CON} = 1.4 V ⁽²⁾⁽³⁾		3.028	3.09	3.15	V
Linearity	Linearity in V _{CON} range 0.556 V to 1.208 V	⁽²⁾ ⁽³⁾		−2		2	%
T _{RESPONSE}	V _{OUT} Rise time from 1.3 V to 3.09 V	V _{IN} = 4.2 V, C _{OUT} = 4.7 μF, L = 3.3 μH, R _{LOAD} = 5 Ω ⁽³⁾⁽⁴⁾			20	30	μs
	V _{OUT} Fall time from 3.09 V to 1.3 V	V _{IN} = 4.2 V, C _{OUT} = 4.7 μF, L = 3.3 μH, R _{LOAD} = 10 Ω ⁽³⁾⁽⁴⁾			20	30	
T _{ON}	Start-up Time	From Enable low to high transition until V _{OUT} reaches 3.09 V, C _{OUT} = 4.7 μF, L = 3.3 μH, I _{OUT} ≤ 1 mA			190	300	μs
η	Efficiency (L = 3.3μH, DCR ≤ 100mΩ)	V _{IN} = 3.6 V, V _{OUT} = 1.3 V, I _{OUT} = 150 mA ⁽⁵⁾⁽³⁾			87		%
		V _{IN} = 3.6 V, V _{OUT} = 3.09 V, I _{OUT} = 400 mA ⁽⁵⁾⁽³⁾			95		
V _{OUT_RIPPLE}	Ripple voltage, PWM mode	V _{IN} = 3 V to 4.5 V, V _{OUT} = 1.3 V, I _{OUT} = 10 mA to 400 mA ⁽³⁾			10		mV _{p-p}
Line _{tr}	Line transient response	V _{IN} = 600 mV step, over V _{IN} range 3 V to 5.5 V T _{RISE} = T _{FALL} = 10 μs, V _{OUT} = 1.3 V, I _{OUT} = 100 mA ⁽³⁾			50		mV _{pk}
Load _{tr}	Load transient response	V _{IN} = 3.1/3.6/4.5 V, V _{OUT} = 1.3 V, transients 0 mA to 100 mA, T _{RISE} = T _{FALL} = 10 μs ⁽³⁾			50		mV _{pk}

(1) Device operating in 100% duty cycle mode

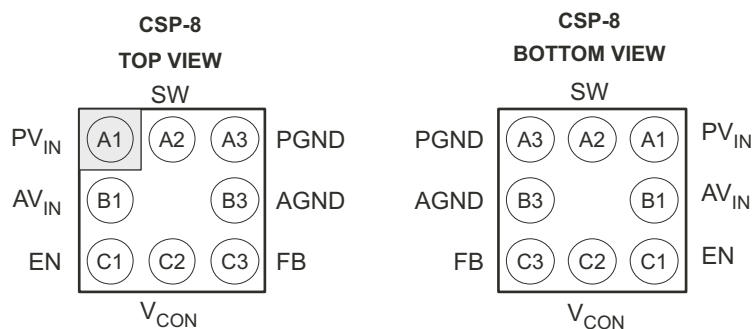
(2) $2.5\text{ V} \leq V_{IN} \leq 6\text{ V}$, with $V_{IN_MIN} = V_{OUT} + 0.5\text{ V}$

(3) The voltage need to be measured on the C_{OUT} using appropriate measurement probes. For the measurements, a proper PCB layout and usage of recommended inductors and capacitors are essential. See parameter measurement information.

(4) Rise/Fall time valid for V_{FB} within specified limits.

(5) Using appropriate inductor with $R_{(DCR)}$ less than 100 m Ω

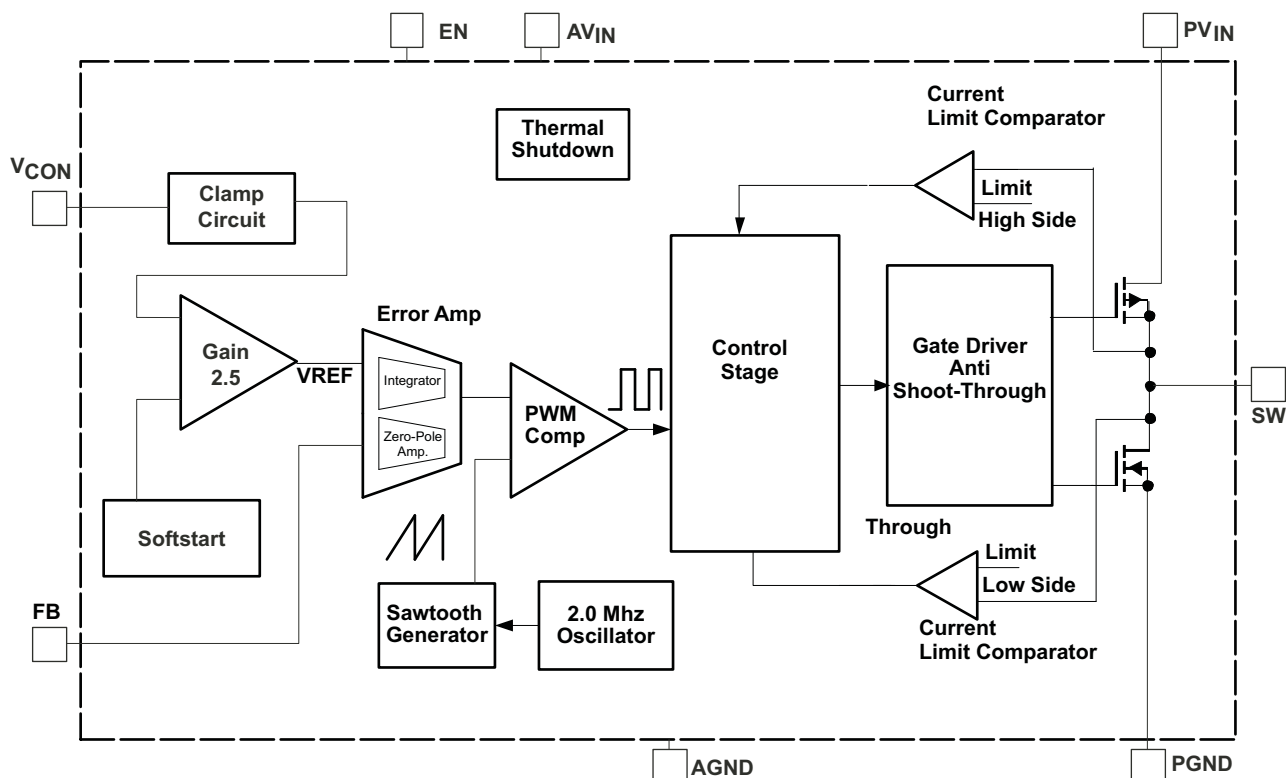
PIN ASSIGNMENTS



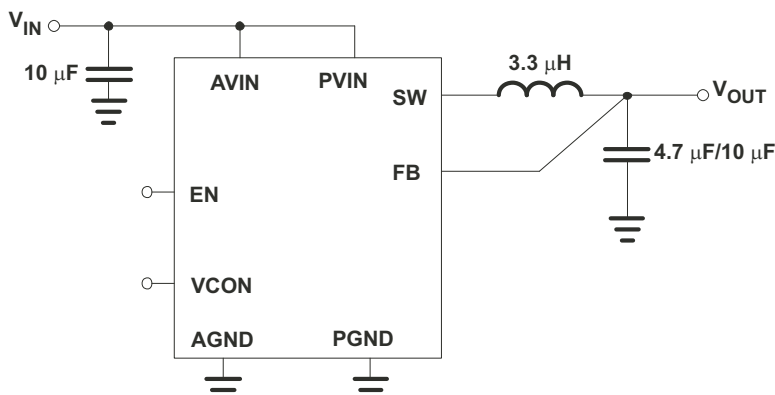
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO. CSP		
PV _{IN}	A1	PWR	V _{IN} power supply input for the PMOSFET
AV _{IN}	B1	PWR	V _{IN} analog supply input for the internal analog circuitry
EN	C1	I	Enable input for the device. Set high for operation, low for shutdown. This pin must be terminated.
V _{CON}	C2	I	Voltage control input. This pin controls the output voltage of the converter. The output voltage follows V _{CON} with a gain of 2.5 for $0.556\text{ V} \leq V_{\text{CON}} \leq 1.208\text{ V}$.
FB	C3	I	Analog Feedback Input Pin for the internal regulation loop. Connect this pin directly to the output capacitor.
AGND	B3	I	Analog GND Pin for the internal analog circuitry.
PGND	A3		Power GND Pin for the NMOSFET
SW	A2		Switch Node to the internal PMOSFET and NMOSFET. Connect the external inductor between this pin and the output capacitor.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



L: LPS4018 3.3 µH, DCR 70 mΩ/VLF3014A 3.3 µH DCR 150 mΩ

C_{IN}: GRM188R60J106M 10 µF Murata 0603 size

C_{OUT}: GRM188R60J106M 10 µF Murata 0603 size

GRM188Ru60J475K 4.7 µF Murata 0603 size

DETAILED DESCRIPTION

OPERATION

The TPS6270x step down converter operates at a 2.0-MHz fixed frequency using pulse-width modulation (PWM) over the entire load range. This ensures low output-voltage ripple for RF-PA power applications.

In PWM operation, the converter uses a unique fast-response voltage-mode control scheme to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors.

At the beginning of each clock cycle initiated by the clock signal, the High-Side MOSFET switch is turned on. The current flows from the input capacitor via the High-Side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch when the current limit of the High-Side MOSFET switch is exceeded. After a short dead time to prevent shoot-through, the Low-Side MOSFET rectifier is turned on, and the inductor current ramps down. The current then flows from the inductor to the output capacitor and to the load. It turns back to the inductor through the Low-Side MOSFET rectifier.

The next cycle is initiated by the clock signal turning off the Low-Side MOSFET rectifier and turning on the High-Side MOSFET switch.

Dynamic Output Voltage Control V_{CON}

The output voltage of TPS6270x can be dynamically adjusted with an external analog voltage applied to the pin V_{CON}. This voltage is typically supplied from an external DAC to adjust the supply voltage for the RF Power amplifier, and therefore to determine the RF output power. The output voltage is set to : V_{OUT} = 2.5 × V_{CON}.

The output voltage can be set in the range between V_{FB, MIN} (1.3 V) and V_{FB, MAX} (3.09 V). The device provides an internal voltage gain factor of 2.5. For dynamic voltage adjustment the V_{CON} voltage range is between V_{CON, MIN} (0.52 V) and V_{CON, MAX} (1.24 V). In Case the V_{CON} voltage is out of this range, the output voltage is internally limited to V_{FB, MIN} (1.3 V) and V_{FB, MAX} (3.09 V). This allows using the TPS6270x as a fixed output voltage converter where the V_{CON} Pin is connected, for example, to GND or V_{IN}.

100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty-cycle mode when the input voltage approaches the nominal output voltage. In order to maintain the output voltage, the High-Side MOSFET switch is turned on 100% for one or more cycles.

With further decreases of V_{IN} , the High-Side MOSFET switch is turned on completely. In this case, the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the entire battery voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN_MIN} = V_{OUT_MIN} + I_{OUT_MAX} \times (R_{DS(on)_MAX} + R_L) \quad (1)$$

With:

I_{OUT_MAX} = maximum output current plus inductor ripple current

$R_{DS(on)_MAX}$ = maximum P-channel switch $R_{DS(on)}$.

R_L = DC resistance of the inductor

V_{OUT_MAX} = nominal output voltage plus maximum output voltage tolerance

ENABLE

The device is enabled by setting the EN pin to high and at first the internal circuits are settled. Afterwards the device activates the soft start circuit and ramps up the output voltage. The output voltage is ramped up from 0 V to 3.09 V within typically 190 μ s after the EN pin changes from low to high. A low signal at the EN pin sets the device in Shutdown Mode with less than 2 μ A current consumption.

SHORT-CIRCUIT PROTECTION

The High-Side and Low-Side MOSFET switches are protected with maximum output current = I_{LIMF} in case a short circuit on the output occurs. When the High-Side MOSFET switch reaches its current limit, it is turned off, and the Low-Side MOSFET switch is turned on. The High-Side MOSFET switch can only turn on again, after the current in the Low-Side MOSFET switch decreases below its current limit.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J , exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the High-Side and Low-Side MOSFETs are turned-off. The device continues its operation when the junction temperature falls by typical 20°C.

UNDERVOLTAGE LOCKOUT

The device stops operation at typ. 1.5 V with falling input voltage and starts operation at typ. 1.7 V with rising input voltage. This prevents malfunction of the device due to low input voltage.

CLOCK DITHERING

In order to reduce switch frequency harmonics in the higher RF bands, the TPS62701 has a built-in clock-dithering circuit.

TYPICAL CHARACTERISTICS

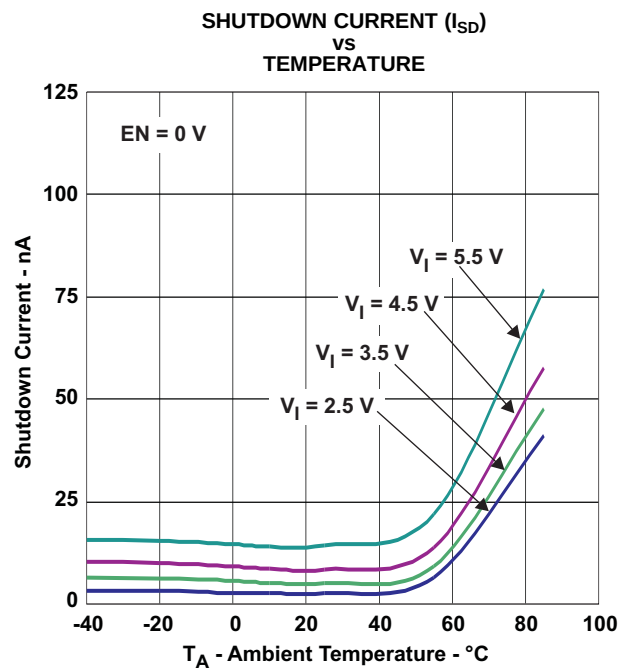
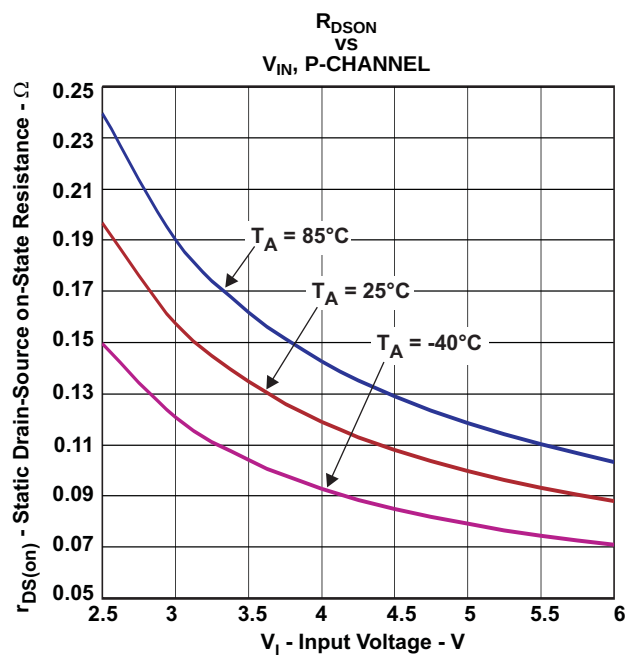
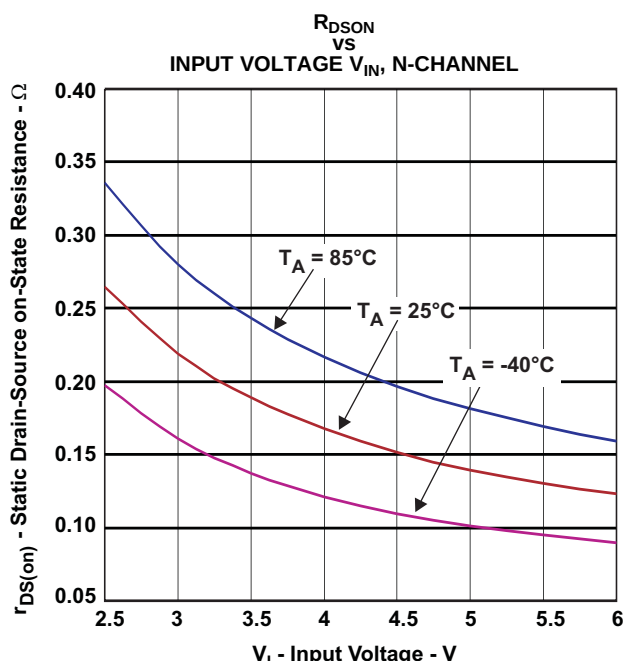
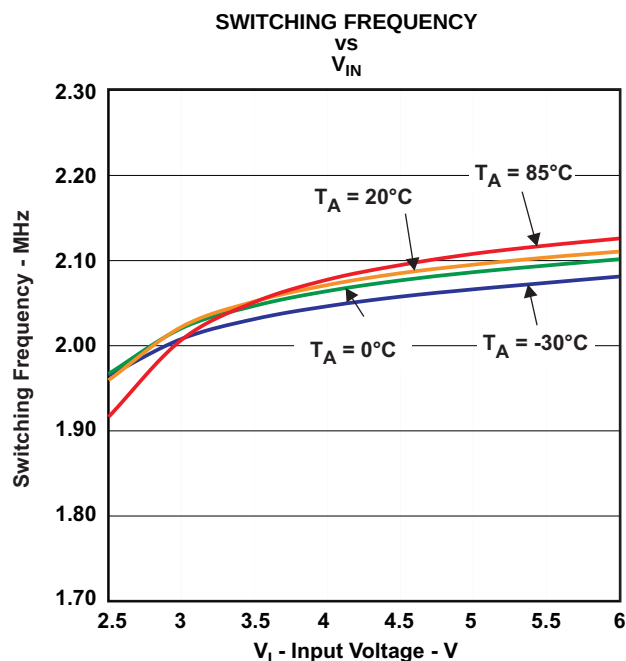
Typical Characteristic Graphs

		FIGURE
Switching Frequency	vs Input Voltage (V_{IN})	Figure 1
$R_{DS(on)}$	vs V_{IN} , N-Channel	Figure 2
$R_{DS(on)}$	vs V_{IN} , P-Channel	Figure 3
Shutdown Current (I_{SD})	vs Temperature	Figure 4
Quiescent Current (I_Q) into AVIN	vs V_{IN}	Figure 5
EN High Threshold Voltage	vs V_{IN}	Figure 6
Efficiency	vs Output Current	Figure 7
Efficiency	vs Output Current	Figure 8
Efficiency	vs Output Voltage	Figure 9
Efficiency	vs Output Voltage	Figure 10

TYPICAL CHARACTERISTICS (continued)

Typical Characteristic Graphs (continued)

		FIGURE
Output Voltage	vs Output Current ($V_{OUT} = 1.3\text{ V}$, $T_A = 25^\circ\text{C}$)	Figure 11
Output Voltage	vs Output Current ($V_{OUT} = 1.3\text{ V}$, $T_A = -40^\circ\text{C}$)	Figure 12
Output Voltage	vs Output Current ($V_{OUT} = 1.3\text{ V}$, $T_A = 85^\circ\text{C}$)	Figure 13
Output Voltage	vs Output Current ($V_{OUT} = 2.75\text{ V}$, $T_A = 25^\circ\text{C}$)	Figure 14
Output Voltage	vs Output Current ($V_{OUT} = 2.75\text{ V}$, $T_A = -40^\circ\text{C}$)	Figure 15
Output Voltage	vs Output Current ($V_{OUT} = 2.75\text{ V}$, $T_A = 85^\circ\text{C}$)	Figure 16
Output Voltage	vs Output Current ($V_{OUT} = 3.09\text{ V}$, $T_A = 25^\circ\text{C}$)	Figure 17
Output Voltage	vs Output Current ($V_{OUT} = 3.09\text{ V}$, $T_A = -40^\circ\text{C}$)	Figure 18
Output Voltage	vs. V_{CON} Voltage ($V_I = 4.2\text{ V}$)	Figure 19
Output Voltage	vs Output Current ($V_{OUT} = 3.09\text{ V}$, $T_A = 85^\circ\text{C}$)	Figure 20
Output Voltage V_{OUT}	vs V_{CON} Voltage	Figure 21
VCON Max Threshold	V_{OUT} $T_A = 25^\circ\text{C}$	Figure 22
VCON Max Threshold	V_{OUT} $T_A = 85^\circ\text{C}$	Figure 23
VCON Max Threshold	V_{OUT} $T_A = -40^\circ\text{C}$	Figure 24
VCON Min Threshold	V_{OUT} $T_A = 25^\circ\text{C}$	Figure 25
VCON Min Threshold	V_{OUT} $T_A = 85^\circ\text{C}$	Figure 26
VCON Min Threshold	V_{OUT} $T_A = -40^\circ\text{C}$	Figure 27
Load Transient Response $V_{OUT} = 1.3\text{ V}$		Figure 28
Load Transient Response $V_{OUT} = 3.09\text{ V}$		Figure 29
Load Transient Response $V_{OUT} = 3.09\text{ V}$		Figure 30
Load Transient Response $V_{OUT} = 3.09\text{ V}$		Figure 31
PWM Mode Operation $V_{OUT} = 1.3\text{ V}$		Figure 32
PWM Mode Operation $V_{OUT} = 3.09\text{ V}$		Figure 33
Output Voltage Ripple At High Duty Cycle Operation		Figure 34
VCON Voltage Response		Figure 35
VCON Output Voltage Response And Synchronous Applied Load Transient		Figure 36
Startup $V_{OUT} 1.3\text{ V}$		Figure 37
Startup $V_{OUT} 3.09\text{ V}$		Figure 38
Line Transient Response		Figure 39



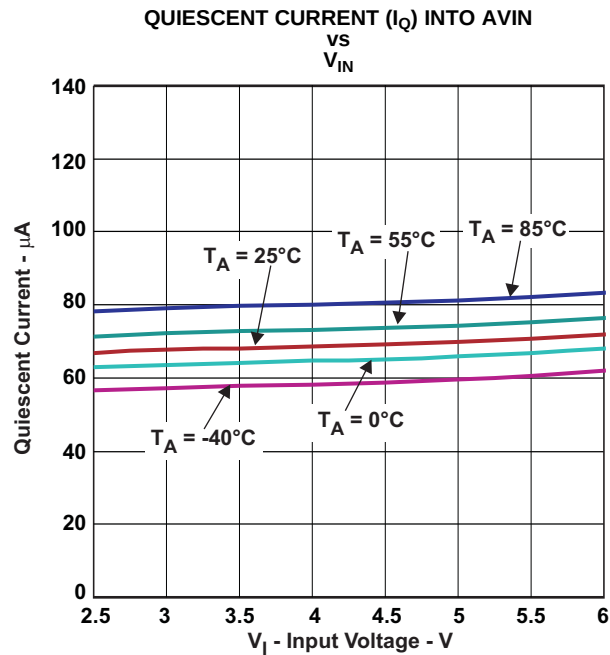


Figure 5.

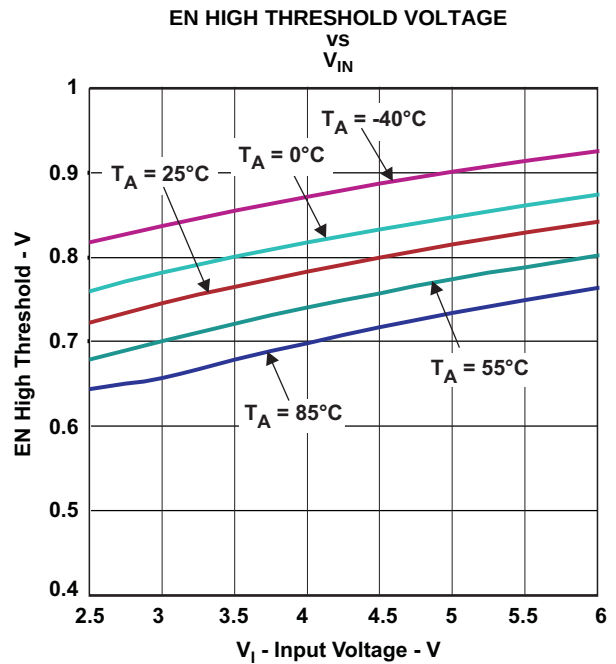


Figure 6.

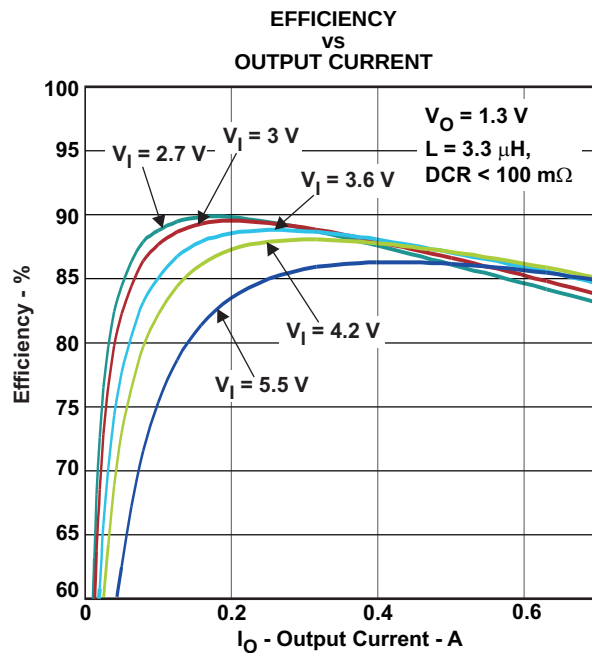


Figure 7.

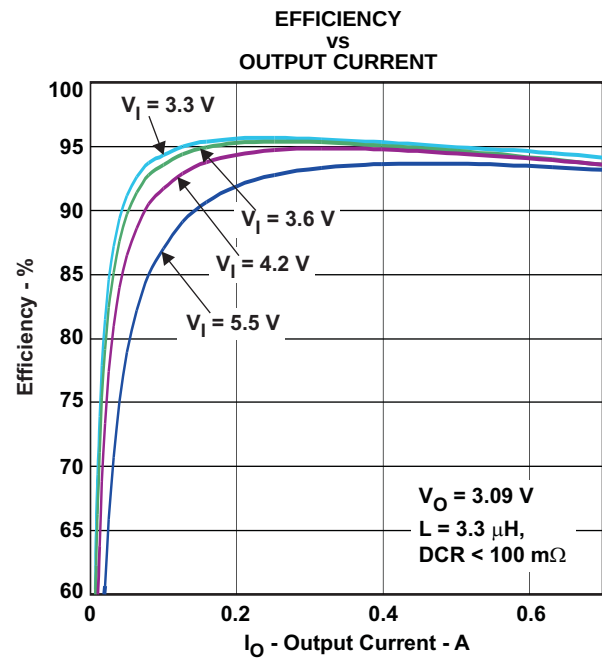


Figure 8.

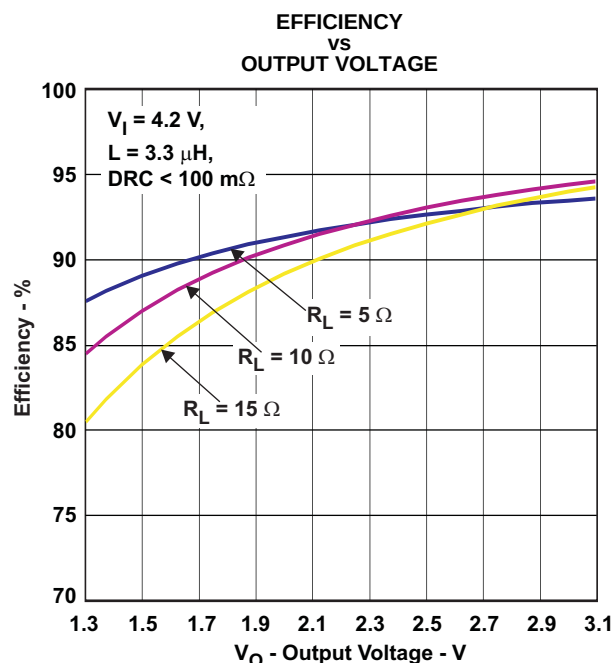


Figure 9.

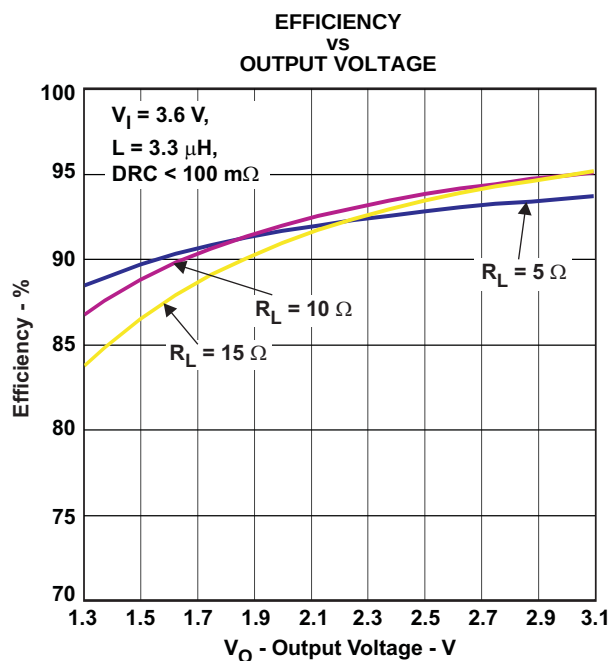


Figure 10.

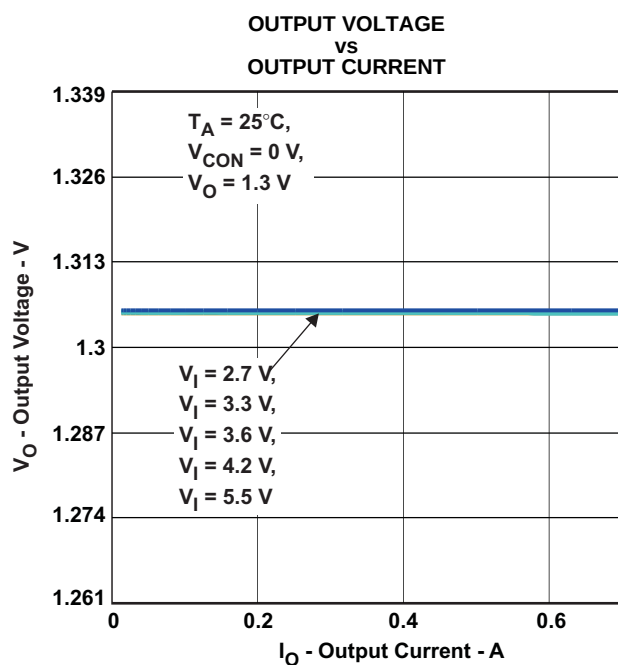


Figure 11.

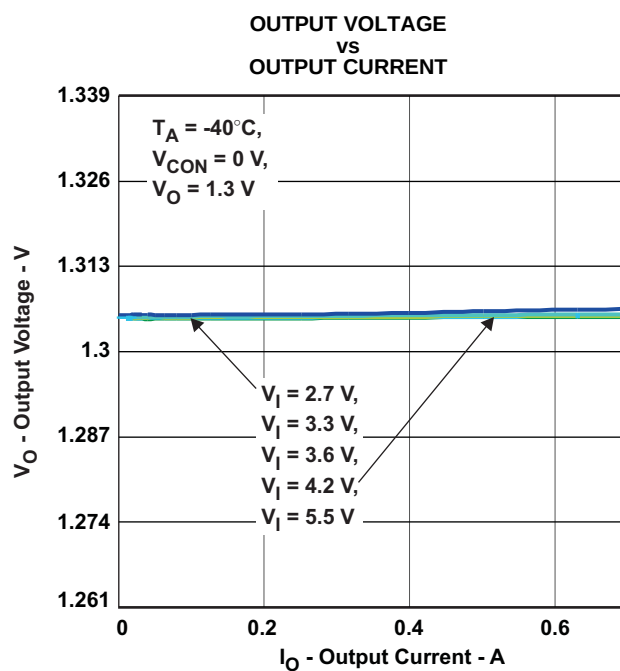


Figure 12.

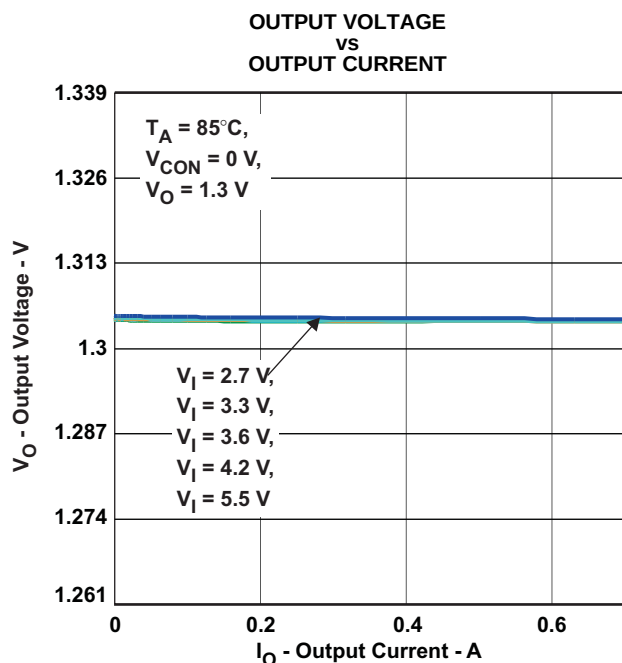


Figure 13.

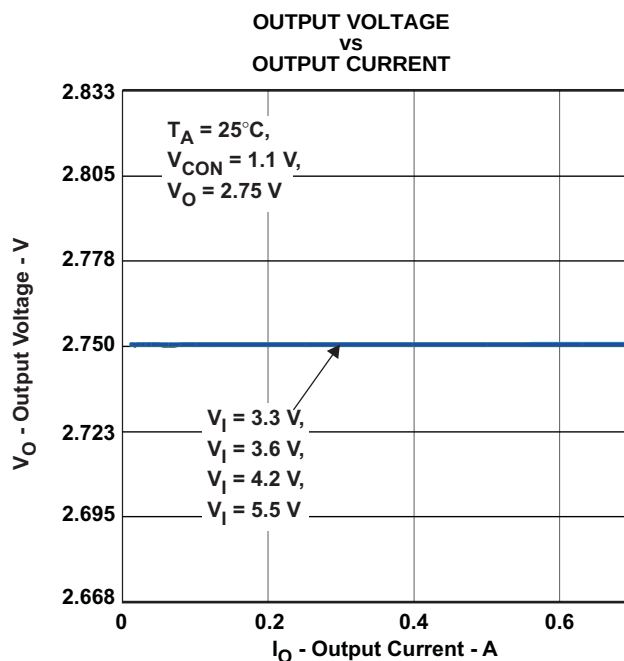


Figure 14.

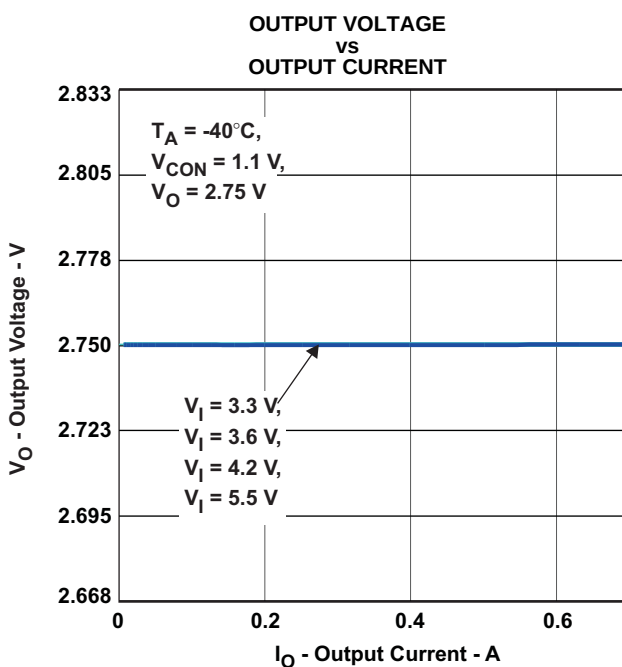


Figure 15.

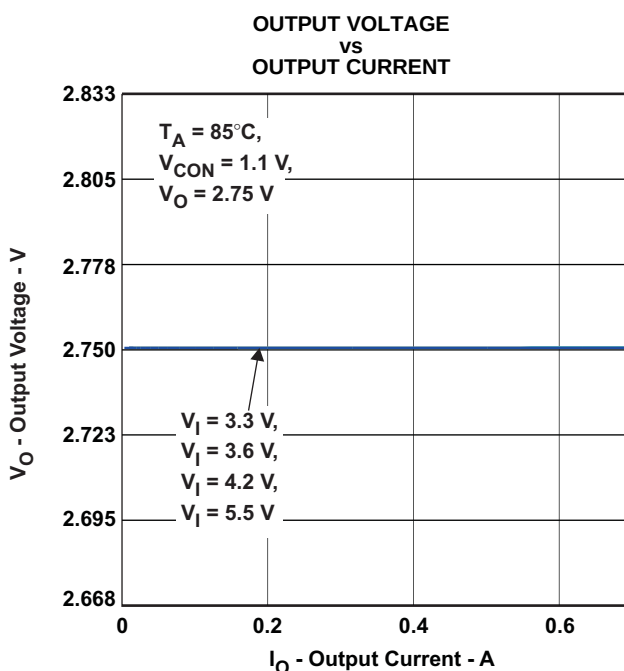


Figure 16.

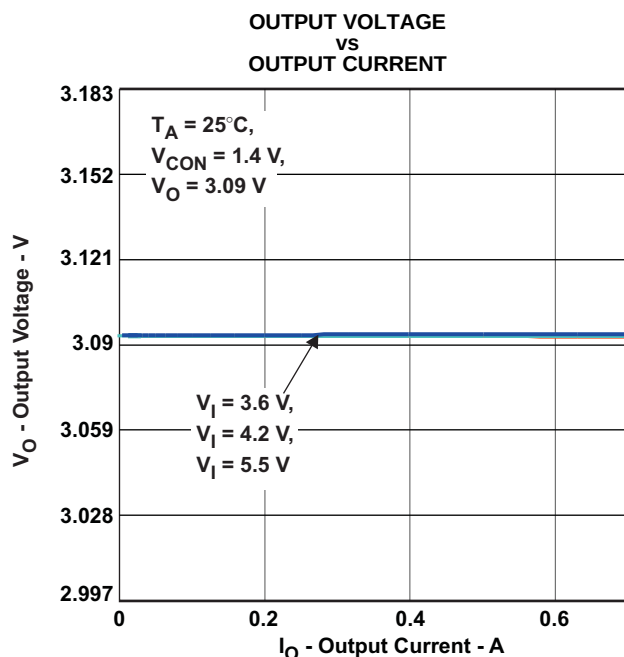


Figure 17.

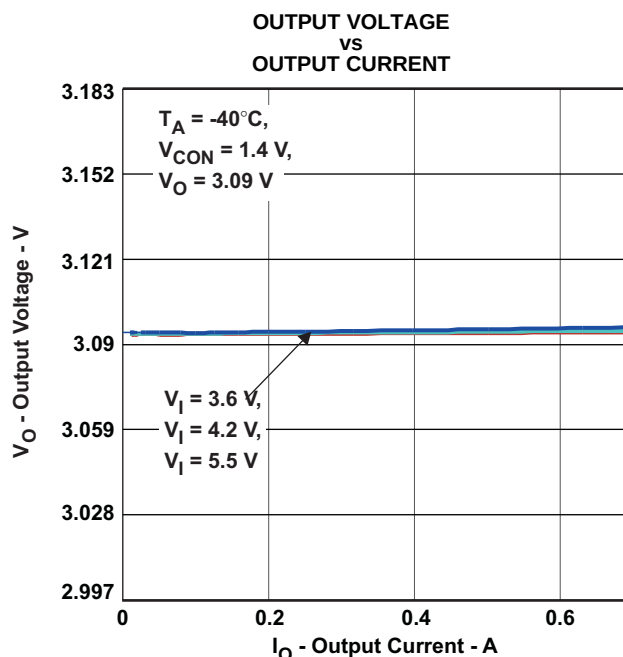


Figure 18.

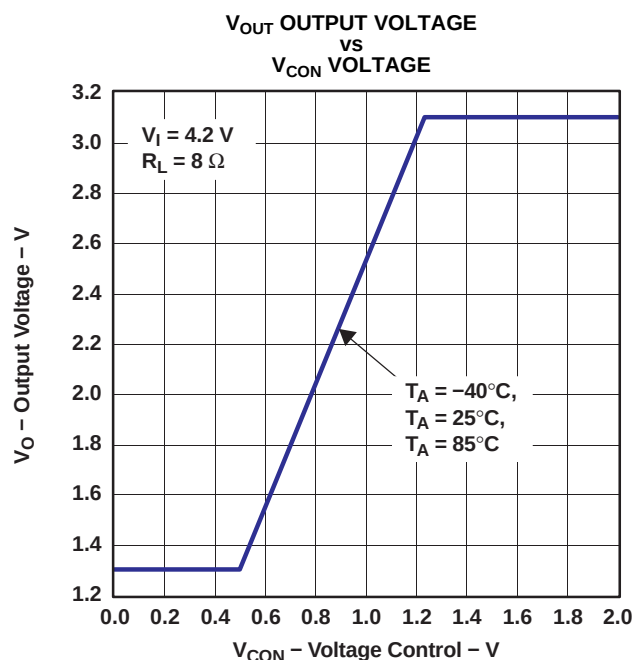


Figure 19.

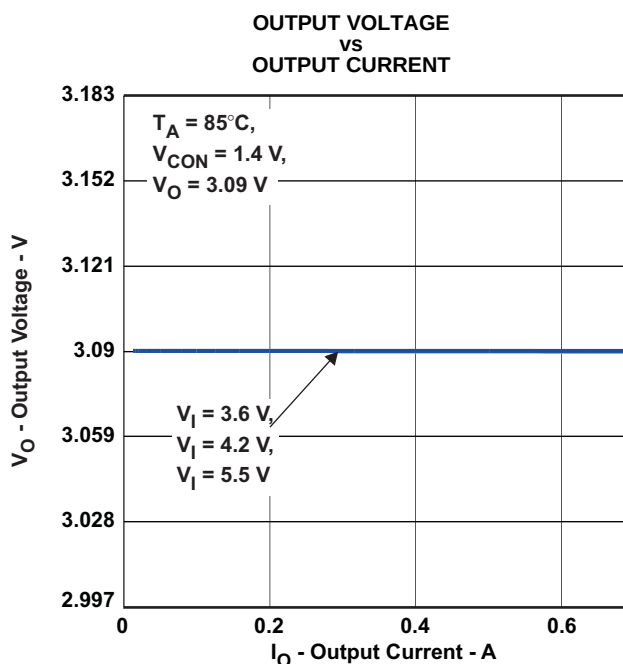


Figure 20.

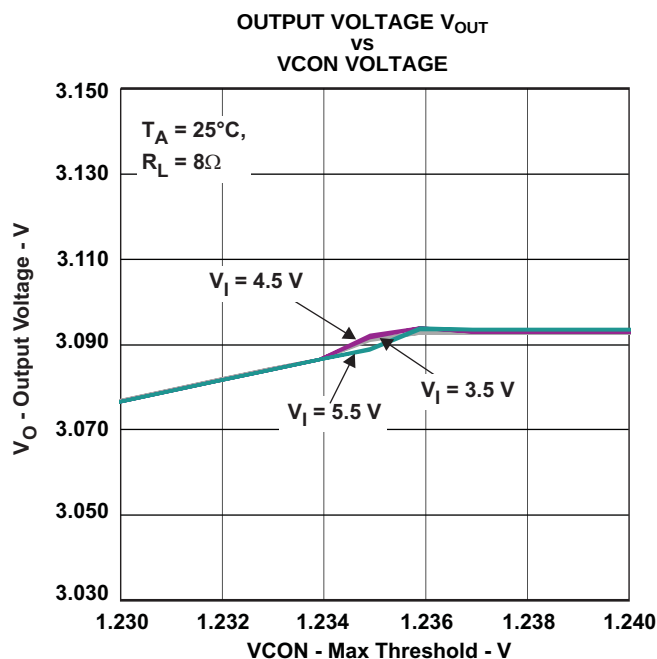


Figure 21.

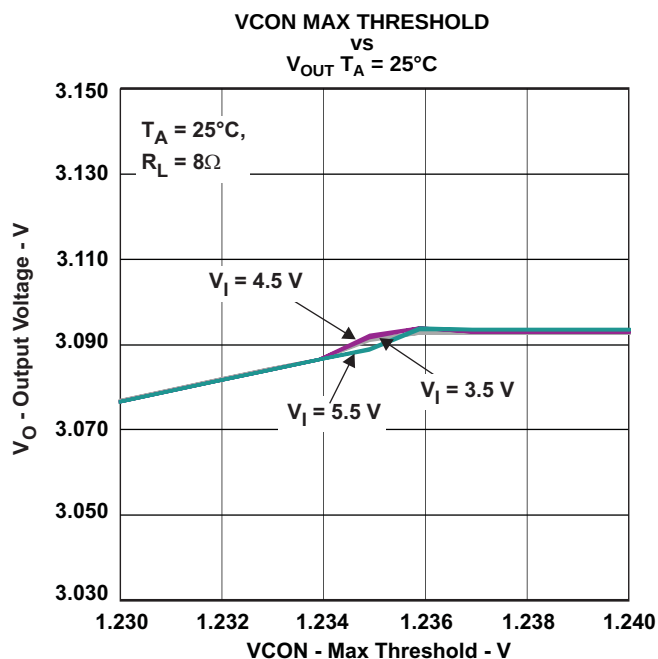


Figure 22.

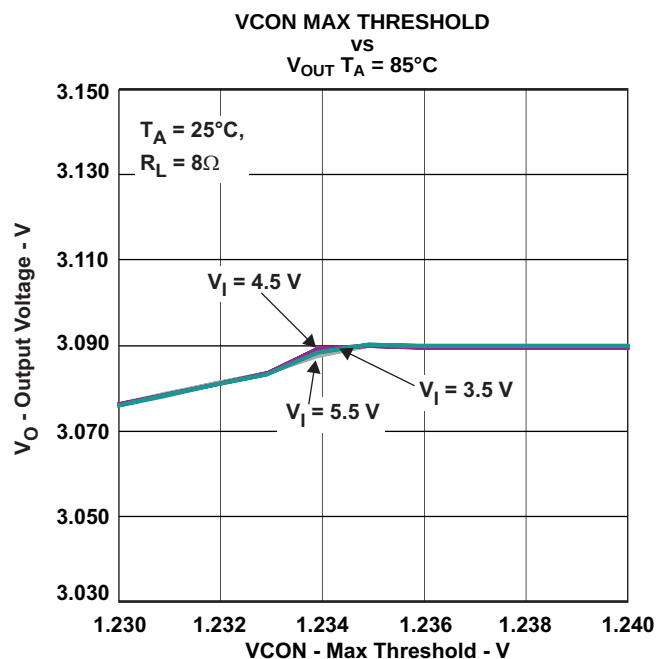


Figure 23.

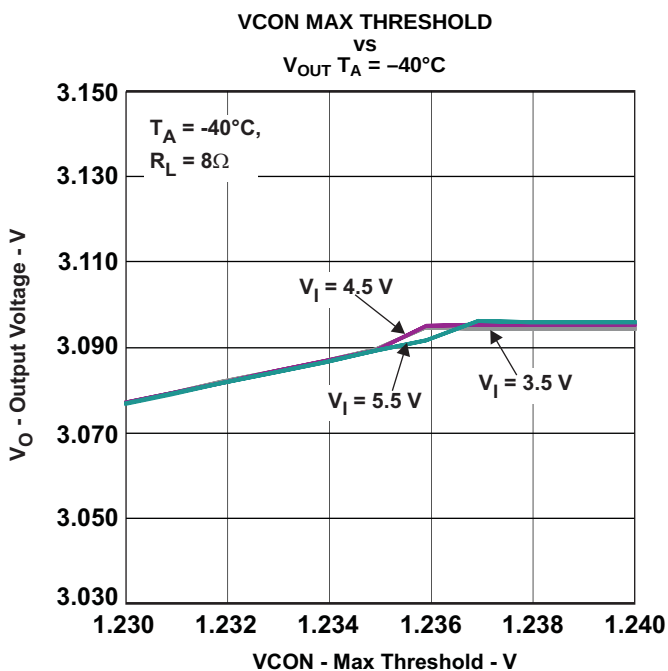


Figure 24.

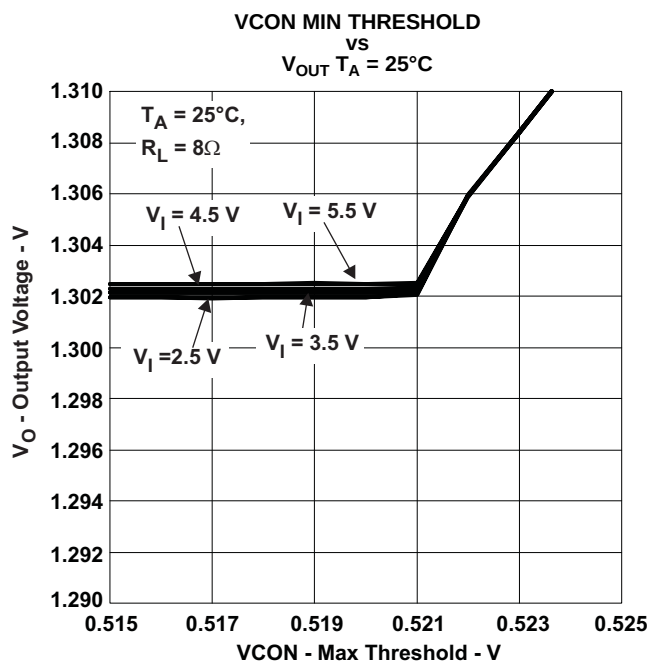


Figure 25.

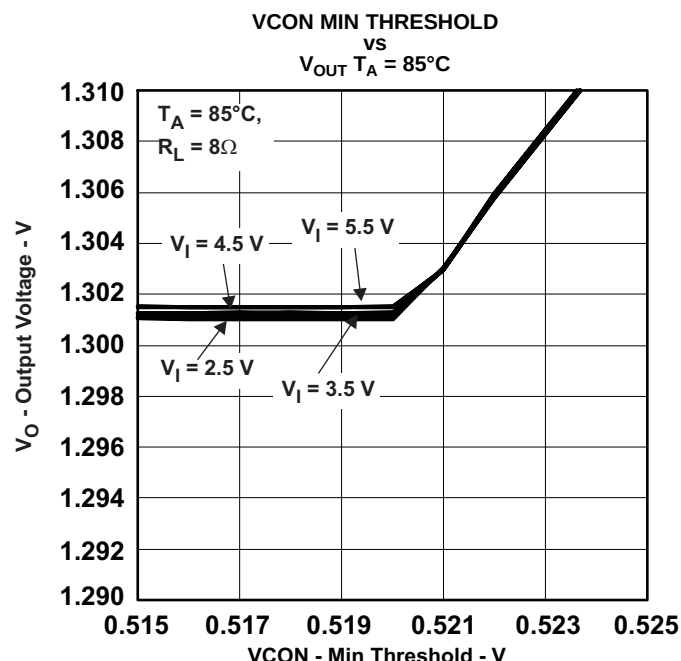


Figure 26.

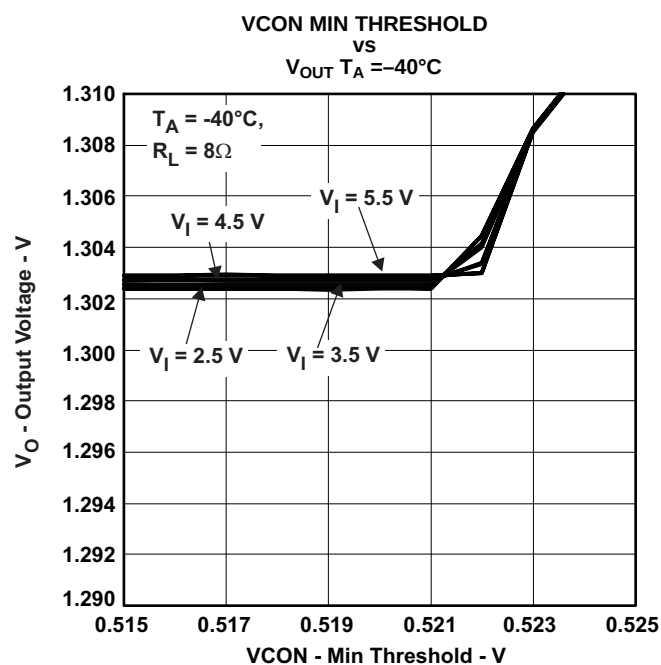


Figure 27.

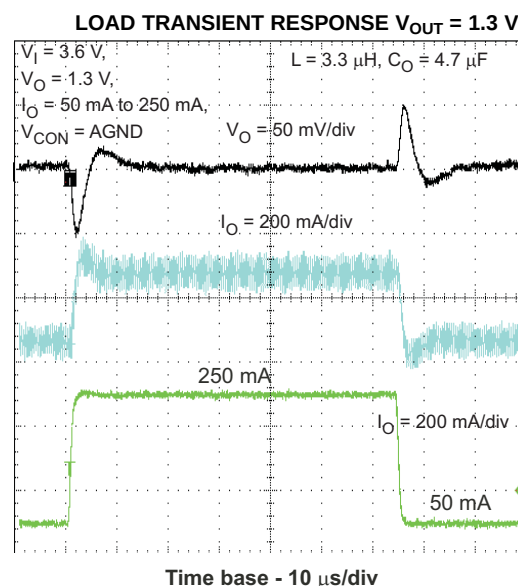


Figure 28.

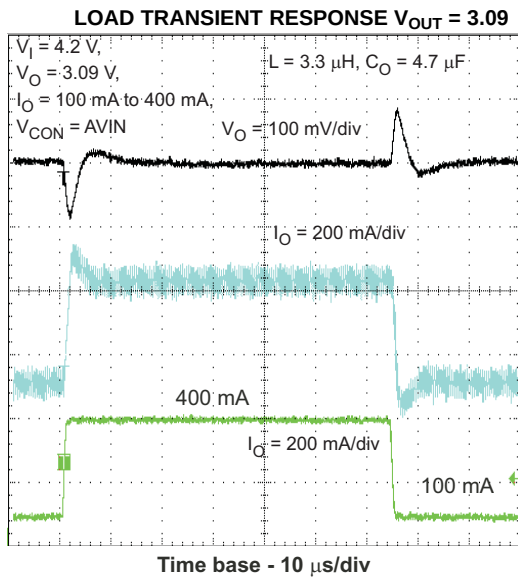


Figure 29.

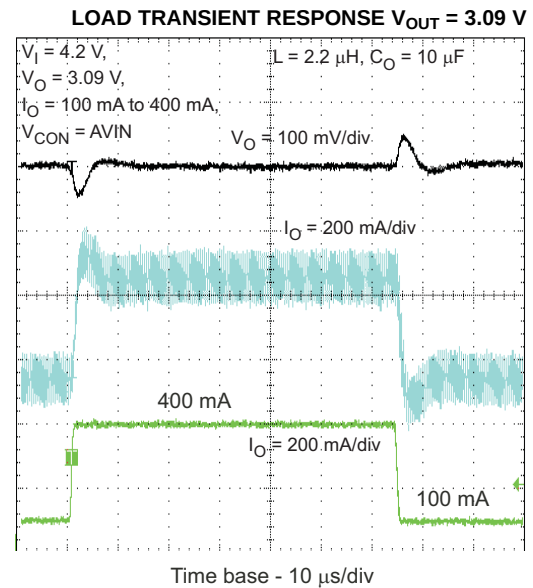


Figure 30.

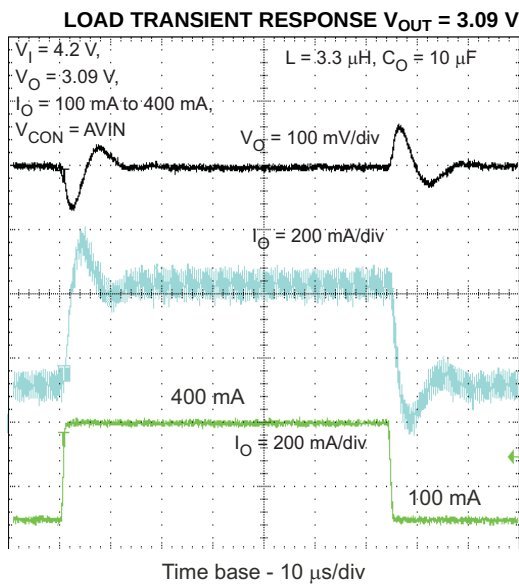


Figure 31.

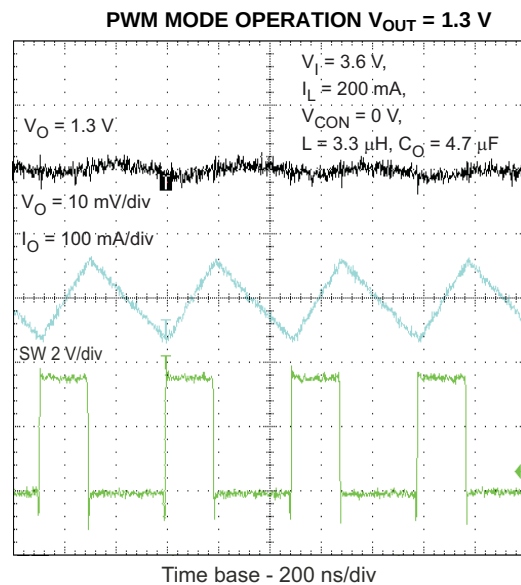


Figure 32.

PWM MODE OPERATION $V_{OUT} = 3.09\text{ V}$

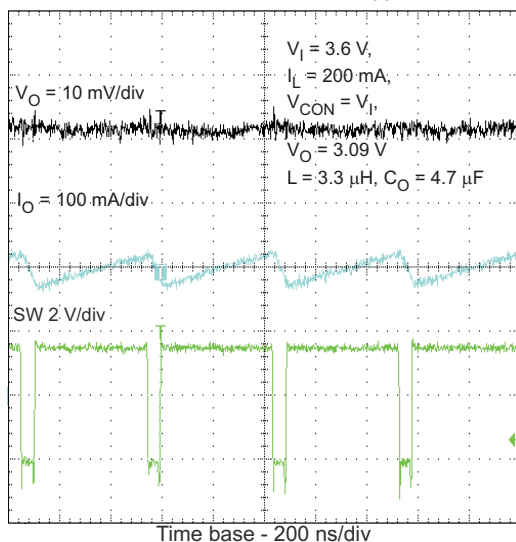


Figure 33.

OUTPUT VOLTAGE RIPPLE AT HIGH DUTY CYCLE OPERATION

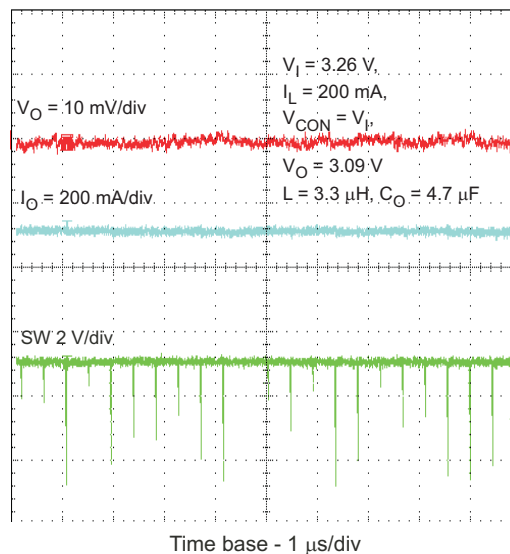


Figure 34.

VCON VOLTAGE RESPONSE

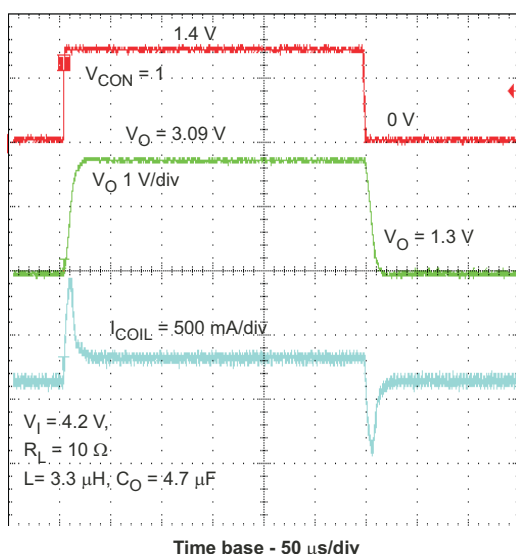


Figure 35.

VCON OUTPUT VOLTAGE RESPONSE AND SYNCHRONOUS APPLIED LOAD TRANSIENT

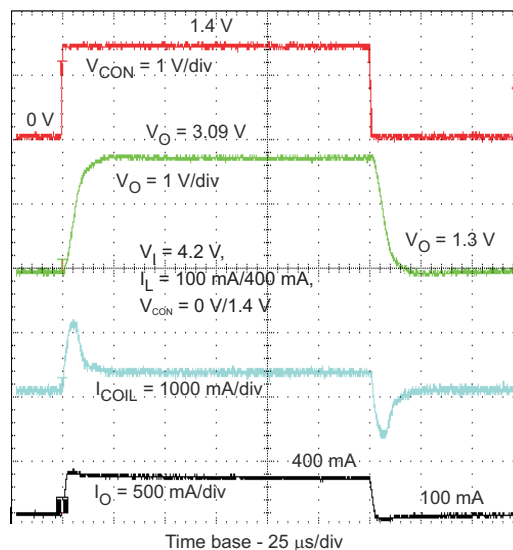


Figure 36.

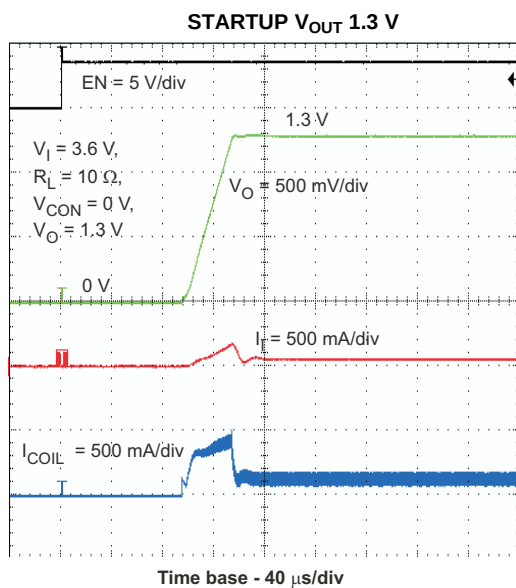


Figure 37.

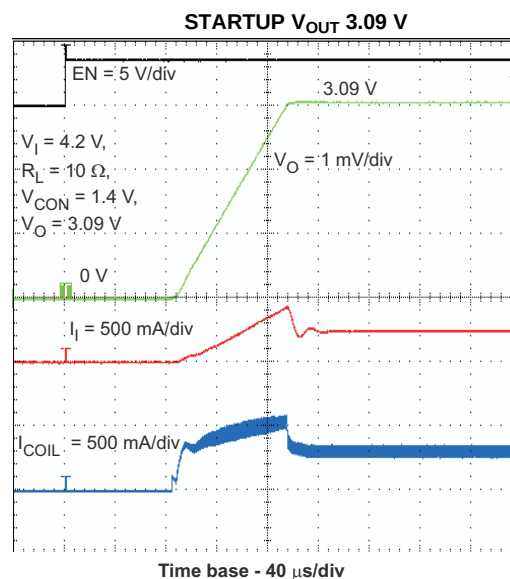


Figure 38.

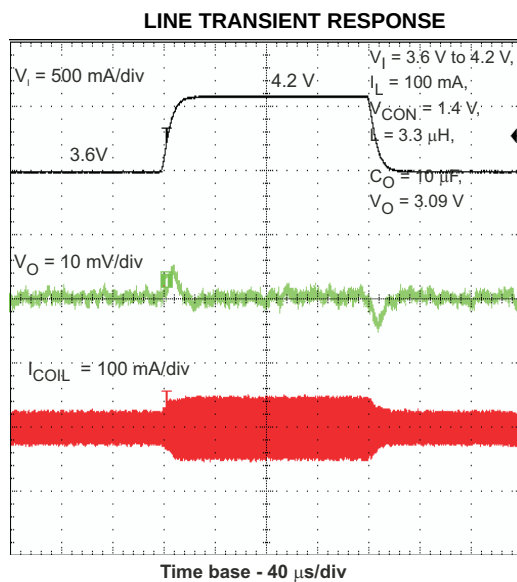


Figure 39.

APPLICATION INFORMATION

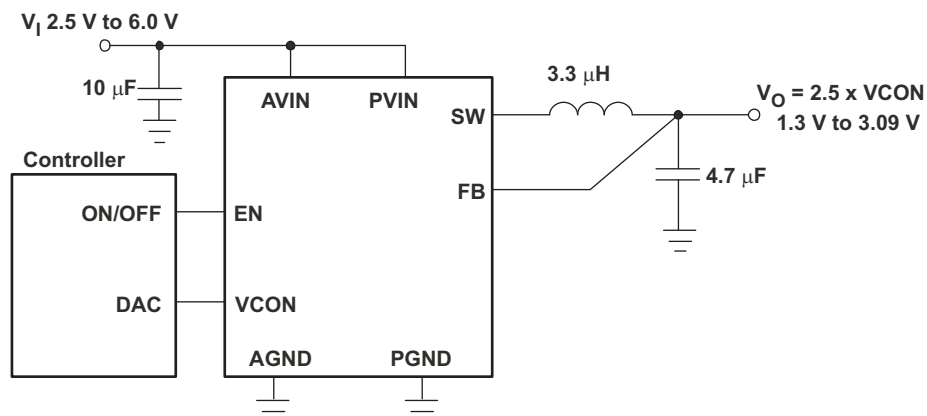


Figure 40. TPS62700 Application Circuit

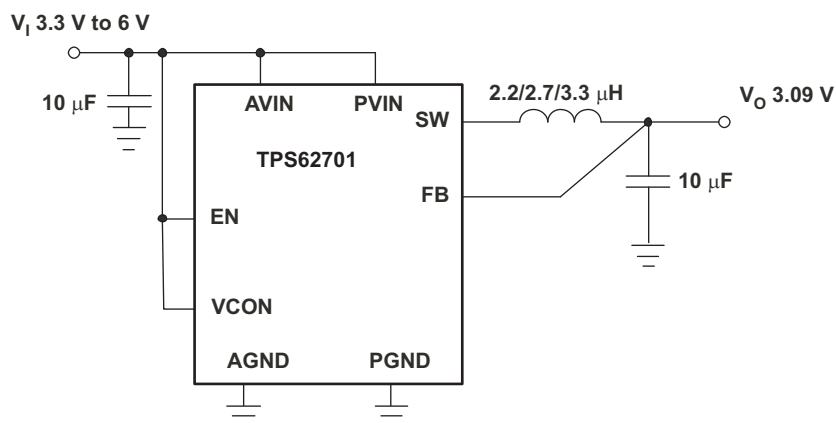


Figure 41. TPS62701 With Fixed V_{OUT} 3.09 V

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must have adequate ratings for dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT} .

[Equation 2](#) calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum peak inductor current as calculated with [Equation 3](#). This is recommended because during heavy load transients, the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \quad (2)$$

$$I_{L_MAX} = I_{OUT_MAX} + \frac{\Delta I_L}{2} \quad (3)$$

Where

f = Switching Frequency (2.0 MHz typical)

L = Inductor Value

ΔI_L = Peak to Peak inductor ripple current

I_{L_MAX} = Maximum Inductor current

A good approach is to select the inductor current and inductance rating for the maximum switch current limit of the TPS6270x.

Accepting larger values of ripple current allows the use of lower inductance values, but results in higher output-voltage ripple, greater core losses, and lower output-current capability.

The total losses of the inductor have a strong impact on the efficiency of the DC/DC conversion and consist of both the losses in the dc resistance (R_L) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic-field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 1. List Of Inductors

DIMENSIONS (mm)	INDUCTOR Series	SUPPLIER
2,5 × 2,0 × 1,2	KSLI-252012AG	Hitachi Metals
2,5 × 2,0 × 1,2	MIPSA2520	FDK
2,5 × 2,0 × 1,2	LQM2HPN	Murata
2,8 × 2,6 × 1,4	VLF3014AT	TDK
3,9 × 3,9 × 1,7	LPS4018	Coilcraft

Output Capacitor Selection

The advanced, fast-response, voltage-mode control scheme of the TPS6270x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output-voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode, and the RMS ripple current is calculated as:

$$I_{\text{RMS}C_{\text{out}}} = V_{\text{OUT}} \times \frac{1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (4)$$

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{\text{OUT}} = V_{\text{OUT}} \times \frac{1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}}{L \times f} \times \left(\frac{1}{8 \times C_{\text{out}} \times f} + \text{ESR} \right) \quad (5)$$

Input Capacitor Selection

Because of the nature of the buck converter due to its pulsating input current, a low-ESR input capacitor is required for best input-voltage filtering, and to minimize interference with other circuits caused by high input-voltage spikes. For most applications, a 10-μF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input-voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

List Of Capacitors

Size	Capacitance μF	TYPE	SUPPLIER
0603	4.7	GRM188R60J475K	Murata
0603	10	GRM188R60J106M	Murata

LAYOUT CONSIDERATIONS

As for all switching power supplies, the PCB layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to achieve the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues, as well as EMI problems. It is critical to provide a low-inductance, low-impedance ground path. Therefore, use wide, short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins PVIN and PGND. The inductor and output capacitor should be placed close to SW and PGND.

The FB line should be connected directly to the output capacitor and routed away from noisy components and traces (e.g., SW line).

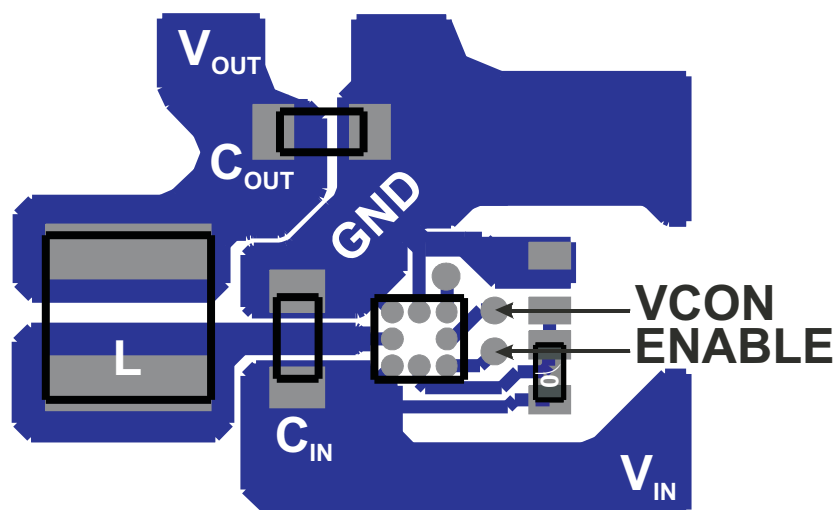
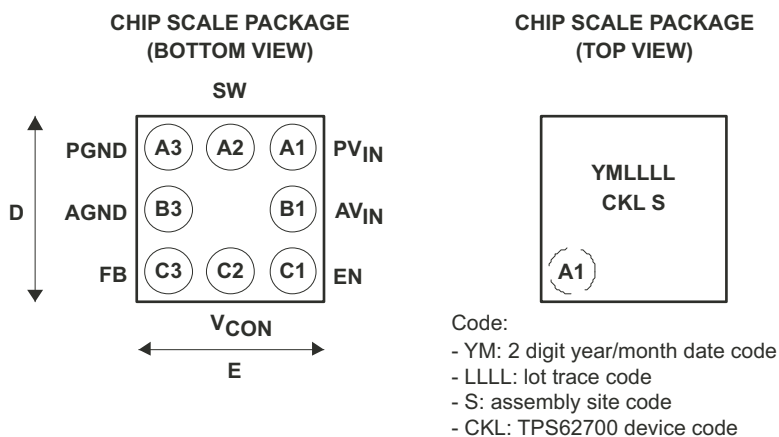


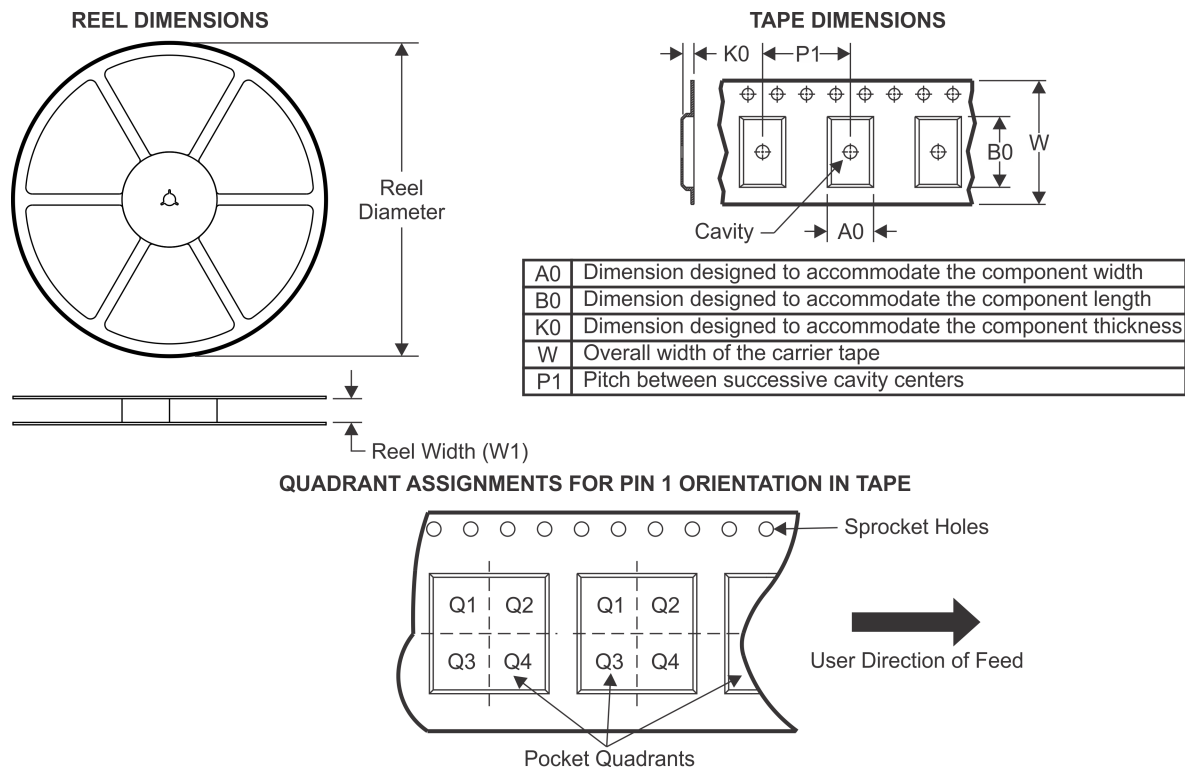
Figure 42. Suggested Board Layout

PACKAGE SUMMARY



PACKAGE DIMENSIONS

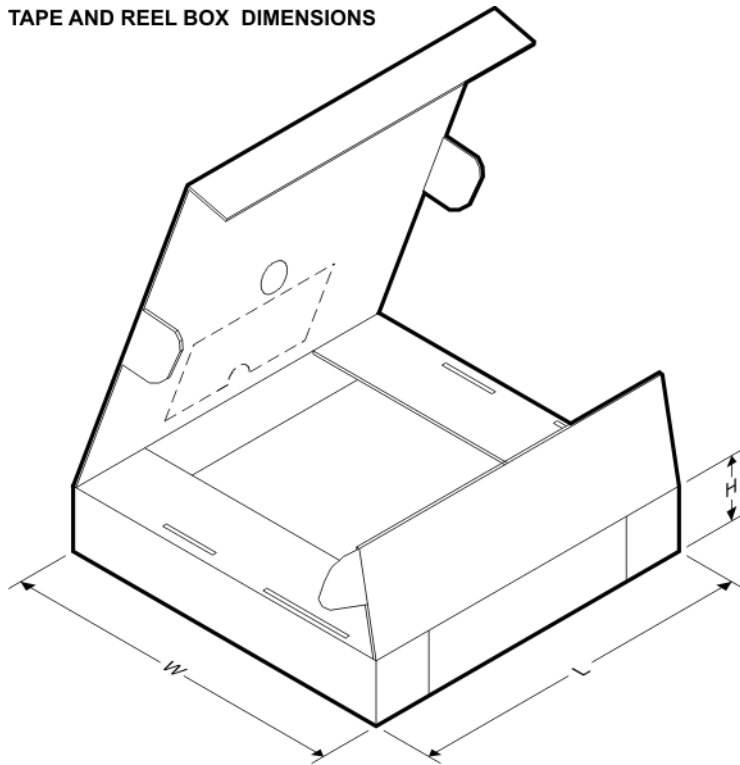
Dimension D	Dimension E2
1,64 mm ± 0,03mm	1,5 mm ± 0,03

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62700YZFR	DSBGA	YZF	8	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1
TPS62701YZFR	DSBGA	YZF	8	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

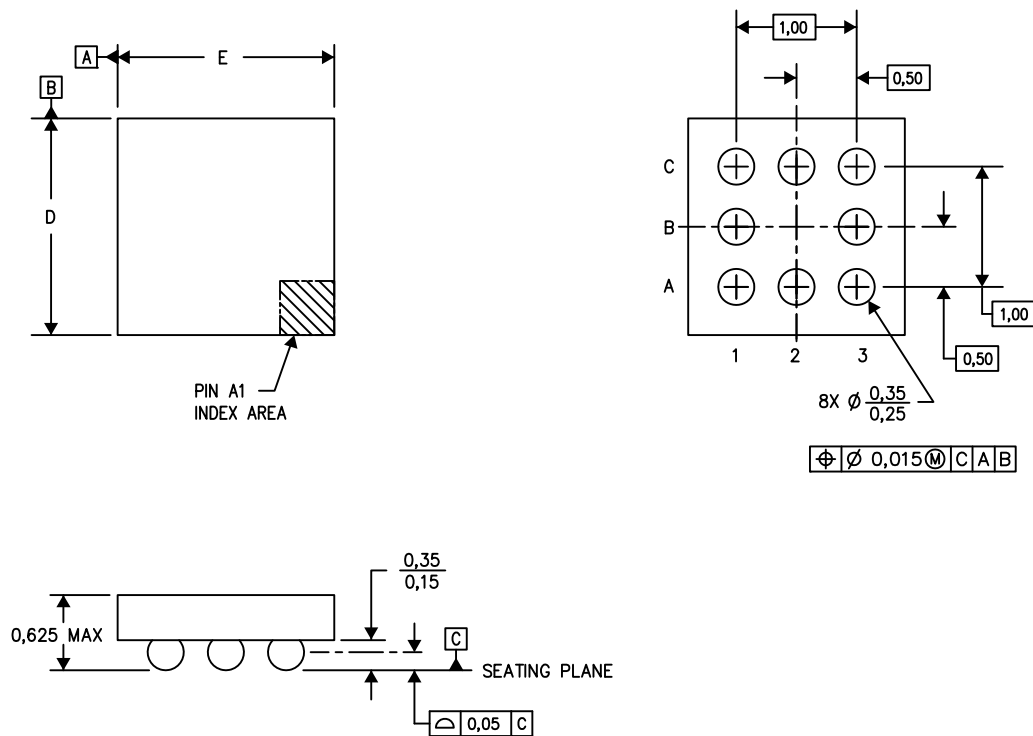


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62700YZFR	DSBGA	YZF	8	3000	182.0	182.0	20.0
TPS62701YZFR	DSBGA	YZF	8	3000	182.0	182.0	20.0

YZF (S-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



4205058-3/P 07/13

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.