

ADS7056EVM

User's Guide



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ADS7056EVM

This user's guide describes the characteristics, operation, and use of the ADS7056 evaluation module (EVM) performance demonstration kit (PDK). This kit is an evaluation platform for the ADS7056 device, which is a 14-bit, 2.5-MSPS, single-ended analog input, successive approximation register (SAR) analog-to-digital converter (ADC) that features an easy-to-use SPI. The EVM-PDK eases the evaluation of the ADS7056 device with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials.



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The following related documents are available through the [Texas Instruments](http://www.ti.com) website.

Table 1. Related Documentation

Device	Literature Number
ADS7056	SBAS769
OPA836	SLOS712
TPS79147	SLVS325
REF1933	SBOS697
SN74AVC4T245	SCES576
LM7705	SNVS420

1 Overview

The ADS7056EVM-PDK is a platform for evaluating the performance of the ADS7056 SAR ADC, which is a single-ended analog input, 14-bit, 2.5-mpsps device. The evaluation kit includes the ADS7056EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over USB for data capture and analysis.

The ADS7056EVM board includes the ADS7056 SAR ADC, all the peripheral analog circuits, and the components required to achieve optimum performance from the ADC.

The PHI controller board primarily serves three functions:

- Provide a communication interface from the EVM to the computer through a USB port
- Provide the digital input and output signals necessary to communicate with the ADS7056 device
- Supply power to all active circuitry on the ADS7056EVM board

Along with the ADS7056EVM and PHI controller board, this evaluation kit includes an A-to-micro-B USB cable to connect to a computer.

1.1 ADS7056EVM-PDK Features

The ADS7056EVM-PDK includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS7056 ADC
- USB powered — no external power supply is required
- The PHI controller board that provides a convenient communication interface to the ADS7056 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for Microsoft® Windows® 7, 64-bit operating systems

1.2 ADS7056EVM Features

The ADS7056EVM includes the following features:

- Onboard low-noise, low-distortion ADC input drivers optimized to meet ADC performance
- Onboard ultra-low noise, low-dropout (LDO) regulators, to generate supplies for the operation amplifier and voltage reference to generate the power supply for ADC

2 Analog Interface

The ADS7056EVM is a low-power, small ADC that supports single-ended analog inputs. The ADS7056EVM uses an OPA836 amplifier to drive the inputs of the ADC. The ADS7056EVM is designed for easy interfacing to analog sources. This section describes driver details, including jumper configuration for the analog input signal source.

2.1 Connectors for Single-Ended Analog Input

The ADS7056EVM is designed for easy interfacing to an external, analog, single-ended source through a subminiature version A (SMA) connector or 100-mil headers. J1 is the SMA connector that allows analog source connectivity through coaxial cables. Alternatively, 100-mil jumper cables or mini-grabbers can be used to connect analog sources to the J6:1 pin. [Table 2](#) lists the analog input connectors.

Table 2. Analog Input Connector Description

Pin Number	Signal	Description
J1	INP	Positive single-ended input provided at the SMA
J6:1	INP	Alternate location to provide the positive single-ended input

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2.2 ADC Single-Ended Input Signal Driver

SAR ADC inputs terminate in switched-capacitor networks that create large instantaneous current loads when the switches are closed, which effectively makes the ADC inputs dynamically low impedance. The single-ended input of the ADS7056EVM are therefore driven by an OPA836 device used in a noninverting, unity-gain configuration to maintain ADC performance with maximum loading at full device throughput of 2.5 msp/s.

2.2.1 Input Signal Path

Figure 1 shows the signal path for positive single-ended input applied to the ADS7056EVM. An OPA836 amplifier is used in buffer configuration and it drives single-ended input of ADS7056EVM. An RC filter value of 33 Ω and 680 pF are selected to achieve SINAD greater than 75 dB and THD less than -85 dB for 2-kHz sine wave input at full throughput of 2.5 msp/s.

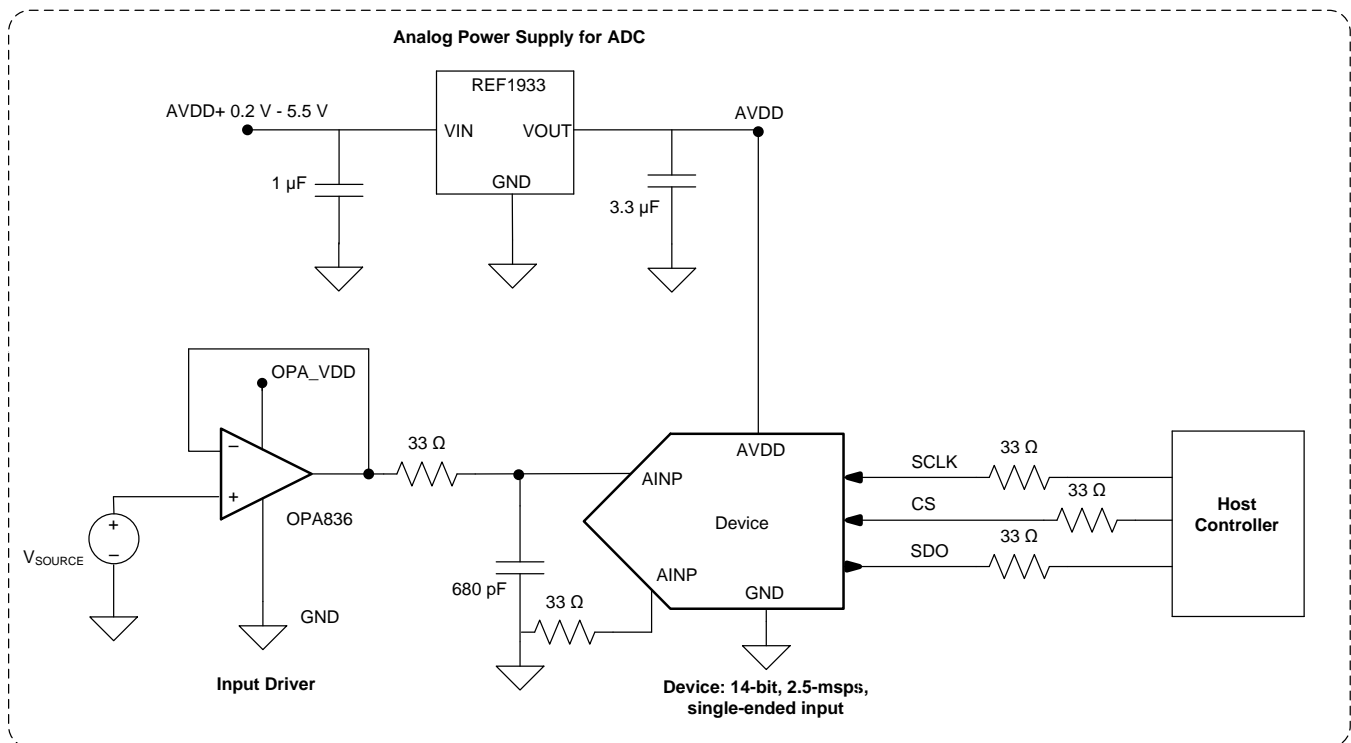


Figure 1. ADS7056EVM Analog Input Path

3 Digital Interfaces

As noted in Section 1, the EVM interfaces with the PHI, which in turn communicates with the computer over USB. The two devices on the EVM that the PHI communicates with are the ADS7056 ADC (over SPI) and the EEPROM (over I2C). The EEPROM comes preprogrammed with the information required to configure and initialize the ADS7056EVM-PDK platform. When the hardware is initialized, the EEPROM is no longer used.

3.1 SPI for ADC Digital I/O

The ADS7056EVM-PDK supports interface and calibration modes detailed in the [Ultra-Low Power, Ultra-Small Size, 14-Bit, 2.5-MSPS, SAR ADC](#) data sheet. The PHI is capable of operating at a 3.3-V logic level and is directly connected to the digital I/O lines of the ADC.

The buffer SN74AVC4T245 (U8) is included in the design to ensure that, if required, the SDO can be driven to a host controller over long cables with minimal distortion.

4 Power Supplies

The device supports a wide range of operation on its analog supplies. The AVDD can operate from 2.35 V to 3.6 V. The DVDD operates from 1.65 V to 3.6 V, independent of the AVDD supply. The analog portion of the device operates from a 5.5-V supply, which in turn generates a 4.7-V V_{DD} supply for the OPA836 operation amplifier using the low-noise, fixed voltage regulator, TPS79147. The 3.3-V AVDD supply for the ADS7056EVM is generated using the low-drift, low-power, voltage reference REF1933.

There is provision given onboard to use an adjustable version of the TPS79901 regulator, to generate a V_{DD} supply other than 4.7 V. [Table 3](#) lists the feedback resistor values to be populated onboard to generate the desired V_{DD} supply voltage.

Table 3. Voltage Settings for AVDD and V_{DD} Supplies

Output Voltage	Device (U6)	C24	R24	R23	C7 and C11
4.7 V (default)	TPS79147 (default)	10 nF (default)	Not installed (default)	Not installed (default)	Not installed (default)
3.3 V	TPS79901	Open	53.6 k Ω	30.1 k Ω	15 pF
3.6 V	TPS79901	Open	60.4 k Ω	30.1 k Ω	15 pF
4.83 V	TPS79901	Open	90.9 k Ω	30.1 k Ω	15 pF

There is provision given for operating the OPA836 operational amplifier and the ADS7056 ADC from the common power supply AVDD. [Table 4](#) lists the modifications required to select a common power supply for the OPA836 and ADS7056 devices.

Table 4. V_{DD} Voltage Selection Settings

OPA836 Supply Source	R10	R11
V_{DD} (default 4.7 V)	Assembled (0 Ω)	Not installed
AVDD	Not installed	Assemble (0 Ω)

The rail-to-rail amplifier cannot output zero volts when operating from a single-supply voltage and can introduce an error at the output when the input signal is near zero. To enable the amplifier output swing to zero volts, the Vs-pin of the OPA836 device is powered from the LM7705 device, which is a -0.23 -V, low-noise, fixed voltage regulator. However, there is provision given to connect the Vs-pin of the OPA836 device to the ground plane. To drive the Vs-pin of the OPA836 device to GND, R9 must be assembled and R18 must be removed.

The digital portion of the ADC operates from a 3.3-V supply, EVM_DVDD from the PHI.

5 ADS7056EVM-PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for proper operation of the ADS7056EVM-PDK.

5.1 Default Jumper Settings

Figure 2 shows the silkscreen plot, which details the jumper locations for ADS7056EVM-PDK.

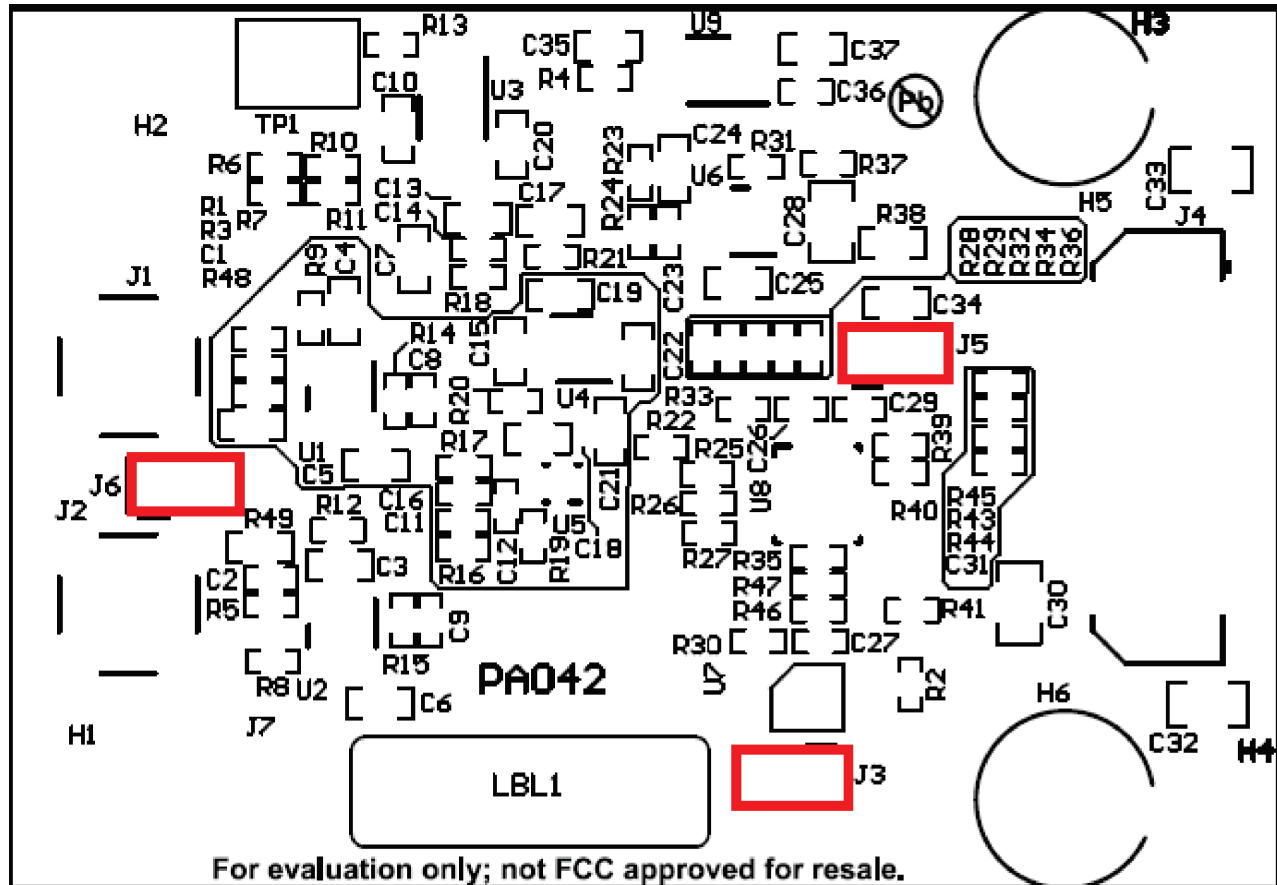


Figure 2. ADS7056EVM-PDK Jumper Locations

Table 5 lists the functionality and default configuration of each jumper. No shunts are required on any location of the EVM for normal operation. Remove any shunts that may be present at locations J3 through J6.

Table 5. Default Jumper Configurations

Reference Designator	Default Configuration	Description
J3	Open	EEPROM write protection
J4	Open	Bias voltage output
J6	Open	Alternate location to provide the positive single-ended input

5.2 EVM Graphical User Interface Software Installation

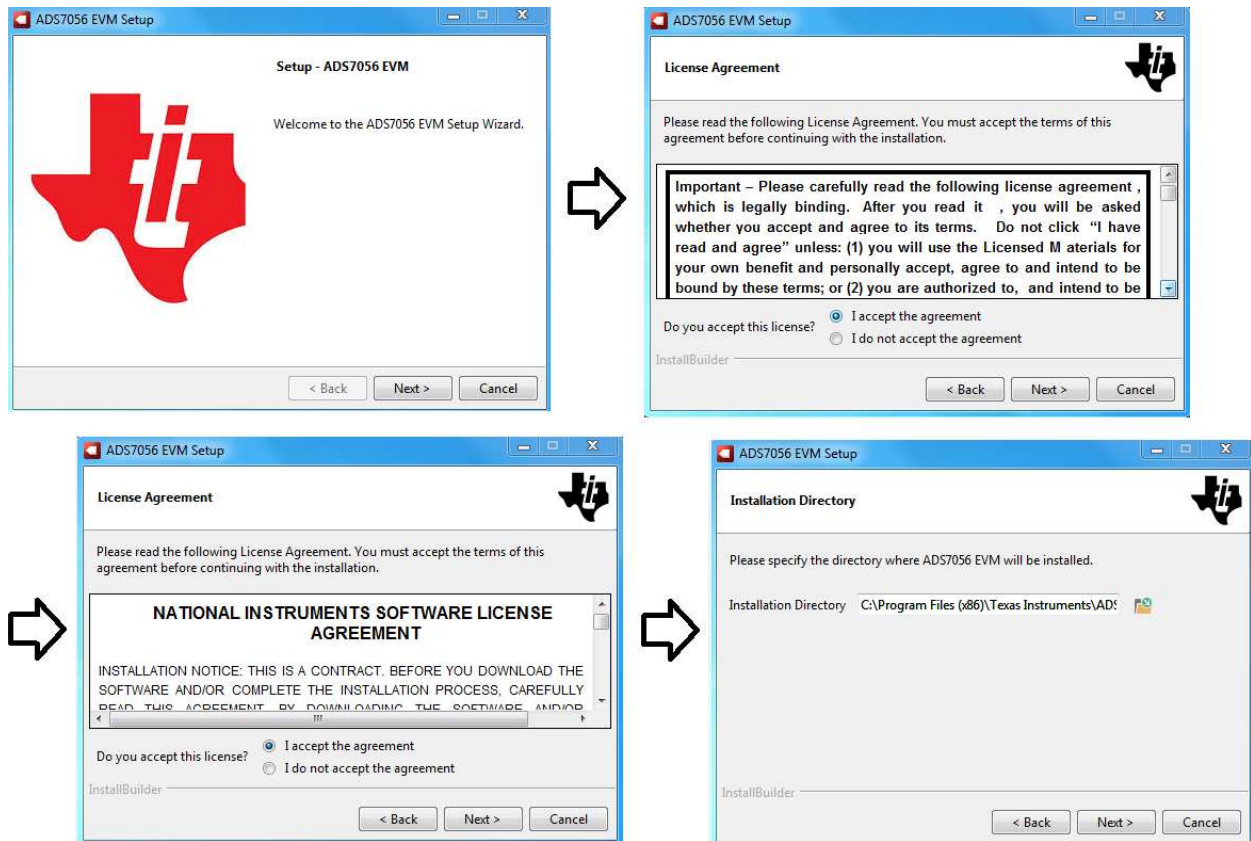
The following steps describe how to install the software for the EVM GUI.

1. Download the latest version of the EVM graphical user interface (GUI) installer from the *Tools and Software* folder of the device, and run the GUI installer to install the EVM GUI software on your computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Failure to disable antivirus software, depending on the antivirus settings, may cause an error message to appear or the *installer.exe* file may be deleted.

2. Accept the License Agreements and follow the on-screen instructions to complete the installation (see Figure 3).



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Figure 3. ADS7056EVM Software Installation Prompts

- As a part of the ADS7056EVM GUI installation, a prompt with a Device Driver Installation Wizard appears on the screen (see Figure 4). Click the *Next* button to proceed, then click the *Finish* button when the installation is complete.

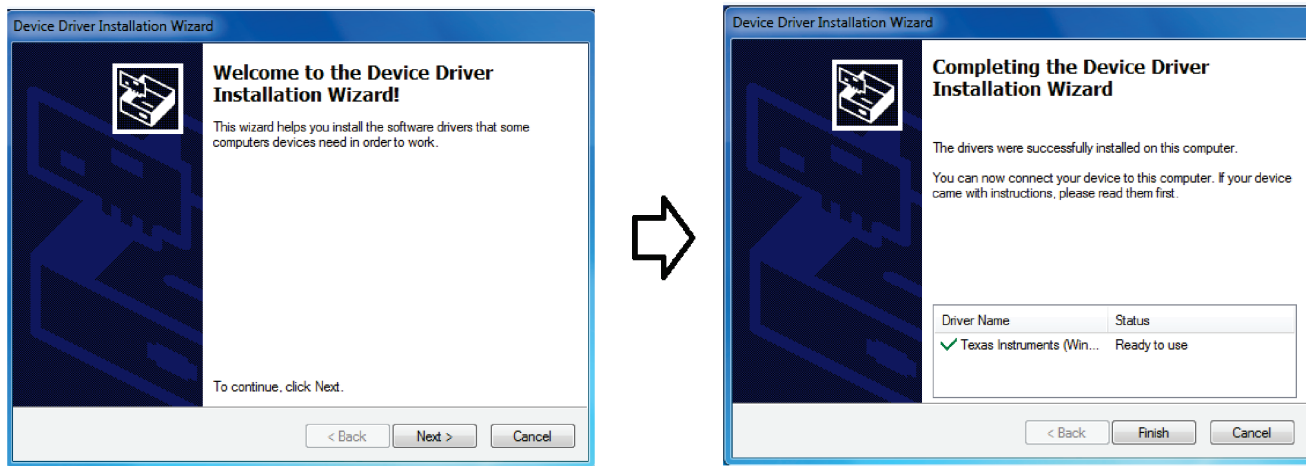


Figure 4. Device Driver Installation Wizard Prompts

NOTE: A notice may appear on the screen stating that Windows cannot verify the publisher of this driver software. Select the *Install this driver software anyway* option.

The device requires the LabVIEW™ Run-Time Engine (see Figure 5) and may prompt for the installation of this software, if not already installed.

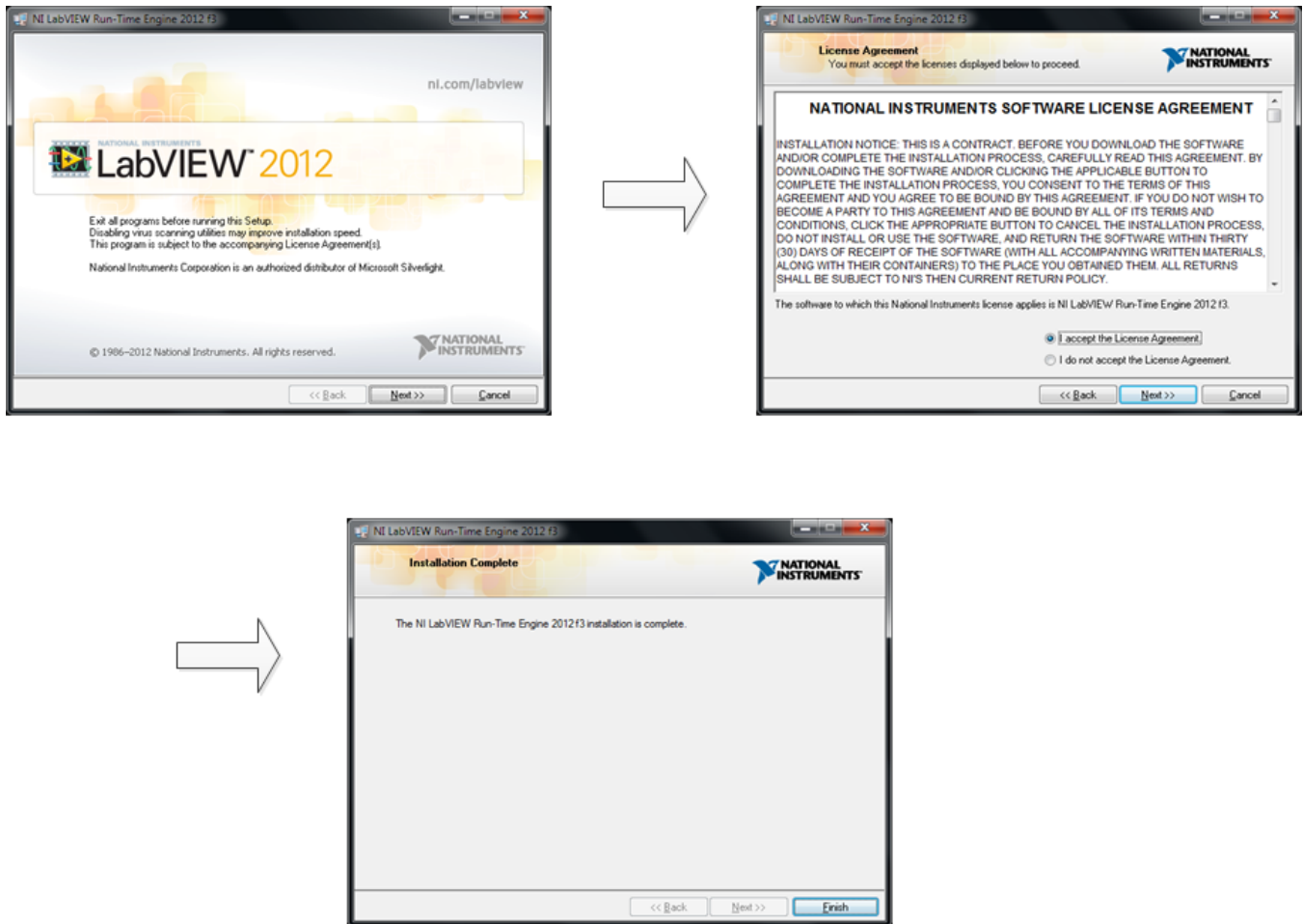
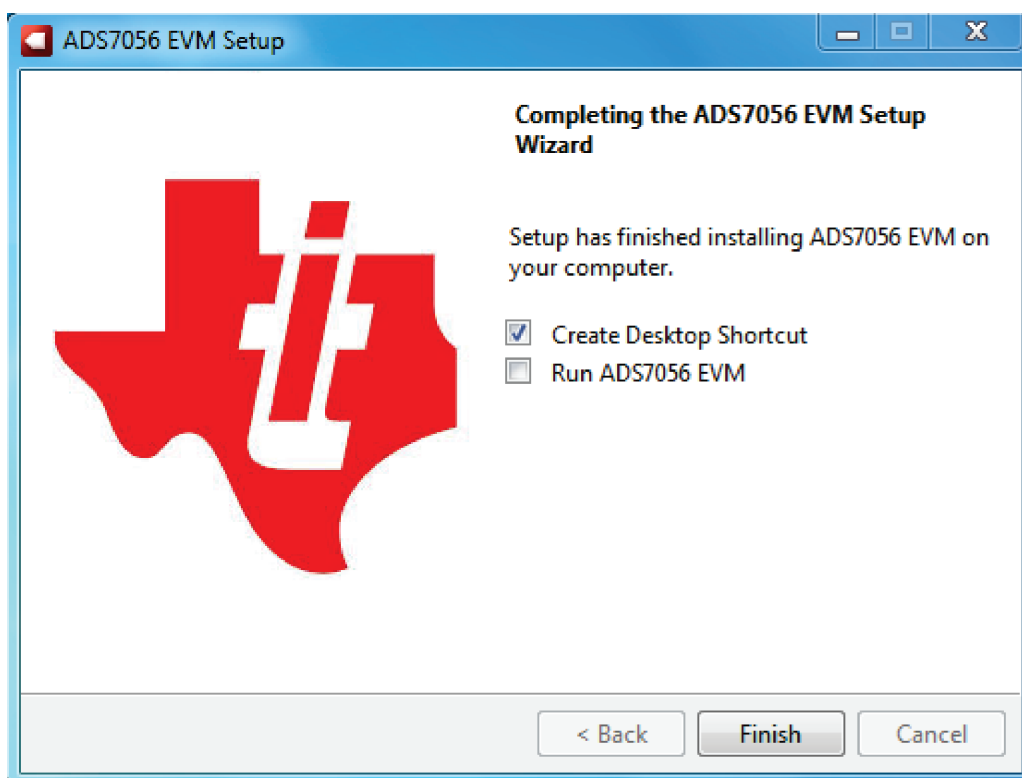


Figure 5. LabVIEW Run-Time Engine Installation

4. After these installations, check the *Create Desktop Shortcut* box, as shown in [Figure 6](#).



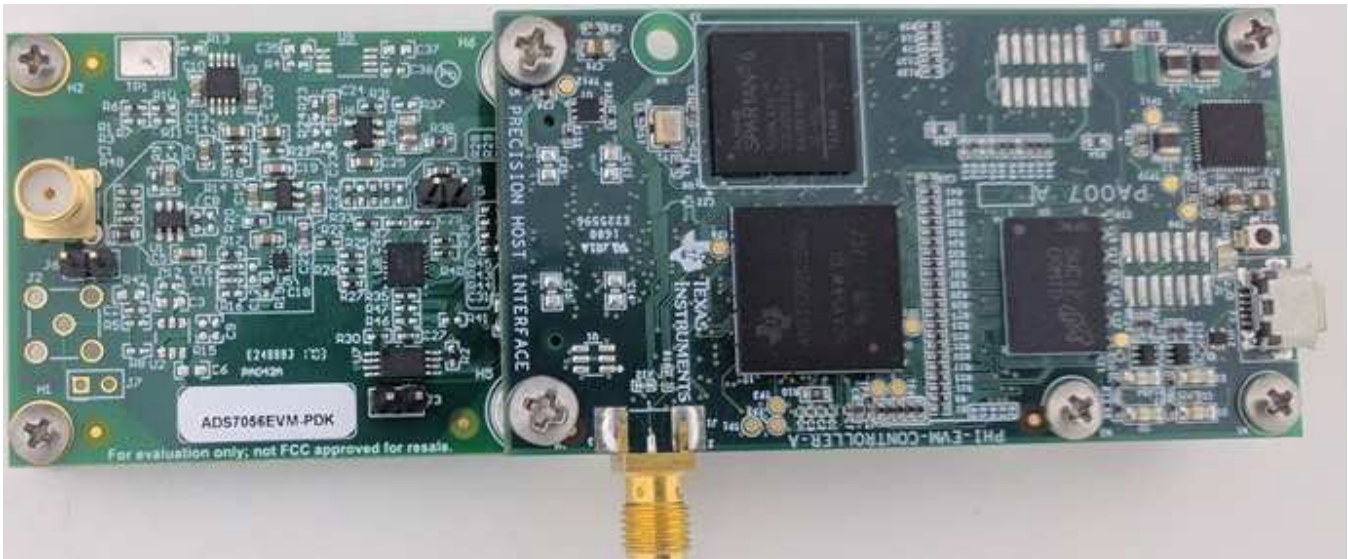
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Figure 6. ADS7056EVM-PDK Installation Final Step

6 ADS7056EVM-PDK Operation

The following instructions are a step-by-step guide to connecting the device to the computer and evaluating the performance of the device.

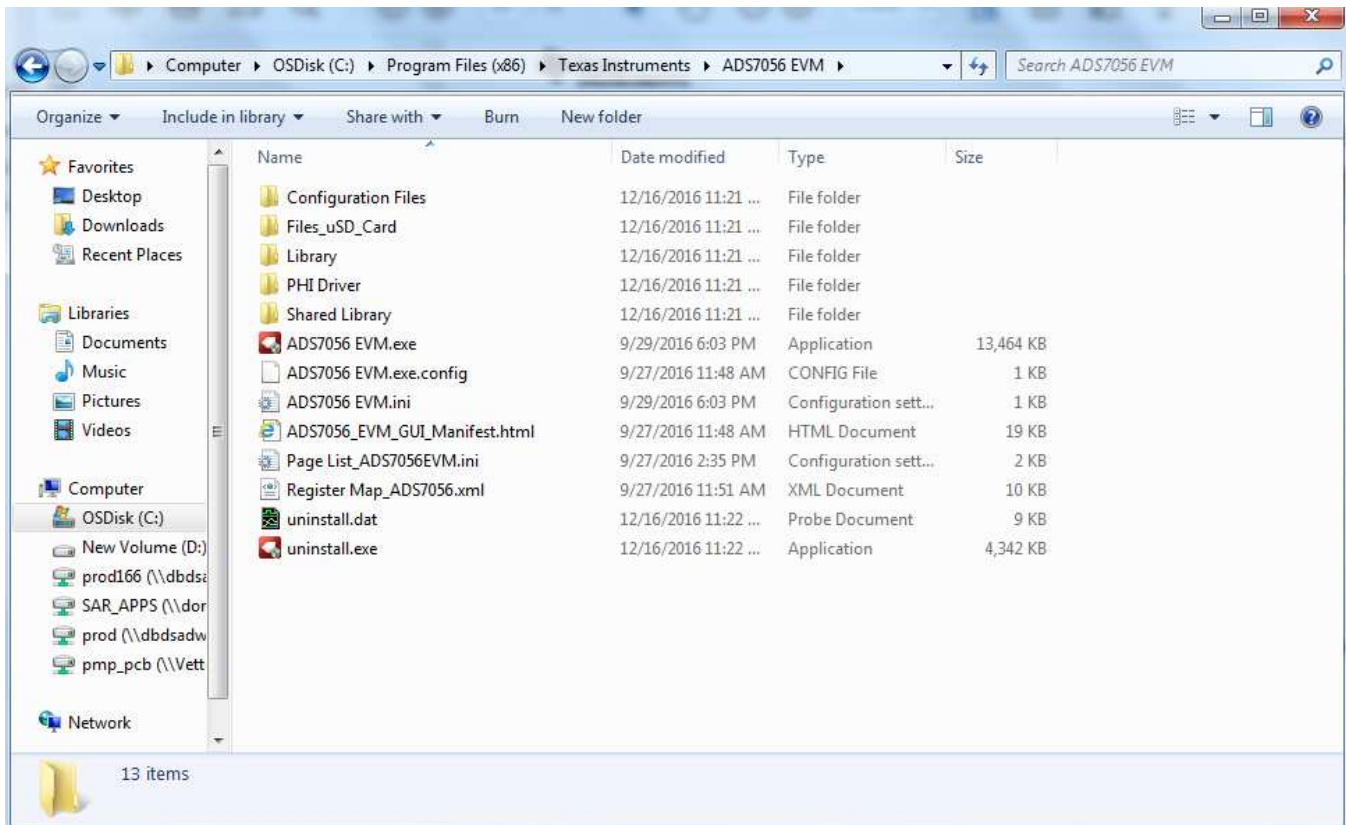
1. Connect the device EVM to the PHI board. Install the two screws as indicated in [Figure 7](#).
2. Use the provided USB cable to connect the PHI to the computer.
 - LED D5 on the PHI lights up, indicating that the PHI is powered up.
 - LEDs D1 and D2 on the PHI start flashing, indicating that the PHI is booted up and communicating with the PC.



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Figure 7. EVM-PDK Hardware Setup and LED Indicators

3. Launch the device EVM GUI software from the installed path, as shown in [Figure 8](#), or using the desktop shortcut created during installation.

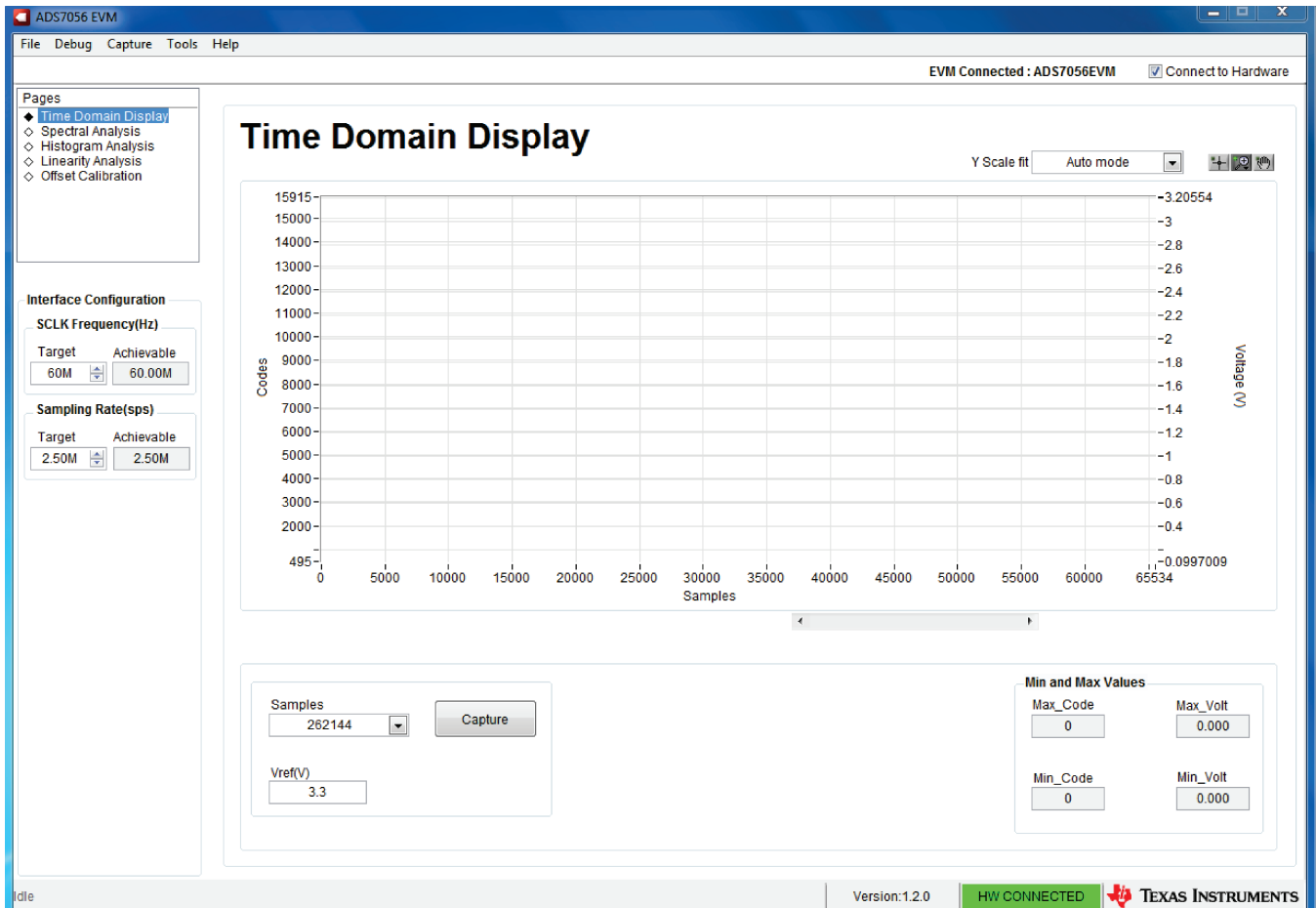


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Figure 8. Launch the EVM GUI Software

6.1 EVM GUI Global Settings for ADC Control

Figure 9 shows the input parameters of the GUI (as well as their default values), through which the various functions of the ADS7056EVM can be exercised. These settings are global because they persist across the GUI tools listed in the top left pane (or from one page to another).



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Figure 9. EVM GUI Global Input Parameters

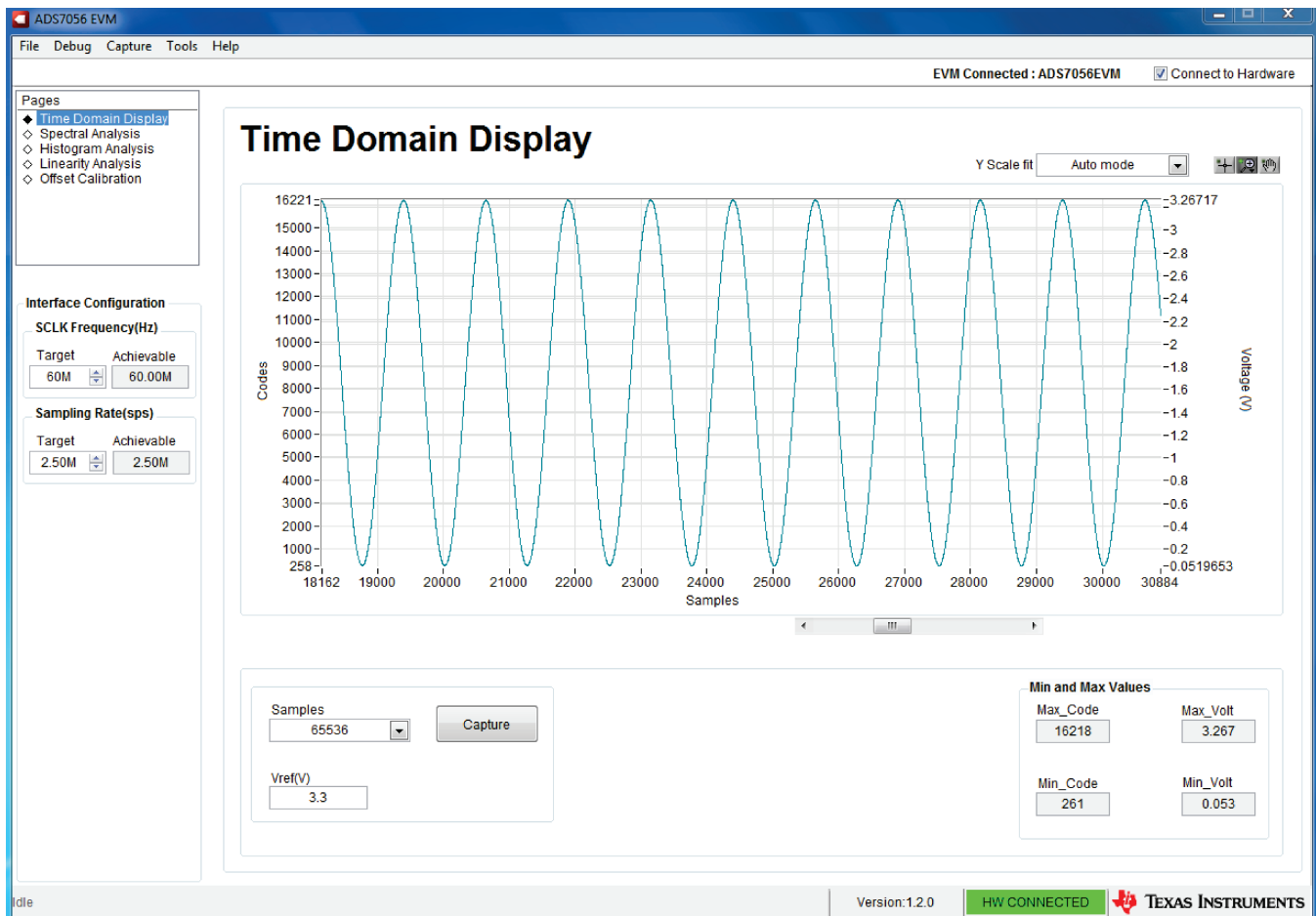
The user can select *SCLK Frequency* and *Sampling Rate* on this pane. The GUI lets the user enter the targeted values for these two parameters, and lets the GUI compute the best values that can be achieved, considering the timing constraints of the device.

The user can specify a target SCLK frequency (Hz) and the GUI tries to match this frequency as closely as possible by changing the PHI PLL settings; however, the achievable frequency may differ from the target value entered. Similarly, the sampling rate of the ADC can be adjusted by modifying the Target Sampling Rate argument (Hz). The achievable ADC sampling rate can differ from the target value, depending on the applied SCLK frequency and the closest match achievable is displayed. This pane, therefore, lets the user try various settings available on the device in an repetitive fashion until the user arrives at the best settings for the corresponding test scenario.

6.2 Time Domain Display Tool

The time domain display tool allows a visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits.

The user can trigger a capture of the data of the selected number of samples from the ADS7056EVM, as per the current interface mode settings using the Capture button as indicated in Figure 10. The sample indices are on the x-axis, and two y-axes show the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the analysis tools described in the subsequent sections triggers calculations to be performed on the same set of data.



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Figure 10. Time Domain Display Tool Options

6.3 Spectral Analysis Tool

The spectral analysis tool (see Figure 11) is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS7056 SAR ADC through single-tone, sinusoidal signal FFT analysis, using the 7-term Blackman-Harris window setting. Alternatively, the window setting of *None* can be used to search for noise spurs over frequency in DC inputs.

For dynamic performance evaluation, the external, single-ended source must have better specifications than the ADC, to ensure that the measured system performance is not limited by the performance of the signal source. Therefore, the external reference source must meet the source requirements listed in Table 6.

Table 6. External Source Requirements for Device Evaluation (SNR and THD)

Specification Description	Specification Value
Signal frequency	2 kHz
External source type	Single-ended
External source common-mode	1.65 V
Minimum SNR	90 dB
Minimum THD	-105 dB

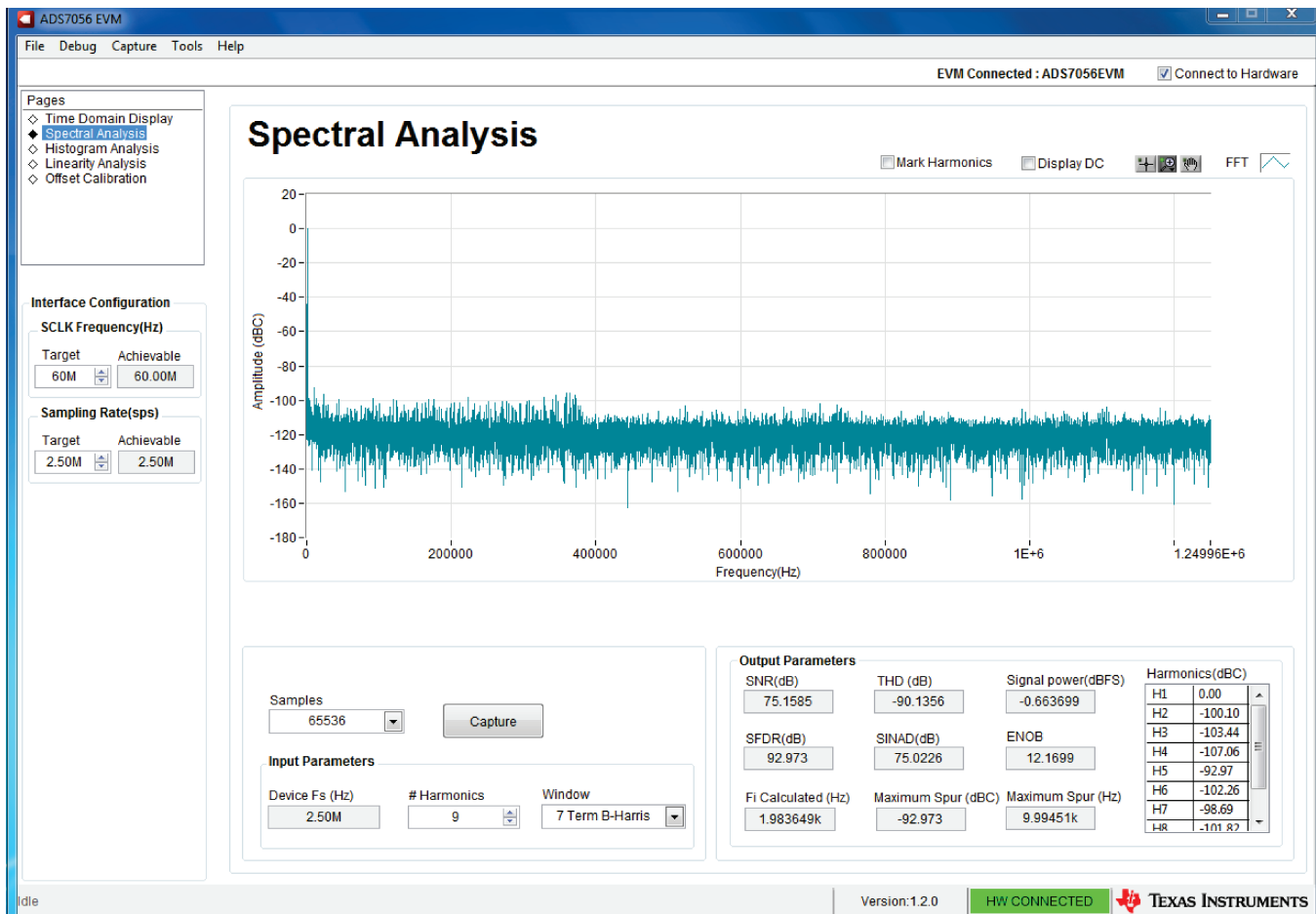
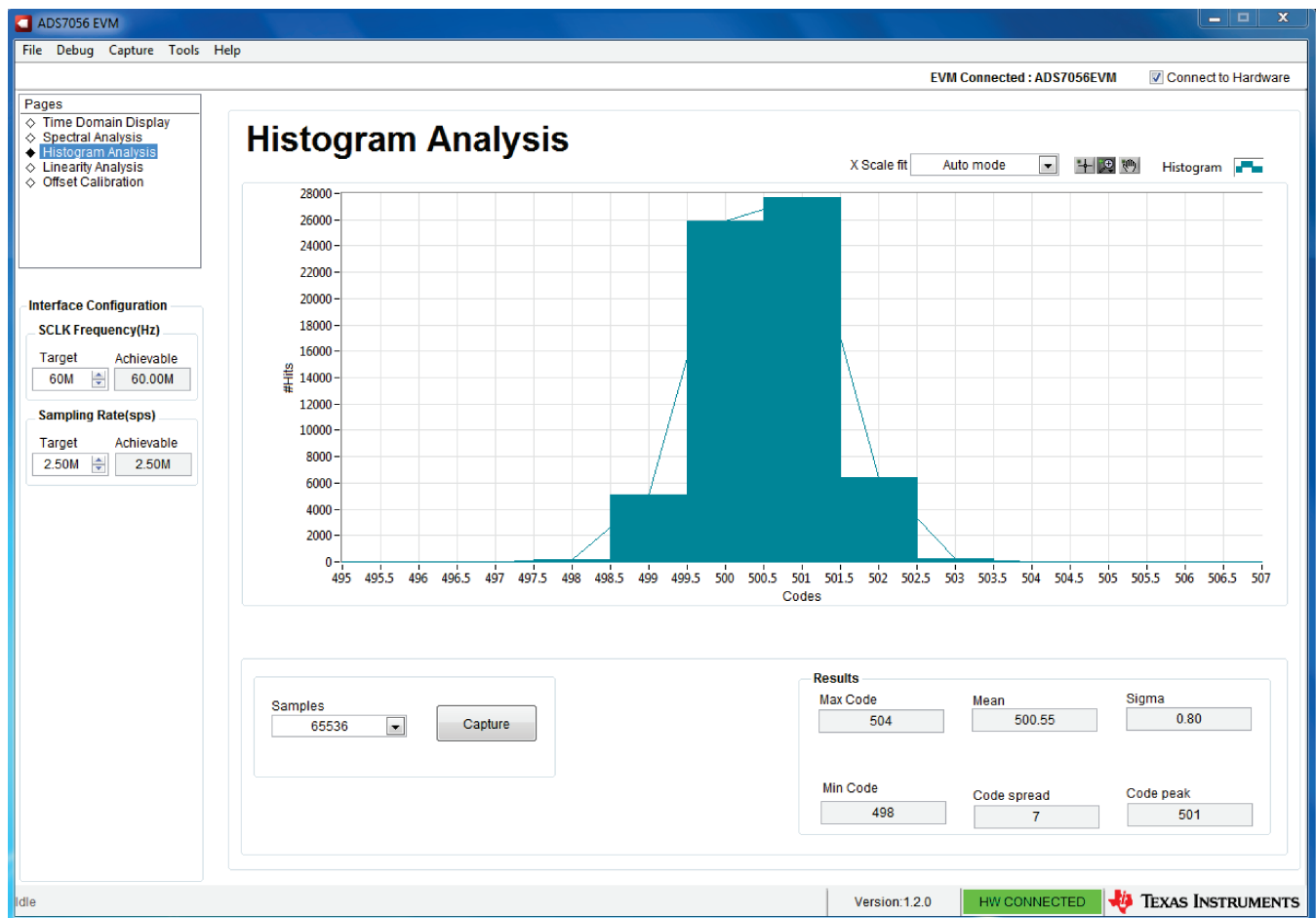


Figure 11. Spectral Analysis Tool

6.4 Histogram Tool

Noise degrades the ADC resolution, and the histogram tool can be used to estimate effective resolution. Effective resolution is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output (from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC) is reflected in the standard deviation of the ADC output code histogram obtained by performing multiple conversions of a DC input applied to a given channel.

The histogram corresponding to a DC input is displayed by clicking the *Capture* button, as shown in Figure 12.



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Figure 12. Histogram Analysis Tool

6.5 Offset Calibration

The ADS7056 device can calibrate its internal offset. The offset calibration can be initiated by the user either on power up or during normal operation. During offset calibration, the analog input pins (AINP and AINM) are disconnected from the sampling stage and connected to an internal reference. The result of the offset calibration is stored in an internal register. For subsequent conversions, the device adjusts the conversion results provided on the SDO output with the value stored in this internal register.

The ADS7056 GUI implements offset calibration, described in the Offset Calibration During Normal Operation section of the [Ultra-Low Power, Ultra-Small Size, 14-Bit, 2.5-MSPS, SAR ADC](#) data sheet. Figure 13 shows the Offset Calibration page of the GUI.

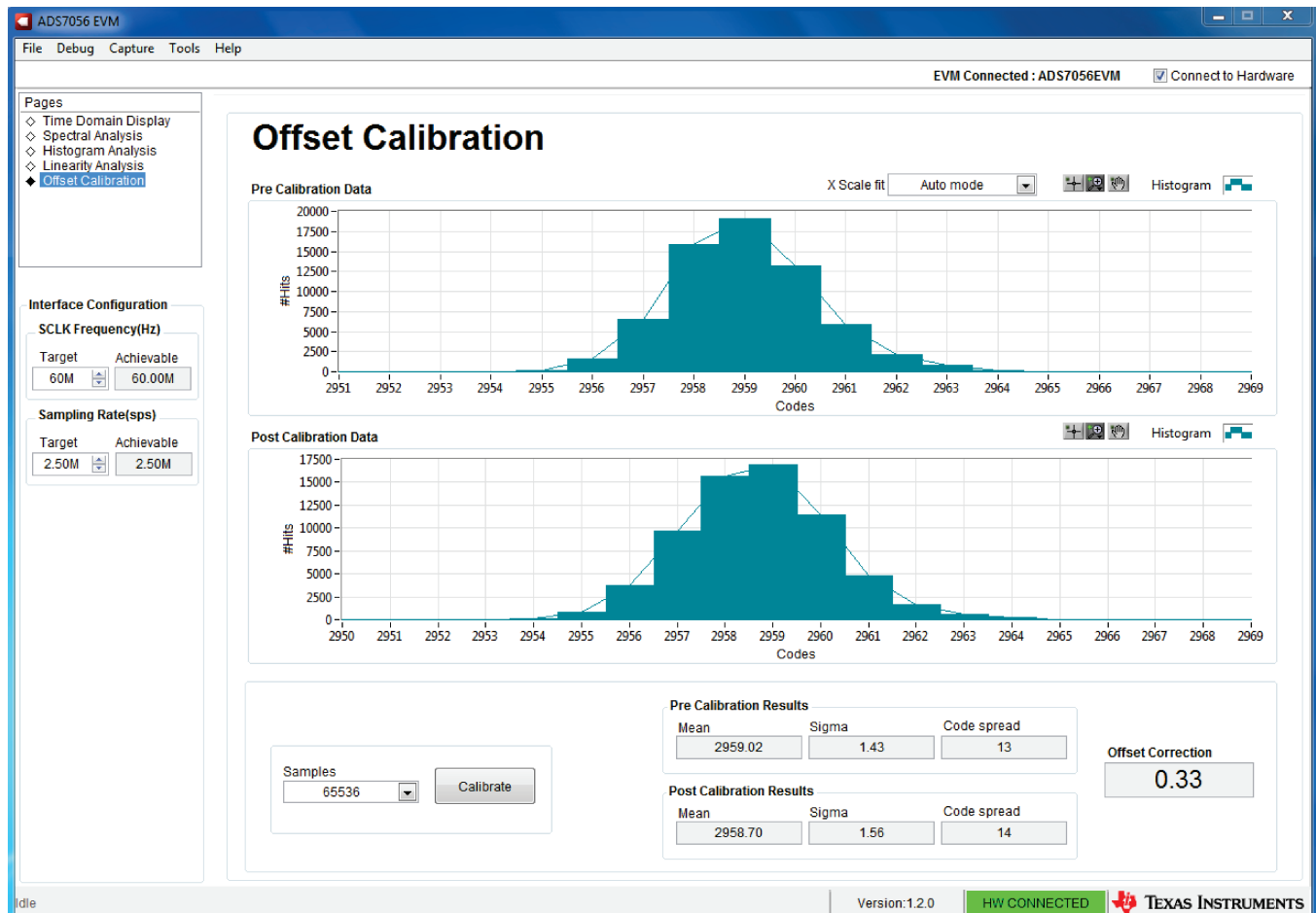


Figure 13. ADS7056 Calibration

The offset calibration test is conducted regardless of the input signal applied to ADC input pin. Users can keep the ADC input floating or apply a fixed DC voltage to the ADC input. Simply click the *Calibrate* button. The GUI first performs a histogram test for the device described in Section 6.4 and populates the first of the two graphs. The precalibrated Mean code is inserted in the indicator. Next, the calibration frame is sent to the ADS7056 device that enables the internal offset calibration logic. The GUI performs the histogram test for a second time and the second graph is populated and Post Calibrated Mean value computed. Finally, the difference between the first and second computed mean is populated in the Calculated Offset Correction indicator.

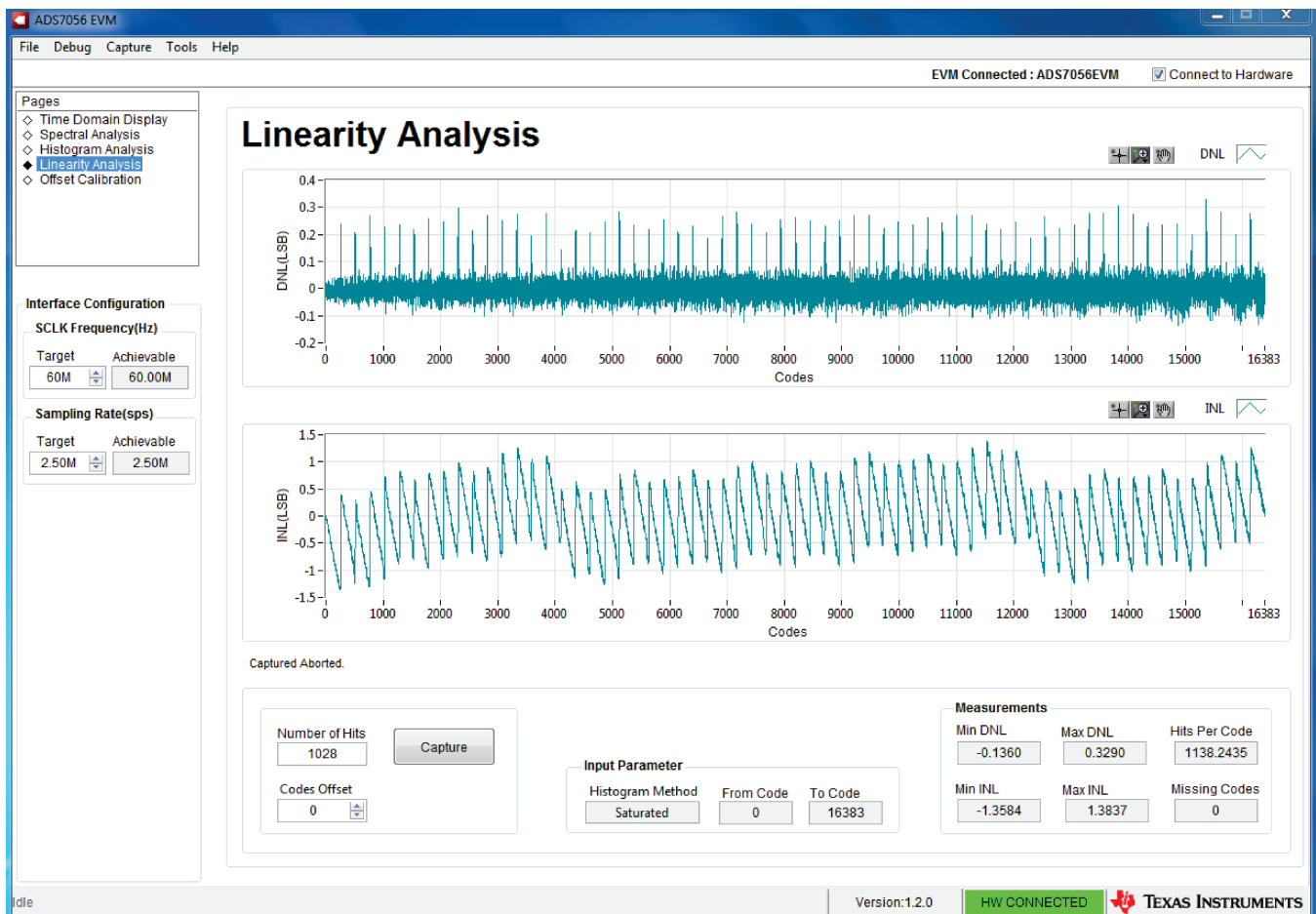
The computed offset for all subsequent attempts to calibrate the device always yields a result within the limits specified in the data sheet. This indicates that after the calibration is performed for the first time, the offset is actually being applied on all subsequent conversions. This computed offset will remain fixed, unless the device is reset or there is a significant change in operating temperature or analog supply voltage.

6.6 Linearity Analysis Tool

The linearity analysis tool measures and generates the DNL and INL plots over code for the specific ADS7056 device installed in the evaluation board (see [Figure 14](#)). A 2-kHz sinusoidal input signal is required, which is slightly saturated (100 mV to 200 mV outside the full-scale range at each input) with very low distortion. The external source linearity must be better than the ADC linearity. The measured system performance must reflect the linearity errors of the ADC and must not be limited by the performance of the signal source. To ensure that the DNL and INL of the ADC are correctly measured, the external source must meet the requirements in [Table 7](#).

Table 7. External Source Requirements for Device Evaluation (Linearity)

Specification Description	Specification Value
Signal frequency	2 kHz
External source type	Single-ended
External source common-mode	1.65 V
Minimum SNR	90 dB
Minimum THD	-105 dB



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Figure 14. Linearity Analysis Tool

7 Bill of Materials, Printed-Circuit Board Layout, and Schematics

This section contains the ADS7056EVM bill of materials (BOM), printed-circuit board (PCB) layout, and schematics.

7.1 Bill of Materials

Table 8 lists the ADS7056EVM BOM.

Table 8. BOM

Manufacturer Part Number	Quantity	Reference Designators	Manufacturer	Description
PA042	1	!PCB	Any	PCB
PA007A	1	!PCB2	Any	PHI-EVM-CONTROLLER
1891	4	@H1, @H2, @H3, @H4	Keystone	3/16 Hex Female Standoff
RM3X4MM 2701	2	@H5, @H6	APM HEXSEAL	Machine Screw Pan PHILLIPS M3
GRM1555C1H121FA01D	1	C1	MuRata	Ceramic Capacitor, 120 pF, 50 V, ±1%, C0G/NP0, 0402
C0603C105K3RACTU	3	C4, C5, C19	Kemet	Ceramic Capacitor, 1 µF, 25 V, ±10%, X7R, 0603
C1608X5R1A106M080AC	1	C7	TDK	Ceramic Capacitor, 10 µF, 10 V, ±20%, X5R, 0603
C1608X7R1A225K080AC	3	C10, C15, C25	TDK	Ceramic Capacitor, 2.2 µF, 10 V, ±10%, X7R, 0603
GRM1555C1H681JA01D	2	C11, C16	MuRata	Ceramic Capacitor, 680 pF, 50 V, ±5%, C0G/NP0, 0402
GRM188R61A226ME15D	2	C13, C17	MuRata	Ceramic Capacitor, 22 µF, 10 V, ±20%, X5R, 0603
GRM155R61A104KA01D	1	C14	MuRata	Ceramic Capacitor, 0.1 µF, 10 V, ±10%, X5R, 0402
GRM188R61A335KE15D	1	C18	MuRata	Ceramic Capacitor, 3.3 µF, 10 V, ±10%, X5R, 0603
GRM188R61A475ME15	1	C20	MuRata	Ceramic Capacitor, 4.7 µF, 10 V, ±20%, X5R, 0603
GRM185C81A105KE36D	3	C21, C22, C34	MuRata	Ceramic Capacitor, 1 µF, 10 V, ±10%, X6S, 0603
0603ZC103KAT2A	1	C24	AVX	Ceramic Capacitor, 0.01 µF, 10 V, ±10%, X7R, 0603
GRM155R61A103KA01D	2	C26, C29	MuRata	Ceramic Capacitor, 0.01 µF, 10 V, ±10%, X5R, 0402
C1005X7R1H104K050BB	1	C27	TDK	Ceramic Capacitor, 0.1 µF, 50 V, ±10%, X7R, 0402
0805YD106MAT2A	1	C28	AVX	Ceramic Capacitor, 10 µF, 16 V, ±20%, X5R, 0805
GRM21BR61C106KE15L	3	C30, C32, C33	MuRata	Ceramic Capacitor, 10 µF, 16 V, ±10%, X5R, 0805
PMSSS 440 0025 PH	4	H1, H2, H3, H4	B&F Fastener Supply	MACHINE SCREW PAN PHILLIPS 4-40
9774050360R	2	H5, H6	Würth Elektronik	ROUND STANDOFF M3 STEEL 5 mm
5-1814832-1	1	J1	TE Connectivity	SMA Straight PCB Socket Die Cast, 50 Ω, TH
PEC02SAAN	3	J3, J5, J6	Sullins Connector Solutions	Header, 100 mil, 2 × 1, Tin, TH
QTH-030-01-L-D-A	1	J4	Samtec	Header (Shrouded), 19.7 mil, 30 × 2, Gold, SMT
THT-14-423-10	1	LBL1	Brady	Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll
CRCW040210K0FKED	2	R2, R30	Vishay-Dale	Resistor, 10.0 kΩ, 1%, 0.063 W, 0402
MCR01MZPF1001	1	R3	Rohm	Resistor, 1.00 k, 1%, 0.063 W, 0402
RC0402JR-070RL	8	R6, R10, R14, R20, R21, R22, R28, R31	Yageo America	Resistor, 0, 5%, 0.063 W, 0402
CRCW040233R0JNED	2	R17, R19	Vishay-Dale	Resistor, 33, 5%, 0.063 W, 0402
CRCW04024R70JNED	1	R18	Vishay-Dale	Resistor, 4.7, 5%, 0.063 W, 0402
ERJ-2RKF49R9X	3	R25, R26, R27	Panasonic	Resistor, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0402
ERJ-2RKF4701X	2	R32, R34	Panasonic	Resistor, 4.70 k, 1%, 0.1 W, 0402
CRCW040210K0JNED	3	R33, R39, R40	Vishay-Dale	Resistor, 10 k, 5%, 0.063 W, 0402
CRCW060310R0FKEA	1	R38	Vishay-Dale	Resistor, 10.0, 1%, 0.1 W, 0603
ERJ-2GE0R00X	2	R43, R45	Panasonic	Resistor, 0, 5%, 0.063 W, 0402
CRCW040220R0FKED	1	R44	Vishay-Dale	Resistor, 20.0, 1%, 0.063 W, 0402
CRCW06031M00JNEA	1	R48	Vishay-Dale	Resistor, 1.0 M, 5%, 0.1 W, 0603
OPA836IDBVR	1	U1	Texas Instruments	Very Low Power, Rail-to-Rail Out, Negative Rail In, VFB Operational Amplifier, 2.5 to 5.5 V, -40 to 125°C, 6-pin SOT23 (DBV6), Green (RoHS and no Sb/Br)
LM7705MMX/NOPB	1	U3	Texas Instruments	Low-Noise Negative Bias Generator, DGK0008A (VSSOP-8)

Table 8. BOM (continued)

Manufacturer Part Number	Quantity	Reference Designators	Manufacturer	Description
REF1933AIDDCR	1	U4	Texas Instruments	Low-Drift, Low-Power, Dual-Output, VREF and VREF / 2 Voltage References, DDC0005A (SOT-5)
ADS7056IRUGR	1	U5	Texas Instruments	Ultra-Low Power, Ultra-Small Size, 14-Bit, 2.5-MSPS, SAR ADC, RUG0008A (X2QFN-8)
TPS79147DBVR	1	U6	Texas Instruments	Single Output High PSRR LDO, 100 mA, Fixed 4.7-V Output, 2.7- to 5.5-V Input, 5-pin SOT-23 (DBV), -40 to 125°C, Green (RoHS and no Sb/Br)
BR24G32FVT-3AGE2	1	U7	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8
SN74AVC4T245RGYR	1	U8	Texas Instruments	4-Bit Dual-supply Bus Transceiver with Configurable Voltage Translation and 3-State Outputs, RGY0016A
GRM1555C1H121FA01D	0	C2	MuRata	Ceramic Capacitor, 120 pF, 50 V, ±1%, C0G/NP0, 0402
C0603C105K3RACTU	0	C3, C6	Kemet	Ceramic Capacitor, 1 µF, 25 V, ±10%, X7R, 0603
885012205008	0	C8, C9	Würth Elektronik	Ceramic Capacitor, 2200 pF, 10 V, ±10%, X7R, 0402
GRM1555C1H681JA01D	0	C12	MuRata	Ceramic Capacitor, 680 pF, 50 V, ±5%, C0G/NP0, 0402
CC0402JRNPO9BN150	0	C23	Yageo America	Ceramic Capacitor, 15 pF, 50 V, ±5%, C0G/NP0, 0402
GRM1555C1H470FA01D	0	C31	MuRata	Ceramic Capacitor, 47 pF, 50 V, ±1%, C0G/NP0, 0402
GRM188R61A226ME15D	0	C35	MuRata	Ceramic Capacitor, 22 µF, 10 V, ±20%, X5R, 0603
GRM155R61A104KA01D	0	C36	MuRata	Ceramic Capacitor, 0.1 µF, 10 V, ±10%, X5R, 0402
GRM185C81A105KE36D	0	C37	MuRata	Ceramic Capacitor, 1 µF, 10 V, ±10%, X6S, 0603
5-1814832-1	0	J2	TE Connectivity	SMA Straight PCB Socket Die Cast, 50Ω, TH
PEC02SAAN	0	J7	Sullins Connector Solutions	Header, 100 mil, 2 × 1, Tin, TH
MCR01MZPF1001	0	R1, R5, R8	Rohm	Resistor, 1.00 k, 1%, 0.063 W, 0402
RC0402JR-070RL	0	R4, R7, R9, R11, R12, R13, R15, R29, R36, R37	Yageo America	Resistor, 0, 5%, 0.063 W, 0402
CRCW040233R0JNED	0	R16	Vishay-Dale	Resistor, 33, 5%, 0.063 W, 0402
CRCW040230K1FKED	0	R23	Vishay-Dale	Resistor, 30.1 k, 1%, 0.063 W, 0402
CRCW040288K7FKED	0	R24	Vishay-Dale	Resistor, 88.7 k, 1%, 0.063 W, 0402
ERJ-2GE0R00X	0	R35, R41, R46, R47	Panasonic	Resistor, 0, 5%, 0.063 W, 0402
CRCW06031M00JNEA	0	R42	Vishay-Dale	Resistor, 1.0 M, 5%, 0.1 W, 0603
5016	0	TP1	Keystone	Test Point, Compact, SMT
OPA836IDBVR	0	U2	Texas Instruments	Very Low Power, Rail-to-Rail Out, Negative Rail In, VFB Operational Amplifier, 2.5 to 5.5 V, -40 to 125°C, 6-pin SOT23 (DBV6), Green (RoHS and no Sb/Br)
REF6133IDGKR	0	U9	Texas Instruments	High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)

7.2 PCB Layout

Figure 15 through Figure 18 show the EVM PCB layout.

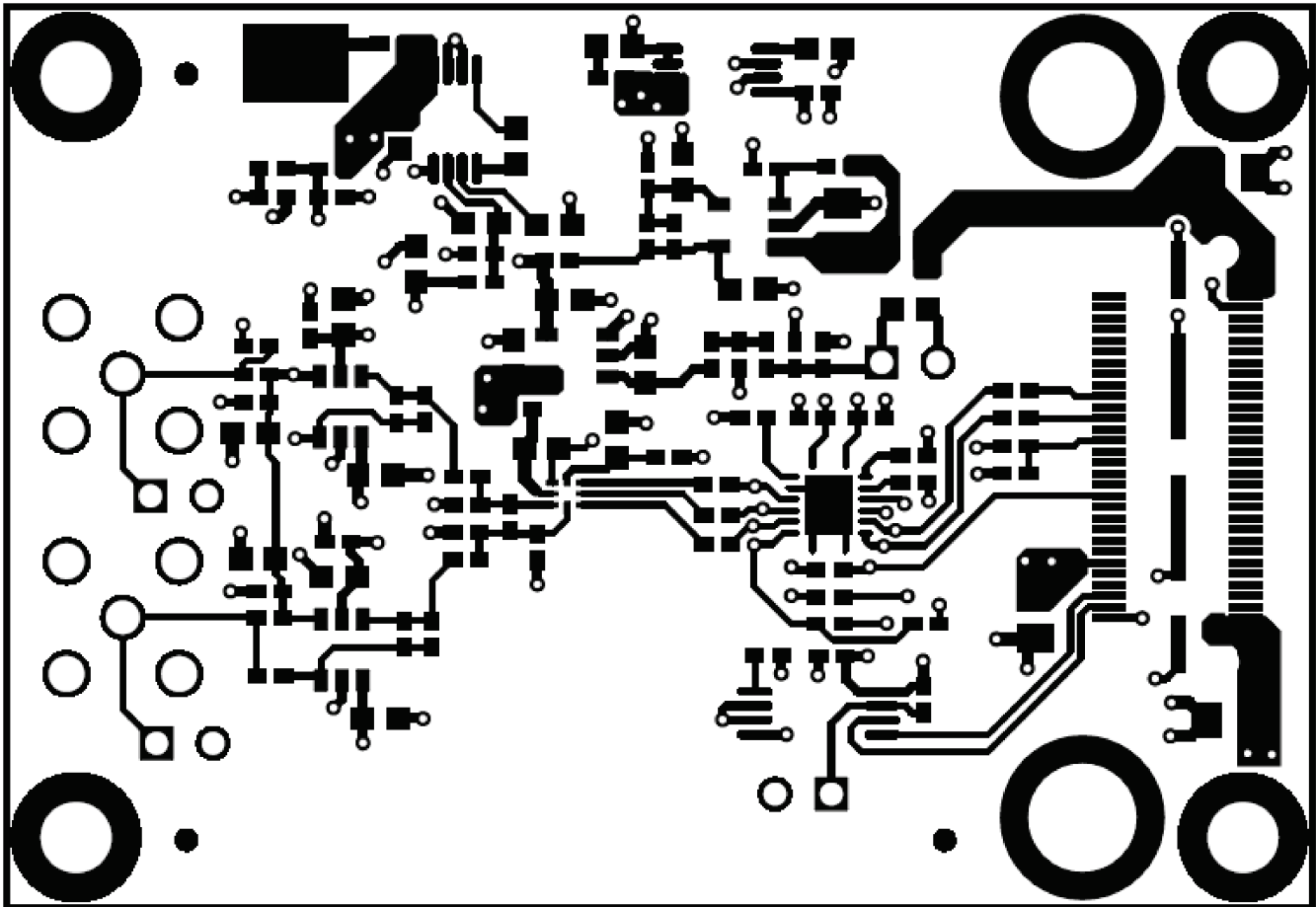


Figure 15. ADS7056EVM PCB Layer 1: Top Layer

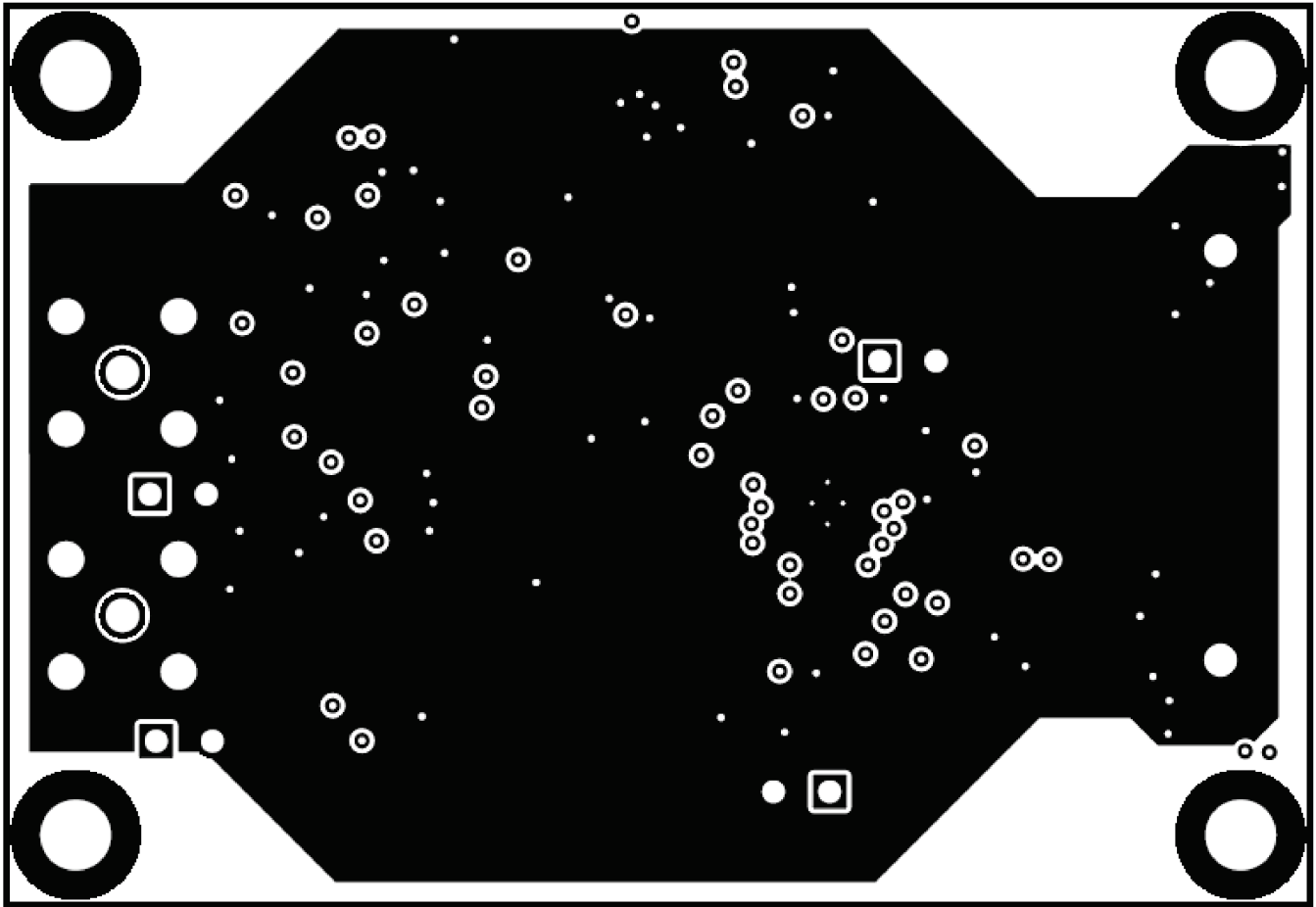


Figure 16. ADS7056EVM PCB Layer 2: GND Plane

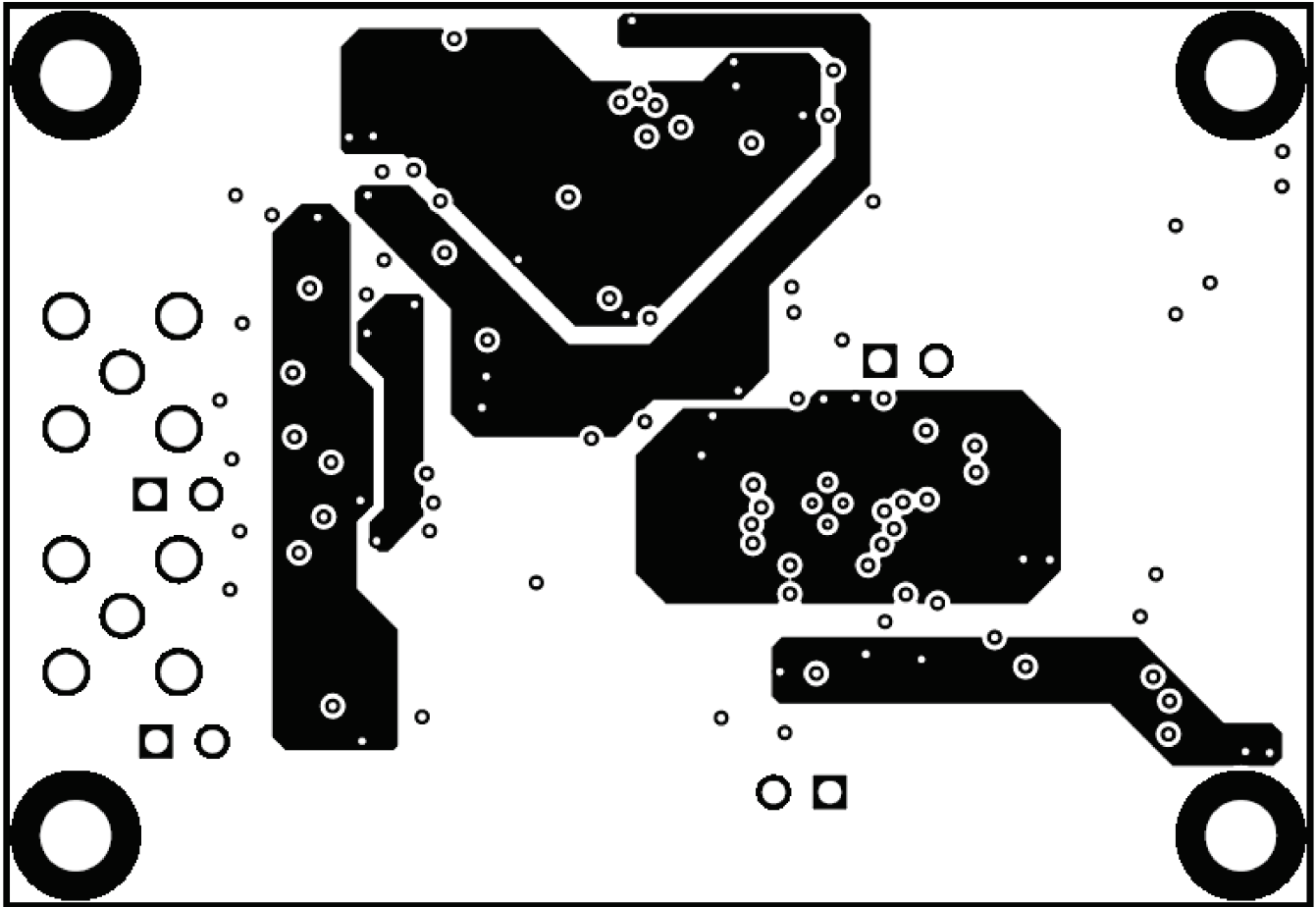


Figure 17. ADS7056EVM PCB Layer 3: Power Planes

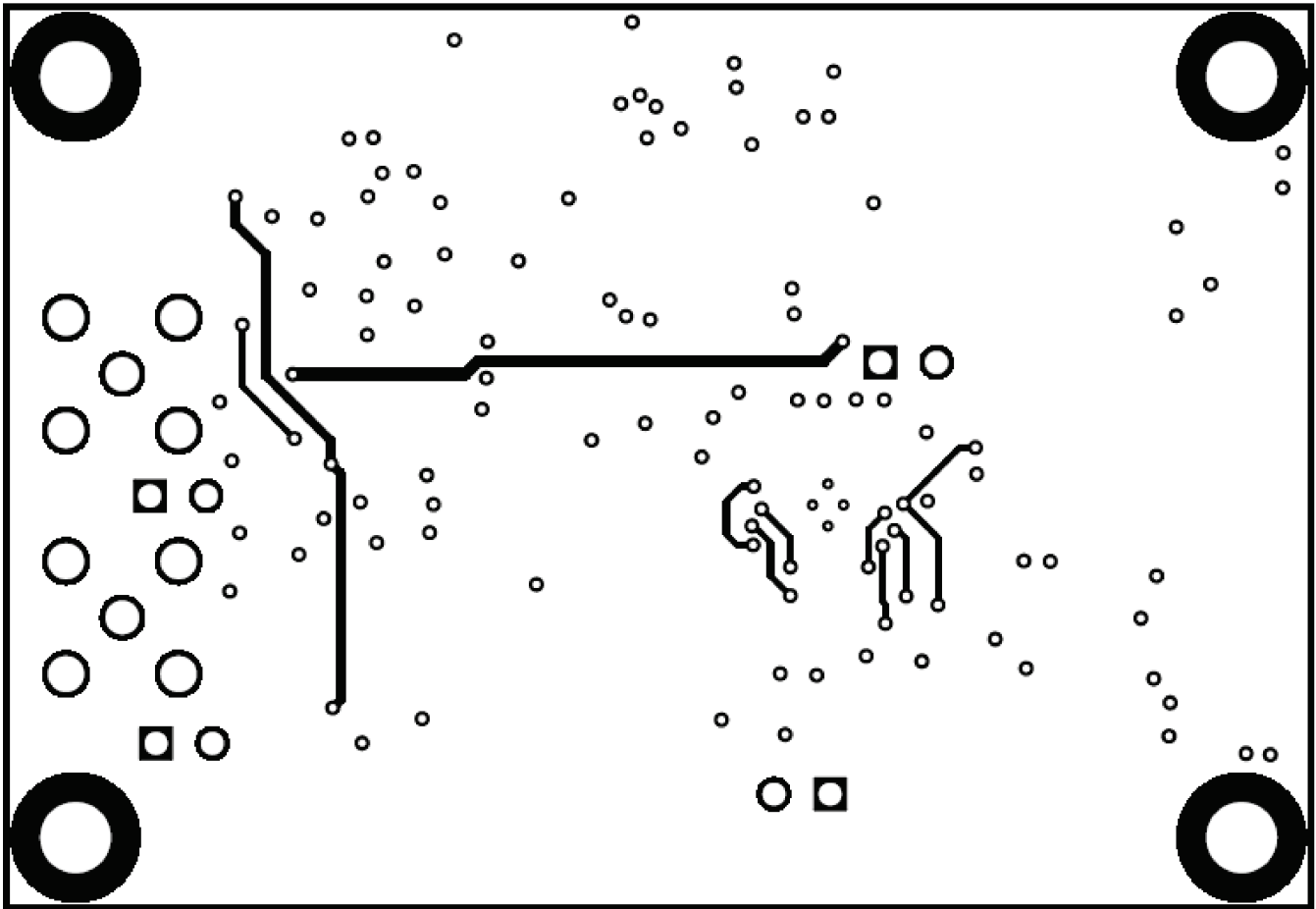


Figure 18. ADS7056EVM PCB Layer 4: Bottom Layer

7.3 Schematics

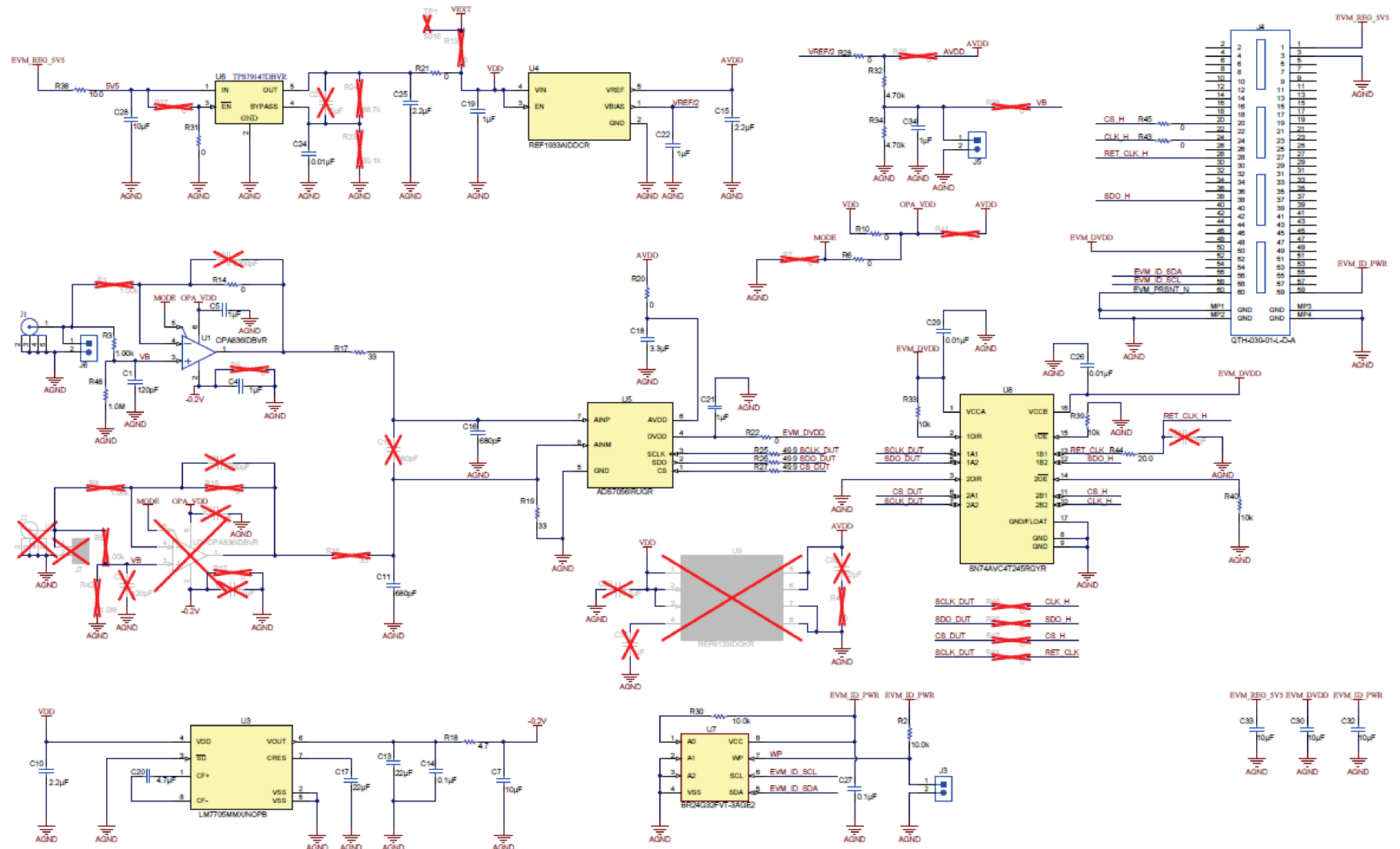
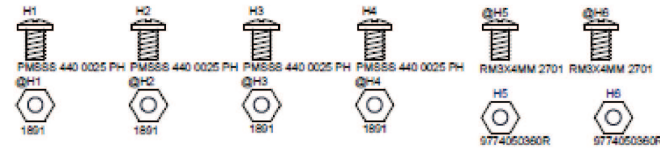


Figure 19. Schematic Diagram (Page 1) of the ADS7056EVM PCB



PCB Number: PA042
PCB Rev: A

PCB LOGO
Texas Instruments

PCB LOGO
Pb-Free Symbol

PCB LOGO
FCC disclaimer

PCB: PA007A

PH-EVM-CONTROLLER

LSL1
PCB Label
Size: 0.65" x 0.20"

Z21
Label Assembly Note
This Assembly Note is for PCB labels only

Z22
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

Z23
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Z24
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Variant/Label Table	
Variant	Label Text
001	ADS7056EVM-PDK

Figure 20. Schematic Diagram (Page 2) of the ADS7056EVM PCB

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1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
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 - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
2. *Limited Warranty and Related Remedies/Disclaimers:*
 - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
 - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
 - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.
3. *Regulatory Notices:*
 - 3.1 *United States*
 - 3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.
 - 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3. 技術基準適合証明を取得後ご使用いただく。

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東京都新宿区西新宿 6 丁目 2 4 番 1 号
西新宿三井ビル

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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