ON Semiconductor®

FSQ0565RS/RQ
Green-Mode Power Switch for Quasi-Resonant Operation - Low EMI and High Efficiency

Features

- Optimized for Quasi-Resonant Converters (QRC)
- Low EMI through Variable Frequency Control and AVS (Alternating Valley Switching)
- High-Efficiency through Minimum Voltage Switching
- Narrow Frequency Variation Range over Wide Load and Input Voltage Variation
- Advanced Burst-Mode Operation for Low Standby Power Consumption
- Simple Scheme for Sync Voltage Detection
- Pulse-by-Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over-Voltage Protection (OVP), Internal Thermal Shutdown (TSD) with Hysteresis, Output Short Protection (OSP)
- Under-Voltage Lockout (UVLO) with Hysteresis
- Internal Startup Circuit
- Internal High-Voltage Sense FET (650V)
- Built-in Soft-Start (17.5ms)

Applications

- Power Supply for LCD TV and Monitor, VCR, SVR, STB, and DVD & DVD Recorder
- Adapter

Description

A Quasi-Resonant Converter (QRC) generally shows lower EMI and higher power conversion efficiency than a conventional hard-switched converter with a fixed switching frequency. The FSQ-series is an integrated Pulse-Width Modulation (PWM) controller and SenseFET specifically designed for quasi-resonant operation and Alternating Valley Switching (AVS). The PWM controller includes an integrated fixed-frequency oscillator, Under-Voltage Lockout (UVLO), Leading-Edge Blanking (LEB), optimized gate driver, internal soft-start, temperature-compensated precise current sources for a loop compensation, and self-protection circuitry. Compared with a discrete MOSFET and PWM controller solution, the FSQ-series can reduce total cost, component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform for cost-effective designs of quasi-resonant switching flyback converters.

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October-2017, Rev. 3

Publication Order Number:
FSQ0565RS/D

Ordering Information

Product Number	PKG.[5]	Operating Temp.	Current Limit	$R_{DS(ON)}$ Max.	Maximum Output Power[1]				Replaces Devices
					$230V_{AC}$±15%[2]		85-265V_{AC}		
					Adapter[3]	Open Frame[4]	Adapter[3]	Open Frame[4]	
FSQ0565RSWDTU	TO-220F-6L	-25 to +85°C	2.25A	2.2Ω	70W	80W	41W	60W	FSCM0565R FSDM0565RE
FSQ0565RQWDTU			3.0A						
FSQ0565RSLDTU	TO-220F-6L (L-Forming)	-25 to +85°C	2.25A	2.2Ω	70W	80W	41W	60W	FSCM0565R FSDM0565RE
FSQ0565RQLDTU			3.0A						

Notes:
1. The junction temperature can limit the maximum output power.
2. $230V_{AC}$ or $100/115V_{AC}$ with doubler.
3. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
4. Maximum practical continuous power in an open-frame design at 50°C ambient.
5. Eco Status, RoHS

Application Diagram

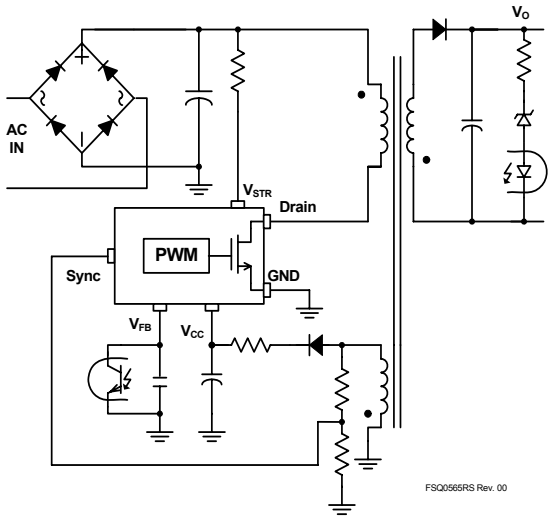


Figure 1. Typical Flyback Application

Block Diagrams

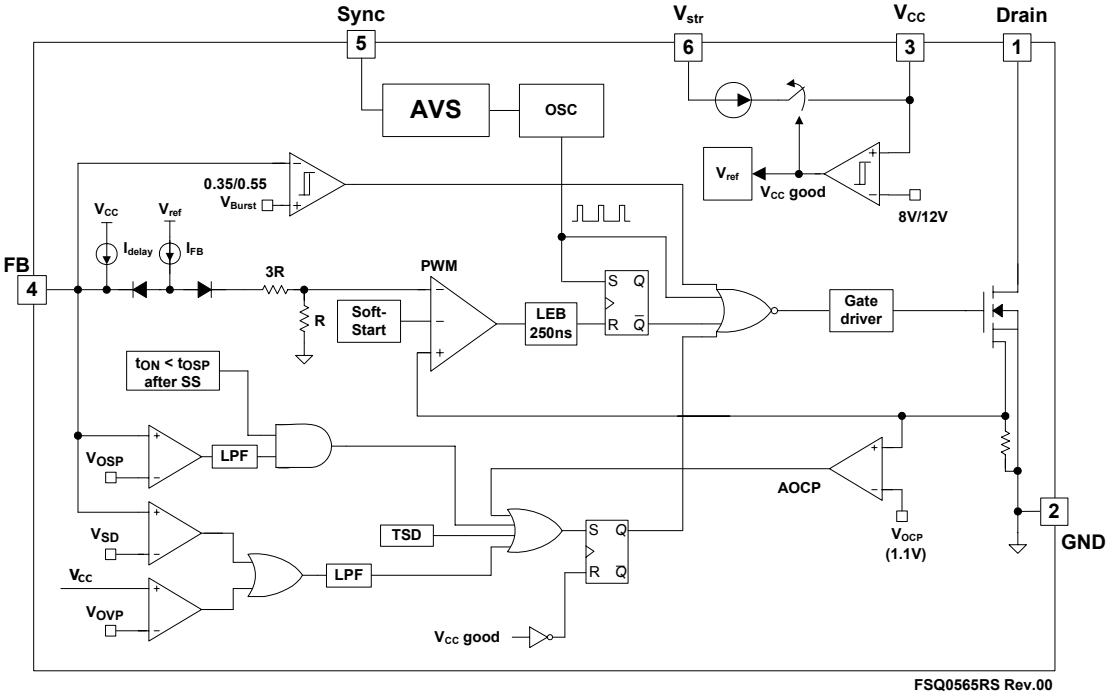


Figure 2. Internal Block Diagram of FSQ0565RS

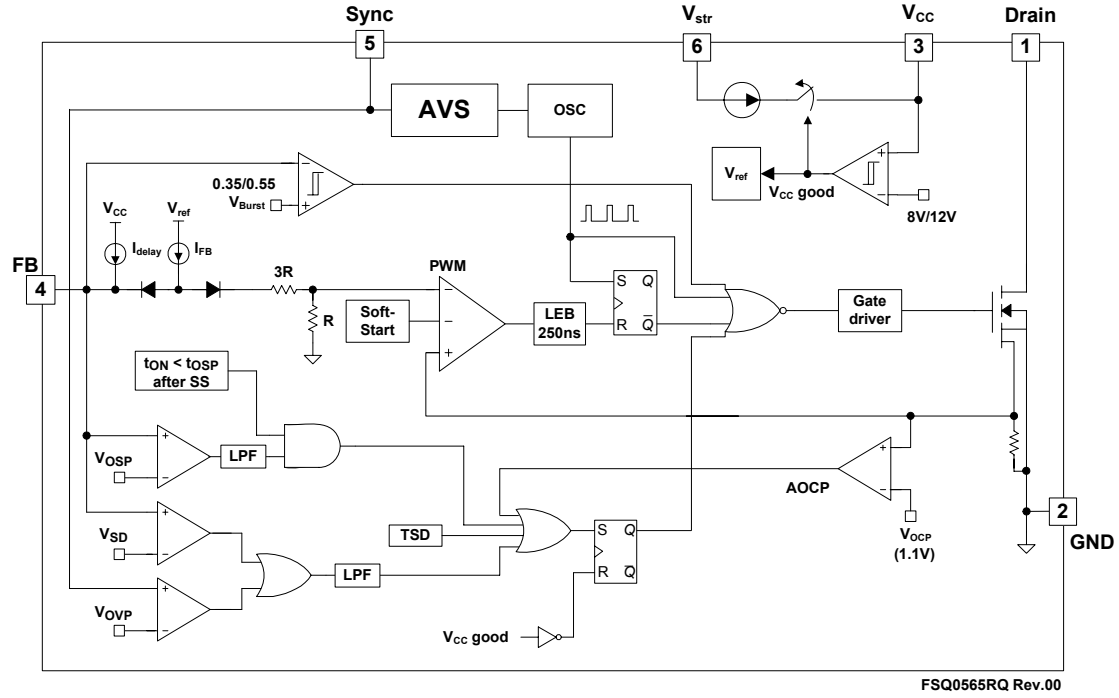


Figure 3. Internal Block Diagram of FSQ0565RQ

Pin Configuration

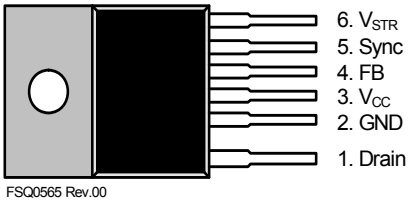


Figure 4. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	Drain	**SenseFET Drain.** High-voltage power SenseFET drain connection.
2	GND	**Ground.** This pin is the control ground and the SenseFET source.
3	V_{CC}	**Power Supply.** This pin is the positive supply input, providing internal operating current for both startup and steady-state operation.
4	FB	**Feedback.** This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 6V, the overload protection triggers, which shuts down the power switch.
5	Sync	**Sync.** This pin is internally connected to the sync-detect comparator for quasi-resonant switching. In normal quasi-resonant operation, the threshold of the sync comparator is 1.2V/1.0V.
6	V_{str}	**Startup.** This pin is connected directly, or through a resistor, to the high-voltage DC link. At startup, the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V_{CC} pin. Once V_{CC} reaches 12V, the internal current source is disabled. It is not recommended to connect V_{str} and Drain together.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A = 25°C, unless otherwise specified.

Symbol	Parameter		Min.	Max.	Unit
V_{str}	V_{str} Pin Voltage		500		V
V_{DS}	Drain Pin Voltage		650		V
V_{CC}	Supply Voltage			20	V
V_{FB}	Feedback Voltage Range		-0.3	13.0	V
V_{Sync}	Sync Pin Voltage		-0.3	13.0	V
I_{DM}	Drain Current Pulsed			11	A
I_D	Continuous Drain Current(6)	T_C = 25°C		2.8	A
		T_C = 100°C		1.7	
E_{AS}	Single Pulsed Avalanche Energy(7)			190	mJ
P_D	Total Power Dissipation (T_C=25°C)			45	W
T_J	Operating Junction Temperature		Internally limited		°C
T_A	Operating Ambient Temperature		-25	+85	°C
T_{STG}	Storage Temperature		-55	+150	°C
ESD	Electrostatic Discharge Capability, Human Body Model		2.0		kV
	Electrostatic Discharge Capability, Charged Device Model		2.0		

Notes:

6. Repetitive rating: pulse-width limited by maximum junction temperature.
7. L=14mH, starting T_J=25°C.

Thermal Impedance

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Package	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance(8)	TO-220F-6L	50	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance(9)		2.8	°C/W

Notes:

8. Free standing with no heat-sink under natural convection.
9. Infinite cooling condition - refer to the SEMI G30-88.

Electrical Characteristics

T_A = 25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
SENSEFET SECTION							
BV_{DSS}	Drain Source Breakdown Voltage		V_{CC} = 0V, I_D = 100μA	650			V
I_{DSS}	Zero-Gate-Voltage Drain Current		V_{DS} = 560V			300	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance		T_J = 25°C, I_D = 0.5A		1.76	2.20	Ω
C_{OSS}	Output Capacitance		V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		78		pF
$t_{d(on)}$	Turn-On Delay Time		V_{DD} = 350V, I_D = 25mA		22		ns
t_r	Rise Time		V_{DD} = 350V, I_D = 25mA		52		ns
$t_{d(off)}$	Turn-Off Delay Time		V_{DD} = 350V, I_D = 25mA		95		ns
t_f	Fall Time		V_{DD} = 350V, I_D = 25mA		50		ns
CONTROL SECTION							
$t_{ON.MAX}$	Maximum On Time		T_J = 25°C	8.8	10.0	11.2	μs
t_B	Blanking Time		T_J = 25°C, V_{sync} = 5V	13.5	15.0	16.5	μs
t_W	Detection Time Window		T_J = 25°C, V_{sync} = 0V		6.0		μs
f_S	Initial Switching Frequency			59.6	66.7	75.8	kHz
Δf_S	Switching Frequency Variation(11)		-25°C < T_J < 85°C		±5	±10	%
t_{AVS}	AVS Triggering Threshold(11)	On Time	at V_{IN} = 240V_{DC}, Lm = 360μH (AVS triggered when V_{AVS} > spec. and t_{AVS} < spec.)		4.0		μs
V_{AVS}		Feedback Voltage			1.2		V
t_{SW}	Switching Time Variance by AVS(11)		Sync = 500kHz sine input V_{FB} = 1.2V, t_{ON} = 4.0μs	13.5		20.5	μs
I_{FB}	Feedback Source Current		V_{FB} = 0V	700	900	1100	μA
D_{MIN}	Minimum Duty Cycle		V_{FB} = 0V			0	%
V_{START}	UVLO Threshold Voltage			11	12	13	V
V_{STOP}			After turn-on	7	8	9	V
$t_{S/S}$	Internal Soft-Start Time		With free-running frequency		17.5		ms
V_{OVP}	Over-Voltage Protection (FSQ0565RS)			18	19	20	V
V_{OVP}	Over-Voltage Protection (FSQ0565RQ)	Threshold Voltage	V_{CC} = 15V, V_{FB} = 2V	7.4	8	9.6	V
t_{OVP}		Blanking Time(11)		1.0	1.7	2.4	μs
BURST-MODE SECTION							
V_{BURH}	Burst-Mode Voltages		T_J = 25°C, t_{PD} = 200ns(10)	0.45	0.55	0.65	V
V_{BURL}				0.25	0.35	0.45	V
Hysteresis					200		mV

Continued on the following page...

Electrical Characteristics (Continued)

T_A = 25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
PROTECTION SECTION							
I_{LIMIT}	Peak Current Limit	FSQ0565RS	T_J = 25°C, di/dt = 370mA/µs	2.00	2.25	2.50	A
I_{LIMIT}		FSQ0565RQ	T_J = 25°C, di/dt = 370mA/µs	2.64	3.0	3.36	A
V_{SD}	Shutdown Feedback Voltage		V_{CC} = 15V	5.5	6.0	6.5	V
I_{DELAY}	Shutdown Delay Current		V_{FB} = 5V	4	5	6	µA
t_{LEB}	Leading-Edge Blanking Time(11)				250		ns
t_{OSP}	Output Short Protection(11)	Threshold Time	T_J = 25°C OSP triggered when $t_{ON} < t_{OSP}$, $V_{FB} > V_{OSP}$ and lasts longer than t_{OSP_FB}		1.2	1.4	µs
V_{OSP}		Threshold Feedback Voltage		1.8	2.0		V
t_{OSP_FB}		Feedback Blanking Time		2.0	2.5	3.0	µs
T_{SD}	Thermal Shutdown(11)	Shutdown Temperature		125	140	155	°C
Hys		Hysteresis			60		
SYNC SECTION							
V_{SH1}	Sync Threshold Voltage 1		V_{CC} = 15V, V_{FB} = 2V	1.0	1.2	1.4	V
V_{SL1}				0.8	1.0	1.2	
t_{sync}	Sync Delay Time(11, 12)				230		ns
V_{SH2}	Sync Threshold Voltage 2		V_{CC} = 15V, V_{FB} = 2V	4.3	4.7	5.1	V
V_{SL2}				4.0	4.4	4.8	
V_{CLAMP}	Low Clamp Voltage		I_{SYNC_MAX} = 800µA, I_{SYNC_MIN} = 50µA	0.0	0.4	0.8	V
TOTAL DEVICE SECTION							
I_{OP}	Operating Supply Current		V_{CC} = 13V	1	3	5	mA
I_{START}	Start Current		V_{CC} = 10V (before V_{CC} reaches V_{START})	350	450	550	µA
I_{CH}	Startup Charging Current		V_{CC} = 0V, V_{STR} = minimum 50V	0.65	0.85	1.00	mA
V_{STR}	Minimum V_{STR} Supply Voltage				26		V

Notes:

10. Propagation delay in the control IC.
11. Guaranteed by design; not tested in production.
12. Includes gate turn-on time.

Comparison Between FSDM0x65RNB and FSQ-Series

Function	FSDM0x65RE	FSQ-Series	FSQ-Series Advantages
Operation Method	Constant Frequency PWM	Quasi-Resonant Operation	■ Improved efficiency by valley switching ■ Reduced EMI noise ■ Reduced components to detect valley point
EMI Reduction	Frequency Modulation	Reduced EMI Noise	■ Valley Switching ■ Inherent Frequency Modulation ■ Alternate Valley Switching
Hybrid Control		CCM or AVS Based on Load and Input Condition	■ Improves efficiency by introducing hybrid control
Burst-Mode Operation	Burst-Mode Operation	Advanced Burst-Mode Operation	■ Improved standby power by advanced burst-mode
Strong Protections	OLP, OVP	OLP, OVP, OSP	■ Improved reliability through precise OSP
TSD	145°C without Hysteresis	140°C with 60°C Hysteresis	■ Stable and reliable TSD operation ■ Converter temperature range

Differences Between FSQ0565RS and FSQ0565RQ

Function	FSQ0565RS	FSQ0565RQ	Remark
I_{LIM}	2.25A	3.0A	■ Lower current peak is suitable to reduce conduction loss ■ Higher current peak is suitable for handling higher power
Over Voltage Protection	V_{CC} OVP (triggered by V_{CC} voltage)	Sync OVP (triggered by Sync voltage)	■ Sync OVP is suitable when V_{CC} voltage is pre regulated.

Typical Performance Characteristics

These characteristic graphs are normalized at T_A= 25°C.

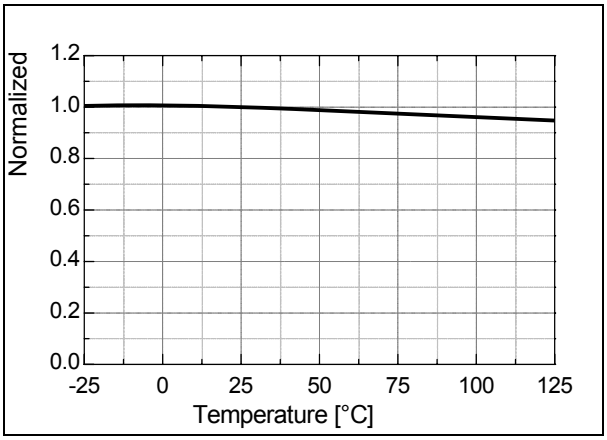


Figure 5. Operating Supply Current (I_{OP}) vs. T_A

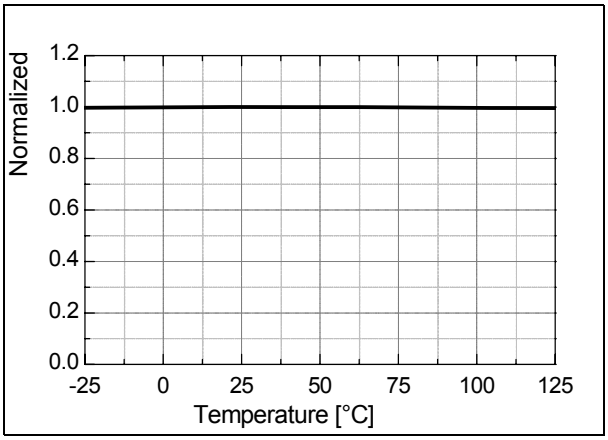


Figure 6. UVLO Start Threshold Voltage (V_{START}) vs. T_A

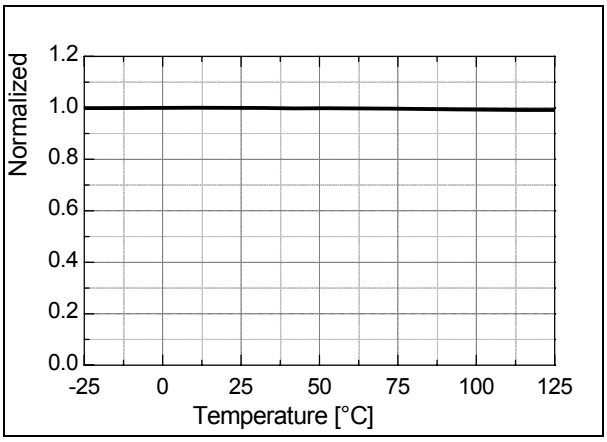


Figure 7. UVLO Stop Threshold Voltage (V_{STOP}) vs. T_A

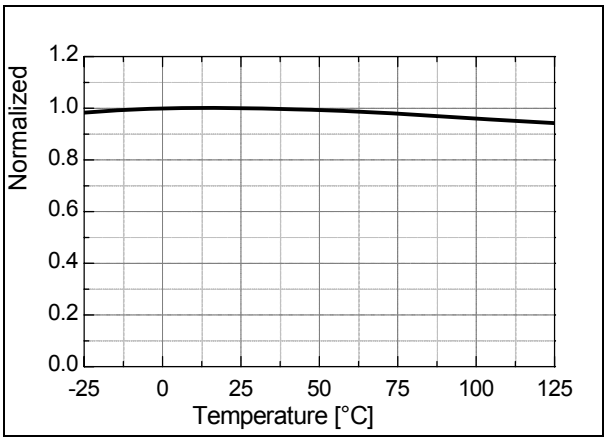


Figure 8. Startup Charging Current (I_{CH}) vs. T_A

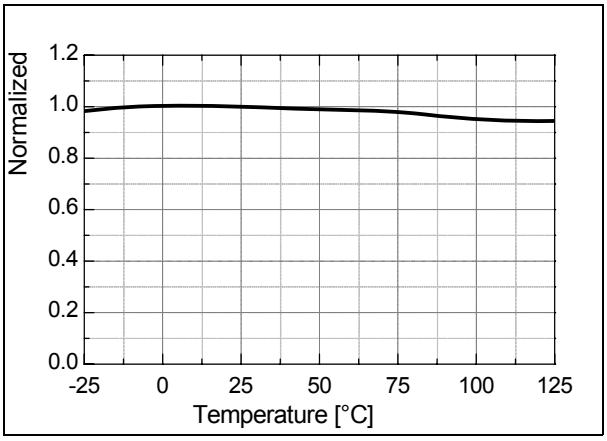


Figure 9. Initial Switching Frequency (f_S) vs. T_A

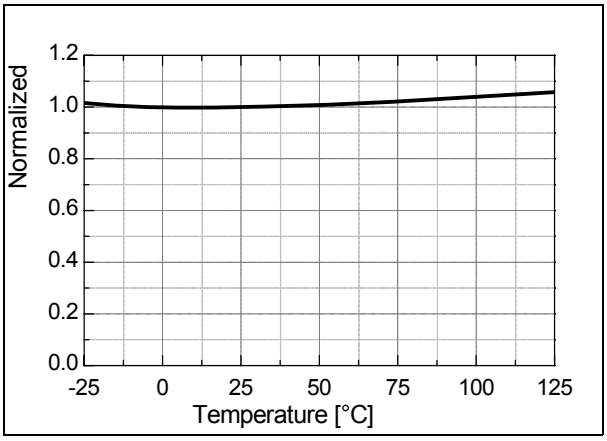


Figure 10. Maximum On Time ($t_{ON.MAX}$) vs. T_A

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at T_A= 25°C.

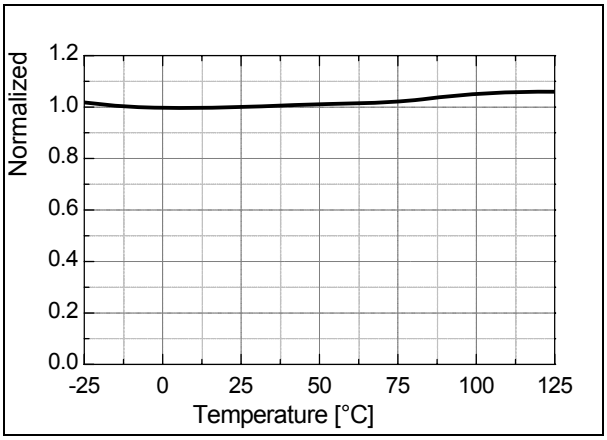


Figure 11. Blanking Time (t_B) vs. T_A

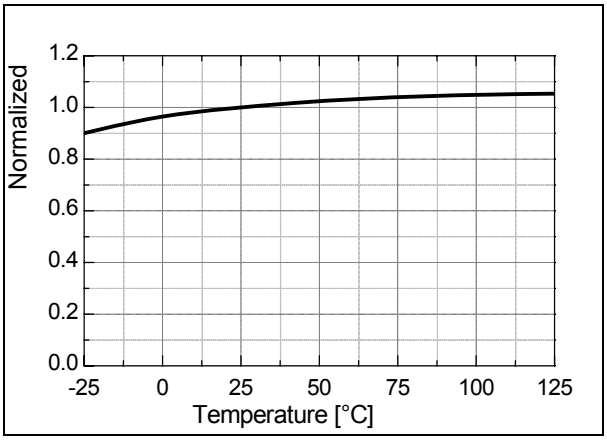


Figure 12. Feedback Source Current (I_{FB}) vs. T_A

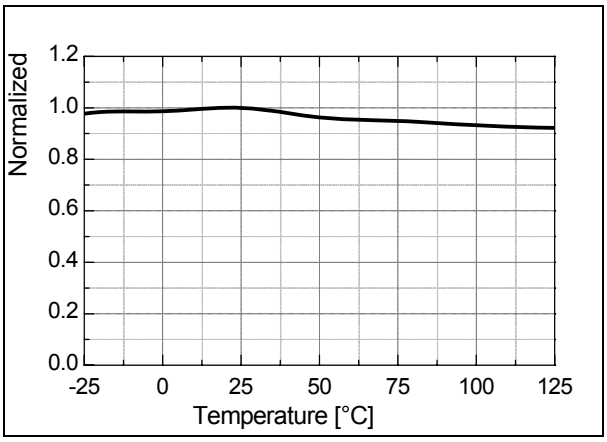


Figure 13. Shutdown Delay Current (I_{DELAY}) vs. T_A

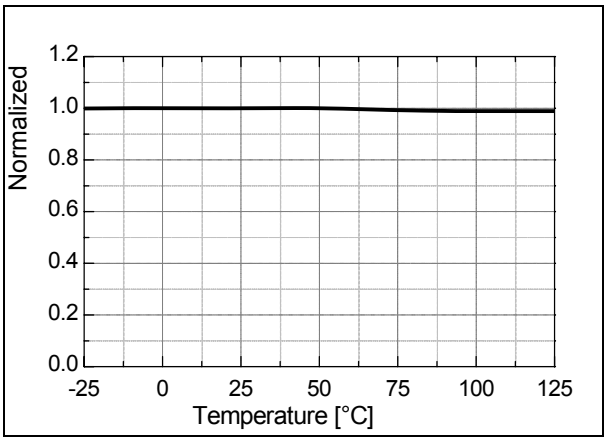


Figure 14. Burst-Mode High Threshold Voltage (V_{burh}) vs. T_A

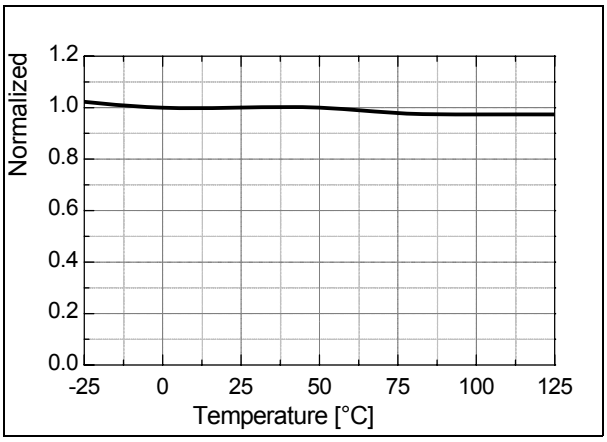


Figure 15. Burst-Mode Low Threshold Voltage (V_{burl}) vs. T_A

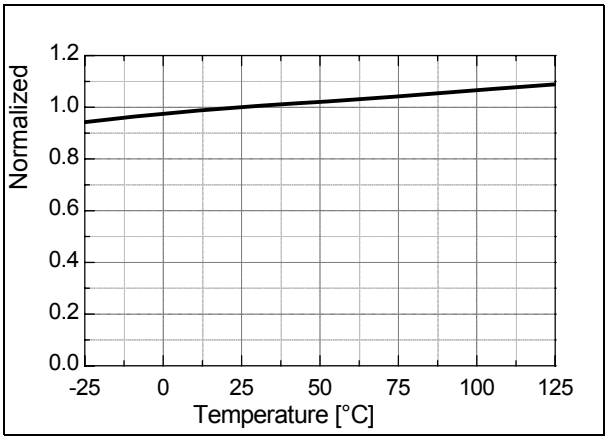


Figure 16. Peak Current Limit (I_{LIM}) vs. T_A

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at T_A= 25°C.

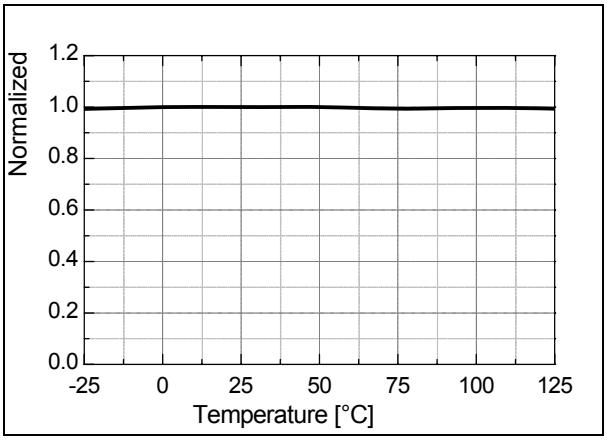


Figure 17. Sync High Threshold Voltage 1 (V_{SH1}) vs. T_A

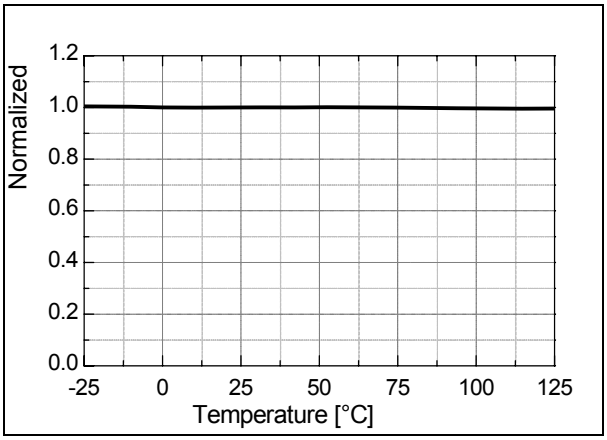


Figure 18. Sync Low Threshold Voltage 1 (V_{SL1}) vs. T_A

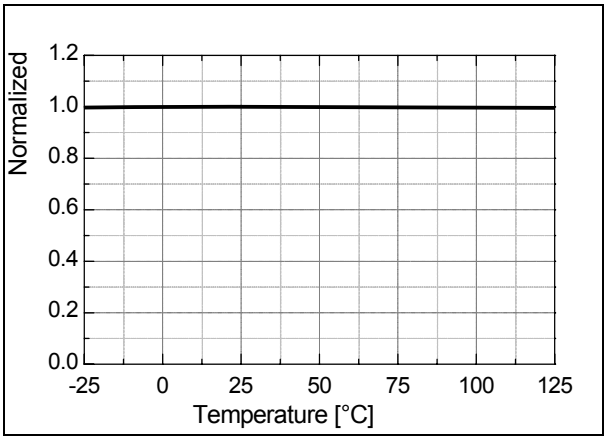


Figure 19. Shutdown Feedback Voltage (V_{SD}) vs. T_A

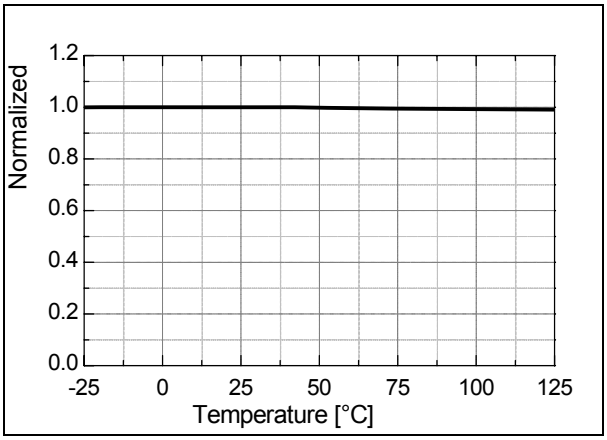


Figure 20. Over-Voltage Protection (V_{OV}) vs. T_A

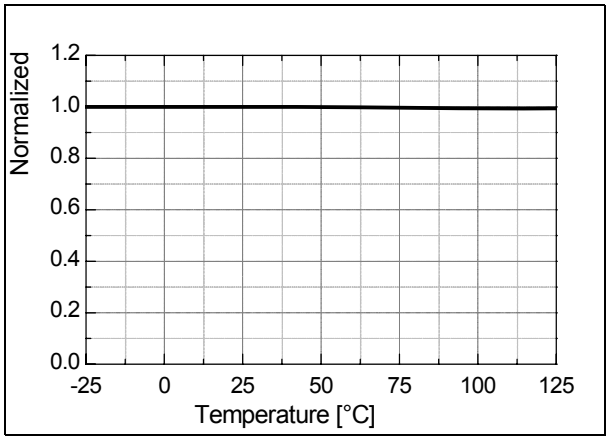


Figure 21. Sync High Threshold Voltage 2 (V_{SH2}) vs. T_A

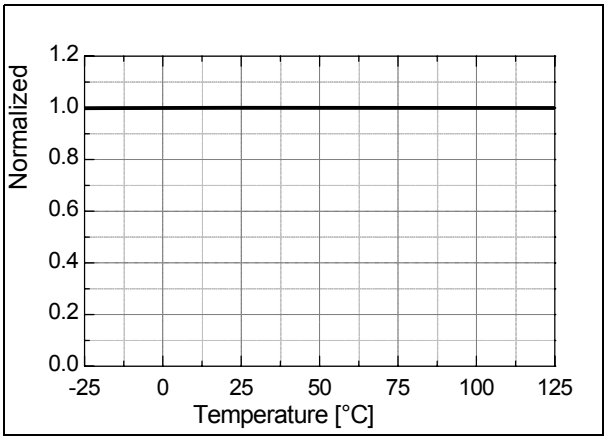


Figure 22. Sync Low Threshold Voltage 2 (V_{SL2}) vs. T_A

Functional Description

1. Startup: At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_a) connected to the V_{CC} pin, as illustrated in Figure 23. When V_{CC} reaches 12V, the power switch begins switching and the internal high-voltage current source is disabled. The power switch continues its normal switching operation and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 8V.

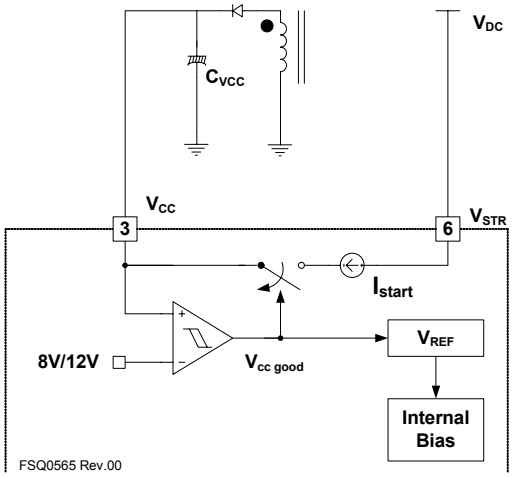


Figure 23. Startup Circuit

2.Feedback Control: power switch employs current-mode control, as shown in Figure 24. An opto-coupler (such as the FOD817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, pulling down the feedback voltage and reducing the duty cycle. This typically happens when the input voltage is increased or the output load is decreased.

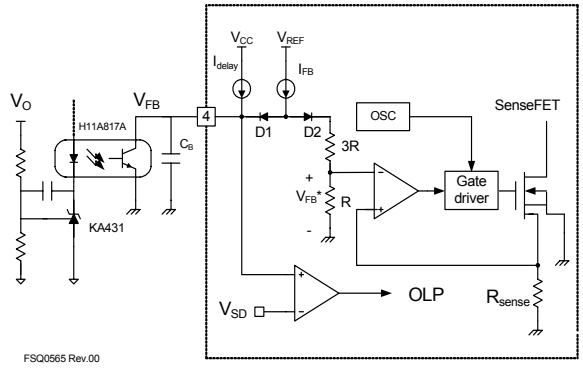


Figure 24. Pulse-Width-Modulation (PWM) Circuit

2.1 Pulse-by-Pulse Current Limit: Because current-mode control is employed, the peak current through the SenseFET is limited by the inverting input of PWM comparator (V_{FB}*), as shown in Figure 24. Assuming that the 0.9mA current source flows only through the internal resistor (3R + R = 2.8k), the cathode voltage of diode D2 is about 2.5V. Since D1 is blocked when the feedback voltage (V_{FB}) exceeds 2.5V, the maximum voltage of the cathode of D2 is clamped at this voltage, clamping V_{FB}*. Therefore, the peak value of the current through the SenseFET is limited.

2.2 Leading-Edge Blanking (LEB): At the instant the internal SenseFET is turned on, a high-current spike usually occurs through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the R_{sense} resistor would lead to incorrect feedback operation in the current-mode PWM control. To counter this effect, the power switch employs a leading-edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the SenseFET is turned on.

3. Synchronization: The FSQ-series employs a quasi-resonant switching technique to minimize the switching noise and loss. The basic waveforms of the quasi-resonant converter are shown in Figure 25. To minimize the MOSFET's switching loss, the MOSFET should be turned on when the drain voltage reaches its minimum value, which is indirectly detected by monitoring the V_{CC} winding voltage, as shown in Figure 25.

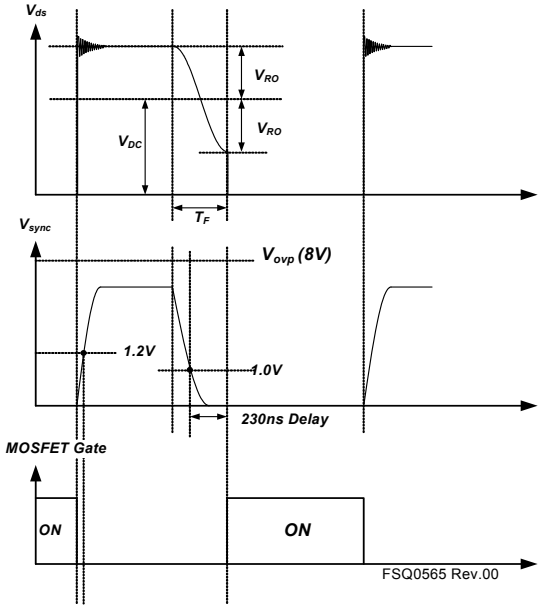


Figure 25. Quasi-Resonant Switching Waveforms

The switching frequency is the combination of blank time (t_B) and detection time window (t_W). In case of a heavy load, the sync voltage remains flat after t_B and waits for valley detection during t_W. This leads to a low switching frequency not suitable for heavy loads. To correct this drawback, additional timing is used. The timing conditions are described in Figures 26, 27, and 28. When the V_{sync} remains flat higher than 4.4V at the end of t_B, which is instant t_X, the next switching cycle starts after internal delay time from t_X. In the second case, the next switching occurs on the valley when the V_{sync} goes below 4.4V within t_B. Once V_{sync} detects the first valley in t_B, the other switching cycle follows classical QRC operation.

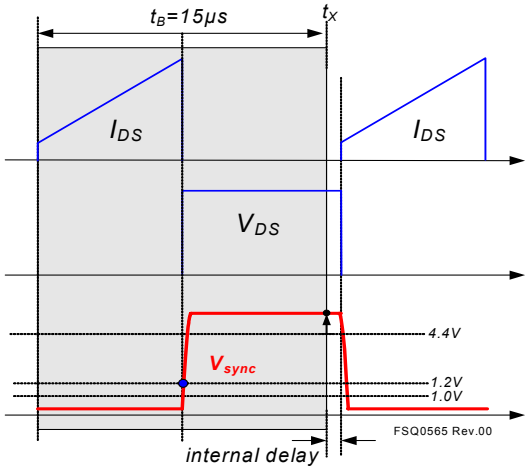


Figure 26. V_{sync} > 4.4V at t_X

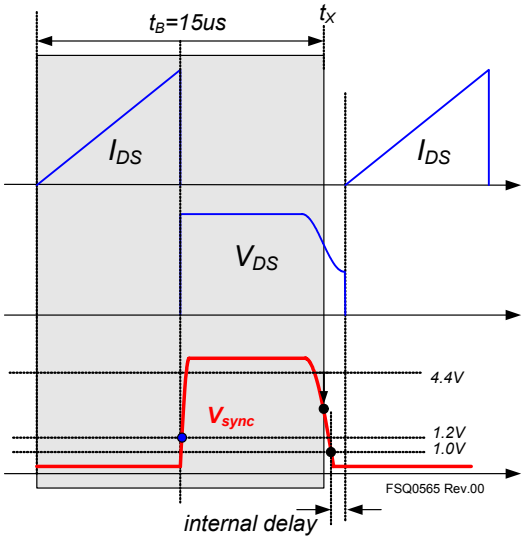


Figure 27. V_{sync} < 4.4V at t_X

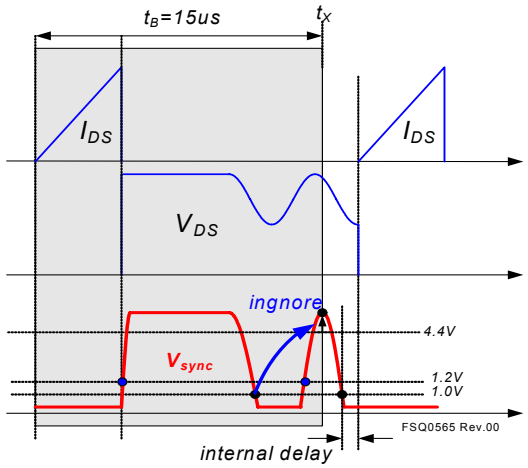


Figure 28. After V_{sync} Finds First Valley

4. Protection Circuits: The FSQ-series has several self-protective functions, such as Overload Protection (OLP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto-restart mode. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} falls down to the Under-Voltage Lockout (UVLO) stop voltage of 8V, the protection is reset and the startup circuit charges the V_{CC} capacitor. When the V_{CC} reaches the start voltage of 12V, normal operation resumes. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, reliability is improved without increasing cost.

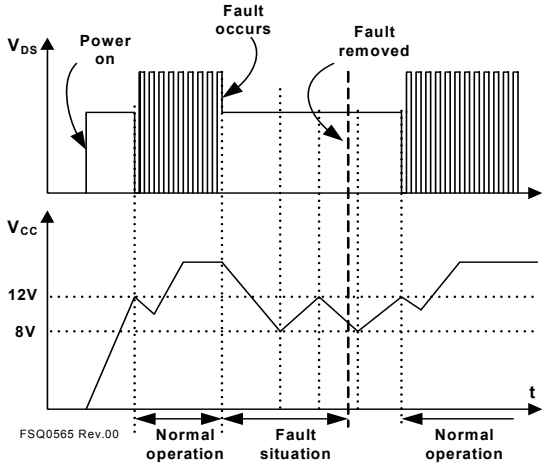


Figure 29. Auto Restart Protection Waveforms

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in the normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_O) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.5V, D1 is blocked and the 5μA current source starts to charge C_B slowly up to V_{CC}. In this condition, V_{FB} continues increasing until it reaches 6V, when the switching operation is terminated, as shown in Figure 30. The delay time for shutdown is the time required to charge C_{FB} from 2.5V to 6V with 5μA. A 20 ~ 50ms delay time is typical for most applications.

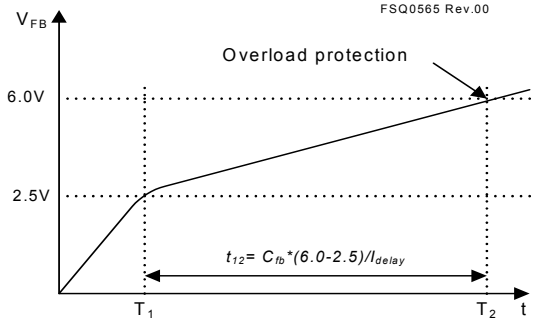


Figure 30. Overload Protection

4.2 Abnormal Over-Current Protection (AOCP): When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the LEB time. Even though the FSQ-series has overload protection, it is not enough to protect the FSQ-series in that abnormal case, since severe current stress is imposed on the SenseFET until OLP triggers. The FSQ-series has an internal AOCP circuit, shown in Figure 31. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the latch, resulting in the shutdown of the SMPS.

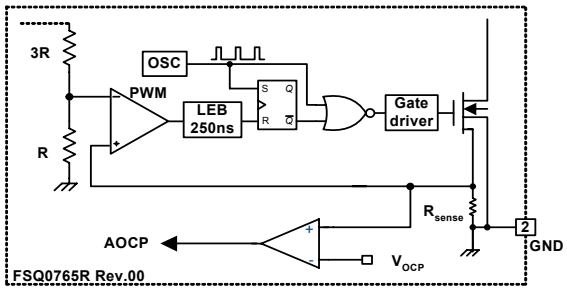


Figure 31. Abnormal Over-Current Protection

4.3 Output-Short Protection (OSP): If the output is shorted, steep current with extremely high di/dt can flow through the SenseFET during the LEB time. Such a steep current brings high voltage stress on the drain of SenseFET when turned off. To protect the device from such an abnormal condition, OSP is included in the FSQ-series. It is comprised of detecting V_{FB} and SenseFET turn-on time. When the V_{FB} is higher than 2V and the SenseFET turn-on time is lower than 1.2μs, the power switch recognizes this condition as an abnormal error and shuts down PWM switching until V_{CC} reaches V_{start} again. An abnormal condition output short is shown in Figure 32.

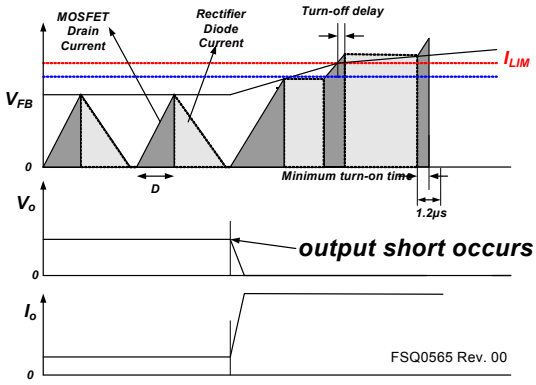


Figure 32. Output Short Waveforms

4.4.1 V_{CC} Over-Voltage Protection (OVP) of FSQ0565RS: If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost zero. In this case, V_{fb} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until overload protection is activated. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before overload protection is activated, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an over-voltage protection (OVP) circuit is employed. In general, V_{CC} is proportional to the output voltage and the

FSQ-series uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, an OVP circuit is activated, resulting in the termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed below 19V.

4.4.2 Sync Over-Voltage Protection (OVP) of FSQ0565RQ: If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost zero. V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection triggers. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection triggers, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the peak voltage of the sync signal is proportional to the output voltage and the FSQ-series uses a sync signal instead of directly monitoring the output voltage. If the sync signal exceeds 8V, an OVP is triggered, shutting down the SMPS. To avoid undesired triggering of OVP during normal operation, two points are considered, as depicted in Figure 33. The peak voltage of the sync signal should be designed below 6V and the spike of the SYNC pin must be as low as possible to avoid getting longer than t_{OVP} by decreasing the leakage inductance shown at V_{CC} winding coil.

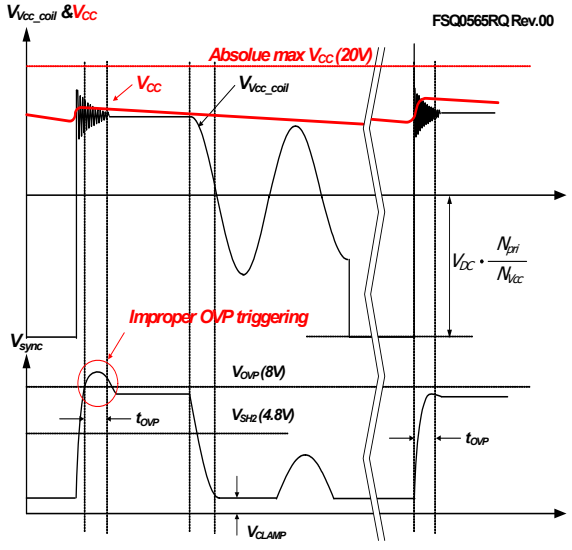


Figure 33. OVP Triggering of FSQ0565RQ

4.5 Thermal Shutdown with Hysteresis (TSD): The SenseFET and the control IC are built in one package. This enables the control IC to detect the abnormally high temperature of the SenseFET. If the temperature exceeds approximately 140°C, the thermal shutdown triggers IC shutdown. The IC resumes operation when the junction temperature decreases 60°C from TSD temperature and V_{CC} reaches startup voltage (V_{start}).

5. Soft-Start: The power switch has an internal soft-start circuit that increases PWM comparator inverting input voltage with the SenseFET current slowly after it starts. The typical soft-start time is 17.5ms. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. This mode helps prevent transformer saturation and reduces stress on the secondary diode during startup.

6. Burst Operation: To minimize power dissipation in stand-by mode, the power switch enters burst-mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 34, the device automatically enters burst-mode when the feedback voltage drops below V_{BURL} (350mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (550mV), switching resumes. The feedback voltage then falls and the process repeats. Burst-mode operation alternately enables and disables switching of the power SenseFET, thereby reducing switching loss in standby mode.

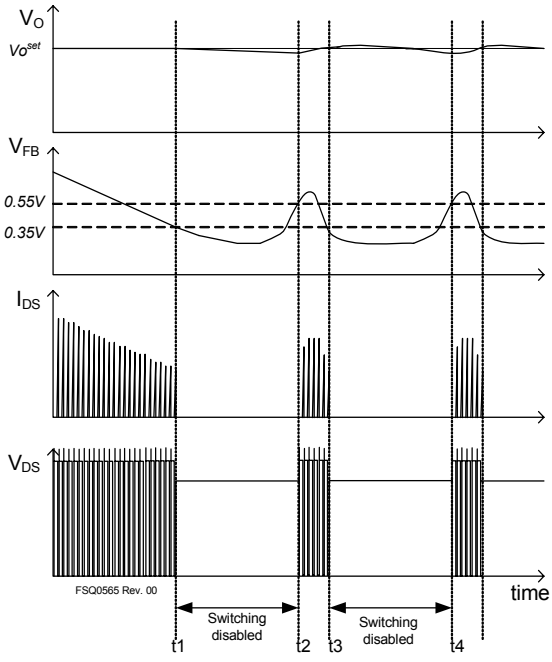


Figure 34. Waveforms of Burst Operation

7. Switching Frequency Limit: To minimize switching loss and Electromagnetic Interference (EMI), the MOSFET turns on when the drain voltage reaches its minimum value in quasi-resonant operation. However, this causes switching frequency to increases at light load conditions. As the load decreases or input voltage increases, the peak drain current diminishes and the switching frequency increases. This results in severe switching losses at light-load condition, as well as intermittent switching and audible noise. These problems create limitations for the quasi-resonant converter topology in a wide range of applications.

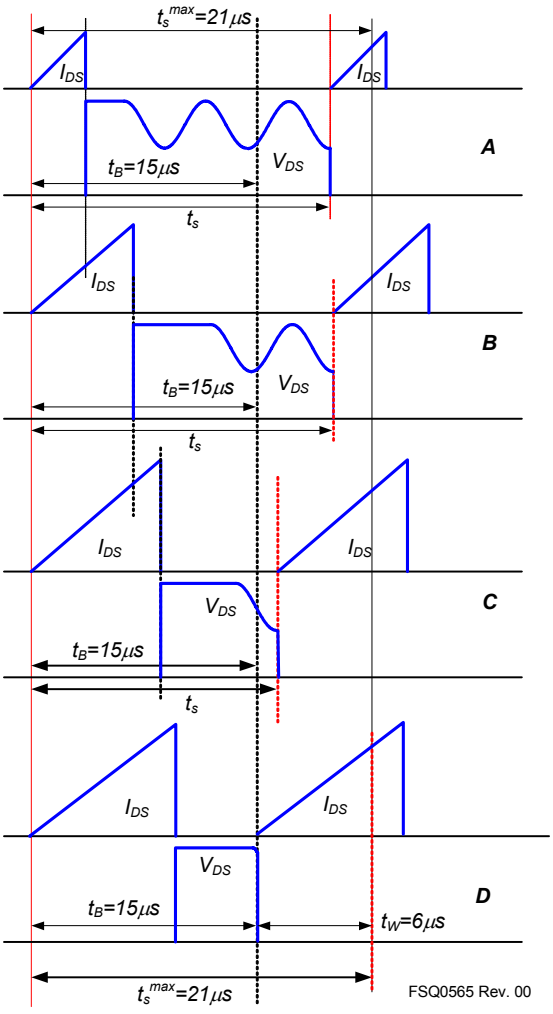


Figure 35. QRC Operation with Limited Frequency

To overcome these problems, FSQ-series employs a frequency-limit function, as shown in Figures 35 and 36. Once the SenseFET is turned on, the next turn-on is prohibited during the blanking time (t_B). After the blanking time, the controller finds the valley within the detection time window (t_W) and turns on the MOSFET, as shown in Figures 35 and Figure 36 (Cases A, B, and C). If no valley is found during t_W, the internal SenseFET is forced to turn on at the end of t_W (Case D). Therefore, the devices have a minimum switching frequency of 48kHz and a maximum switching frequency of 67kHz.

8. AVS (Alternating Valley Switching): Due to the quasi-resonant operation with limited frequency, the switching frequency varies depending on input voltage, load transition, and so on. At high input voltage, the switching on time is relatively small compared to low input voltage. The input voltage variance is small and the switching frequency modulation width becomes small. To improve the EMI performance, AVS is enabled when input voltage is high and the switching on time is small.

Internally, quasi-resonant operation is divided into two categories; one is first-valley switching and the other is second-valley switching after blanking time. In AVS, two successive occurrences of first-valley switching and the other two successive occurrences of second-valley switching is alternatively selected to maximize frequency modulation. As depicted in Figure 36, the switching frequency hops when the input voltage is high. The internal timing diagram of AVS is described in Figure 37.

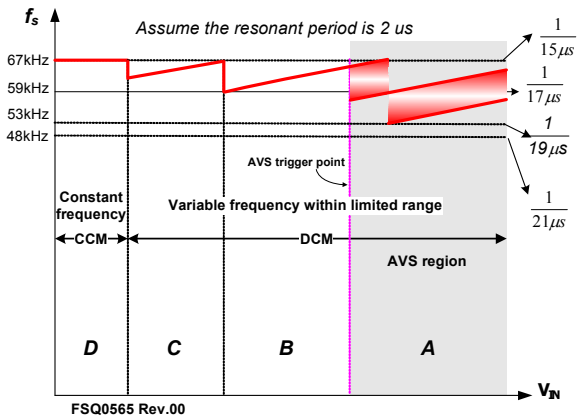


Figure 36. Switching Frequency Range

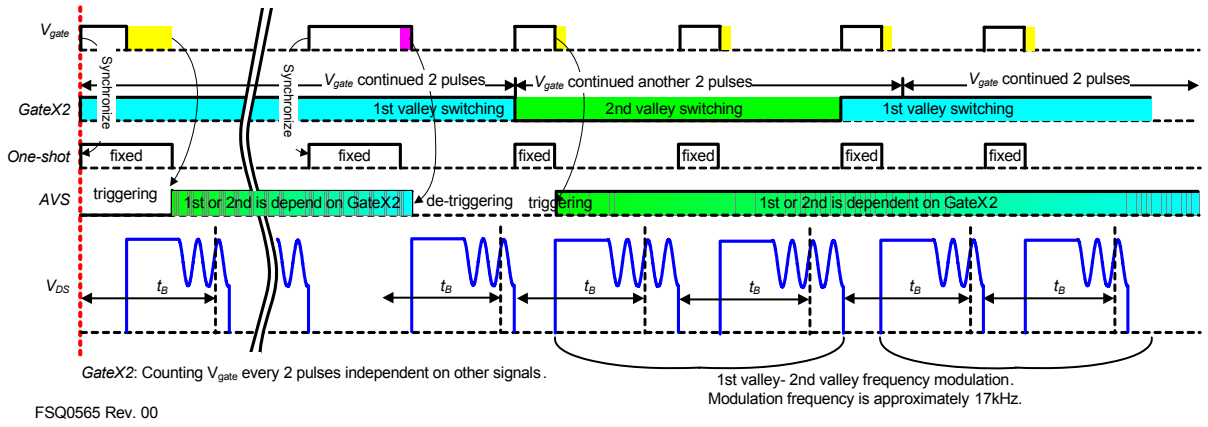


Figure 37. Alternating Valley Switching (AVS)

PCB Layout Guide

Due to the combined scheme, power switch shows better noise immunity than conventional PWM controller and MOSFET discrete solutions. Furthermore, internal drain current sense eliminates noise generation caused by a sensing resistor. There are some recommendations for PCB layout to enhance noise immunity and suppress the noise inevitable in power-handling components.

There are typically two grounds in the conventional SMPS: power ground and signal ground. The power ground is the ground for primary input voltage and power, while the signal ground is ground for PWM controller. In power switch, those two grounds share the same pin, GND. Normally the separate grounds do not share the same trace and meet only at one point, the GND pin. More, wider patterns for both grounds are good for large currents by decreasing resistance.

Capacitors at the V_{CC} and FB pins should be as close as possible to the corresponding pins to avoid noise from the switching device. Sometimes Mylar® or ceramic capacitors with electrolytic for V_{CC} is better for smooth operation. The ground of these capacitors needs to connect to the signal ground (not power ground).

The cathode of the snubber diode should be close to the Drain pin to minimize stray inductance. The Y-capacitor between primary and secondary should be directly connected to the power ground of DC link to maximize surge immunity.

Because the voltage range of feedback and sync line is small, it is affected by the noise of the drain pin. Those traces should not draw across or close to the drain line.

When the heat sink is connected to the ground, it should be connected to the power ground. If possible, avoid using jumper wires for power ground and drain.

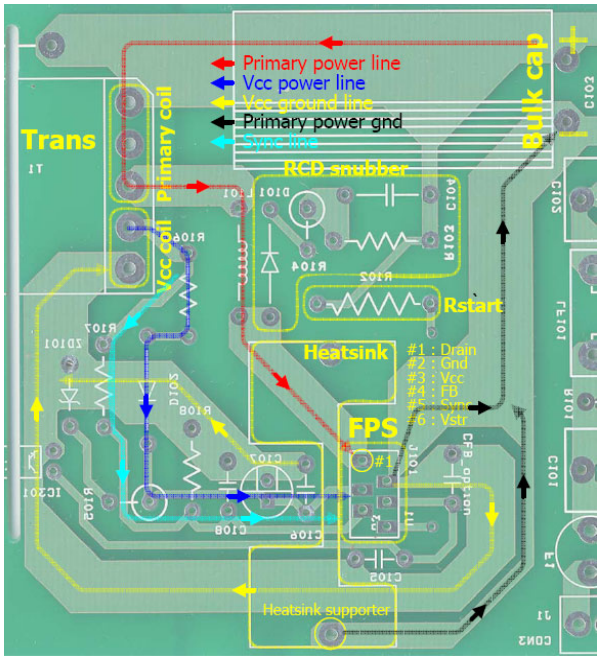


Figure 38. Recommended PCB Layout

Mylar® is a registered trademark of DuPont Teijin Films.

Typical Application Circuit

Application	Device	Input Voltage Range	Rated Output Power	Output Voltage (Maximum Current)
LCD Monitor Power Supply	FSQ0565RS	85-265V_{AC}	50W	5.0V (2.0A) 14V (2.8A)

Features

- Average efficiency of 25%, 50%, 75%, and 100% load conditions is higher than 80% at universal input
- Low standby mode power consumption (<1W at 230V_{AC} input and 0.5W load)
- Reduce EMI noise through valley switching operation
- Enhanced system reliability through various protection functions
- Internal soft-start (17.5ms)

Key Design Notes

- The delay time for overload protection is designed to be about 23ms with C105 of 33nF. If faster/slower triggering of OLP is required, C105 can be changed to a smaller/larger value (e.g. 100nF for 70ms).
- The input voltage of V_{Sync} must be between 4.7V and 8V just after MOSFET turn-off to guarantee hybrid control and to avoid OVP triggering during normal operation.
- The SMD-type 100nF capacitor must be placed as close as possible to V_{CC} pin to avoid malfunction by abrupt pulsating noises and to improve surge immunity.

1. Schematic

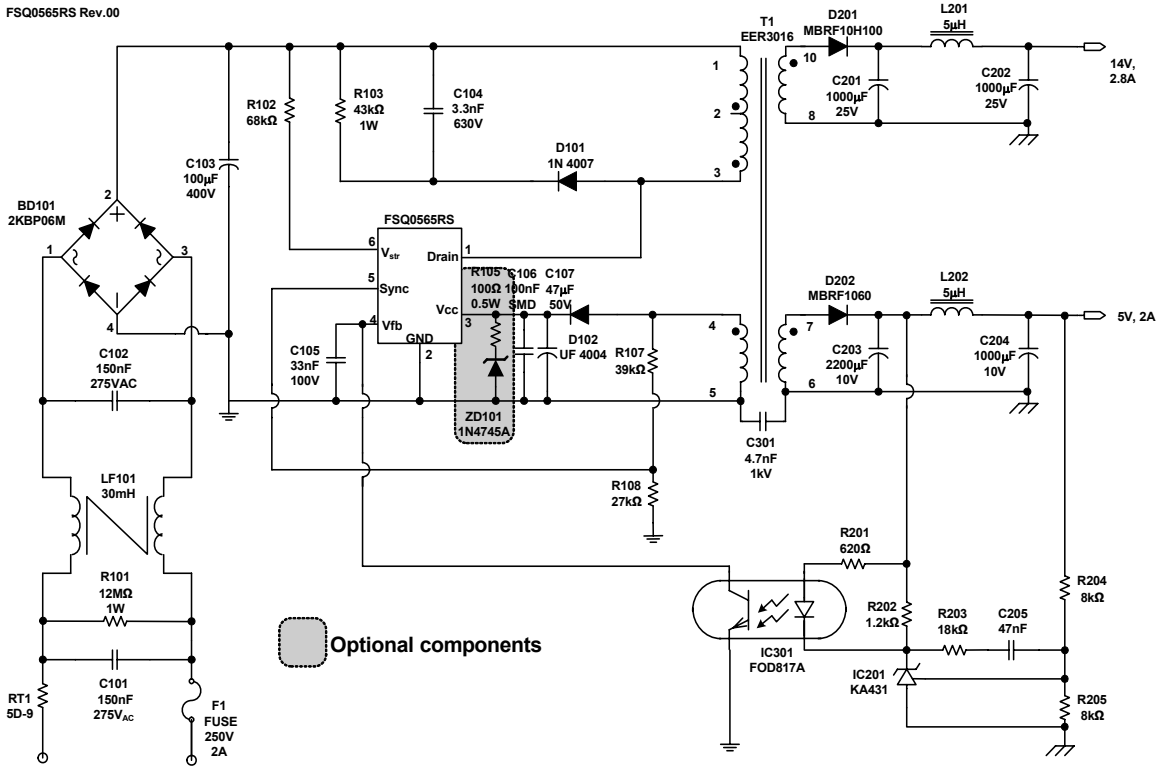


Figure 39. Demo Circuit of FSQ0565RS

2. Transformer

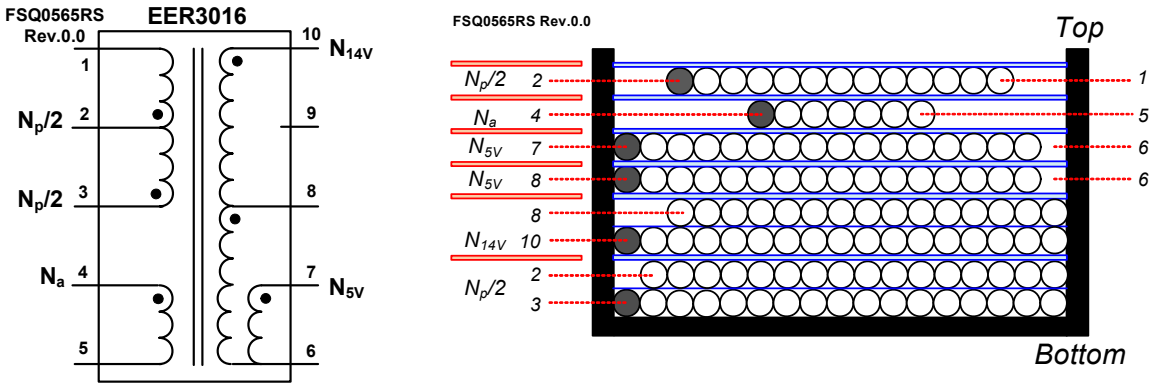


Figure 40. Transformer Schematic Diagram of FSQ0565RS

3. Winding Specification

Position	No	Pin (s→f)	Wire	Turns	Winding Method
Top	Insulation: Polyester Tape t = 0.025mm, 4 Layers				
	$N_p/2$	2 → 1	0.4ϕ × 1	10	Center Solenoid Winding
	Insulation: Polyester Tape t = 0.025mm, 2 Layers				
	N_a	4 → 5	0.15ϕ × 1	7	Center Solenoid Winding
	Insulation: Polyester Tape t = 0.025mm, 2 Layers				
	N_{5V}	7 → 6	0.4ϕ × 3(TIW)	3	Solenoid Winding
	Insulation: Polyester Tape t = 0.025mm, 2 Layers				
	N_{5V}	8 → 6	0.4ϕ × 3(TIW)	3	Solenoid Winding
	Insulation: Polyester Tape t = 0.025mm, 2 Layers				
	$N_{14V}/2$	10 → 8	0.4ϕ × 3(TIW)	5	Solenoid Winding
	Insulation: Polyester Tape t = 0.025mm, 2 Layers				
Bottom	$N_p/2$	3 → 2	0.4ϕ × 1	32	Two-Layer Solenoid Winding

4. Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 3	600μH ± 10%	67kHz, 1V
Leakage	1 - 3	15μH Maximum	Short all other pins

5. Core & Bobbin

- Core: EER3016 (Ae=109.7mm^2)
- Bobbin: EER3016

6. Demo Board Part List

Part	Value	Note	Part	Value	Note
Resistor			C205	47nF/50V	Film (Sehwa)
R101	1MΩ	1W	C301	4.7nF/1kV	Y-cap(Samwha)
R102	75kΩ	1/2W	**Inductor**		
R103	43kΩ	1W	L201	5μH	5A Rating
R104	0Ω	jumper	L202	5μH	5A Rating
R105	100Ω	*optional*, 1/4W	**Diode**		
R107	39kΩ	1/4W, 1%	D101	IN4007	VISHAY
R108	27kΩ	1/4W, 1%	D102	UF4004	VISHAY
R201	620Ω	1/4W	ZD101	1N4745A	1W 16V Zener Diode (optional)
R202	1.2kΩ	1/4W	D201	MBRF10H100	10A,100V Schottky Rectifier
R203	18kΩ	1/4W, 1%	D202	MBRF1060	10A,60V Schottky Rectifier
R204	8kΩ	1/4W, 1%	**IC**		
R205	8kΩ	1/4W, 1%	IC101	FSQ0565RS	Power Switch
Capacitor			IC201	KA431 (TL431)	Voltage Reference
C101	150nF/275V_{AC}	Box Capacitor(PILKOR)	IC202	FOD817A	Opto-Coupler
C102	150nF/275V_{AC}	Box Capacitor(PILKOR)	**Fuse**		
C103	100μF/400V	Electrolytic (Samwha)	Fuse	2A/250V	
C104	3.3nF/630V	Film (Sehwa)	**NTC**		
C105	33nF/50V	Film (Sehwa)	RT101	5D-9	
C106	100nF/50V	Mono (PILKOR)	**Bridge Diode**		
C107	47μF/50V	Electrolytic (Samyoung)	BD101	2KBP06M	Bridge Diode
C201	1000μF/25V	Low-ESR Electrolytic Capacitor(Samwha)	**Line Filter**		
C202	1000μF/25V	Low-ESR Electrolytic Capacitor(Samwha)	LF101	30mH	
C203	2200μF/10V	Low-ESR Electrolytic Capacitor(Samwha)	**Transformer**		
C204	1000μF/10V	Low-ESR Electrolytic Capacitor(Samwha)	T1	EER3016	Ae=109.7mm^2

Package Dimensions

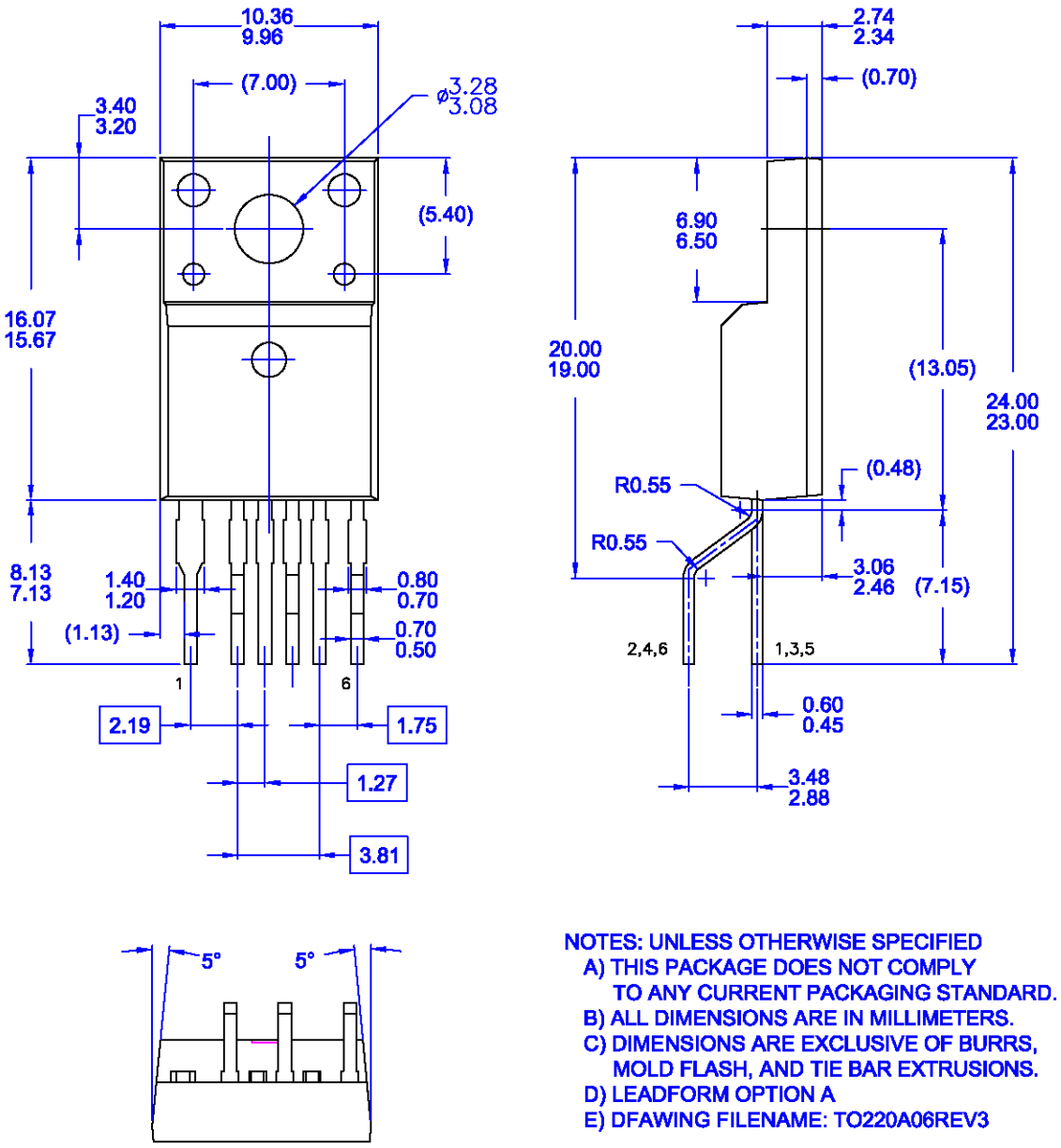


Figure 41. 6-Lead, TO-220 Package (Forming)

Package Dimensions (Continued)

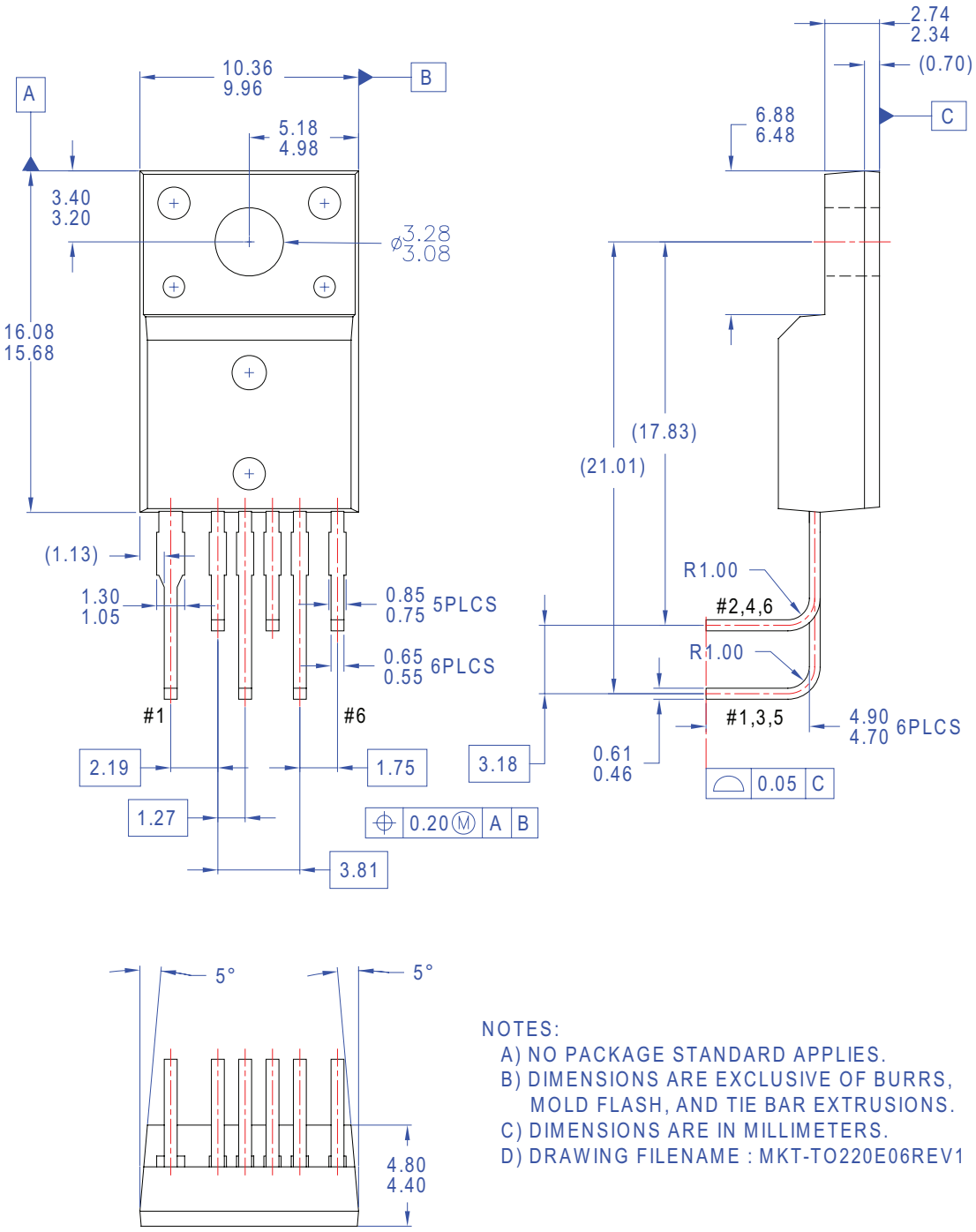


Figure 42. 6-Lead, TO-220 Package (L-Forming)

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