

# SN54251, SN54LS251 SN54S251, SN74251, SN74LS251, (TIM9905), SN74S251 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SDLS085 - DECEMBER 1972 - REVISED MARCH 1988

- Three-State Versions of '151, 'LS151, 'S151
- Three-State Outputs Interface Directly with System Bus
- Perform Parallel-to-Serial Conversion
- Permit Multiplexing from N-lines to One Line
- Complementary Outputs Provide True and Inverted Data
- Fully Compatible with Most TTL Circuits

| TYPE      | MAX NO.<br>OF COMMON<br>OUTPUTS | TYPICAL AVG PROP<br>DELAY TIME<br>(D TO Y) | TYPICAL<br>POWER<br>DISSIPATION |
|-----------|---------------------------------|--------------------------------------------|---------------------------------|
| SN54251   | 49                              | 17 ns                                      | 250 mW                          |
| SN74251   | 129                             | 17 ns                                      | 250 mW                          |
| SN54LS251 | 49                              | 17 ns                                      | 35 mW                           |
| SN74LS251 | 129                             | 17 ns                                      | 35 mW                           |
| SN54S251  | 39                              | 8 ns                                       | 275 mW                          |
| SN74S251  | 129                             | 8 ns                                       | 275 mW                          |

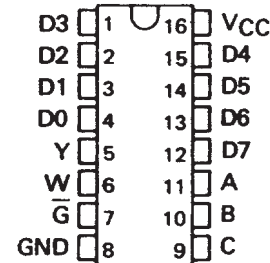
## description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources and feature a strobe-controlled three-state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit a number of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the 'average output disable time is shorter than the average output enable time. The SN54251 and SN74251 have output clamp diodes to attenuate reflections on the bus line.

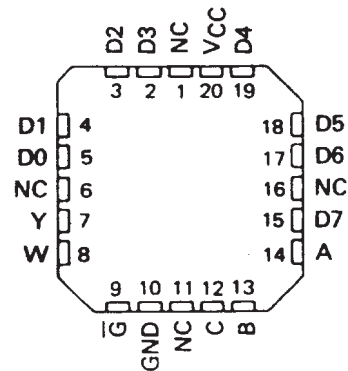
SN54251, SN54LS251, SN54S251 . . . J OR W PACKAGE  
SN74251 . . . N PACKAGE  
SN74LS251, SN74S251 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS251, SN54S251 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

| INPUTS |   |   |           | OUTPUTS |            |
|--------|---|---|-----------|---------|------------|
| SELECT |   |   | ENABLE    | Y       | W          |
| C      | B | A | $\bar{G}$ |         |            |
| X      | X | X | H         | Z       | Z          |
| L      | L | L | L         | D0      | $\bar{D0}$ |
| L      | L | H | L         | D1      | $\bar{D1}$ |
| L      | H | L | L         | D2      | $\bar{D2}$ |
| L      | H | H | L         | D3      | $\bar{D3}$ |
| H      | L | L | L         | D4      | $\bar{D4}$ |
| H      | L | H | L         | D5      | $\bar{D5}$ |
| H      | H | L | L         | D6      | $\bar{D6}$ |
| H      | H | H | L         | D7      | $\bar{D7}$ |

H = high logic level, L = low logic level

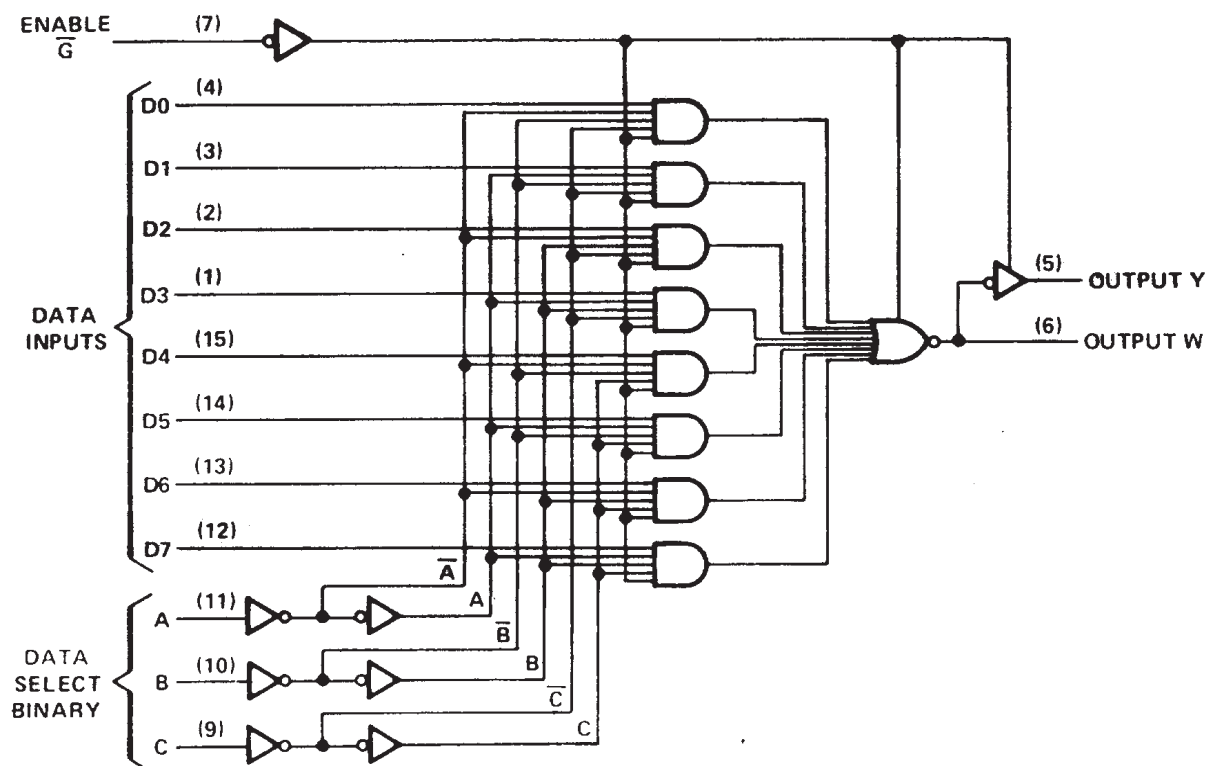
X = irrelevant, Z = high impedance (off)

D0, D1 . . . D7 = the level of the respective D input

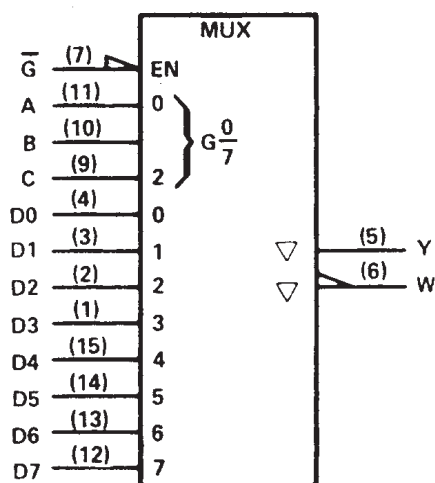
**SN54251, SN54LS251 SN54S251,  
SN74251, SN74LS251, (TIM9905), SN74S251  
DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS**

SDLS085 - DECEMBER 1972 - REVISED MARCH 1988

**logic diagram (positive logic)**



**logic symbol†**



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for D, J, N, and W packages.

# SN54251 SN74251, DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SDLS085 – DECEMBER 1972 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|                                               |                |
|-----------------------------------------------|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)         | 7 V            |
| Input voltage                                 | 5.5 V          |
| Off-state output voltage                      | 5.5 V          |
| Operating free-air temperature range: SN54251 | –55°C to 125°C |
| SN74251                                       | 0°C to 70°C    |
| Storage temperature range                     | –65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

|                                       | SN54251 |     |     | SN74251 |     |      | UNIT |
|---------------------------------------|---------|-----|-----|---------|-----|------|------|
|                                       | MIN     | NOM | MAX | MIN     | NOM | MAX  |      |
| Supply voltage, $V_{CC}$              | 4.5     | 5   | 5.5 | 4.75    | 5   | 5.25 | V    |
| High-level output current, $I_{OH}$   |         |     | –2  |         |     | –5.2 | mA   |
| Low-level output current, $I_{OL}$    |         |     | 16  |         |     | 16   | mA   |
| Operating free-air temperature, $T_A$ | –55     |     | 125 | 0       |     | 70   | °C   |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                | TEST CONDITIONS†                                                                            | MIN                    | TYP‡ | MAX            | UNIT          |
|----------------------------------------------------------|---------------------------------------------------------------------------------------------|------------------------|------|----------------|---------------|
| $V_{IH}$ High-level input voltage                        |                                                                                             | 2                      |      |                | V             |
| $V_{IL}$ Low-level input voltage                         |                                                                                             |                        |      | 0.8            | V             |
| $V_{IK}$ Input clamp voltage                             | $V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$                                                 |                        |      | –1.5           | V             |
| $V_{OH}$ High-level output voltage                       | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$    | 2.4                    | 3.2  |                | V             |
| $V_{OL}$ Low-level output voltage                        | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$ |                        | 0.2  | 0.4            | V             |
| $I_{OZ}$ Off-state (high-impedance-state) output current | $V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}$                                                 | $V_O = 2.4 \text{ V}$  |      | 40             | $\mu\text{A}$ |
|                                                          |                                                                                             | $V_O = 0.4 \text{ V}$  |      | –40            |               |
| $V_O$ Output clamp voltage                               | $V_{CC} = \text{MAX}, V_{IH} = 4.5 \text{ V}$                                               | $I_O = -12 \text{ mA}$ |      | –1.5           | V             |
|                                                          |                                                                                             | $I_O = 12 \text{ mA}$  |      | $V_{CC} + 1.5$ |               |
| $I_I$ Input current at maximum input voltage             | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$                                                  |                        |      | 1              | mA            |
| $I_{IH}$ High-level input current                        | $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$                                                  |                        |      | 40             | $\mu\text{A}$ |
| $I_{IL}$ Low-level input current                         | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$                                                  |                        |      | –1.6           | mA            |
| $I_{OS}$ Short-circuit output current§                   | $V_{CC} = \text{MAX}$                                                                       | –18                    |      | –55            | mA            |
| $I_{CC}$ Supply current                                  | $V_{CC} = \text{MAX},$ All inputs at 4.5 V, All outputs open                                |                        | 38   | 62             | mA            |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time.

SN54251 SN74251,  
DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SDLS085 – DECEMBER 1972 – REVISED MARCH 1988

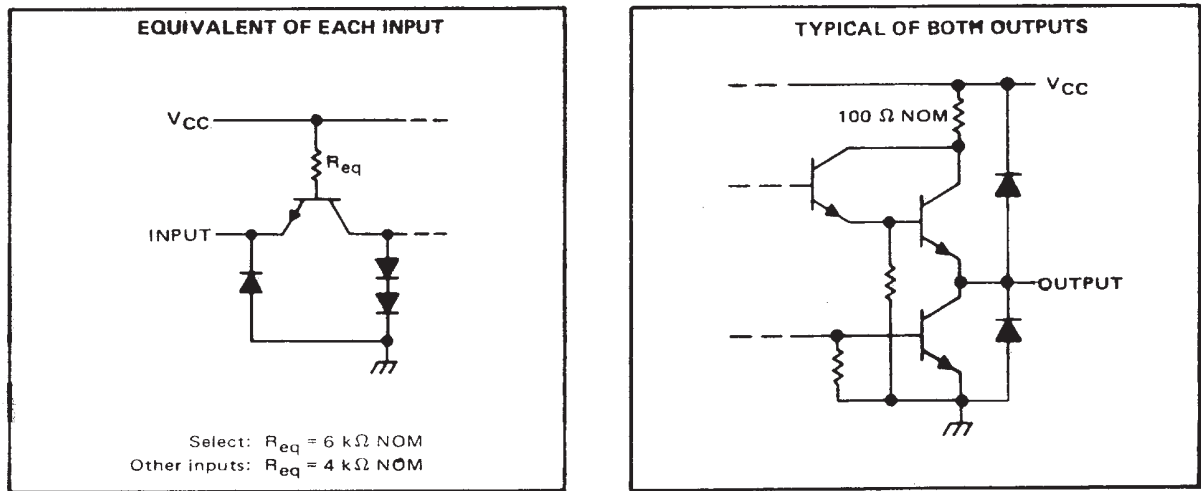
switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER† | FROM<br>(INPUT)          | TO<br>(OUTPUT) | TEST CONDITIONS                          | MIN | TYP | MAX | UNIT |
|------------|--------------------------|----------------|------------------------------------------|-----|-----|-----|------|
| tPLH       | A, B, or C<br>(4 levels) | Y              | CL = 50 pF,<br>RL = 400 Ω,<br>See Note 2 | 29  | 45  | ns  |      |
| tPHL       |                          |                |                                          | 28  | 45  |     |      |
| tPLH       | A, B, or C<br>(3 levels) | W              |                                          | 20  | 33  | ns  |      |
| tPHL       |                          |                |                                          | 21  | 33  |     |      |
| tPLH       | Any D                    | Y              |                                          | 17  | 28  | ns  |      |
| tPHL       |                          |                |                                          | 18  | 28  |     |      |
| tPLH       | Any D                    | W              |                                          | 10  | 15  | ns  |      |
| tPHL       |                          |                |                                          | 9   | 15  |     |      |
| tPZH       | G̅                       | Y              |                                          | 17  | 27  | ns  |      |
| tPZL       |                          |                |                                          | 26  | 40  |     |      |
| tPZH       | G̅                       | W              |                                          | 17  | 27  | ns  |      |
| tPZL       |                          |                |                                          | 24  | 40  |     |      |
| tPHZ       | G̅                       | Y              | CL = 5 pF,<br>RL = 400 Ω,<br>See Note 2  | 5   | 8   | ns  |      |
| tPLZ       |                          |                |                                          | 15  | 23  |     |      |
| tPHZ       | G̅                       | W              |                                          | 5   | 8   | ns  |      |
| tPLZ       |                          |                |                                          | 15  | 23  |     |      |

†tPLH = Propagation delay time, low-to-high-level output  
tPHL = Propagation delay time, high-to-low-level output  
tPZH = Output enable time to high level  
tPZL = Output enable time to low level  
tPHZ = Output disable time from high level  
tPLZ = Output disable time from low level

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



# SN54LS251 SN74LS251, DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SDLS085 – DECEMBER 1972 – REVISED MARCH 1988

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|                                                 |                |
|-------------------------------------------------|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)           | 7 V            |
| Input voltage                                   | 7 V            |
| Off-state output voltage                        | 5.5 V          |
| Operating free-air temperature range: SN54LS251 | 55°C to 125°C  |
| SN74LS251                                       | 0°C to 70°C    |
| Storage temperature range                       | –65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

|                                      | SN54LS251 |     |     | SN74LS251 |     |       | UNIT |
|--------------------------------------|-----------|-----|-----|-----------|-----|-------|------|
|                                      | MIN       | NOM | MAX | MIN       | NOM | MAX   |      |
| $V_{CC}$ Supply voltage              | 4.5       | 5   | 5.5 | 4.75      | 5   | 5.25  | V    |
| $V_{IH}$ High-level input voltage    | 2         |     |     | 2         |     |       | V    |
| $V_{IL}$ Low-level input voltage     |           |     | 0.7 |           |     | 0.8   | V    |
| $I_{OH}$ High-level output current   |           |     | – 1 |           |     | – 2.6 | mA   |
| $I_{OL}$ Low-level output current    |           |     | 4   |           |     | 8     | mA   |
| $T_A$ Operating free-air temperature | – 55      |     | 125 | 0         |     | 70    | °C   |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER         |                       | TEST CONDITIONS†                                                                             |  | SN54LS251              |        | SN74LS251 |       | UNIT |
|-------------------|-----------------------|----------------------------------------------------------------------------------------------|--|------------------------|--------|-----------|-------|------|
|                   |                       |                                                                                              |  | MIN                    | TYP ‡  | MAX       | MIN   |      |
| V <sub>IK</sub>   |                       | V <sub>CC</sub> = MIN, I <sub>I</sub> = – 18 mA                                              |  | – 1.5                  |        | – 1.5     |       | V    |
| V <sub>OH</sub>   |                       | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX<br>I <sub>OH</sub> = MAX |  | 2.4                    | 3.4    | 2.4       | 3.1   | V    |
| V <sub>OL</sub>   |                       | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = MAX                       |  | I <sub>OL</sub> = 4 mA |        | 0.25 0.4  |       | V    |
|                   |                       |                                                                                              |  | I <sub>OL</sub> = 8 mA |        | 0.35 0.5  |       |      |
| I <sub>OZ</sub>   |                       | V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V                                                 |  | V <sub>O</sub> = 2.7 V |        | 20        |       | μA   |
|                   |                       |                                                                                              |  | V <sub>O</sub> = 0.4 V |        | – 20      |       |      |
| I <sub>I</sub>    |                       | V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V                                                  |  | 0.1                    |        | 0.1       |       | mA   |
| I <sub>IH</sub>   |                       | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V                                                |  | 20                     |        | 20        |       | μA   |
| I <sub>IL</sub>   | Enable $\overline{G}$ | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4                                                  |  | – 0.2                  |        | – 0.2     |       | mA   |
|                   | All other             |                                                                                              |  | – 0.4                  |        | – 0.4     |       |      |
| I <sub>OS</sub> § |                       | V <sub>CC</sub> = MAX                                                                        |  | – 30                   | – 130  | – 30      | – 130 | mA   |
| I <sub>CC</sub>   |                       | V <sub>CC</sub> = MAX, See Note 3                                                            |  | Condition A            | 6.1 10 | 6.1 10    | mA    |      |
|                   |                       |                                                                                              |  | Condition B            | 7.1 12 | 7.1 12    |       |      |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 3:  $I_{CC}$  is measured with the outputs open and all data and select inputs at 4.5 V under the following conditions:

- A. Enable grounded.
- B. Strobe at 4.5 V.

SN54LS251 SN74LS251, (TIM9905),  
DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

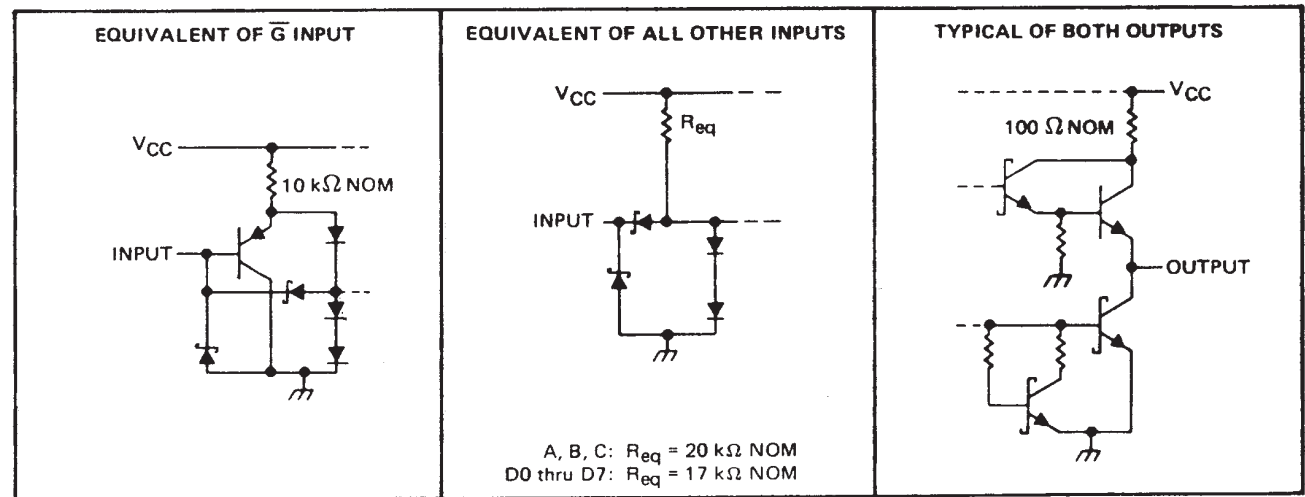
SDLS085 – DECEMBER 1972 – REVISED MARCH 1988

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER† | FROM<br>(INPUT)          | TO<br>(OUTPUT) | TEST CONDITIONS                         | MIN | TYP | MAX | UNIT |
|------------|--------------------------|----------------|-----------------------------------------|-----|-----|-----|------|
| tPLH       | A, B, or C<br>(4 levels) | Y              | CL = 15 pF,<br>RL = 2 kΩ,<br>See Note 2 | 29  | 45  | ns  |      |
| tPHL       |                          |                |                                         | 28  | 45  |     |      |
| tPLH       | A, B, or C<br>(3 levels) | W              |                                         | 20  | 33  | ns  |      |
| tPHL       |                          |                |                                         | 21  | 33  |     |      |
| tPLH       | Any D                    | Y              |                                         | 17  | 28  | ns  |      |
| tPHL       |                          |                |                                         | 18  | 28  |     |      |
| tPLH       | Any D                    | W              |                                         | 10  | 15  | ns  |      |
| tPHL       |                          |                |                                         | 9   | 15  |     |      |
| tPZH       | G̅                       | Y              |                                         | 30  | 45  | ns  |      |
| tPZL       |                          |                |                                         | 26  | 40  |     |      |
| tPZH       | G̅                       | W              |                                         | 17  | 27  | ns  |      |
| tPZL       |                          |                |                                         | 24  | 40  |     |      |
| tPHZ       | G̅                       | Y              | CL = 5 pF,<br>RL = 2 kΩ,<br>See Note 2  | 30  | 45  | ns  |      |
| tPLZ       |                          |                |                                         | 15  | 25  |     |      |
| tPHZ       | G̅                       | W              |                                         | 37  | 55  | ns  |      |
| tPLZ       |                          |                |                                         | 15  | 25  |     |      |

$t_{PLH}$  = Propagation delay time, low-to-high-level output  
 $t_{PHL}$  = Propagation delay time, high-to-low-level output  
 $t_{PZH}$  = Output enable time to high level  
 $t_{PZL}$  = Output enable time to low level  
 $t_{PHZ}$  = Output disable time from high level  
 $t_{PLZ}$  = Output disable time from low level  
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



# SN54S251 SN74S251, DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SDLS085 – DECEMBER 1972 – REVISED MARCH 1988

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|                                                |                |
|------------------------------------------------|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)          | 7 V            |
| Input voltage                                  | 5.5 V          |
| Off-state output voltage                       | 5.5 V          |
| Operating free-air temperature range: SN54S251 | –55°C to 125°C |
| SN74S251                                       | 0°C to 70°C    |
| Storage temperature range                      | –65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

|                                       | SN54S251 |     |     | SN74S251 |     |      | UNIT |
|---------------------------------------|----------|-----|-----|----------|-----|------|------|
|                                       | MIN      | NOM | MAX | MIN      | NOM | MAX  |      |
| Supply voltage, $V_{CC}$              | 4.5      | 5   | 5.5 | 4.75     | 5   | 5.25 | V    |
| High-level output current, $I_{OH}$   |          |     | –2  |          |     | –6.5 | mA   |
| Low-level output current, $I_{OL}$    |          |     | 20  |          |     | 20   | mA   |
| Operating free-air temperature, $T_A$ | –55      |     | 125 | 0        |     | 70   | °C   |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                | TEST CONDITIONS†                                    |                                                     | MIN | TYP‡ | MAX  | UNIT          |
|----------------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----|------|------|---------------|
| $V_{IH}$ High-level input voltage                        |                                                     |                                                     | 2   |      |      | V             |
| $V_{IL}$ Low-level input voltage                         |                                                     |                                                     |     |      | 0.8  | V             |
| $V_{IK}$ Input clamp voltage                             | $V_{CC} = \text{MIN},$                              | $I_I = -18 \text{ mA}$                              |     |      | –1.2 | V             |
| $V_{OH}$ High-level output voltage                       | $V_{CC} = \text{MIN},$<br>$V_{IL} = 0.8 \text{ V},$ | $V_{IH} = 2 \text{ V},$<br>$I_{OH} = \text{MAX}$    | 2.4 | 3.4  |      | V             |
|                                                          |                                                     |                                                     |     |      | 3.2  |               |
| $V_{OL}$ Low-level output voltage                        | $V_{CC} = \text{MIN},$<br>$V_{IL} = 0.8 \text{ V},$ | $V_{IH} = 2 \text{ V},$<br>$I_{OL} = 20 \text{ mA}$ |     |      | 0.5  | V             |
| $I_{OZ}$ Off-state (high-impedance-state) output current | $V_{CC} = \text{MAX},$<br>$V_{IH} = 2 \text{ V}$    | $V_O = 2.4 \text{ V}$                               |     |      | 50   | $\mu\text{A}$ |
|                                                          |                                                     | $V_O = 0.5 \text{ V}$                               |     |      | –50  |               |
| $I_I$ Input current at maximum input voltage             | $V_{CC} = \text{MAX},$                              | $V_I = 5.5 \text{ V}$                               |     |      | 1    | mA            |
| $I_{IH}$ High-level input current                        | $V_{CC} = \text{MAX},$                              | $V_I = 2.7 \text{ V}$                               |     |      | 50   | $\mu\text{A}$ |
| $I_{IL}$ Low-level input current                         | $V_{CC} = \text{MAX},$                              | $V_I = 0.5 \text{ V}$                               |     |      | –2   | mA            |
| $I_{OS}$ Short-circuit output current§                   | $V_{CC} = \text{MAX}$                               |                                                     | –40 |      | –100 | mA            |
| $I_{CC}$ Supply current                                  | $V_{CC} = \text{MAX},$                              | All inputs at 4.5 V,<br>All outputs open            |     | 55   | 85   | mA            |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.



# SN54S251 SN74S251, DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

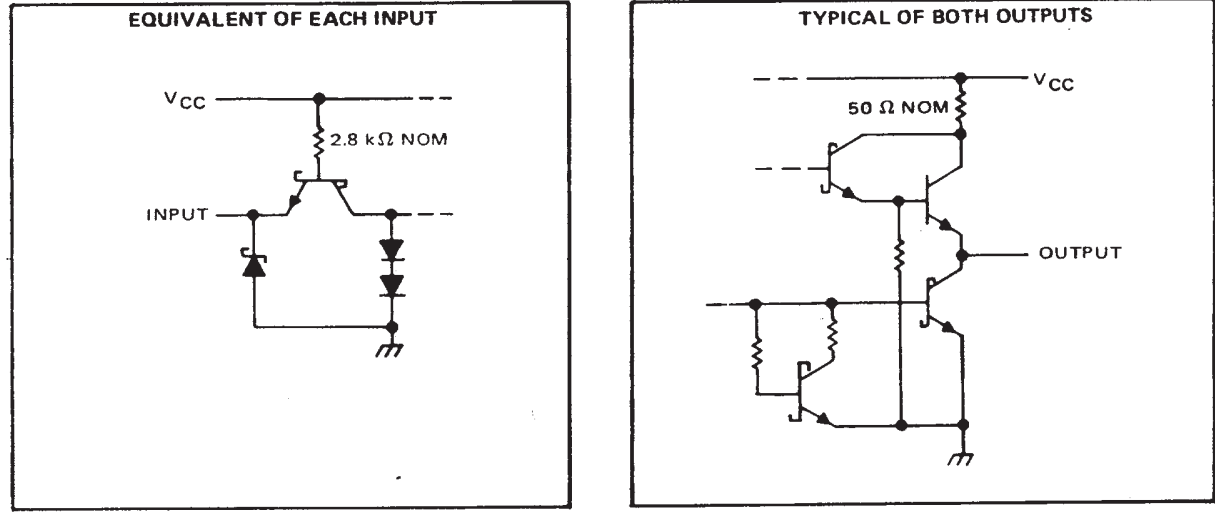
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switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER† | FROM<br>(INPUT)          | TO<br>(OUTPUT) | TEST CONDITIONS                          | MIN | TYP  | MAX | UNIT |
|------------|--------------------------|----------------|------------------------------------------|-----|------|-----|------|
| tPLH       | A, B, or C<br>(4 levels) | Y              | CL = 15 pF,<br>RL = 280 Ω,<br>See Note 2 | 12  | 18   | ns  |      |
| tPHL       |                          |                |                                          | 13  | 19.5 |     |      |
| tPLH       | A, B, or C<br>(3 levels) | W              |                                          | 10  | 15   | ns  |      |
| tPHL       |                          |                |                                          | 9   | 13.5 |     |      |
| tPLH       | Any D                    | Y              |                                          | 8   | 12   | ns  |      |
| tPHL       |                          |                |                                          | 8   | 12   |     |      |
| tPLH       | Any D                    | W              |                                          | 4.5 | 7    | ns  |      |
| tPHL       |                          |                |                                          | 4.5 | 7    |     |      |
| tPZH       | G̅                       | Y              | CL = 50 pF,<br>RL = 280 Ω,<br>See Note 2 | 13  | 19.5 | ns  |      |
| tPZL       |                          |                |                                          | 14  | 21   |     |      |
| tPZH       | G̅                       | W              |                                          | 13  | 19.5 | ns  |      |
| tPZL       |                          |                |                                          | 14  | 21   |     |      |
| tPHZ       | G̅                       | Y              | CL = 5 pF,<br>RL = 280 Ω,<br>See Note 2  | 5.5 | 8.5  | ns  |      |
| tPLZ       |                          |                |                                          | 9   | 14   |     |      |
| tPHZ       | G̅                       | W              |                                          | 5.5 | 8.5  | ns  |      |
| tPLZ       |                          |                |                                          | 9   | 14   |     |      |

- †t<sub>PLH</sub> = Propagation delay time, low-to-high-level output  
t<sub>PHL</sub> = Propagation delay time, high-to-low-level output  
t<sub>PZH</sub> = Output enable time to high level  
t<sub>PZL</sub> = Output enable time to low level  
t<sub>PHZ</sub> = Output disable time from high level  
t<sub>PLZ</sub> = Output disable time from low level  
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

## schematics of inputs and outputs





**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)  | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|--------------------------|-------------------------|
| 7601601EA        | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 7601601EA<br>SNJ54LS251J | <a href="#">Samples</a> |
| 7601601FA        | ACTIVE        | CFP          | W                  | 16   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 7601601FA<br>SNJ54LS251W | <a href="#">Samples</a> |
| 7601601FA        | ACTIVE        | CFP          | W                  | 16   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | 7601601FA<br>SNJ54LS251W | <a href="#">Samples</a> |
| JM38510/30905BEA | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30905BEA     | <a href="#">Samples</a> |
| JM38510/30905BEA | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30905BEA     | <a href="#">Samples</a> |
| M38510/30905BEA  | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30905BEA     | <a href="#">Samples</a> |
| M38510/30905BEA  | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>30905BEA     | <a href="#">Samples</a> |
| SN54LS251J       | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | SN54LS251J               | <a href="#">Samples</a> |
| SN54LS251J       | ACTIVE        | CDIP         | J                  | 16   | 1              | TBD                        | Call TI                 | N / A for Pkg Type   | -55 to 125   | SN54LS251J               | <a href="#">Samples</a> |
| SN74LS251D       | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | LS251                    | <a href="#">Samples</a> |
| SN74LS251D       | ACTIVE        | SOIC         | D                  | 16   | 40             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | LS251                    | <a href="#">Samples</a> |
| SN74LS251DR      | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | LS251                    | <a href="#">Samples</a> |
| SN74LS251DR      | ACTIVE        | SOIC         | D                  | 16   | 2500           | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | LS251                    | <a href="#">Samples</a> |
| SN74LS251N       | ACTIVE        | PDIP         | N                  | 16   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | N / A for Pkg Type   | 0 to 70      | SN74LS251N               | <a href="#">Samples</a> |
| SN74LS251N       | ACTIVE        | PDIP         | N                  | 16   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | N / A for Pkg Type   | 0 to 70      | SN74LS251N               | <a href="#">Samples</a> |
| SN74LS251NE4     | ACTIVE        | PDIP         | N                  | 16   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | N / A for Pkg Type   | 0 to 70      | SN74LS251N               | <a href="#">Samples</a> |
| SN74LS251NE4     | ACTIVE        | PDIP         | N                  | 16   | 25             | Green (RoHS<br>& no Sb/Br) | NIPDAU                  | N / A for Pkg Type   | 0 to 70      | SN74LS251N               | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)  | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|--------------------------|-------------------------|
| SN74LS251NSR     | ACTIVE        | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | 74LS251                  | <a href="#">Samples</a> |
| SN74LS251NSR     | ACTIVE        | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | NIPDAU                  | Level-1-260C-UNLIM   | 0 to 70      | 74LS251                  | <a href="#">Samples</a> |
| SNJ54LS251FK     | ACTIVE        | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | SNJ54LS251FK             | <a href="#">Samples</a> |
| SNJ54LS251FK     | ACTIVE        | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | SNJ54LS251FK             | <a href="#">Samples</a> |
| SNJ54LS251J      | ACTIVE        | CDIP         | J               | 16   | 1           | TBD                     | Call TI                 | N / A for Pkg Type   | -55 to 125   | 7601601EA<br>SNJ54LS251J | <a href="#">Samples</a> |
| SNJ54LS251J      | ACTIVE        | CDIP         | J               | 16   | 1           | TBD                     | Call TI                 | N / A for Pkg Type   | -55 to 125   | 7601601EA<br>SNJ54LS251J | <a href="#">Samples</a> |
| SNJ54LS251W      | ACTIVE        | CFP          | W               | 16   | 1           | TBD                     | Call TI                 | N / A for Pkg Type   | -55 to 125   | 7601601FA<br>SNJ54LS251W | <a href="#">Samples</a> |
| SNJ54LS251W      | ACTIVE        | CFP          | W               | 16   | 1           | TBD                     | Call TI                 | N / A for Pkg Type   | -55 to 125   | 7601601FA<br>SNJ54LS251W | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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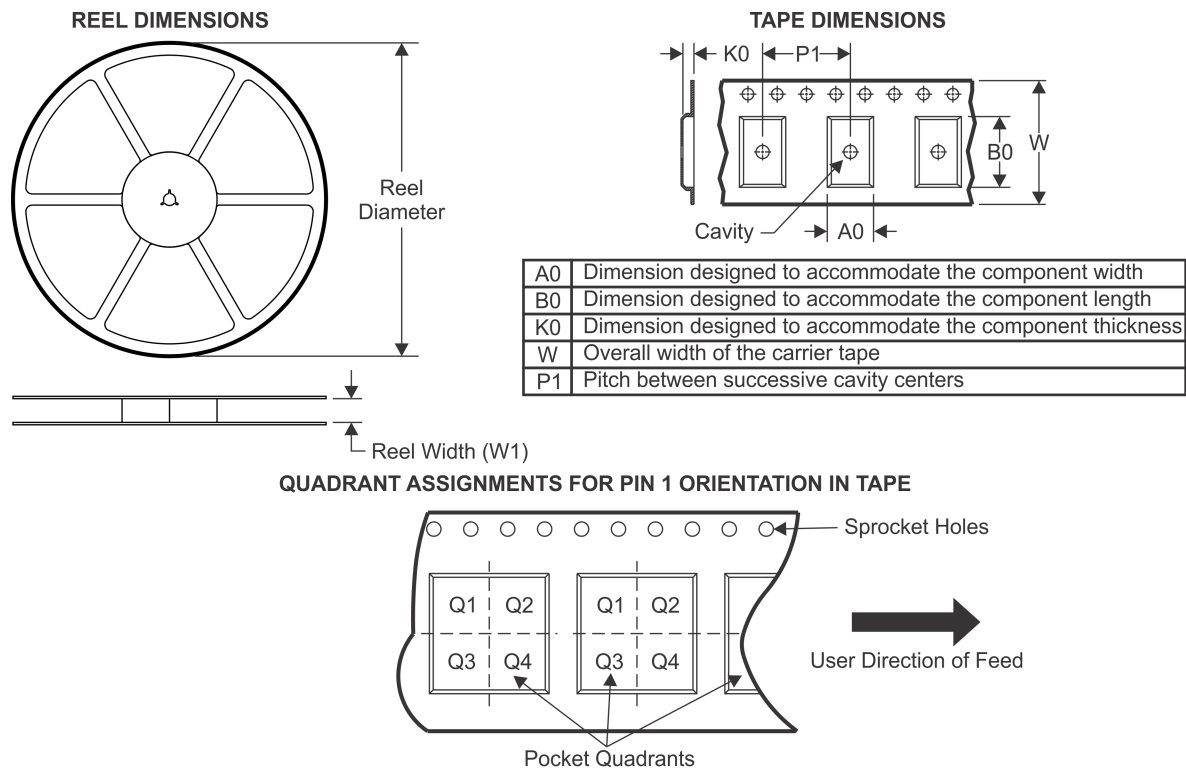
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS251, SN74LS251 :**

- Catalog: [SN74LS251](#)
- Military: [SN54LS251](#)

NOTE: Qualified Version Definitions:

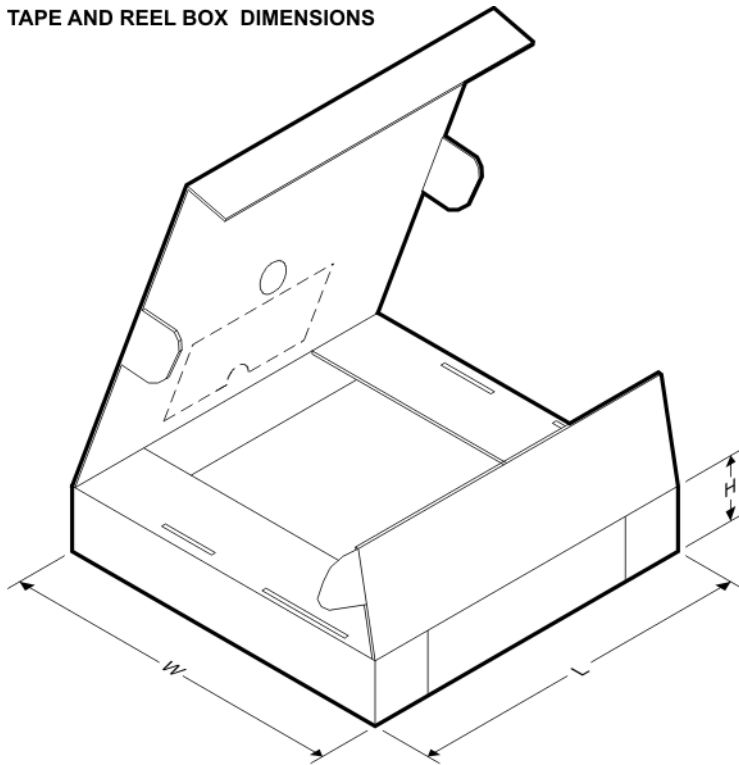
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS251DR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LS251NSR | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

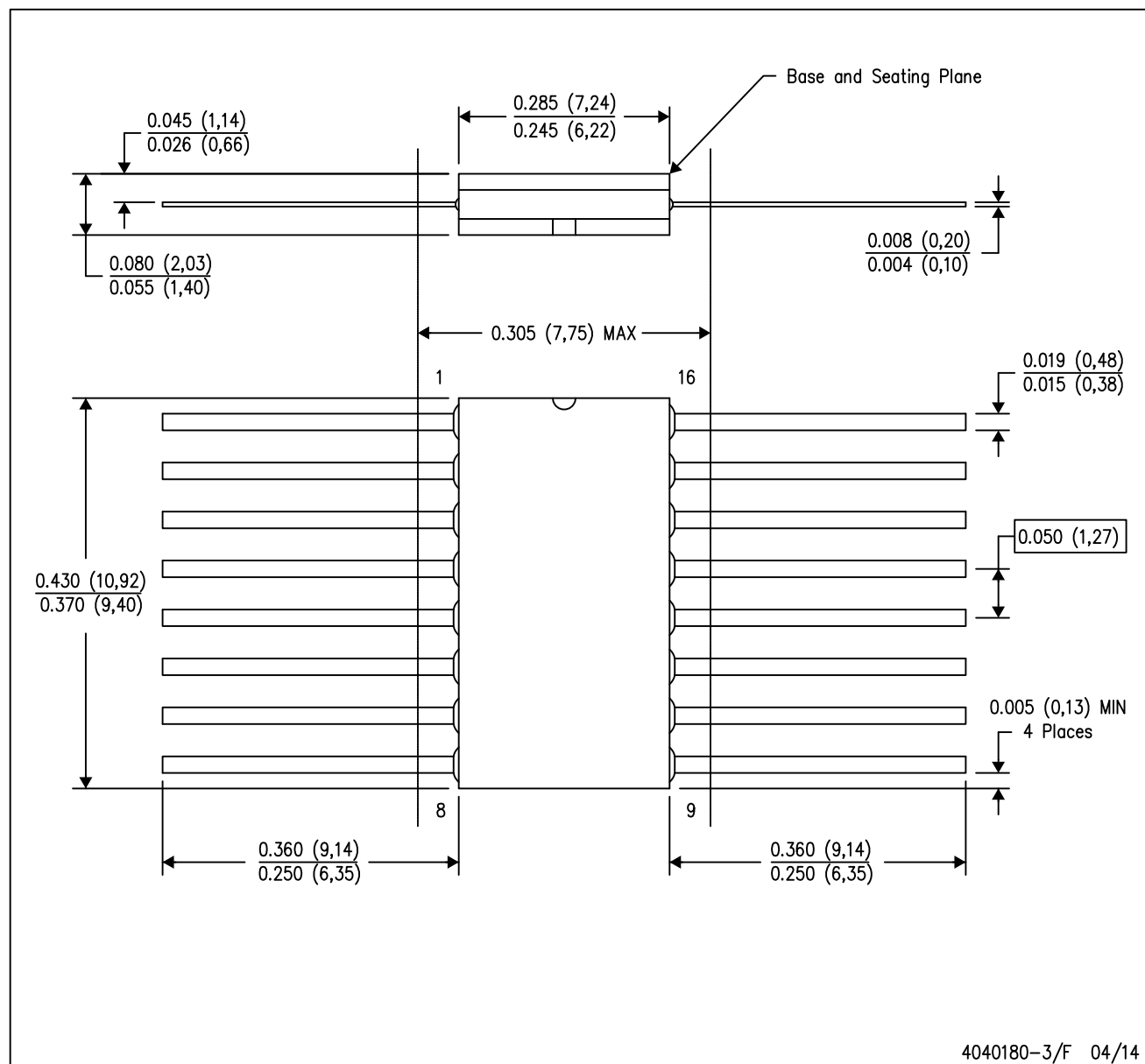


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS251DR  | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| SN74LS251NSR | SO           | NS              | 16   | 2000 | 367.0       | 367.0      | 38.0        |

## W (R-GDFP-F16)

## CERAMIC DUAL FLATPACK



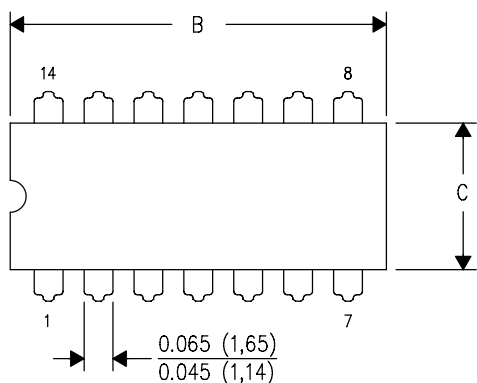
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP2-F16

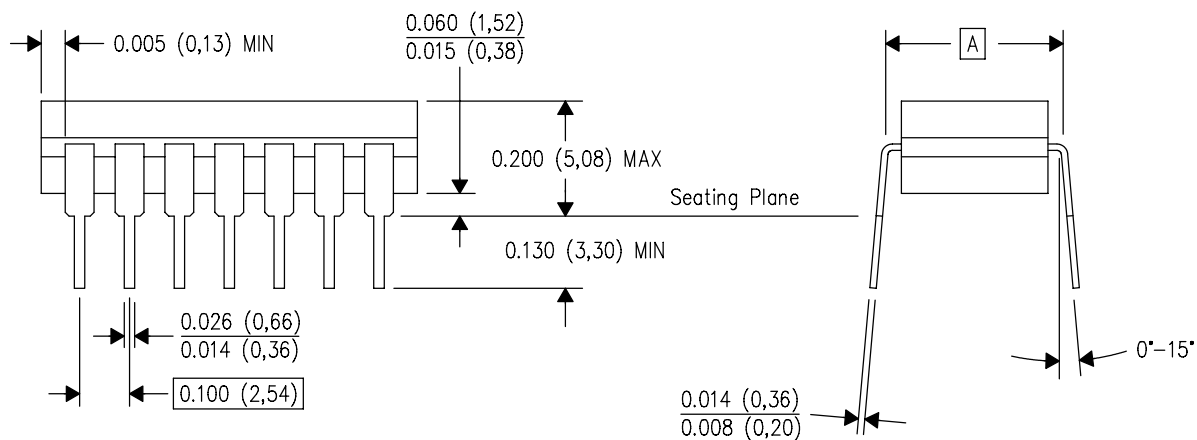
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



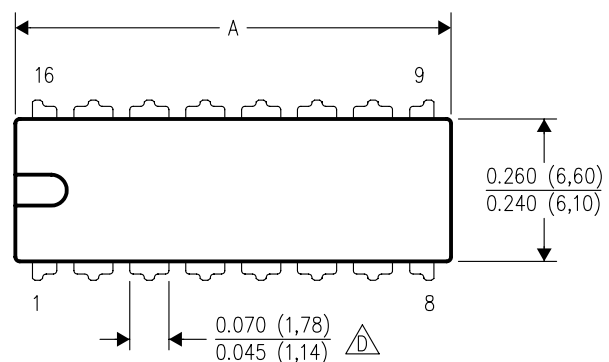
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

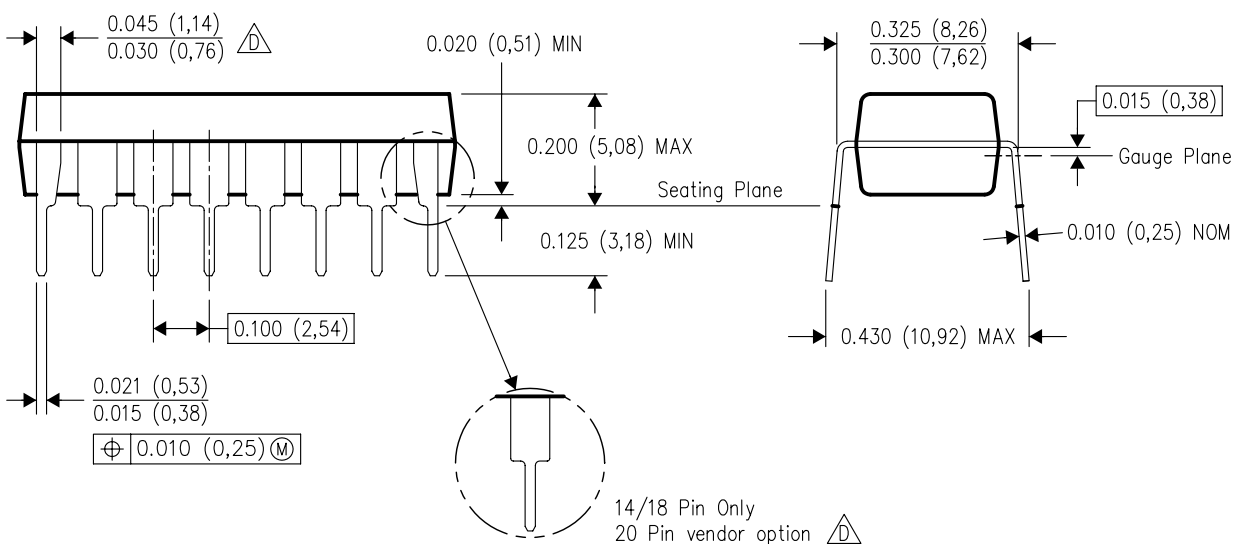
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

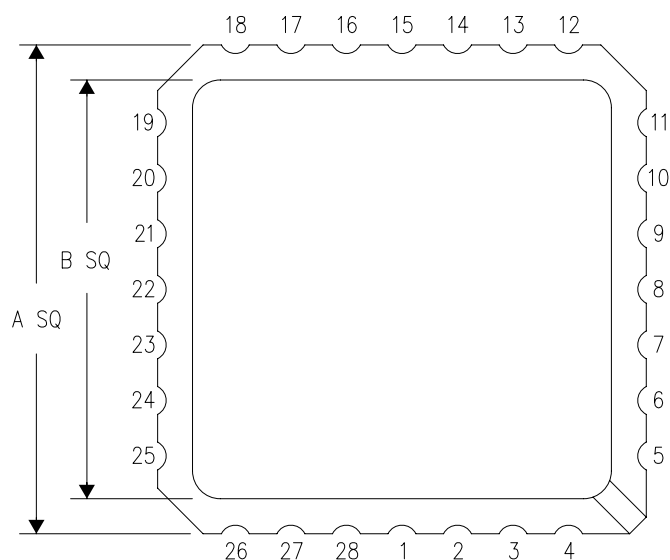
- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



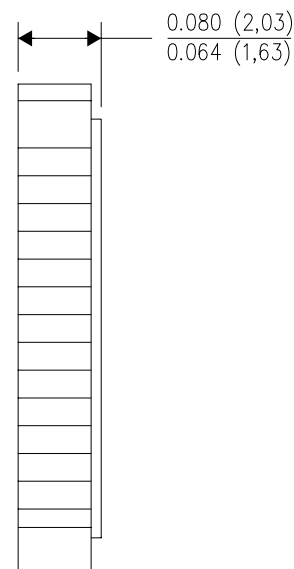
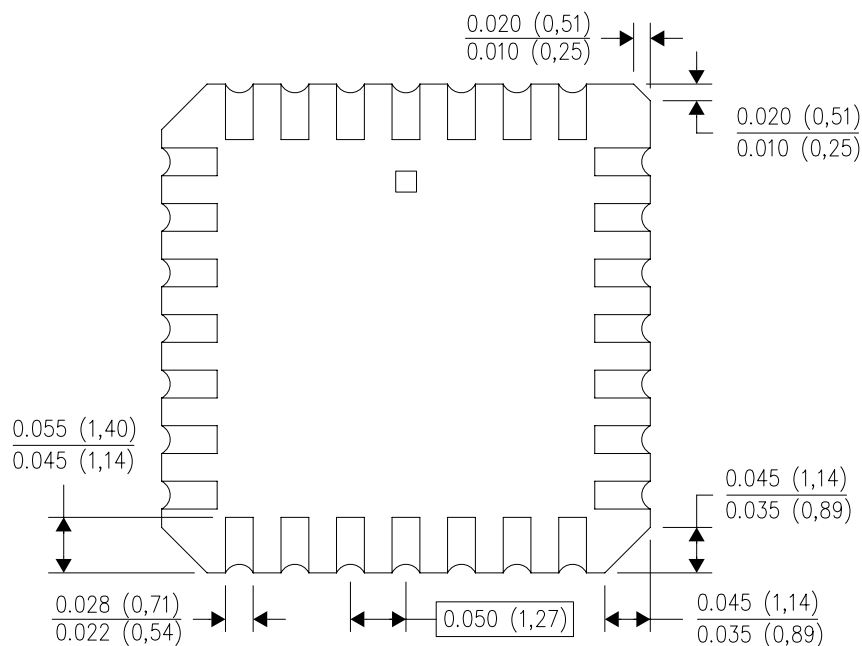
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |

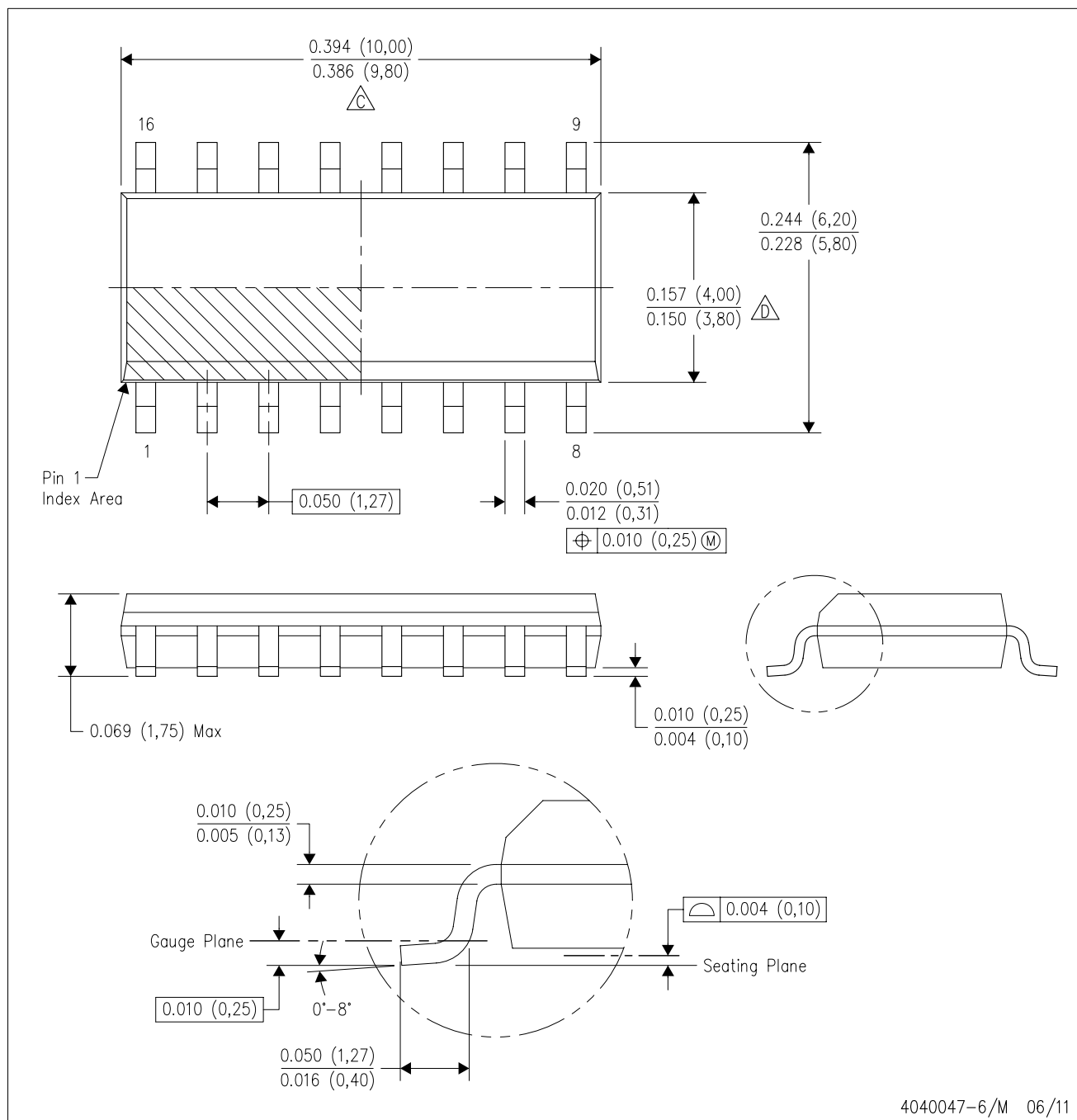


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

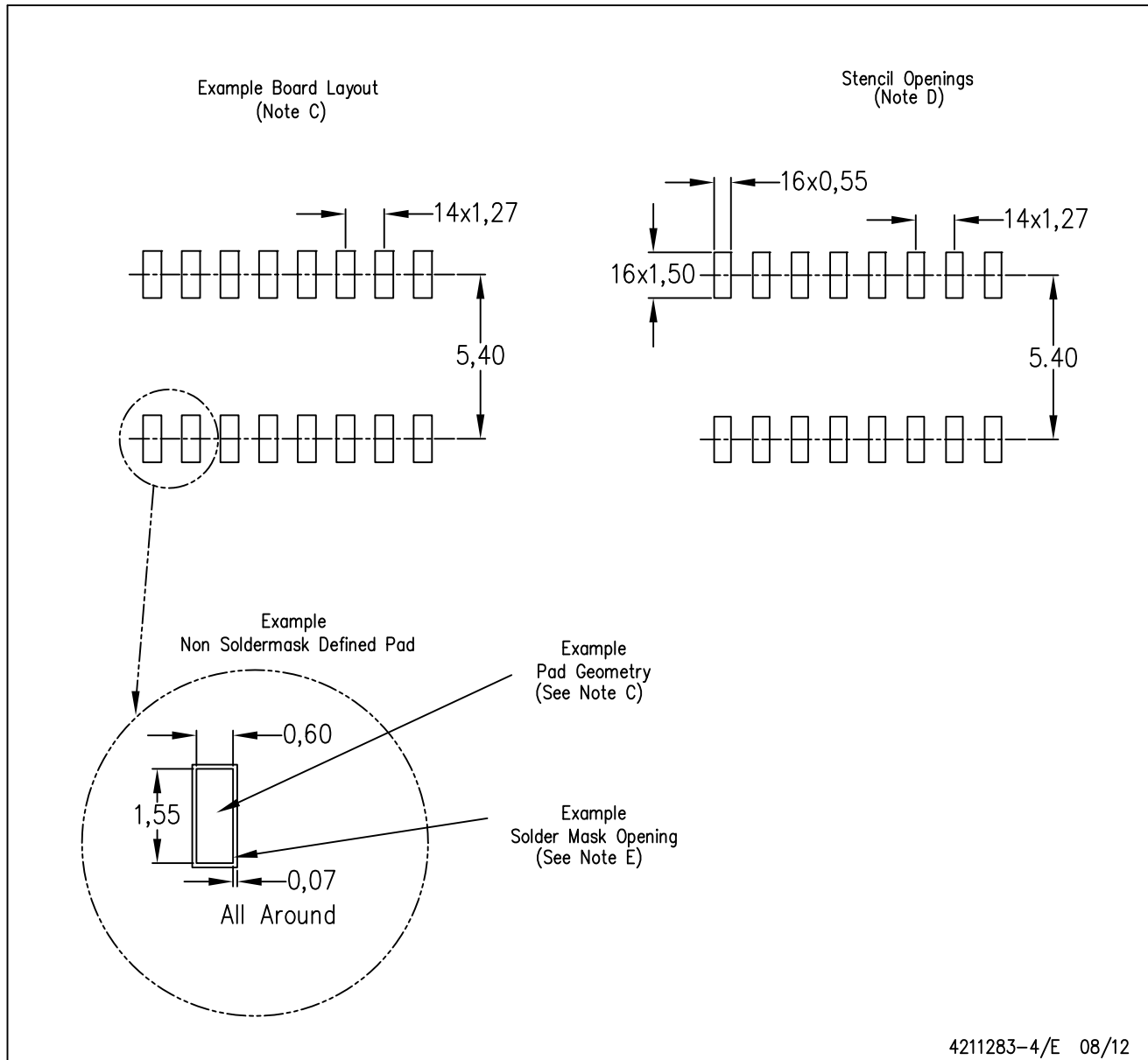


4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



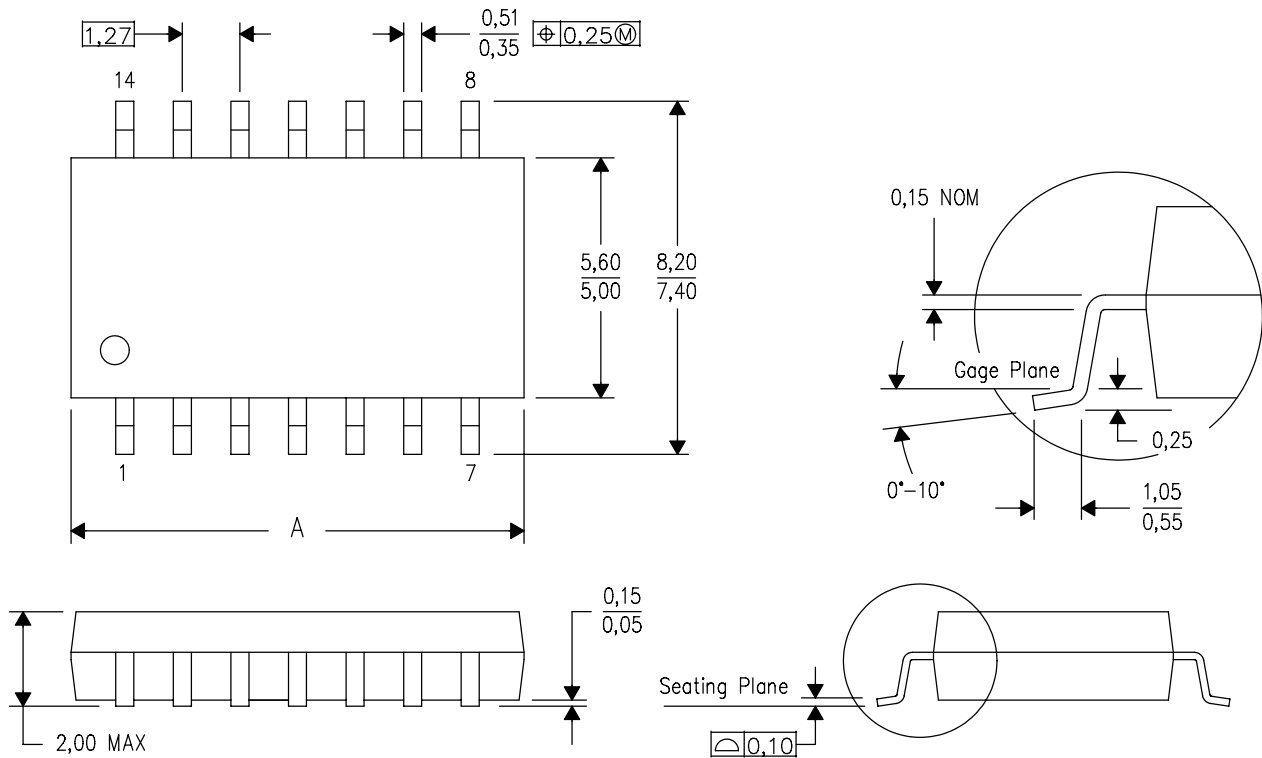
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14    | 16    | 20    | 24    |
|---------------|-------|-------|-------|-------|
| A MAX         | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN         | 9,90  | 9,90  | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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