NB6L611MNGEVB

NB6L611MNG Evaluation Board User's Manual

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Introduction

ON Semiconductor has developed the QFN16EVB evaluation board for its high-performance devices packaged in the 16-pin QFN. This evaluation board was designed to provide a flexible and convenient platform to quickly evaluate, characterize and verify the operation of various ON Semiconductor products. Many QFN16EVBs are dedicated with a device already installed, and can be ordered from www.onsemi.com at the specific device web page.

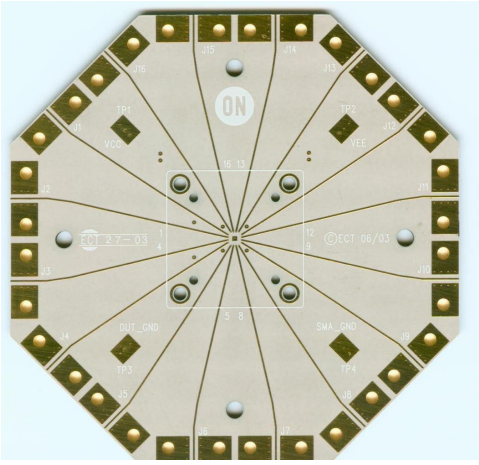
This evaluation board manual contains:

- Information on 16-lead QFN Evaluation Board
- Assembly Instructions
- Appropriate Lab Setup
- Bill of Materials

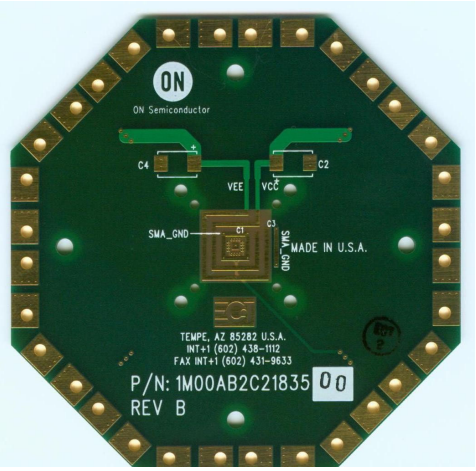
This user's manual provides detailed information on board contents, layout and its use. It should be used in conjunction with an appropriate ON Semiconductor device datasheet located at www.onsemi.com. The datasheet contains the technical device specifications.

Board Layout

The QFN16 Evaluation Board provides a high bandwidth, 50 Ω controlled impedance environment and is implemented in four layers. The first layer or primary trace layer is 0.008″ thick Rogers RO4003 material, and is designed to have equal electrical length on all signal traces from the device under test (DUT) pins to the SMA connectors. The second layer is the 1.0 oz copper ground plane and is primarily dedicated for the SMA connector ground plane. FR4 dielectric material is placed between the second and third layers and between third and fourth layers. The third layer is also 1.0 oz copper plane. A portion of this layer is designated for the device V_{CC} and DUTGND power planes. The fourth layer is the secondary trace layer.



Top View



Bottom View

Figure 1. Top and Bottom View of the 16 QFN Evaluation Board

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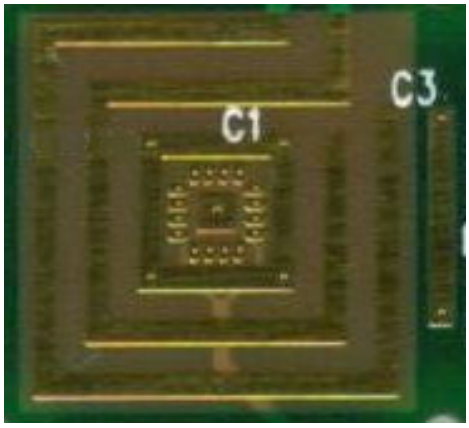


Figure 2. Enlarged Bottom View

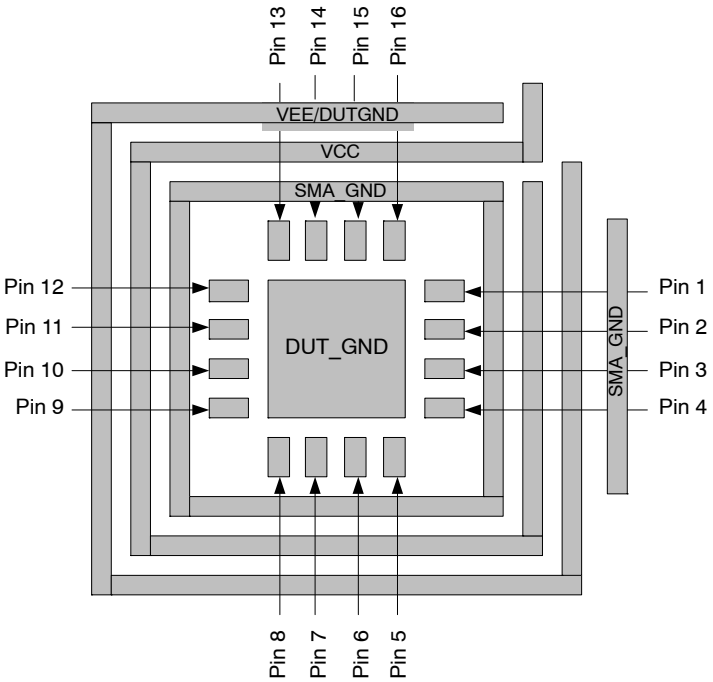


Figure 3. Enlarged Bottom View of the Evaluation Board

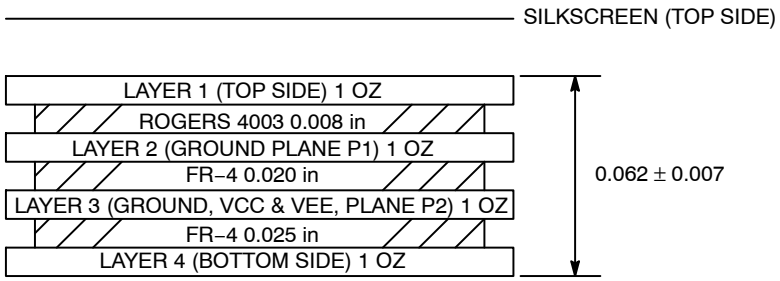
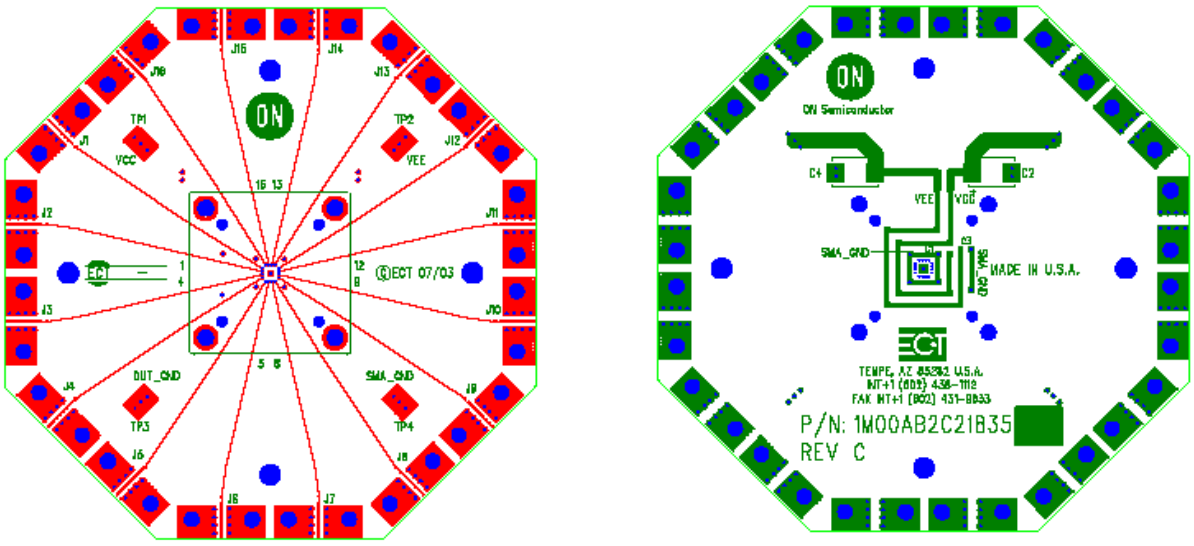


Figure 4. Evaluation Board Layout, 4 Layer



Top View **Bottom View**

Figure 5. Evaluation Board Layout

Evaluation Board Assembly Instructions

The QFN−16 evaluation board is designed for characterizing devices in a 50 Ω laboratory environment using high bandwidth equipment. Each signal trace on the board has a via at the DUT pin, which provides an option of placing a termination resistor on the board bottom, depending on the input/output configuration (see Table 1, Configuration for Device: NB6L611). Table 4 contains the Bill of Materials for this evaluation board.

The QFN16EVB was designed to accommodate a custom QFN−16 socket. Therefore, some external components are installed on the bottom side of the board.

Solder the Device on the Evaluation Board

The soldering of a device to the evaluation board can be accomplished by hand soldering or solder reflow techniques using solder paste. Make sure pin 1 of the device is located properly and all the pins are aligned to the footprint pads. Solder the QFN−16 device to the evaluation board. As mentioned earlier, many QFN16EVBs are dedicated with a device already installed, and can be ordered from onsemi.com at the specific device web page.

Connecting Power and Ground

On the top side of the evaluation board, solder the four surface mount test point clips (anvils) to the pads labeled V_{CC}, V_{EE}/DUTGND, SMAGND, and ExPad. ExPad is connected to the exposed flag of the QFN package. For proper operation, the exposed flag is typically recommended to be tied to V_{EE}/DUTGND, the negative supply of the device.

The positive power supply connector is labeled V_{CC}. Depending on the device, the negative power supply nomenclature is labeled either GND or V_{EE}. To help avoid confusion with the use of this board, the negative supply connector is labeled V_{EE}/DUTGND. SMAGND is the ground for the SMA connectors and is not to be confused with the device ground, V_{EE}/DUTGND. SMAGND and DUTGND can be connected in single-supply applications. The power pin layout and typical connection of the evaluation board is shown in Figure 6.

It is recommended to add bypass capacitors to reduce unwanted noise from the power supplies. Connect 0.1 μF capacitors from V_{CC} and V_{EE}/DUTGND to SMA_GND.

Output Loading/Termination

ECL/PECL/LVPECL Outputs

Most ECL outputs are open emitter and need to be DC loaded and AC terminated to V_{CC} − 2.0 V via a 50 Ω resistor. If no internal resistors are provided on the device, 0402 chip resistor pads are provided on the bottom side of the evaluation board to terminate the ECL driver. Solder the chip resistors to the bottom side of the board between the appropriate input device pads and the ground pads. If internal resistors are provided, the VT pins should be wired to SMAGND. (More information on termination is provided in AND8020).

For standard ECL lab setup and test, a split (dual) power supply is recommended enabling the 50 Ω internal impedance in the oscilloscope, or other measuring instrument, to be used as an ECL output load/termination. By offsetting V_{CC} = +2.0 V, SMAGND = V_{CC} − 2.0 V, (SMAGND is the system ground, 0V); V_{CC} is 2.0 V, and V_{EE}/DUTGND is −3.0 V, −1.3 V or −0.5 V; see Table 2, Power Supply Levels).

CML Outputs

Likewise, CML outputs need to be terminated to V_{CC} via a 50 Ω resistor. If no internal resistors are provided on the device, 0402 chip resistor pads are provided on the bottom side of the evaluation board to terminate the CML driver. If internal resistors are provided, the V_T pins should be wired to V_{CC}.

For CML lab setup and test, operation with negative supply voltages is recommended to enable the 50 Ω internal impedance in the oscilloscope, or other measuring instrument, to be used as a CML output termination; (V_{CC} = 0 V, SMAGND = 0 V, and V_{EE}/DUTGND = −5.0 V, −3.3 V, −2.5 V, or −1.8 V).

LVDS Outputs

LVDS outputs are typically terminated with 100 Ω across the Q/$\overline{Q}$ output pair. The 100 Ω can be added on the QFN16EVB, but it is not provided on the board, since there are several user dependent LVDS output measurement techniques.

For LVDS lab setup and test, a single supply is typically used, ie. V_{CC} = 3.3 V and DUTGND = 0 V.

Installing the SMA Connectors

Each configuration indicates the number of SMA connectors needed to populate an evaluation board for a given device. Each input and output requires one SMA connector. Install all the required SMA connectors onto the board and solder the center signal conductor pin to the board on J1 through J16. Please note that the alignment of the signal connector pin of the SMA connector to the metal trace on the board can influence lab results. The launch and reflection of the signals are largely influenced by imperfect alignment and soldering of the SMA connector.

Validating the Assembled Board

After assembling the evaluation board, it is recommended to perform continuity checks on all soldered areas before commencing with the evaluation process. Time Domain Reflectometry (TDR) is another highly recommended validation test.

NB6L611MNGEVB ASSEMBLY

Table 1. CONFIGURATION FOR DEVICE: NB6L611

	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
Device Pin #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SMA Connector	Yes	Yes	Yes	Yes	No	Yes	No	No	Yes	Yes	Yes	Yes	No	No	No	No
Wire	No	No	No	No	V_{CC}	No	V_{EE}	V_{CC}	No	No	No	No	V_{CC}	V_{EE}	No	V_{CC}

NOTE: DUTGND/V_{EE} = Exposed Pad and must be tied to DUTGND/V_{EE}.

CONFIGURATIONS

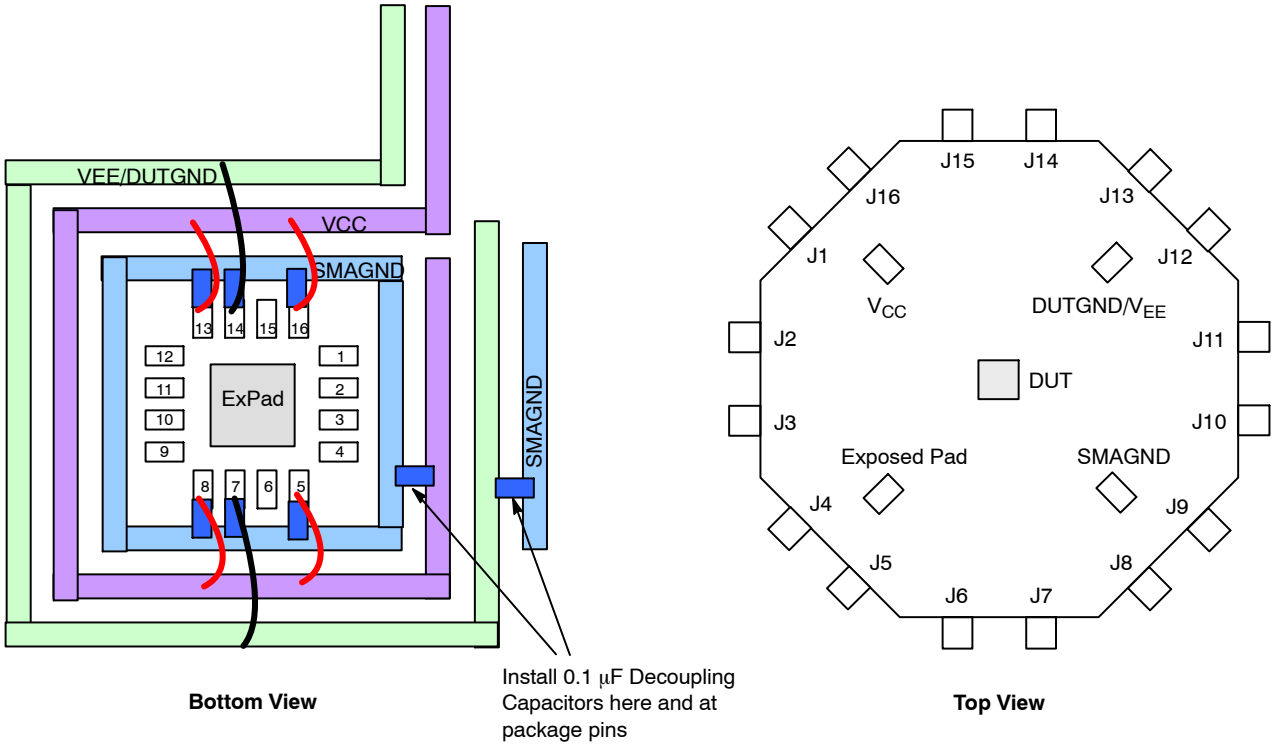
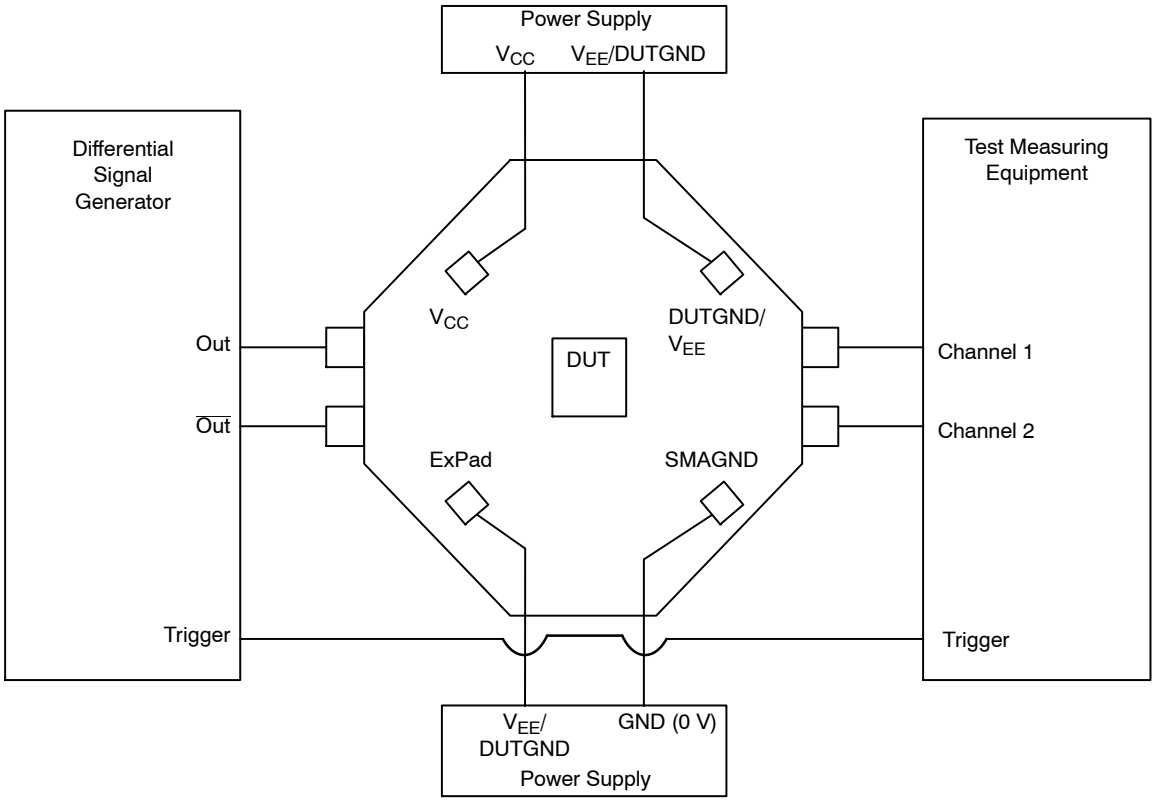


Figure 6. Power Supply Configuration for Device NB6L611

NB6L611MNGEVB TEST



1. Connect appropriate power supplies to V_{CC}, V_{EE}/DUTGND, SMAGND, and ExPad (see Table 2).
2. Connect a signal generator to the input SMA connectors. Setup input signal according to the device data sheet.
3. Connect a test measurement device to the device's output SMA connectors.

NOTE: The test measurement device must contain 50 Ω termination.

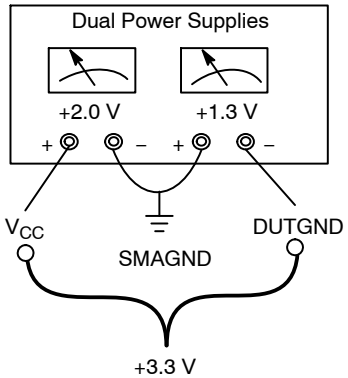
Figure 7. Basic Lab Setup (Typical)

Table 2. POWER SUPPLY LEVELS

Outputs	Power Supply	V_{CC}	V_{EE}/DUTGND	SMAGND	ExPad (typ)
ECL/LVPECL	2.5 V	+2.0 V	−0.5 V	0 V	V_{EE}/DUTGND
ECL/LVPECL	3.3 V	+2.0 V	−1.3 V	0 V	V_{EE}/DUTGND

Table 3. NB6xxx, LVPECL OUTPUTS "SPLIT" POWER SUPPLY CONFIGURATION

Device Pin Power Supply Convertor	"Spilt" Power Supply
V_{CC}	V_{CC} = +2.0 V
SMAGND	V_{TT} = 0 V
DUTGND	DUTGND = −0.5 V or −1.3 V



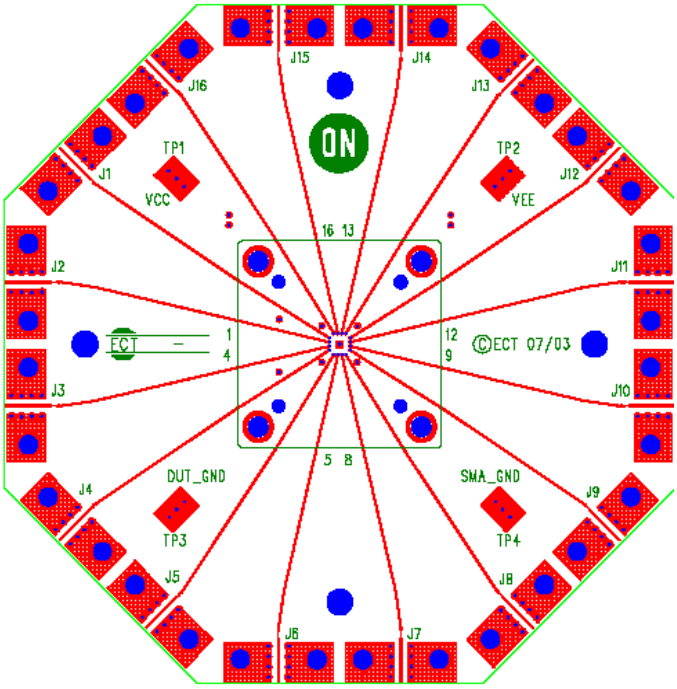
Offset / "Split" Power Supply Configuration

Figure 8. "Split" or Dual Power Supply Connections

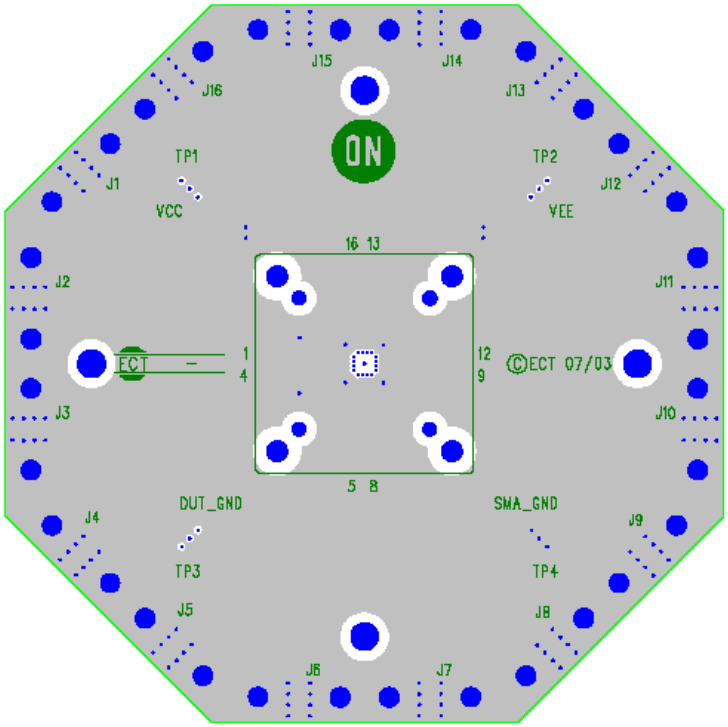
Table 4. BILL OF MATERIALS

Components	Manufacturer	Description	Part Number	Qty	Web Site
SMA Connector	Rosenberger	SMA Connector, Side Launch, Gold Plated	32K243−40ME3	9	http://www.rosenberger.de http://www.rosenbergerna.com
Surface Mount Test Points	Keystone*	SMT Miniature Test Point	5015	4	http://www.keyelco.com
Chip Capacitor	AVC Corporation*	0603 0.01 μF ±10%	06035C103KAT2A	na	http://www.avxcorp.com
		0603 0.1 μF ±10%	0603C104KAT2A	8	
Chip Resistor	Panasonic*	0402 50 Ω ±1% Precision Thick Film Chip Resistor	ERJ−2RKF49R9X	na	http://www.panasonic.com
Evaluation Board	ON Semiconductor	QFN 16 Evaluation Board	QFN16EVB	1	http://www.onsemi.com
Device Samples	ON Semiconductor	QFN 16 Package Device	NB6L611MNG	1	http://www.onsemi.com

*Components are available through most distributors, i.e. www.newark.com, www.digikey.com

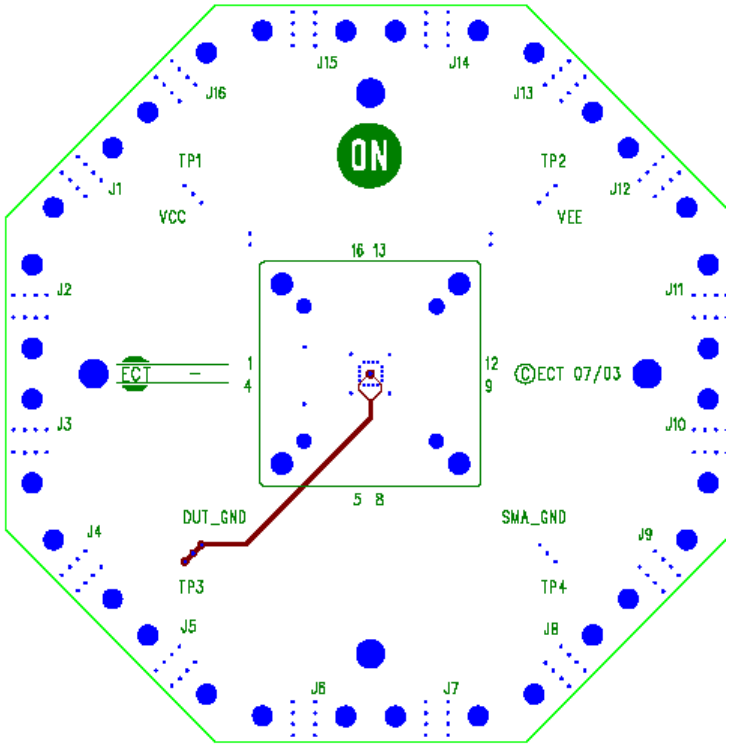


Top Layer

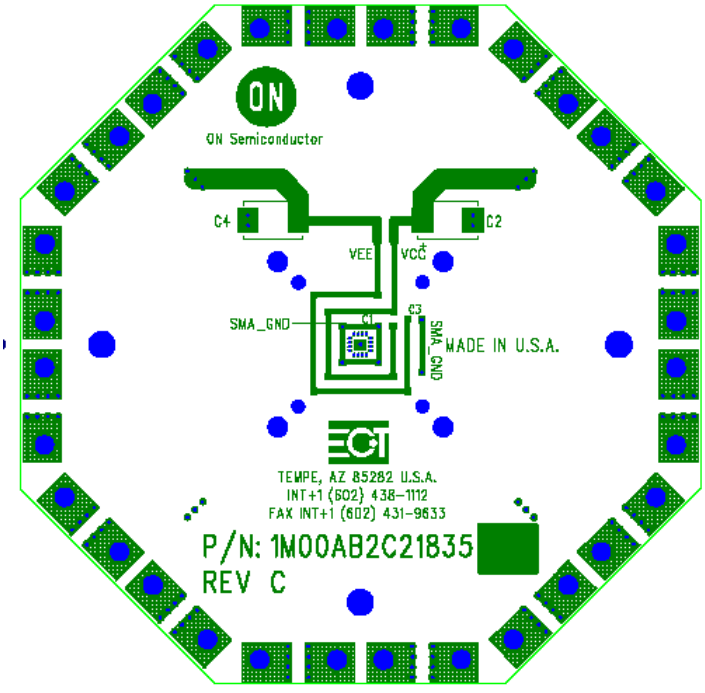


Second Layer (SMA_GND Plane)

Figure 9. Gerber Files



Third Layer (DUT_GND Trace)



Bottom Layer

Figure 10. Gerber Files

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