11-Bit, 125-MSPS Analog-To-Digital Converter

FEATURES

- 11-bit Resolution
- 125-MSPS Sample Rate
- High SNR: 66.3 dBFS at 100 MHz f_{IN}
- High SFDR: 81 dBc at 100 MHz f_{IN}
- 2.3-V_{PP} Differential Input Voltage
- Internal Voltage Reference
- 3.3-V Single-Supply Voltage
- Analog Power Dissipation: 578 mW
- Serial Programming Interface
- TQFP-64 PowerPAD™ Package
- Pin-Compatible With:
  - ADS5500 (14-Bit, 125 MSPS)
  - ADS5541 (14-Bit, 105 MSPS)
  - ADS5542 (14-Bit, 80 MSPS)
  - ADS5520 (12-Bit, 125 MSPS)
  - ADS5521 (12-Bit, 105 MSPS)
  - ADS5522 (12-Bit, 80 MSPS)
- Recommended Operational Amplifiers: THS3201, THS3202, THS4503, THS4509, THS9001, OPA695, OPA847

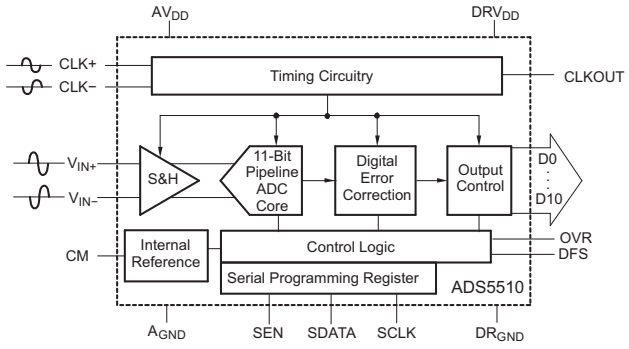
APPLICATIONS

- Wireless Communication
  - Communication Receivers
  - Base Station Infrastructure
- Test and Measurement Instrumentation
- Single and Multichannel Digital Receivers
- Communication Instrumentation
  - Radar
  - Infrared
- Video and Imaging
- Medical Equipment

DESCRIPTION

The ADS5510 is a high-performance, 11 bit, 125 MSPS analog-to-digital converter (ADC). To provide a complete converter solution, it includes a high-bandwidth linear sample-and-hold stage (S&H) and internal reference. Designed for applications demanding the highest speed and highest dynamic performance in little space, the ADS5510 has excellent power consumption of 578 mW at 3.3-V single-supply voltage. This allows an even higher system integration density. The provided internal reference simplifies system design requirements. Parallel CMOS-compatible output ensures seamless interfacing with common logic.

The ADS5510 is available in 64-pin TQFP PowerPAD package over the industrial temperature range.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5510	HTQFP-64(2) PowerPAD	PAP	–40°C to 85°C	ADS5510I	ADS5510IPAP	Tray, 160
					ADS5510IPAPR	Tape and Reel, 1000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Thermal pad size: 3,5 mm x 3,5 mm (min), 4 mm x 4 mm (max). θ_{JA} = 21.47°C/W and θ_{JC} = 2.99°C/W, when used with 2 oz. copper trace and pad soldered directly to a JEDEC standard, four-layer, 3 in x 3 in PCB.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

				UNIT
V_{SS}	Supply Voltage	AV_{DD} to A_{GND}, DRV_{DD} to DR_{GND}	–0.3 to 3.7	V
		A_{GND} to DR_{GND}	±0.1	V
	Analog input to A_{GND}(2)(3)		–0.3 to minimum (AVDD + 0.3, 3.6)	V
	Logic input to DR_{GND}		–0.3 to DRV_{DD}	V
	Digital data output to DR_{GND}		–0.3 to DRV_{DD}	V
	Operating temperature range		–40 to 85	°C
T_J	Junction temperature		105	°C
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) If the input signal can exceed 3.6 V, then a resistor greater than or equal to 25 Ω should be added in series with each of the analog input pins to support input voltages up to 3.8 V. For input voltages above 3.8 V, the device can only handle transients and the duty cycle of the overshoot should be limited to less than 5% for inputs up to 3.9 V.
(3) The overshoot duty cycle can be defined as the ratio of the total time of overshoot to the total intended device lifetime, expressed as a percentage. The total time of overshoot is the integrated time of all overshoot occurrences over the lifetime of the device.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			MIN	TYP	MAX	UNIT
Supplies						
AV_{DD}	Analog supply voltage		3	3.3	3.6	V
DRV_{DD}	Output driver supply voltage		3	3.3	3.6	V
Analog input						
	Differential input range			2.3		V_{PP}
V_{CM}	Input common-mode voltage(1)		1.45	1.55	1.65	V
Digital Output						
	Maximum output load			10		pF
	Clock Input					
	ADCLK input sample rate (sine wave) $1/t_C$	DLL ON	60		125	MSPS
		DLL OFF	2		80	
	Clock amplitude, sine wave, differential		1	3		V_{PP}
	Clock duty cycle			50%		
T_A	Open free-air temperature range		–40		85	°C

(1) Input common-mode should be connected to CM.

ELECTRICAL CHARACTERISTICS

Typical values given at T_A = 25°C, min and max specified over the full recommended operating temperature range, AV_{DD} = DRV_{DD} = 3.3 V, sampling rate = 125 MSPS, 50% clock duty cycle, DLL On, 3-V_{PP} differential clock, and –1 dBFS differential input, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				11		bits
Analog Inputs						
	Differential input range			2.3		V_{PP}
	Differential input impedance	See Figure 24		6.6		kΩ
	Differential input capacitance	See Figure 24		4		pF
	Analog input common-mode current (per input)			300		µA
	Analog input bandwidth	Source impedance = 50 Ω		750		MHz
	Voltage overload recovery time			4		Clock cycles
Internal Reference Voltages						
$V_{(REFM)}$	Reference bottom voltage			0.95		V
$V_{(REFP)}$	Reference top voltage			2.1		V
	Reference error		–4%	±0.9%	4%	
V_{CM}	Common-mode voltage output			1.55 ±0.05		V
Dynamic DC Characteristics and Accuracy						
	No missing codes			Tested		
DNL	Differential nonlinearity error	f_{IN} = 10 MHz	-0.5	±0.25	0.5	LSB
INL	Integral nonlinearity error	f_{IN} = 10 MHz	-1.5	±0.8	1.5	LSB
	Offset error		-11	+2.5	+11	mV
	Offset temperature coefficient			0.01		mV/°C
PSRR	DC power-supply rejection ratio	Δoffset error/ΔAV_{DD} from AV_{DD} = 3 V to AV_{DD} = 3.6 V		0.25		mV/V
	Gain error (1)		-2	±0.45	+2	%FS
	Gain temperature coefficient			0.01		Δ%/°C
Dynamic AC Characteristics						
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz	62.5	66.7		dBFS
		f_{IN} = 70 MHz		66.5		
		f_{IN} = 100 MHz		66.3		
		f_{IN} = 130 MHz		66		
		f_{IN} = 170 MHz		65.5		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz	73	84		dBc
		f_{IN} = 70 MHz		81		
		f_{IN} = 100 MHz		82		
		f_{IN} = 130 MHz		78		
		f_{IN} = 170 MHz		72		
HD2	Second-harmonic	f_{IN} = 10 MHz	73	91		dBc
		f_{IN} = 70 MHz		87		
		f_{IN} = 100 MHz		84		
		f_{IN} = 130 MHz		79		
		f_{IN} = 170 MHz		74		

(1) Gain error is specified by design and characterization; it is not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

Typical values given at T_A = 25°C, min and max specified over the full recommended operating temperature range, AV_{DD} = DRV_{DD} = 3.3 V, sampling rate = 125 MSPS, 50% clock duty cycle, DLL On, 3-V_{PP} differential clock, and –1 dBFS differential input, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
HD3	Third-harmonic	f_{IN} = 10 MHz	73	84		dBc
		f_{IN} = 70 MHz		81		
		f_{IN} = 100 MHz		82		
		f_{IN} = 130 MHz		78		
		f_{IN} = 170 MHz		72		
SINAD	Signal-to-noise + distortion	f_{IN} = 10 MHz	62	66.5		dBFS
		f_{IN} = 70 MHz		66.3		
		f_{IN} = 100 MHz		66		
		f_{IN} = 130 MHz		65.6		
		f_{IN} = 170 MHz		65		
ENOB	Effective number of bits	f_{IN} = 10 MHz	10.0	10.8		Bits
IMD	Two-tone intermodulation distortion	f = 50.1 MHz, 46.1 MHz (-7 dBFS each tone)		85		dBFS
PSRR	AC power supply rejection ratio	Supply noise frequency ≤ 100 MHz		35		dB
Power Supply						
I_{CC}	Total supply current	f_{IN} = 10 MHz		236	260	mA
$I_{(AVDD)}$	Analog supply current	f_{IN} = 10 MHz		175	190	mA
$I_{(DRVDD)}$	Output buffer supply current	f_{IN} = 10 MHz		61	70	mA
	Power dissipation	Analog only		578	627	mW
		Output buffer power with 10-pF load on digital output to ground		202	231	
	Standby power	With Clocks running		180	250	mW

DIGITAL CHARACTERISTICS

Valid over full recommended operating temperature range, AV_{DD} = DRV_{DD} = 3.3 V, unless otherwise noted

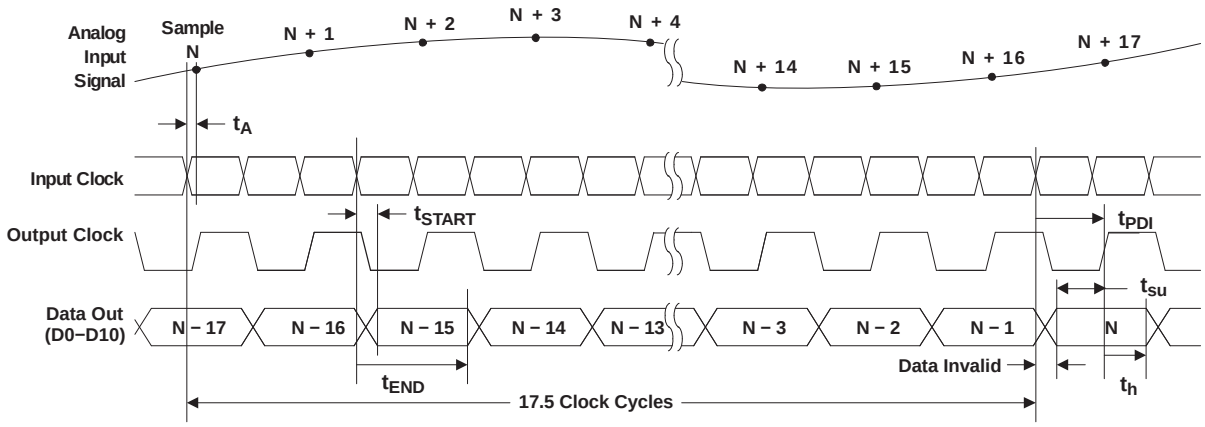
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs						
V_{IH}	High-level input voltage		2.4			V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level input current				10	µA
I_{IL}	Low-level input current				-10	µA
	Input current for RESET			–20		µA
	Input capacitance			4		pF
Digital Outputs						
V_{OL}	Low-level output voltage	C_{LOAD} = 10 pF		0.3	0.4	V
V_{OH}	High-level output voltage	C_{LOAD} = 10 pF	2.4	3		V
	Output capacitance			3		pF

TIMING CHARACTERISTICS(1)(2)

Typical values given at T_A = 25°C, min and max specified over the full recommended operating temperature range, AV_{DD} = DRV_{DD} = 3.3 V, sampling rate = 125 MSPS, 50% clock duty cycle, 3-V_{PP} differential clock, and C_{LOAD} = 10 pF, unless otherwise noted

PARAMETER		DESCRIPTION	MIN	TYP	MAX	UNIT
Switching Specification						
t_A	Aperture delay	Input CLK falling edge to data sampling point		1		ns
	Aperture jitter (uncertainty)	Uncertainty in sampling instant		300		fs
t_{SETUP}	Data setup time	Data valid(3) to 50% of CLKOUT rising edge	2.3	2.7		ns
t_{HOLD}	Data hold time	50% of CLKOUT rising edge to data becoming invalid(3)	1.7	2		ns
t_{START}	Input clock to output data valid start (4)(5)	Input clock rising edge to data valid start delay		2	2.6	ns
t_{END}	Input clock to output data valid end (4)(5)	Input clock rising edge to data valid end delay	5.8	6.9		ns
t_{JIT}	Output clock jitter	Uncertainty in CLKOUT rising edge, peak-to-peak		150	210	ps_{PP}
t_r	Output clock rise time	Rise time of CLKOUT from 20% to 80% of DRV_{DD}		1.7	1.9	ns
t_f	Output clock fall time	Fall time of CLKOUT from 80% to 20% of DRV_{DD}		1.5	1.7	ns
t_{PDI}	Input clock to output clock delay	Input clock rising edge, zero crossing, to output clock rising edge 50%	4.2	4.8	5.5	ns
t_r	Data rise time	Data rise time measured from 20% to 80% of DRV_{DD}		3.6	4.6	ns
t_f	Data fall time	Data fall time measured from 80% to 20% of DRV_{DD}		2.8	3.7	ns
	Output enable(OE) to data output delay	Time required for outputs to have stable timings with regard to input clock(6) after OE is activated			1000	Clock cycles
	Wakeup time	Time to valid data after coming out of software power down			1000	Clock cycles
		Time to valid data after stopping and restarting the clock			1000	
	Latency	Time for a sample to propagate to the ADC outputs		17.5		Clock cycles

(1) Timing parameters are ensured by design and characterization, and not tested in production.
(2) See Table 5 through Table 8 in the *Application Information* section for timing information at additional sampling frequencies.
(3) Data valid refers to 2 V for LOGIC HIGH and 0.8 V for LOGIC LOW.
(4) See the *Output Information* section for details on using the input clock for data capture.
(5) These specifications apply when the CLKOUT polarity is set to rising edge (according to Table 2). Add 1/2 clock period for the valid number for a falling edge CLKOUT polarity.
(6) Data outputs are available within a clock from assertion of OE; however, it takes 1000 clock cycles to ensure stable timing with respect to input clock.



A. It is recommended that the loading at CLKOUT and all data lines are accurately matched to ensure that the above timing matches closely with the specified values.

Figure 1. Timing Diagram

RESET TIMING CHARACTERISTICS

Typical values given at T_A = 25°C, min and max specified over the full recommended operating temperature range, AV_{DD} = DRV_{DD} = 3.3 V, and 3-V_{PP} differential clock, unless otherwise noted

PARAMETER		DESCRIPTION	MIN	TYP	MAX	UNIT
Switching Specification						
t_1	Power-on delay	Delay from power-on of AVDD and DRVDD to RESET pulse active	10			ms
t_2	Reset pulse width	Pulse width of active RESET signal	2			µs
t_3	Register write delay	Delay from RESET disable to SEN active	2			µs
	Power-up time	Delay from power-up of AV_{DD} and DRV_{DD} to output stable		40		ms

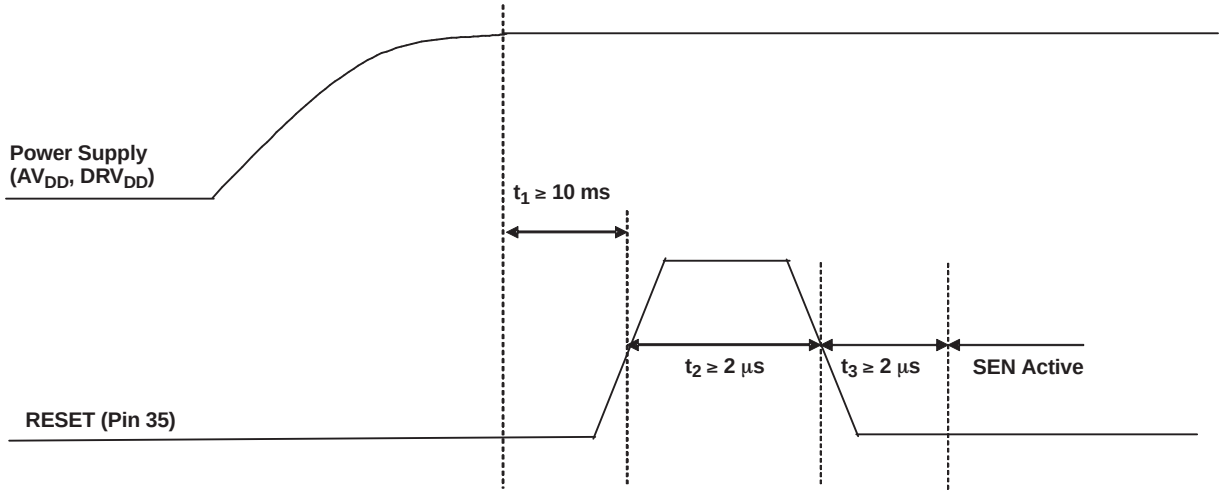


Figure 2. Reset Timing Diagram

SERIAL PROGRAMMING INTERFACE CHARACTERISTICS

The ADS5510 has a three-wire serial interface. The ADS5510 latches serial data SDATA on the falling edge of serial clock SCLK when SEN is active.

- Serial shift of bits is enabled when SEN is low. SCLK shifts serial data at the falling edge.
- Minimum width of data stream for a valid loading is 16 clocks.
- Data is loaded at every 16th SCLK falling edge while SEN is low.
- In case the word length exceeds a multiple of 16 bits, the excess bits are ignored.
- Data can be loaded in multiples of 16-bit words within a single active SEN pulse.
- The first 4-bit nibble is the address of the register while the last 12 bits are the register contents.

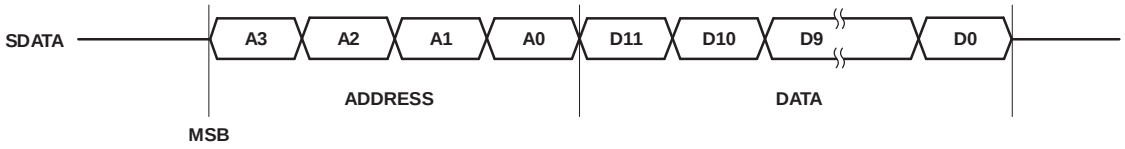


Figure 3. DATA Communication is 2-Byte, MSB First

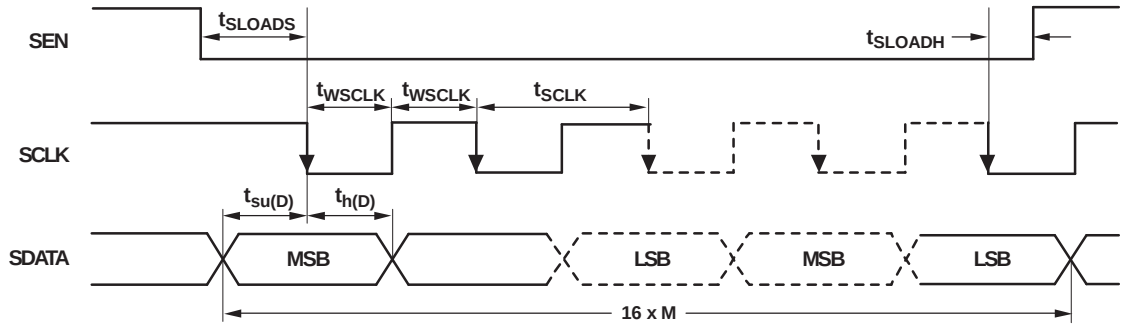


Figure 4. Serial Programming Interface Timing Diagram

Table 1. Serial Programming Interface Timing Characteristics

SYMBOL	PARAMETER	MIN(1)	TYP(1)	MAX(1)	UNIT
t_{SCLK}	SCLK period	50			ns
t_{WSCLK}	SCLK duty cycle	25%	50%	75%	
t_{SLOADS}	SEN to SCLK setup time	8			ns
t_{SLOADH}	SCLK to SEN hold time	6			ns
t_{DS}	Data setup time	8			ns
t_{DH}	Data hold time	6			ns

(1) Typ, min, and max values are characterized, but not production tested.

Table 2. Serial Register Table(1)

A3	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
														DLL CTRL		Clock DLL
1	1	0	1	0	0	0	0	0	0	0	0	0	0	**0**	0	Internal DLL is on; recommended for 60 MSPS to 125 MSPS clock speeds.
1	1	0	1	0	0	0	0	0	0	0	0	0	0	**1**	0	Internal DLL is off; recommended for 2 MSPS to 80 MSPS clock speeds.
					TP<1>	TP<0>										Test Mode
1	1	1	0	0	**0**	**0**	0	0	0	0	0	0	0	X	0	Normal mode of operation
1	1	1	0	0	**0**	**1**	0	0	0	0	0	0	0	X	0	All outputs forced to 0
1	1	1	0	0	**1**	**0**	0	0	0	0	0	0	0	X	0	All outputs forced to 1
1	1	1	0	0	**1**	**1**	0	0	0	0	0	0	0	X	0	Each output bit toggles between 0 and 1. (2)(3)
				PDN												Power Down
1	1	1	1	**0**	0	0	0	0	0	0	0	0	0	X	0	Normal mode of operation
1	1	1	1	**1**	0	0	0	0	0	0	0	0	0	X	0	Device is put in power-down (low-current) mode.

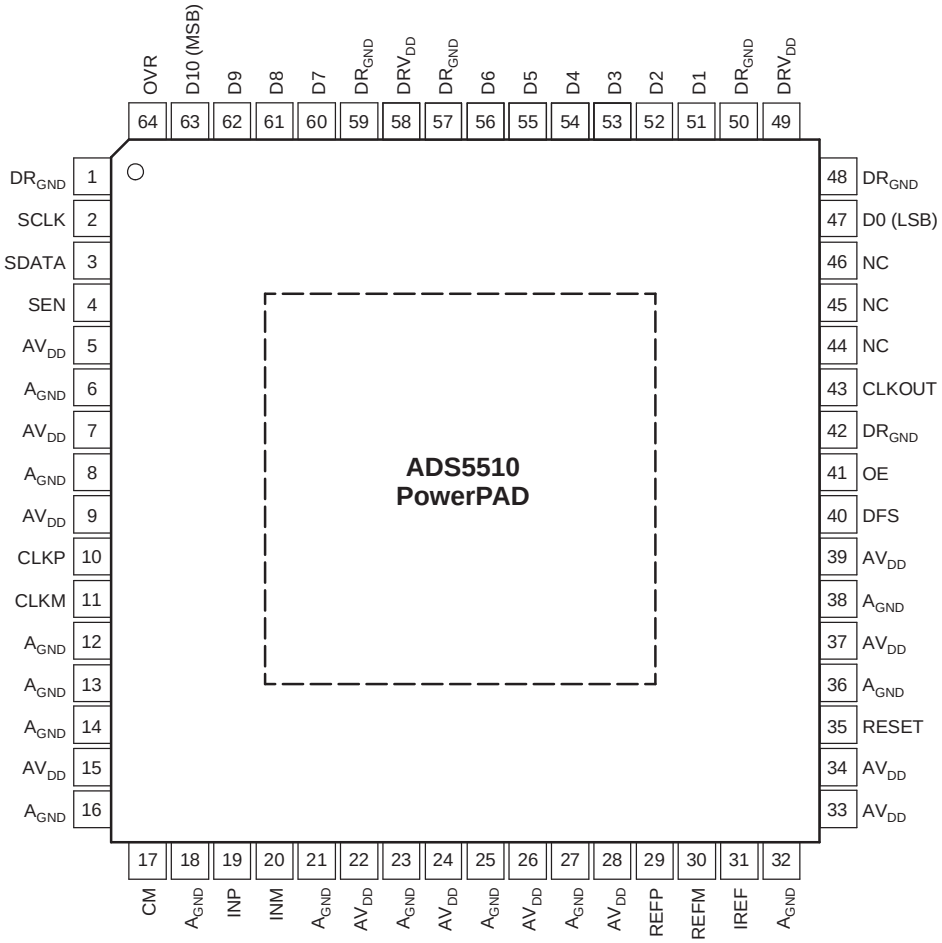
(1) The register contents default to the appropriate setting for normal operation up on RESET.
(2) The patterns given are applicable to the straight offset binary output format. If two's complement output format is selected, the test mode outputs will be the binary two's complement equivalent of these patterns as described in the *Output Information* section.
(3) While each bit toggles between 1 and 0 in this mode, there is no assured phase relationship between the data bits D0 through D10. For example, when D0 is a 1, D1 in not assured to be a 0, and vice versa.

Table 3. Data Format Select (DFS) Table

DFS-PIN VOLTAGE (V_{DFS})	DATA FORMAT	CLOCK OUTPUT POLARITY
$V_{DFS} < \frac{2}{12} \times AV_{DD}$	Straight Binary	Data valid on rising edge
$\frac{4}{12} \times AV_{DD} < V_{DFS} < \frac{5}{12} \times AV_{DD}$	Two's Complement	Data valid on rising edge
$\frac{7}{12} \times AV_{DD} < V_{DFS} < \frac{8}{12} \times AV_{DD}$	Straight Binary	Data valid on falling edge
$V_{DFS} > \frac{10}{12} \times AV_{DD}$	Two's Complement	Data valid on falling edge

PIN CONFIGURATION

PAP PACKAGE
HTQFP-64
(TOP VIEW)



PIN CONFIGURATION (continued)

PIN ASSIGNMENTS(1)

TERMINAL		NO. OF PINS	I/O	DESCRIPTION
NAME	NO.			
AV_{DD}	5, 7, 9, 15, 22, 24, 26, 28, 33, 34, 37, 39	12	I	Analog power supply
A_{GND}	6, 8, 12, 13, 14, 16, 18, 21, 23, 25, 27, 32, 36, 38	14	I	Analog ground
DRV_{DD}	49, 58	2	I	Output driver power supply
DR_{GND}	1, 42, 48, 50, 57, 59	6	I	Output driver ground
NC	44, 45, 46	2	—	Not connected
INP	19	1	I	Differential analog input (positive)
INM	20	1	I	Differential analog input (negative)
REFP	29	1	O	Reference voltage (positive); 0.1-µF capacitor in series with a 1-Ω resistor to GND
REFM	30	1	O	Reference voltage (negative); 0.1-µF capacitor in series with a 1-Ω resistor to GND
IREF	31	1	I	Current set; 56-kΩ resistor to GND; do not connect capacitors
CM	17	1	O	Common-mode output voltage
RESET	35	1	I	Reset (active high), 200-kΩ resistor to AV_{DD}(2)
OE	41	1	I	Output enable (active high)
DFS	40	1	I	Data format and clock out polarity select(3)(4)
CLKP	10	1	I	Data converter differential input clock (positive)
CLKM	11	1	I	Data converter differential input clock (negative)
SEN	4	1	I	Serial interface chip select(4)
SDATA	3	1	I	Serial interface data(4)
SCLK	2	1	I	Serial interface clock(4)
D0 (LSB) to D10 (MSB)	47, 51-56, 60-63	11	O	11 bit parallel data output
OVR	64	1	O	Over-range indicator bit
CLKOUT	43	1	O	CMOS clock out in sync with data

(1) PowerPAD is connected to analog ground.
(2) If unused, the RESET pin should be tied to AGND. See the serial programming interface section for details.
(3) Table 3 defines the voltage levels for each mode selectable via the DFS pin.
(4) Pins OE, DFS, SEN, SDATA, and SCLK have internal clamping diodes to the DRVDD supply. Any external circuit driving these pins must also run off the same supply voltage as DRVDD.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay

The delay in time between the falling edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine wave clock results in a 50% duty cycle.

Maximum Conversion Rate

The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate

The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL)

The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error

The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error does not account for variations in the internal reference voltages (see the *Electrical Specifications* section for limits on the variation of V_{REFP} and V_{REFM}).

Offset Error

The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift

The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference ($T_{MAX} - T_{MIN}$).

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first eight harmonics.

$$SNR = 10Log_{10}\frac{P_S}{P_N}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference or dBFS (dB to Full-Scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log_{10}\frac{P_S}{P_N + P_D}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB)

The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first eight harmonics (P_D).

$$THD = 10Log_{10}\frac{P_S}{P_D}$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion (IMD3)

IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to Full-Scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

DC Power Supply Rejection Ration (DC PSRR)

The DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

Reference Error

The reference error is the variation of the actual reference voltage (VREFP - VREFM) from its ideal value. The reference error is typically given as a percentage.

Voltage Overload Recovery Time

The voltage overload recovery time is defined as the time required for the ADC to recover to within 1% of the full-scale range in response to an input voltage overload of 10% beyond the full-scale range.

TYPICAL CHARACTERISTICS

Typical values given at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = -1 dBFS, sampling rate = 125 MSPS, DLL On, and 3-V differential clock, unless otherwise noted

SPECTRAL PERFORMANCE
(FFT for 20 MHZ input signal)

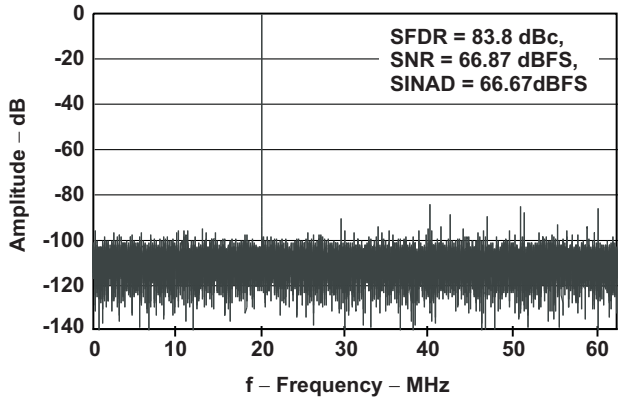


Figure 5.

SPECTRAL PERFORMANCE
(FFT for 40 MHZ input signal)

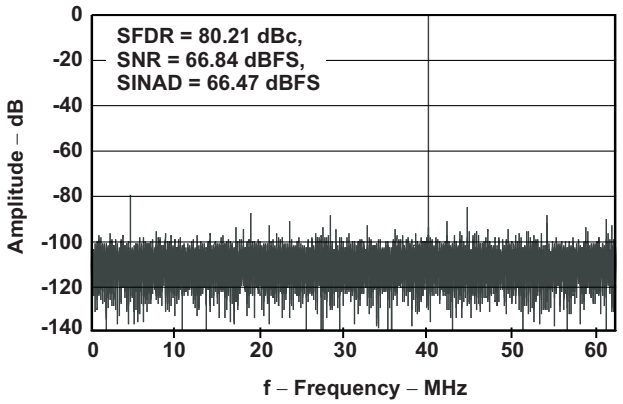


Figure 6.

SPECTRAL PERFORMANCE
(FFT for 70 MHZ input signal)

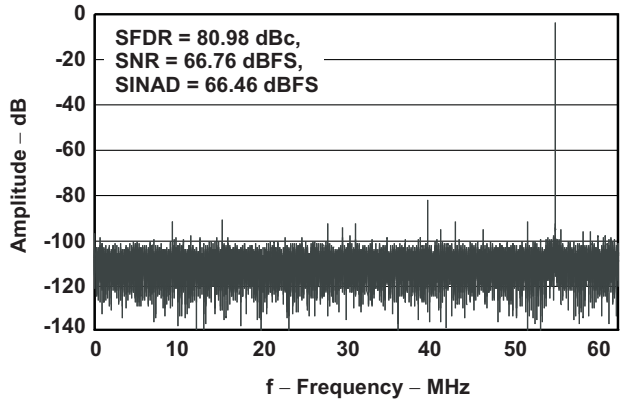


Figure 7.

SPECTRAL PERFORMANCE
(FFT for 100 MHZ input signal)

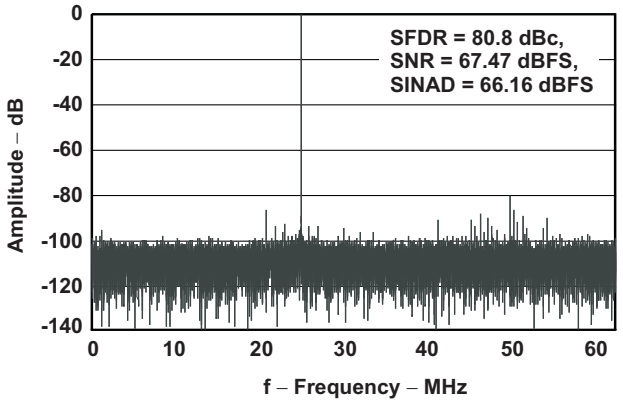


Figure 8.

SPECTRAL PERFORMANCE
(FFT for 150 MHZ input signal)

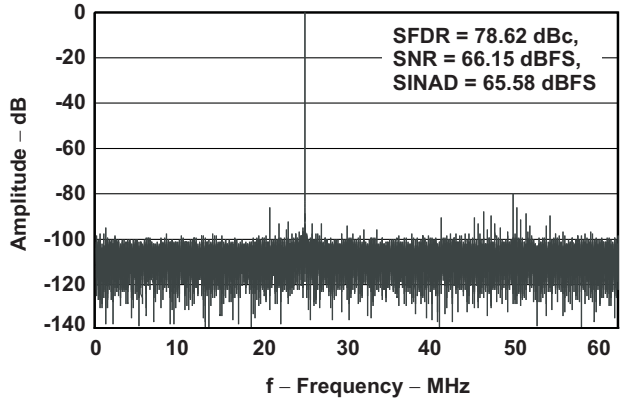


Figure 9.

SPECTRAL PERFORMANCE
(FFT for 170 MHZ input signal)

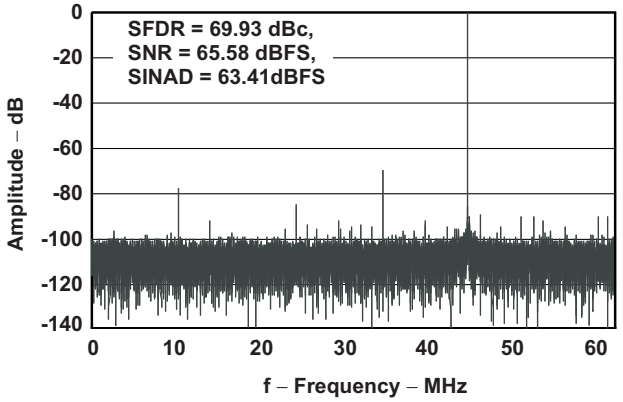


Figure 10.

TYPICAL CHARACTERISTICS (continued)

Typical values given at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = -1 dBFS, sampling rate = 125 MSPS, DLL On, and 3-V differential clock, unless otherwise noted

TWO-TONE INTERMODULATION

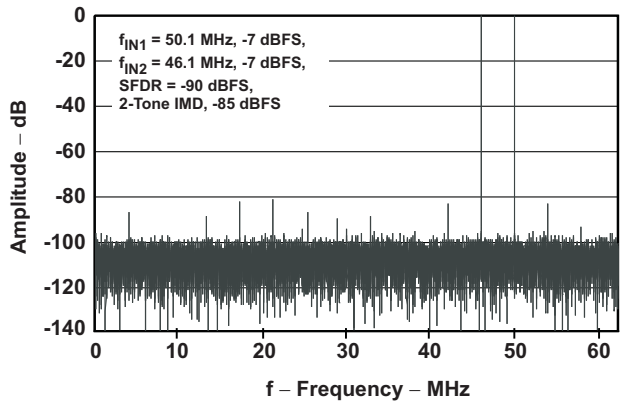


Figure 11.

SPURIOUS FREE DYNAMIC RANGE
vs
INPUT FREQUENCY

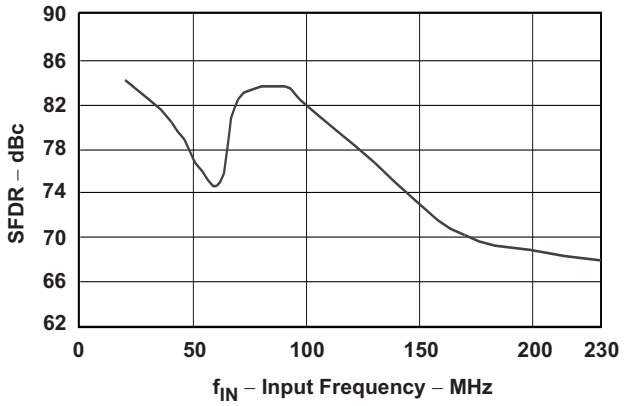


Figure 12.

SIGNAL-TO-NOISE RATIO
vs
INPUT FREQUENCY

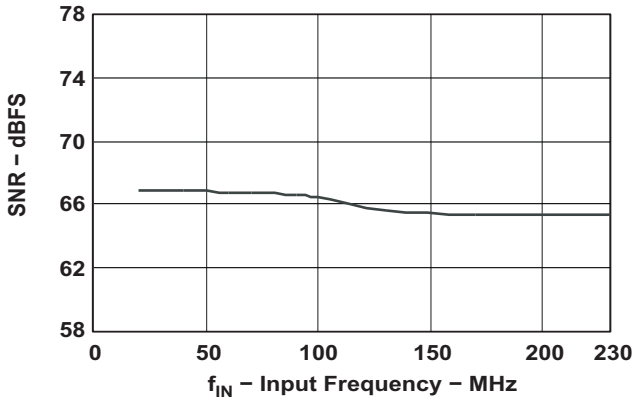


Figure 13.

AC PERFORMANCE
vs
ANALOG SUPPLY VOLTAGE

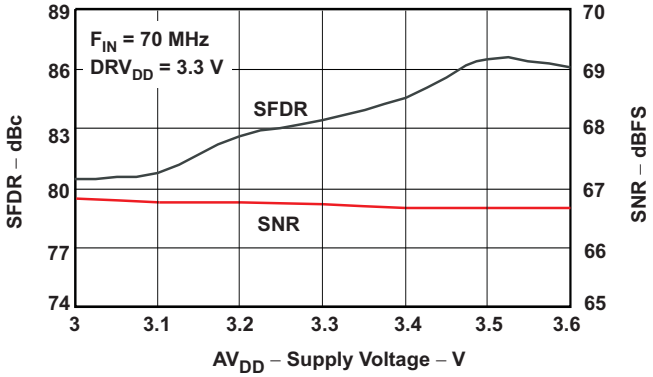


Figure 14.

AC PERFORMANCE
vs
DIGITAL SUPPLY VOLTAGE

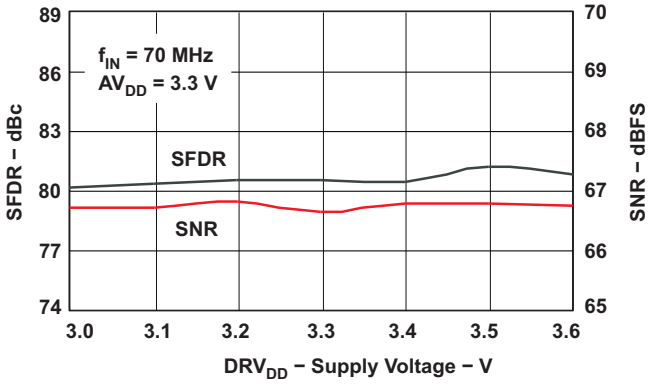


Figure 15.

AC PERFORMANCE
vs
TEMPERATURE

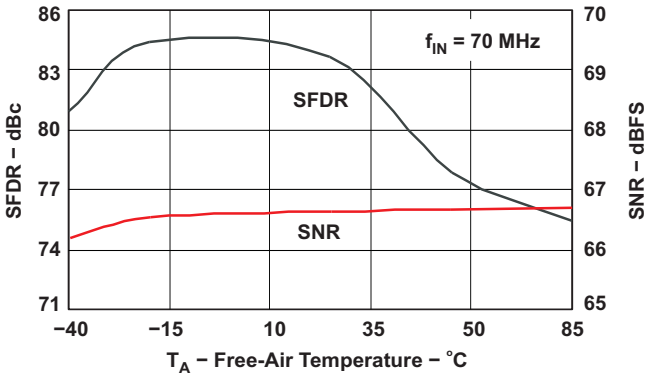


Figure 16.

TYPICAL CHARACTERISTICS (continued)

Typical values given at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = -1 dBFS, sampling rate = 125 MSPS, DLL On, and 3-V differential clock, unless otherwise noted

AC PERFORMANCE
vs
INPUT AMPLITUDE

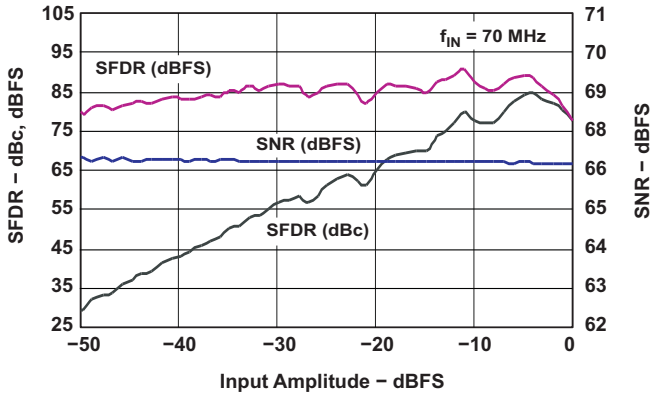


Figure 17.

AC PERFORMANCE
vs
CLOCK AMPLITUDE

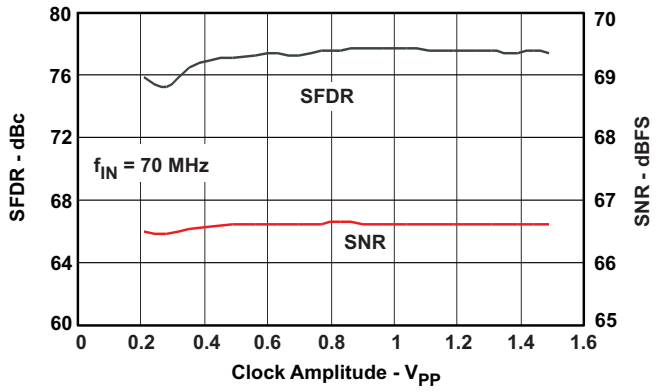


Figure 18.

AC PERFORMANCE
vs
CLOCK DUTY CYCLE

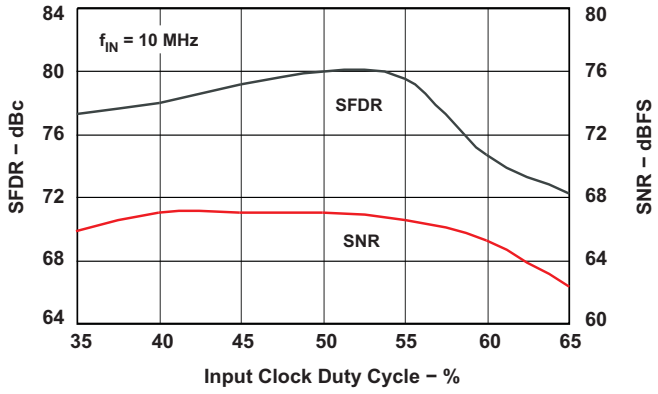


Figure 19.

OUTPUT NOISE
vs
HISTOGRAM

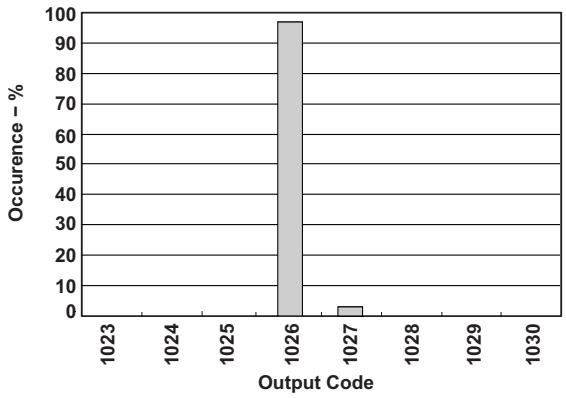


Figure 20.

POWER DISSIPATION
vs
SAMPLE RATE

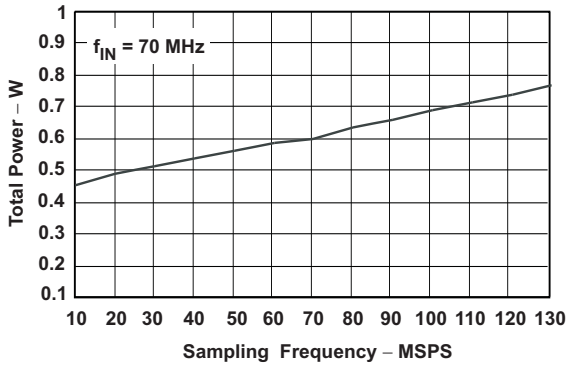


Figure 21.

TYPICAL CHARACTERISTICS (continued)

Typical values given at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = -1 dBFS, and 3-V differential clock, unless otherwise noted

DLL ON for FS > 80 MSPS

DLL OFF for FS ≤ 80 MSPS

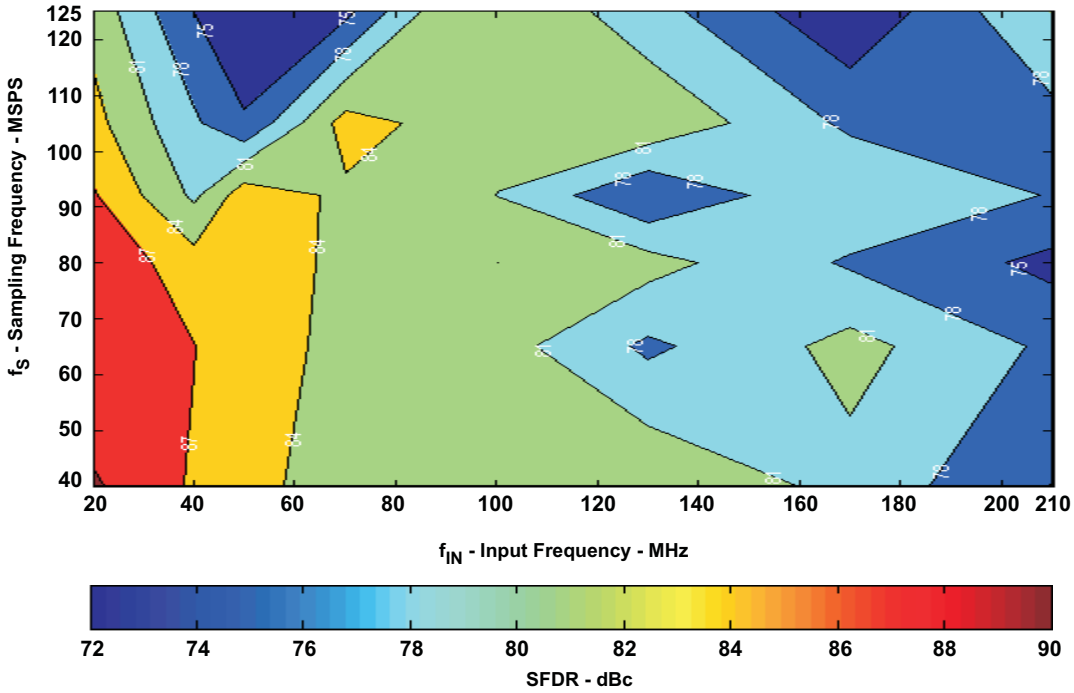


Figure 22. SFDR Contour in dBc

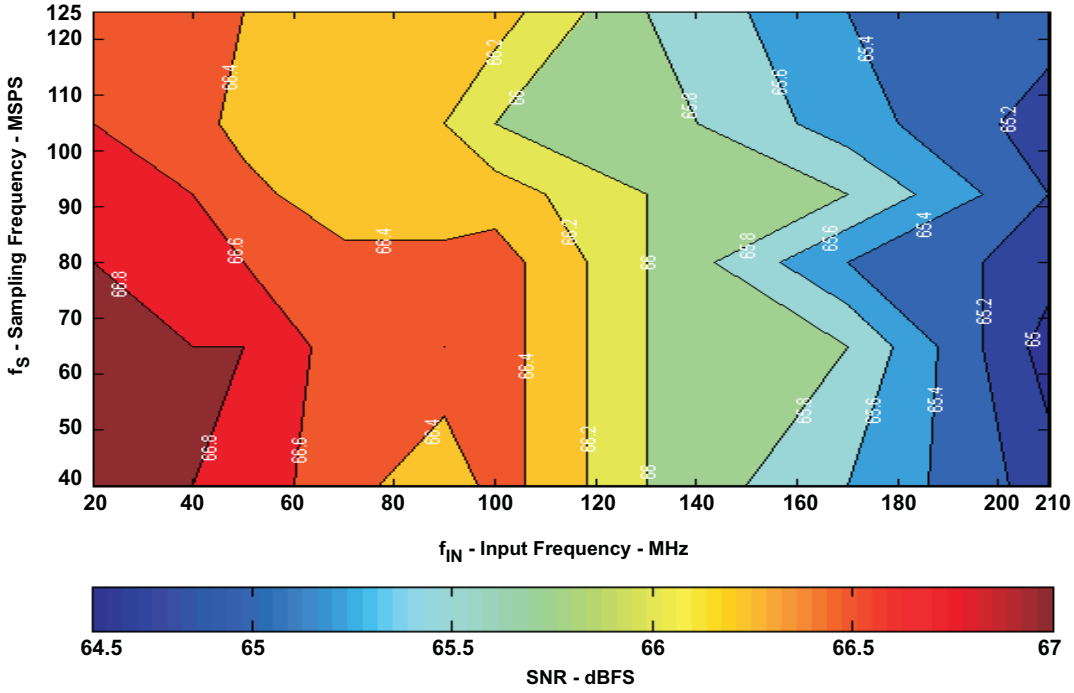


Figure 23. SNR Contour in dBFS

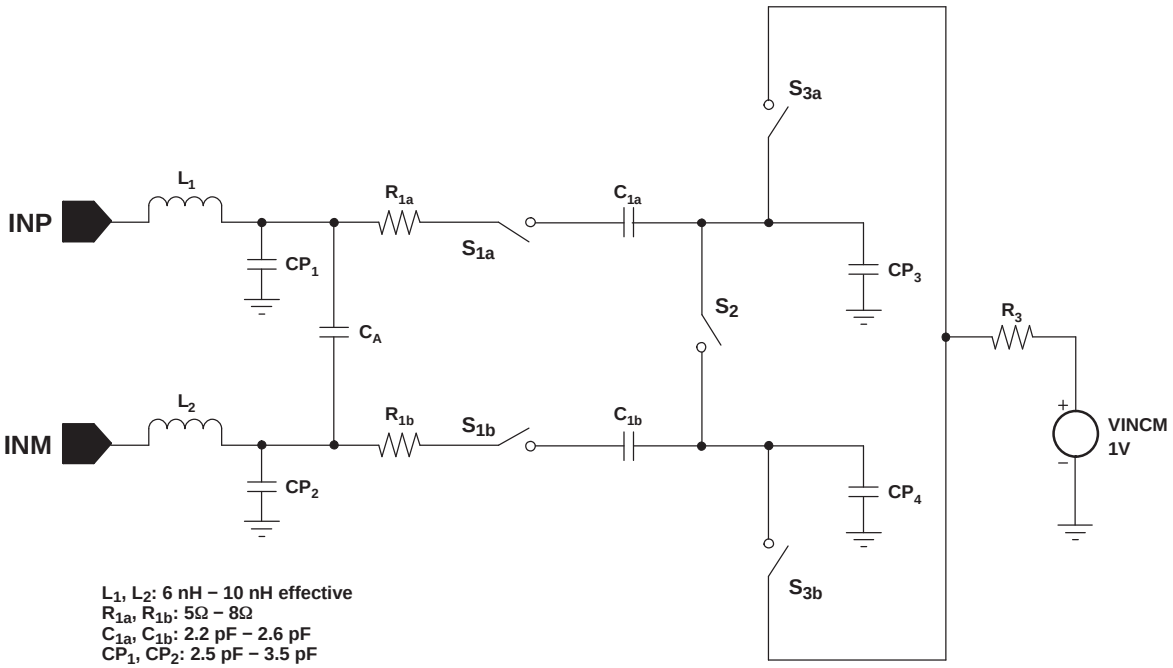
APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5510 is a low-power, 11-bit, 125 MSPS, CMOS, switched capacitor, pipeline ADC that operates from a single 3.3-V supply. The conversion process is initiated by a falling edge of the external input clock. Once the signal is captured by the input S&H, the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of 17.5 clock cycles, after which the output data is available as a 11-bit parallel word, coded in either straight offset binary or binary two's complement format.

INPUT CONFIGURATION

The analog input for the ADS5510 consists of a differential sample-and-hold architecture implemented using the switched capacitor technique shown in Figure 24.



L_1, L_2: 6 nH – 10 nH effective
R_{1a}, R_{1b}: 5Ω – 8Ω
C_{1a}, C_{1b}: 2.2 pF – 2.6 pF
CP_1, CP_2: 2.5 pF – 3.5 pF
CP_3, CP_4: 1.2 pF – 1.8 pF
C_A: 0.8 pF – 1.2 pF
R_3: 80 Ω – 120 Ω
Swithches: S_{1a}, S_{1b}: On Resistance: 35 Ω – 50 Ω
S_2: On Resistance: 7.5 Ω – 15 Ω
S_{3a}, S_{3b}: On Resistance: 40 Ω – 60 Ω
All switches OFF Resistance: 10 GΩ

A. All Switches are ON in sampling phase which is approximately one half of a clock period.

Figure 24. Analog Input Stage

This differential input topology produces a high level of ac-performance for high sampling rates. It also results in a very high usable input bandwidth, especially important for high intermediate-frequency (IF) or undersampling applications. The ADS5510 requires each of the analog inputs (INP, INM) to be externally biased around the common-mode level of the internal circuitry (CM, pin 17). For a full-scale differential input, each of the differential lines of the input signal (pins 19 and 20) swings symmetrically between CM + 0.575 V and CM – 0.575 V. This means that each input is driven with a signal of up to CM ± 0.575 V, so that each input has a maximum differential signal of 1.15 V_{PP} for a total differential input signal swing of 2.3 V_{PP}. The maximum swing is determined by the two reference voltages, the top reference (REFP, pin 29), and the bottom reference (REFM, pin 30).

The ADS5510 obtains optimum performance when the analog inputs are driven differentially. The circuit shown in Figure 25 illustrates one possible configuration using an RF transformer.

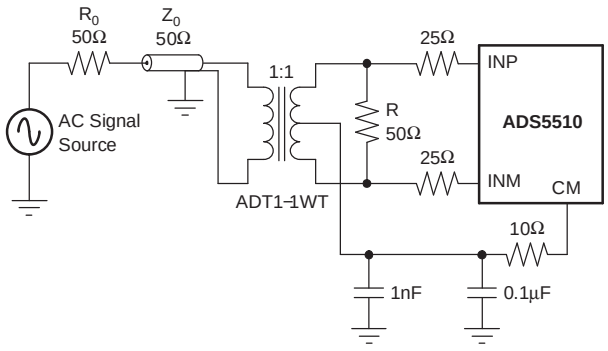


Figure 25. Transformer Input to Convert Single-Ended Signal to Differential Signal

The single-ended signal is fed to the primary winding of an RF transformer. Placing a 25-Ω resistor in series with INP and INM is recommended to dampen ringing due to ADC kickback.

Since the input signal must be biased around the common-mode voltage of the internal circuitry, the common-mode voltage (V_{CM}) from the ADS5510 is connected to the center-tap of the secondary winding.

To ensure a steady low-noise V_{CM} reference, best performance is attained when the CM output (pin 17) is filtered to ground with a 10-Ω series resistor and parallel 0.1-µF and 0.001-µF low-inductance capacitors, as illustrated in Figure 24.

Output V_{CM} (pin 17) is designed to directly drive the ADC input. When providing a custom CM level, be aware that the input structure of the ADC sinks a common-mode current in the order of 600 µA (300 µA per input). Equation 1 describes the dependency of the common-mode current and the sampling frequency:

$$\frac{600\mu A \times f_S \text{ (in MSPS)}}{125 \text{ MSPS}} \quad (1)$$

Where:

f_S > 2 MSPS.

This equation helps to design the output capability and impedance of the driving circuit accordingly.

When it is necessary to buffer or apply a gain to the incoming analog signal, it is possible to combine single-ended operational amplifiers with an RF transformer, or to use a differential input/output amplifier without a transformer, to drive the input of the ADS5510. Texas Instruments offers a wide selection of single-ended operational amplifiers (including the THS3201, THS3202, OPA695, and OPA847) that can be selected depending on the application. An RF gain block amplifier, such as Texas Instruments THS9001, can also be used with an RF transformer for high input frequency applications. The THS4503 is a recommended differential input/output amplifier. Table 4 lists the recommended amplifiers.

Table 4. Recommended Amplifiers to Drive the Input of the ADS5510

INPUT SIGNAL FREQUENCY	RECOMMENDED AMPLIFIER	TYPE OF AMPLIFIER	USE WITH TRANSFORMER?
DC to 20 MHz	THS4503	Differential In/Out Amp	No
DC to 50 MHz	OPA847	Operational Amp	Yes
DC to 100 MHz	THS4509	Differential In/Out Amp	No
10 MHz to 120 MHz	OPA695	Operational Amp	Yes
	THS3201	Operational Amp	Yes
	THS3202	Operational Amp	Yes
Over 100 MHz	THS9001	RF Gain Block	Yes

When using single-ended operational amplifiers (such as the THS3201, THS3202, OPA695, or OPA847) to provide gain, a three-amplifier circuit is recommended with one amplifier driving the primary of an RF transformer and one amplifier in each of the legs of the secondary driving the two differential inputs of the ADS5510. These three amplifier circuits minimize even-order harmonics. For high frequency inputs, an RF gain block amplifier can be used to drive a transformer primary; in this case, the transformer secondary connections can drive the input of the ADS5510 directly, as shown in Figure 25, or with the addition of the filter circuit shown in Figure 26.

Figure 26 illustrates how R_{IN} and C_{IN} can be placed to isolate the signal source from the switching inputs of the ADC and to implement a low-pass RC filter to limit the input noise in the ADC. It is recommended that these components be included in the ADS5510 circuit layout when any of the amplifier circuits discussed previously are used. The components allow fine-tuning of the circuit performance. Any mismatch between the differential lines of the ADS5510 input produces a degradation in performance at high input frequencies, mainly characterized by an increase in the even-order harmonics. In this case, special care should be taken to keep as much electrical symmetry as possible between both inputs.

Another possible configuration for lower-frequency signals is the use of differential input/output amplifiers that can simplify the driver circuit for applications requiring dc-coupling of the input. Flexible in their configurations (see Figure 27), such amplifiers can be used for single-ended-to-differential conversion signal amplification.

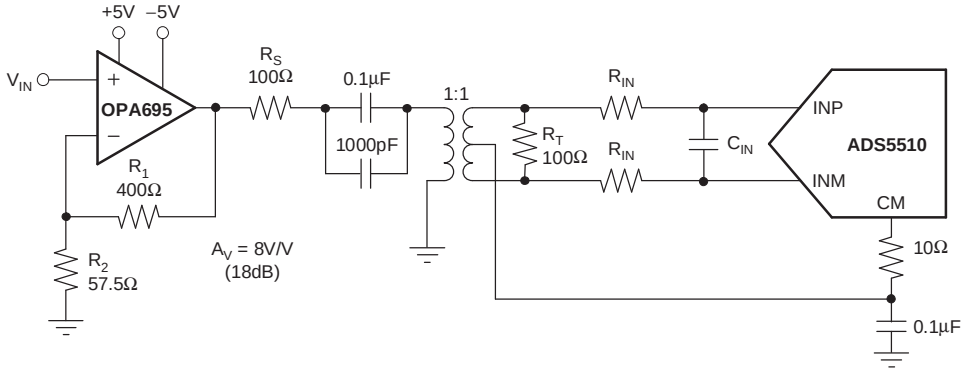


Figure 26. Converting a Single-Ended Input Signal to a Differential Signal Using an RF Transformer

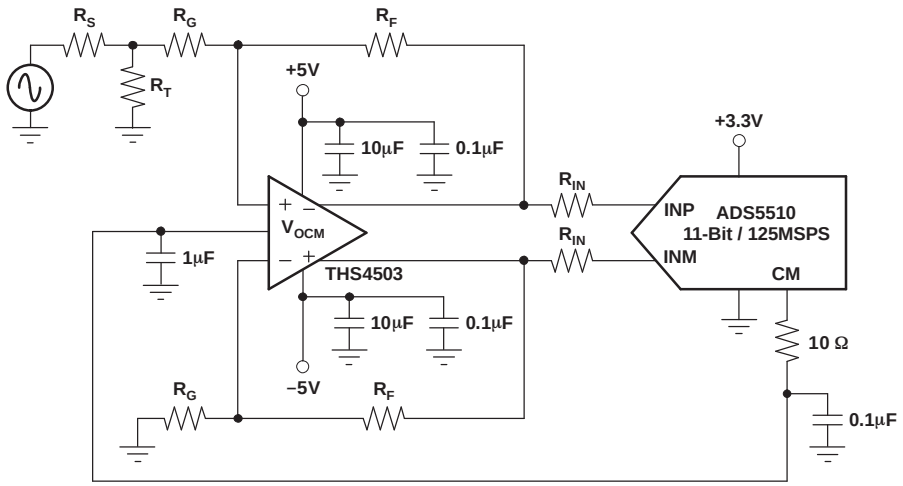


Figure 27. Using the THS4503 with the ADS5510

POWER-SUPPLY SEQUENCE

The preferred power-up sequence is to ramp AV_{DD} first, followed by DRV_{DD}, including a simultaneous ramp of AV_{DD} and DRV_{DD}. In the event that DRV_{DD} ramps up first in the system, care must be taken to ensure that AV_{DD} ramps up within 10 ms. Optionally, it is recommended to put a 2-kΩ resistor from REFP (pin 29) to AVDD as shown in Figure 28. This helps to make the device more robust to power supply ramp-up timings.

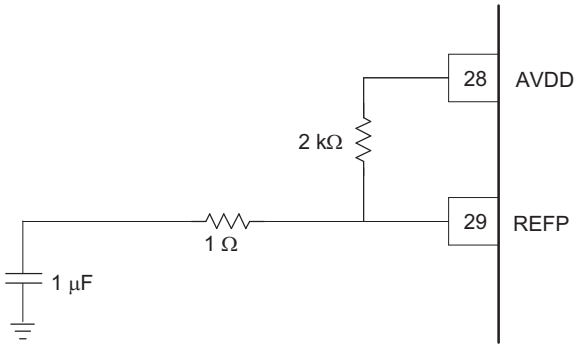


Figure 28.

POWER-DOWN

The device enters power-down in one of two ways: either by reducing the clock speed or by setting the PDN bit throughout the serial programming interface. Using the reduced clock speed, power-down may be initiated for clock frequency below 2 MSPS. The exact frequency at which the power down occurs varies from device to device.

Using the serial interface PDN bit to power down the device places the outputs in a high-impedance state and only the internal reference remains on to reduce the power-up time. The power-down mode reduces power dissipation to approximately 180 mW.

REFERENCE CIRCUIT

The ADS5510 has built-in internal reference generation, requiring no external circuitry on the printed circuit board (PCB). For optimum performance, it is best to connect both REFP and REFM to ground with a 1-µF decoupling capacitor (the 1-Ω resistor shown in Figure 29 is optional). In addition, an external 56.2-kΩ resistor should be connected from IREF (pin 31) to AGND to set the proper current for the operation of the ADC, as shown in Figure 29. No capacitor should be connected between pin 31 and ground; only the 56.2-kΩ resistor should be used.

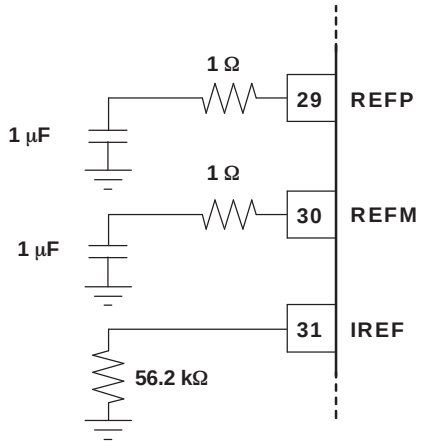


Figure 29. REFP, REFM, and IREF Connections for Optimum Performance

CLOCK INPUT

The ADS5510 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. The common-mode voltage of the clock inputs is set internally to CM (pin 17) using internal 5-kΩ resistors that connect CLKP (pin 10) and CLKM (pin 11) to CM (pin 17), as shown in Figure 30.

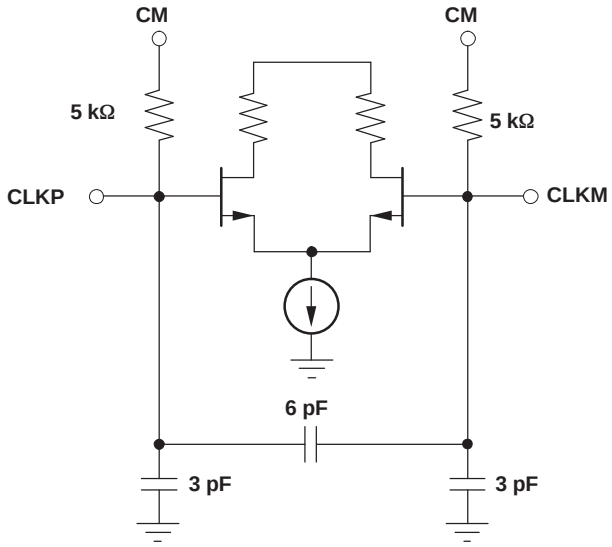


Figure 30. Clock Inputs

When driven with a single-ended CMOS clock input, it is best to connect CLKM (pin 11) to ground with a 0.01-µF capacitor, while CLKP is ac-coupled with a 0.01-µF capacitor to the clock source, as shown in Figure 31.

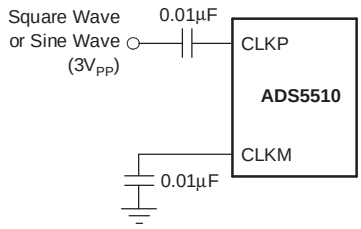


Figure 31. AC-Coupled, Single-Ended Clock Input

The ADS5510 clock input can also be driven differentially, reducing susceptibility to common-mode noise. In this case, it is best to connect both clock inputs to the differential input clock signal with 0.01-µF capacitors, as shown in Figure 32.

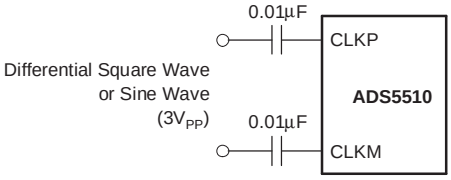


Figure 32. AC-Coupled, Differential Clock Input

For high input frequency sampling, it is recommended to use a clock source with low jitter. Additionally, the internal ADC core uses both edges of the clock for the conversion process. This means that, ideally, a 50% duty cycle should be provided. Figure 19 shows the performance variation of the ADC versus clock duty cycle.

Bandpass filtering of the source can help produce a 50% duty cycle clock and reduce the effect of jitter. When using a sinusoidal clock, the clock jitter further improves as the amplitude is increased. In that sense, using a differential clock allows for the use of larger amplitudes without exceeding the supply rails and absolute maximum ratings of the ADC clock input. Figure 18 shows the performance variation of the device versus input clock amplitude. For detailed clocking schemes based on transformer or PECL-level clocks, see the ADS55xxEVM User's Guide (SLWU010), available for download from www.ti.com.

INTERNAL DLL

In order to obtain the fastest sampling rates achievable with the ADS5510, the device uses an internal digital delay lock loop (DLL). Nevertheless, the limited frequency range of operation of DLL degrades the performance at clock frequencies below 60 MSPS. In order to operate the device below 60 MSPS, the internal DLL must be shut off using the DLL OFF mode described in the *Serial Interface Programming* section. The *Typical Performance Curves* show the performance obtained in both modes of operation: DLL ON (default) and DLL OFF. In either of the two modes, the device enters power-down mode if no clock or slow clock is provided. The limit of the clock frequency where the device functions properly with default settings is ensured to be over 2 MHz.

OUTPUT INFORMATION

The ADC provides 11 data outputs (D10 to D0, with D10 being the MSB and D0 the LSB), a data-ready signal (CLKOUT, pin 43), and an out-of-range indicator (OVR, pin 64) that equals 1 when the output reaches the full-scale limits.

Two different output formats (straight offset binary or two's complement) and two different output clock polarities (latching output data on rising or falling edge of the output clock) can be selected by setting DFS (pin 40) to one of four different voltages. Table 3 details the four modes. In addition, output enable control (OE, pin 41, active high) is provided to put the outputs into a high-impedance state.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 0x7FF in straight offset binary output format and 0x3FF in two's complement output format. For a negative input overdrive, the output code is 0x000 in straight offset binary output format and 0x400 in two's complement output format. These outputs to an overdrive signal are ensured through design and characterization.

The output circuitry of the ADS5510, by design, minimizes the noise produced by the data switching transients, and, in particular, its coupling to the ADC analog circuitry. Output D1 (pin 51) senses the load capacitance and adjusts the drive capability of all the output pins of the ADC to maintain the same output slew rate described in the timing diagram of Figure 1. Care should be taken to ensure that all output lines (including CLKOUT) have nearly the same load as D1 (pin 51). This circuit also reduces the sensitivity of the output timing versus supply voltage or temperature. Placing external resistors in series with the outputs is ***not*** recommended.

The timing characteristics of the digital outputs change for sampling rates below the 125 MSPS maximum sampling frequency. Table 5 and Table 6 show the setup, hold, input clock to output data delays, and rise and fall times for different sampling frequencies with the DLL on and off, respectively.

Table 7 and Table 8 show the rise and fall times at additional sampling frequencies with DLL on and off, respectively.

To use the input clock as the data capture clock, it is necessary to delay the input clock by a delay, t_d, that results in the desired setup or hold time. Use either Equation 2or Equation 3 to calculate the value of t_d.

Desired setup time = $t_d - t_{START}$

Desired hold time = $t_{END} - t_d$

Table 5. Timing Characteristics at Additional Sampling Frequencies (DLL ON)

f_S (MSPS)	t_{SETUP} (ns)			t_{HOLD} (ns)			t_{START} (ns)			t_{END} (ns)			t_r (ns)			t_f (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
105	2.4	3.1		2.2	2.6			1.7	2.6	5.8	7.3			4.4	5.1		3.3	3.8
93	3.2	4.6		2.3	3.7													
80	2.8	3.7		2.8	3.3			0.5	1.7	5.3	7.9			5.8	6.6		4.4	5.3
65	3.8	4.6		3.6	4.1			–0.5	0.8	5.3	8.5			6.7	7.2		5.5	6.4

Table 6. Timing Characteristics at Additional Sampling Frequencies (DLL OFF)

f_S (MSPS)	t_{SETUP} (ns)			t_{HOLD} (ns)			t_{START} (ns)			t_{END} (ns)			t_r (ns)			t_f (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80	3.2	4.2		1.8	3			3.8	5	8.4	11			5.8	6.6		4.4	5.3
65	4.3	5.7		2	3			2.8	4.5	8.3	11.8			6.6	7.2		5.5	6.4
40	8.5	11		2.6	3.5			–1	1.5	8.9	14.5			7.5	8		7.3	7.8
20	17	25.7		2.5	4.7			–9.8	2	9.5	21.6			7.5	8		7.6	8
10	27	51		4	6.5			-30	-3	11.5	31							
2	284	370		8	19			185	320	515	576			50	82		75	150

Table 7. Timing Characteristics at Additional Sampling Frequencies (DLL ON)

f_S (MSPS)	CLKOUT, Rise Time t_r (ns)			CLKOUT, Fall Time t_f (ns)			CLKOUT Jitter, Peak-to-Peak t_{JIT} (ps)			Input-to-Output Clock Delay t_{PDI} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
105		2	2.2		1.7	1.8		175	250	4	4.7	5.5
80		2.5	2.8		2.1	2.3		210	315	3.7	4.3	5.1
65		3.1	3.5		2.6	2.9		260	380	3.5	4.1	4.8

Table 8. Timing Characteristics at Additional Sampling Frequencies (DLL OFF)

f_S (MSPS)	CLKOUT, Rise Time t_r (ns)			CLKOUT, Fall Time t_f (ns)			CLKOUT Jitter, Peak-to-Peak t_{JIT} (ps)			Input-to-Output Clock Delay t_{PDI} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80		2.5	2.8		2.1	2.3		210	315	7.1	8	8.9
65		3.1	3.5		2.6	2.9		260	380	7.8	8.5	9.4
40		4.8	5.3		4	4.4		445	650	9.5	10.4	11.4
20		8.3	9.5		7.6	8.2		800	1200	13	15.5	18
10										16	20.7	25.5
2		31	52		36	65		2610	4400	537	551	567

SERIAL PROGRAMMING INTERFACE

The ADS5510 has internal registers for the programming of some of the modes described in the previous sections. The registers should be reset after power-up by applying a 2 μs (minimum) high pulse on RESET (pin 35); this also resets the entire ADC and sets the data outputs to low. This pin has a 200-kΩ internal pullup resistor to AVDD. The programming is done through a three-wire interface. The timing diagram and serial register setting in the *Serial Programing Interface* section describe the programming of this register.

Table 2 shows the different modes and the bit values to be written to the register to enable them.

Note that some of these modes may modify the standard operation of the device and possibly vary the performance with respect to the typical data shown in this data sheet.

Applying a RESET signal is *must* to set the internal registers to their default states for normal operation. If the hardware RESET function is not used in the system, the RESET pin must be tied to ground and it is necessary to write the default values to the internal registers through the serial programming interface. The registers must be written in the following order.

Write 9000h (Address 9, Data 000)
Write A000h (Address A, Data 000)
Write B000h (Address B, Data 000)
Write C000h (Address C, Data 000)
Write D000h (Address D, Data 000)
Write E000h (Address E, Data 804)
Write 0000h (Address 0, Data 000)
Write 1000h (Address 1, Data 000)
Write F000h (Address F, Data 000)

NOTE:

This procedure is only required if a RESET pulse is not provided to the device.

PowerPAD PACKAGE

The PowerPAD package is a thermally enhanced standard size IC package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques and can be removed and replaced using standard repair procedures.

The PowerPAD package is designed so that the lead frame die pad (or thermal pad) is exposed on the bottom of the IC. This provides a low thermal resistance path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the printed circuit board (PCB), using the PCB as a heatsink.

Assembly Process

1. Prepare the PCB top-side etch pattern including etch for the leads as well as the thermal pad as illustrated in the *Mechanical Data* section. The recommended thermal pad dimension is 8 mm x 8 mm.
2. Place a 5-by-5 array of thermal vias in the thermal pad area. These holes should be 13 mils in diameter. The small size prevents wicking of the solder through the holes.
3. It is recommended to place a small number of 25 mil diameter holes under the package, but outside the thermal pad area to provide an additional heat path.
4. Connect all holes (both those inside and outside the thermal pad area) to an internal copper plane (such as a ground plane).
5. Do not use the typical web or spoke via connection pattern when connecting the thermal vias to the ground plane. The spoke pattern increases the thermal resistance to the ground plane.
6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area.
7. Cover the entire bottom side of the PowerPAD vias to prevent solder wicking.
8. Apply solder paste to the exposed thermal pad area and all of the package terminals.

For more detailed information regarding the PowerPAD package and its thermal properties, see either the application brief SLMA004B (*PowerPAD Made Easy*) or technical brief SLMA002 (*PowerPAD Thermally Enhanced Package*).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS5510IPAP	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5510I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

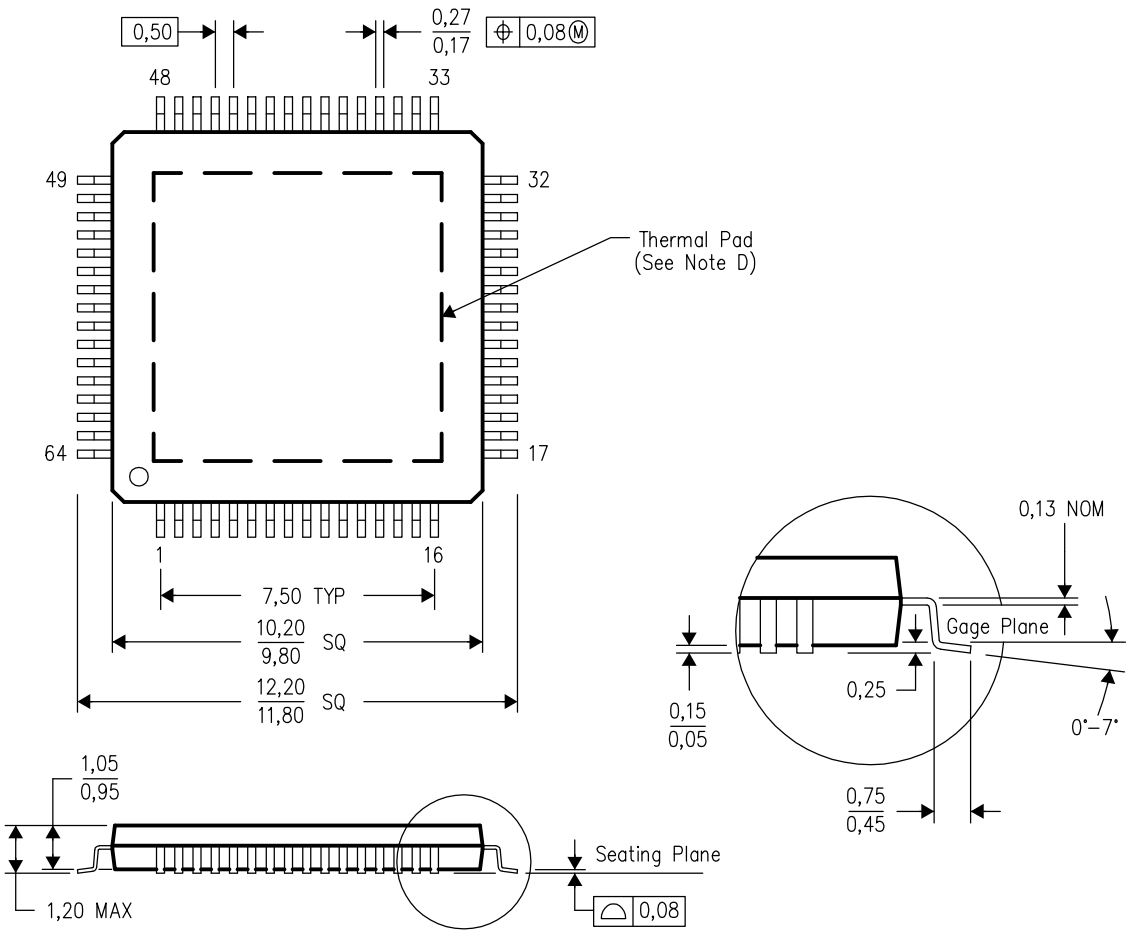
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

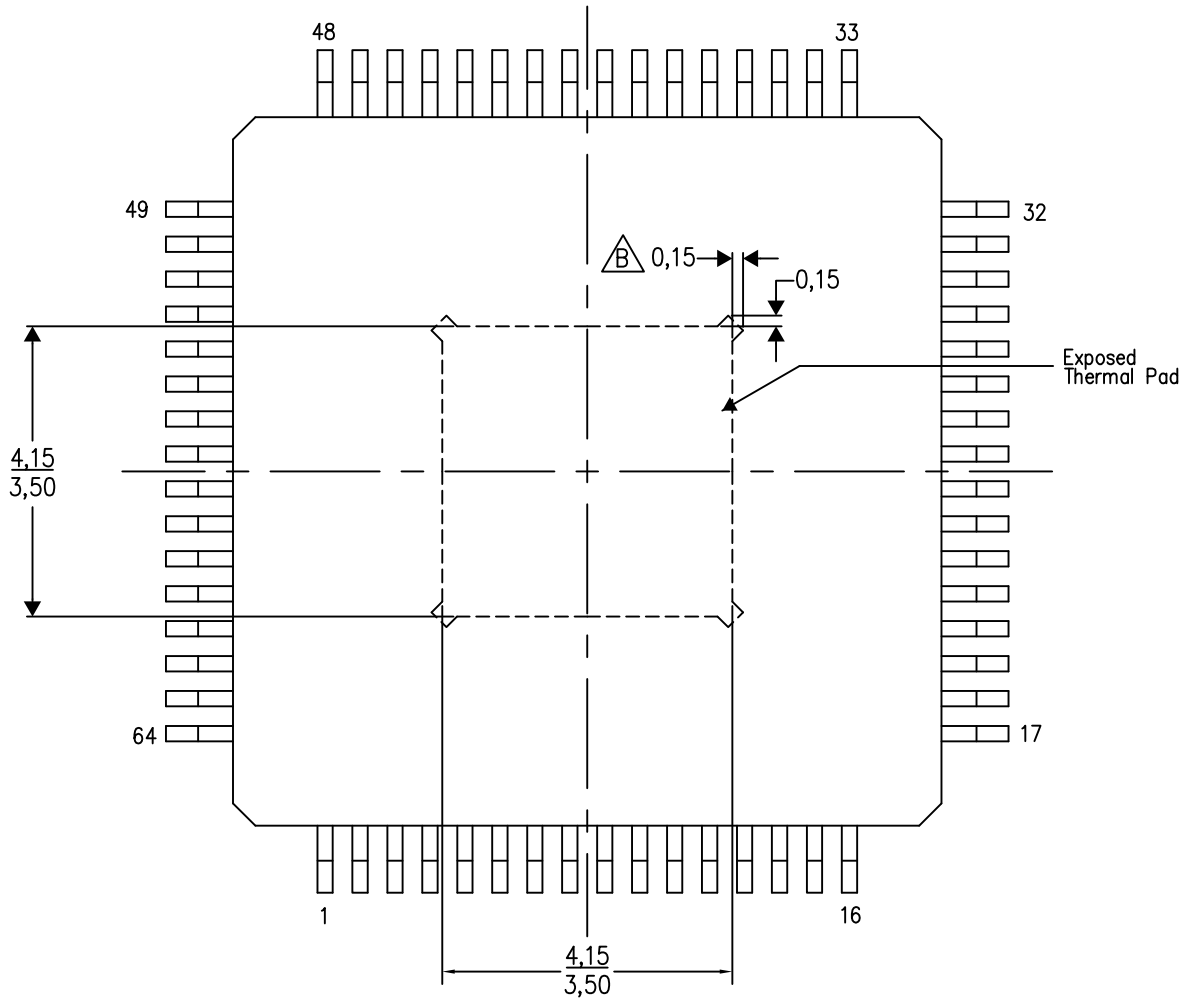
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

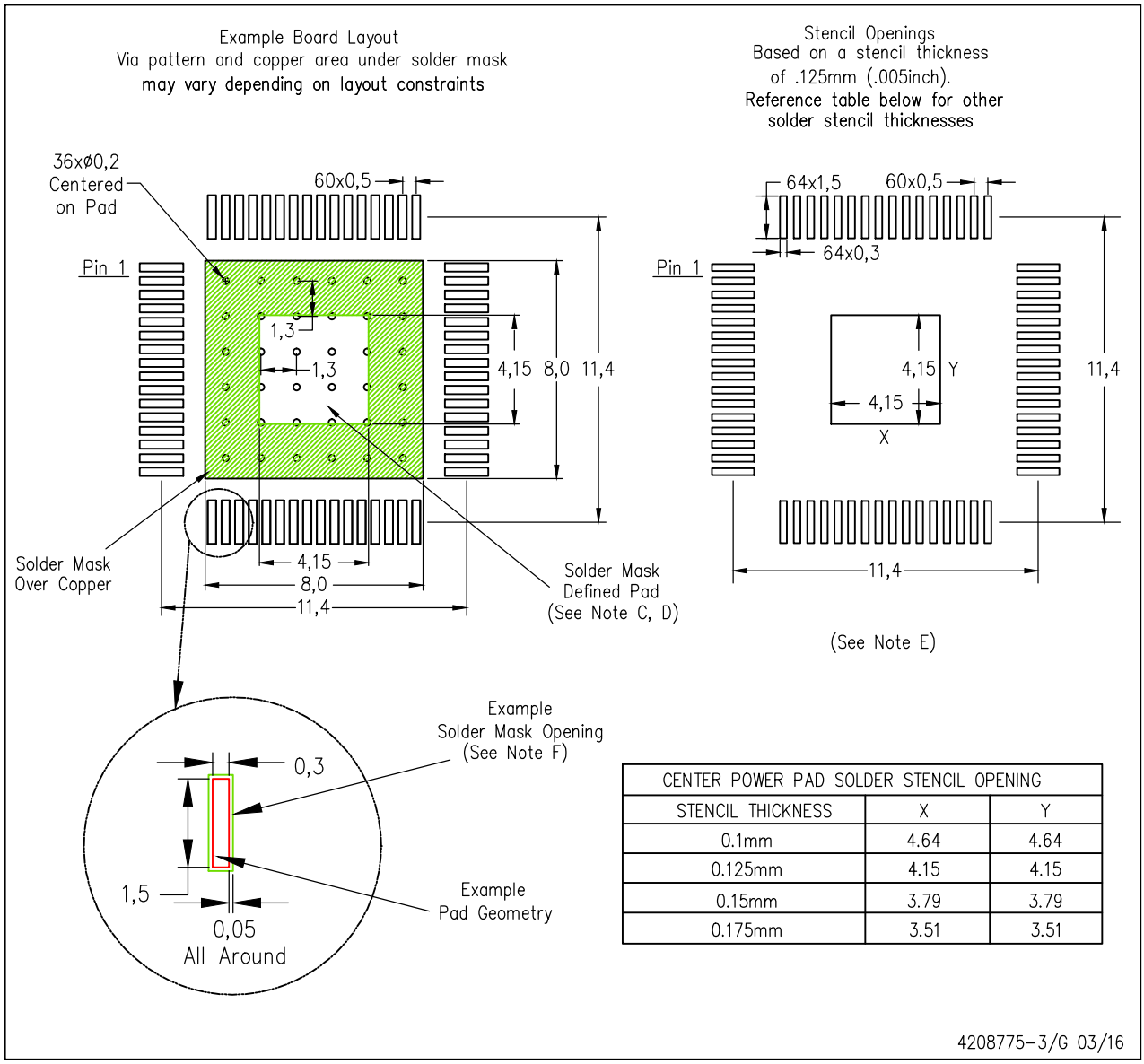
4206326–2/P 05/14

NOTES: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

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PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	4.64	4.64
0.125mm	4.15	4.15
0.15mm	3.79	3.79
0.175mm	3.51	3.51

4208775–3/G 03/16

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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