Vol 54 No 2, March 2020

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StudentZone—ADALM2000 Activity: Op Amp Settling Time

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Settling Time Background

Objective

The settling time of an amplifier, or any signal chain for that matter, is defined as the time it takes the output to respond to a step change in the input and to come into and remain within a defined error band around the final value, as measured relative to the 50% point of the input pulse, as shown in Figure 1.

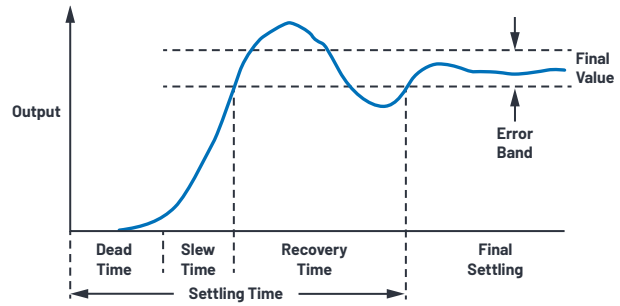

Figure 1. Settling time.

- Error band is usually defined to be a percentage of the step; for example, 1%, 0.5%, 0.1%, etc.
- Settling time is often nonlinear; it may take 30 times as long to settle to 0.01% as to 0.1%.
- Manufacturers often choose an error band that makes the op amp look good.

Unlike a digital-to-analog converter (DAC), there is no obvious error band for an operational amplifier (op amp); a DAC naturally has an error band of 1 LSB, or perhaps ±1 LSB. An appropriate band must be chosen and defined, along with other definitions such as the step size (1 V, 5 V, 10 V, etc.). The error band choice will depend on the performance of the op amp, but since the value chosen will vary from device to device, comparisons are often difficult. This is true because amplifier settling is not as simple as a single-pole RC system, and many different time constants may be involved. Examples include early op amps using dielectrically isolated (DI) processes. These had very fast settling to 1% of full scale, but they took forever to settle to 0.1%. Similarly, some very high precision op amps have thermal effects that cause settling to 0.001% or better to take tens of milliseconds, although they will settle to 0.025% in a few microseconds.

It should also be noted that thermal effects can cause significant differences between short-term settling time (generally measured in nanoseconds) and long-term settling time (generally measured in microseconds or milliseconds). In many ac applications, long-term settling time is not important, but if it is in dc data acquisition systems, it must be measured on a much different time scale than short-term settling time.

Measuring Settling Time

Measuring fast settling time with high accuracy is very difficult. Great care is required in order to generate fast, highly accurate, low noise, flat top pulses. Large amplitude step voltages will overdrive many oscilloscope front ends when the input scaling is set for high sensitivity.

Materials

- ADALM2000 active learning module
- Solderless breadboard and jumper wire kit
- Two 10 kΩ resistors
- One 10 kΩ potentiometer
- Two Schottky diodes (the 1N914 silicon diodes supplied in the ADALP2000 analog parts kit can be used, but will not work as well)
- One OP27 op amp
- One OP37 op amp
- One OP97 slow settling amplifier
- Two 0.1 µF capacitors (used to decouple the Vp and Vn power supplies)

Directions

Build the test setup as shown in Figure 2. Remember to supply power to the op amp, +5 V to Pin 7 and –5 V to Pin 4 with 0.1 µF capacitors used to decouple the Vp and Vn power supplies. This arrangement is useful in making settling time measurements on op amps, such as this setup, operating in inverting mode. The

signal at the false summing node (the wiper of the potentiometer) represents the difference between the output and the input signal, multiplied by the constant k; that is, the error signal.

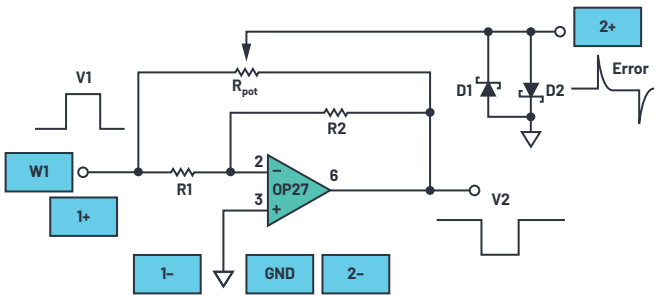

Figure 2. Measuring settling time using a false summing node.

$$Error = k(V1 - V2)$$
$$k = \frac{R1}{R1 + R2} \quad (1)$$

There are many subtleties involved in making this setup work reliably. The resistances should be low in value to minimize parasitic time constants. The back-to-back Schottky diode clamps, D1 and D2, help prevent scope overdrive and allow the use of a high vertical sensitivity setting. Regular diodes such as the 1N914 types supplied in the parts kit will clamp at a much higher voltage and may store more charge due to higher capacitance than Schottky diodes, thus with R1 = R2 = 10 kΩ, then k = 0.5. Thus, the error band at the error output will be 5 mV for 1% settling with a 1 V input step.

Hardware Setup

Waveform Generator 1 should be configured for a 60 kHz square wave 1 V amplitude peak-to-peak and 0 V offset. Scope Channel 1 is used to monitor the input square wave and should be set to 500 mV/div and used as the trigger source. Scope Channel 2 is used to alternately measure the op amp output, V2, and the error signal at the wiper of the potentiometer. Channel 2 should be set to 500 mV/div when observing the output of the amplifier, but should be set to a more sensitive scale of 100 mV/div when observing the error signal.

Procedure

First, use an OP27 amplifier from the analog parts kit for your measurements. The potentiometer should be set near the center of its adjustment range beforehand and should be fine-tuned such that the flat portion of both halves of the signal are nearly equal and centered near 0 V (see Figure 4). Export the error waveform showing the settling to both rising and falling input steps for inclusion in your lab report. You can also store the error waveform, Scope Channel 2, for the OP27 as a reference waveform (REF1) for future comparison to the settling response of other amplifiers.

Next, replace the OP27 amplifier with an OP37 amplifier from the parts kit. Again, export the error waveform showing the settling to both rising and falling input steps for inclusion in your lab report. Overlay the OP37 settling waveform with the saved reference waveform of the OP27. Compare the settling time and general characteristics of each. You should store the error waveform for the OP37 as a reference waveform (REF2) for future comparison.

Finally, replace the OP37 with the much slower settling OP97 amplifier. Again, export the error waveform showing the settling to both rising and falling input steps for inclusion in your lab report. Overlay the OP97 settling waveform with the saved reference waveforms of the OP27 and OP37. Compare the settling time and general characteristics of each.

Figure 4. Example settling waveforms.

Questions

- The faster amplifiers show a ringing settling characteristic. What circuit component(s) could you add to remove the ringing (perhaps at the cost of a longer settling time)?
- Try using lower value resistors for R1 and R2 (1 kΩ for example) and a lower value for the potentiometer (5 kΩ or lower). How does this change the settling waveforms you see, if any?

You can find the answer at the StudentZone blog.

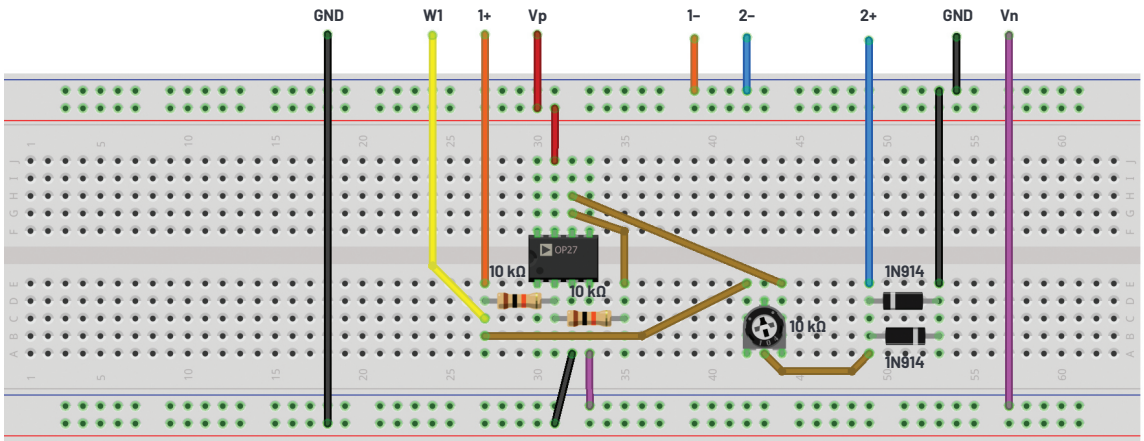

Figure 3. Op amp settling time breadboard circuit.

Additional Background on Settling Time Measurements

In some cases, a second (very fast) amplifier stage may be used after the false summing node to increase the error signal level. Many modern digitizing oscilloscopes, such as the ADALM2000 module, are less sensitive to input overdrive and can be used to measure the error waveform directly. This must be verified for each oscilloscope by examining the operating manual carefully. Note that a direct measurement allows measurements of settling time in both the inverting and noninverting modes. An example of the output step response to a flat pulse input for the OP27 and OP97 op amps is shown in Figure 4. Notice that a settling time of 1% is approximately 2.8 µs for the OP27 and 4.2 µs for the OP97.

In making settling time measurements of this type, it is also imperative to use a pulse source capable of generating a pulse with very fast rise and fall times and enough flatness. In other words, if the op amp under test has a settling time to 0.1% of 20 ns, the applied pulse should settle to better than 0.05% in less than 5 ns. This is beyond the capabilities of the AWG sources built into the ADALM2000 module.

This type of source can be expensive, but a simple circuit as shown in Figure 5 can be used with a reasonably flat generator to ensure a flat pulse output.

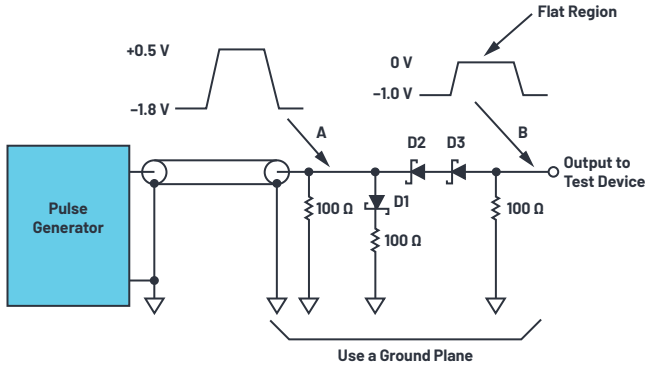

Figure 5. A simple flat pulse generator.

The circuit in Figure 5 works best if low capacitance Schottky diodes are used for D1, D2, and D3, and the lead lengths on all the connections are minimized. A short length of 50 Ω coax can be used to connect the pulse generator to the circuit, but the best results are obtained if the test fixture is connected directly to the output of the generator. The pulse generator is adjusted to output a positive-going pulse at A (see Figure 5) that rises from approximately –1.8 V to +0.5 V in less than 5 ns (assuming the settling time of the test device is in the order of 20 ns). Shorter rise times may generate ringing, and longer rise times can degrade the test device settling time; therefore, some optimization is required in the actual circuit to achieve the best performance. When pulse generator output A goes above 0 V, D1 begins to conduct, and D2/D3 are reverse biased. The 0 V region of signal B at the input of the device to be tested is flat, neglecting the leakage current and stray capacitance of the D2-D3 series combination. The D1 diode and its 100 Ω resistor help maintain an approximate 50 Ω termination during the time the pulse at A is positive.

About the Author

Doug Mercer received his B.S.E.E. degree from Rensselaer Polytechnic Institute (RPI) in 1977. Since joining Analog Devices in 1977, he has contributed directly or indirectly to more than 30 data converter products and he holds 13 patents. He was appointed to the position of ADI Fellow in 1995. In 2009, he transitioned from full-time work and has continued consulting at ADI as a Fellow Emeritus contributing to the Active Learning Program. In 2016 he was named Engineer in Residence within the ECSE department at RPI. He can be reached at doug.mercer@analog.com.

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Antoniu Miclaus is a system applications engineer at Analog Devices, where he works on ADI academic programs, as well as embedded software for Circuits from the Lab®, QA automation, and process management. He started working at Analog Devices in February 2017 in Cluj-Napoca, Romania. He is currently an M.Sc. student in the software engineering master's program at Babes-Bolyai University and he has a B.Eng. in electronics and telecommunications from Technical University of Cluj-Napoca. He can be reached at antoniu.miclaus@analog.com.