SBOS214B – SEPTEMBER 2001 – REVISED JULY 2004

4-Channel, Rail-to-Rail, CMOS BUFFER AMPLIFIER

FEATURES

- UNITY GAIN BUFFER
- RAIL-TO-RAIL INPUT/OUTPUT
- WIDE BANDWIDTH: 8MHz
- HIGH SLEW RATE: 10V/µs
- LOW QUIESCENT CURRENT: 1.1mA
- TINY PACKAGE: MSOP-10, TSSOP-14

APPLICATIONS

- TFT-LCD REFERENCE DRIVERS
- NOTEBOOKS
- ELECTRONIC GAMES
- ELECTRONIC BOOKS
- PERSONAL COMMUNICATION DEVICES
- PDA
- ACTIVE FILTERS
- ADC/DAC BUFFER

DESCRIPTION

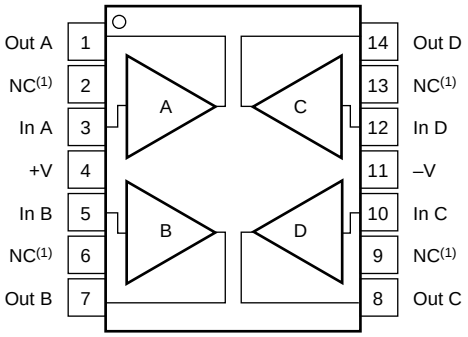
The BUF04701 is a 4-channel, low-power, high-voltage rail-to-rail input/output buffer. Operating on supplies ranging from 3.5V to 12V (±1.75V to ±6V), the BUF04701 has a 3dB bandwidth of 8MHz with a slew rate of 10V/µs, and requires only 1.1mA quiescent current. The BUF04701 features rail-to-rail input and output capability, giving maximum dynamic range at any supply voltage.

Featuring fast slewing and settling times, as well as a high output drive, the BUF04701 is ideal for use as a voltage reference buffer in Thin Film Transistor Liquid Crystal Displays (TFT-LCDs).

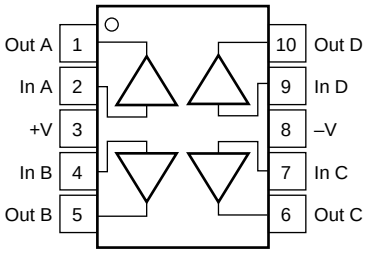
The BUF04701 is available in an MSOP-10 package, providing the smallest footprint and thinnest package option available, as well as the TSSOP-14 package with a pinout that corresponds to standard quad op amps. This makes it easy to replace quad op amps in existing LCD displays with the low cost BUF04701, without changing the layout. The BUF04701 operates over a temperature range of –40°C to +125°C.

BUF04701 RELATED PRODUCTS

FEATURES	PRODUCT
1.2 MHz BW, 3.3mA I_Q	BUF11702
7MHz GBW, 1.5mA I_Q, V_S 3.5 - 12	OPA4743
5.9MHz GBW, 4.5mA I_Q, V_S = 4V - 44V	TLE2144/2
10MHz GBW, 2.5mA I_Q, 16V/µs SR	TLC084



TSSOP-14 (PW)



MSOP-10 (DGS)

NOTE: (1) NC Means No Internal Connection

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	13.2V
Signal Input Terminals, Voltage[2]	(V–) –0.5V to (V+) + 0.5V
Current[2]	10mA
Output Short-Circuit[3]	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
Quad						
BUF04701	MSOP-10	DGS	–40°C to +125°C	BUF04701	BUF04701AIDGSR	Tape and Reel, 2500
BUF04701	TSSOP-14	PW	–40°C to +125°C	04701A	BUF04701AIPWR	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ELECTRICAL CHARACTERISTICS: V_S = +3.5V to +12V

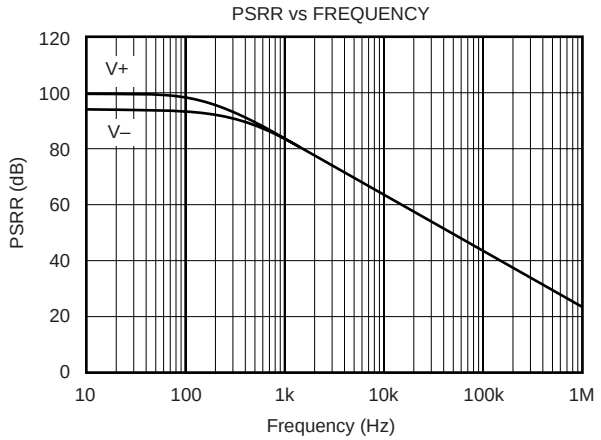
Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C**

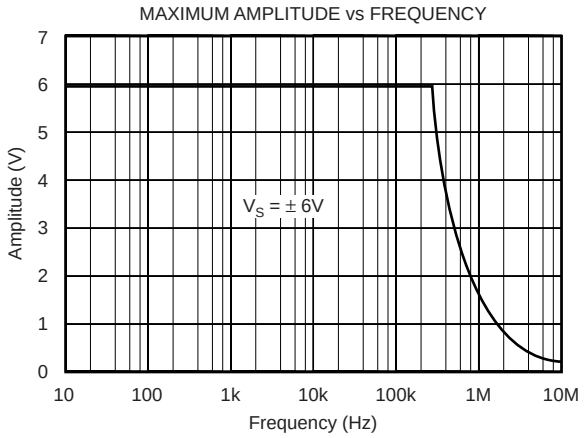
At T_A = +25°C, R_L = 10kΩ connected to V_S/2 and V_{OUT} = V_S/2, unless otherwise noted.

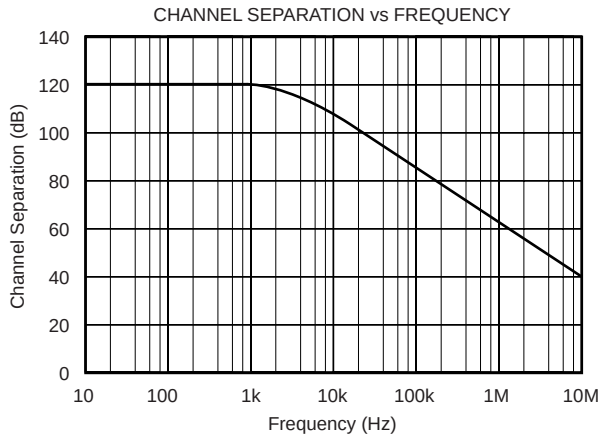
PARAMETER		CONDITION	BUF04701 MIN	BUF04701 TYP	BUF04701 MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±5, V_{CM} = 0		±1.5	±7	mV
Drift	**dV_{OS}/dT**			**±8**		**µV/°C**
vs Power Supply	PSRR	V_S = 3.5V to 12V, V_{CM} = V_S/2 – 0.5V		20	100	µV/V
Over Temperature		**V_S = 3.5V to 12V, V_{CM} = V_S/2 – 0.5V**			**200**	**µV/V**
Channel Separation, DC				1		µV/V
f = 10kHz				110		dB
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}			Limited by Output Range		
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_{CM} = V_S/2		1	±10	pA
INPUT IMPEDANCE						
Common-Mode				$5 \cdot 10^{12}$ || 4		Ω || pF
NOISE						
Input Voltage Noise, f = 0.1Hz to 10Hz		V_S = ±6V, V_{CM} = 0		11		µVrms
Input Voltage Noise Density, f = 10kHz	e_n	V_S = ±6V, V_{CM} = 0		30		nV/√Hz
Input Current Noise Density, f = 1kHz	i_n	V_S = ±6V, V_{CM} = 0		2.5		fA/√Hz
TRANSFER CHARACTERISTIC						
Gain			0.9975	1.000	1.0025	
over Temperature			**0.995**	**1.000**	**1.005**	
OUTPUT						
Voltage Output Swing from Rail		R_L = 10kΩ		75		mV
		R_L = 2kΩ		150	200	mV
over Temperature		**R_L = 2kΩ**			**250**	**mV**
Short-Circuit Current	I_{SC}			±32		mA
FREQUENCY RESPONSE		C_L = 10pF				
Bandwidth –3dB	BW			8		MHz
Slew Rate	SR	V_S = ±6V		10		V/µs
Settling Time, 0.1%	t_S	V_S = ±6V, 5V Step		9		µs
Overload Recovery Time		V_{IN} = V_S		0.2		µs
Total Harmonic Distortion + Noise	THD+N	V_S = ±6V, V_O = 1Vrms, G = 1, f = 6kHz, V_{CM} = V_S/2		0.001		%
POWER SUPPLY						
Specified Voltage Range, Single Supply	V_S		3.5		12	V
Specified Voltage Range, Dual Supplies			±1.75		±6	V
Operating Voltage Range				+3.5 to +12		V
Quiescent Current (per amplifier)	I_Q	I_O = 0		1.1	1.5	mA
over Temperature					**1.7**	**mA**
TEMPERATURE RANGE						
Specified Range			–40		+125	°C
Operating Range			–40		+125	°C
Storage Range			–65		+150	°C
Thermal Resistance	θ_{JA}					
TSSOP Surface Mount				100		°C/W
MSOP Surface Mount				200		°C/W

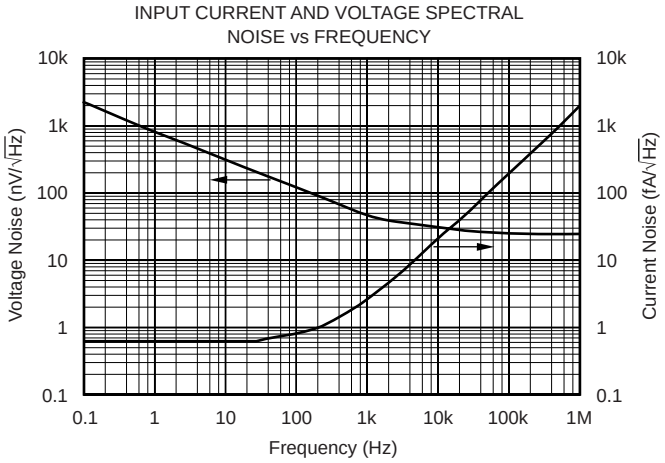
TYPICAL CHARACTERISTICS

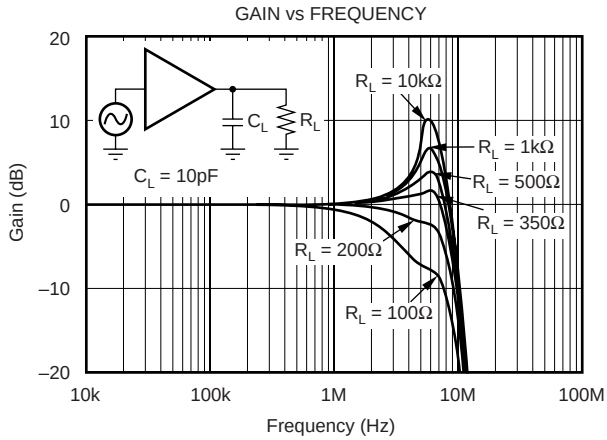
At T_A = +25°C, V_S = ±6V, and R_L = 10kΩ, unless otherwise noted.

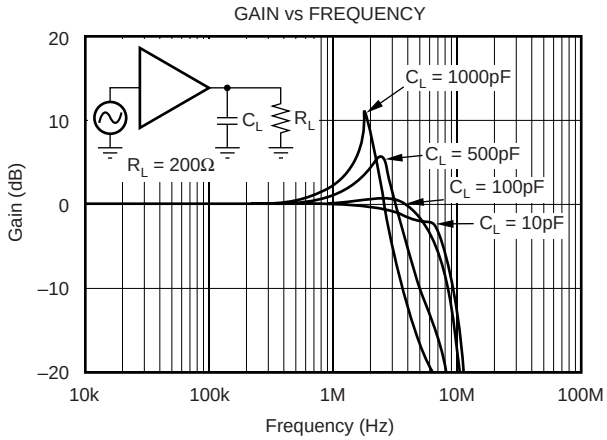






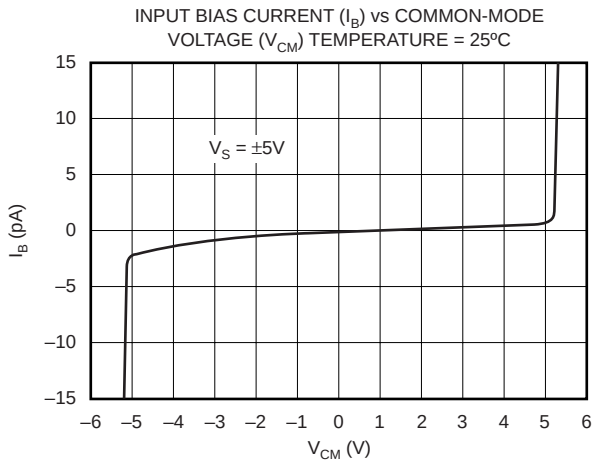


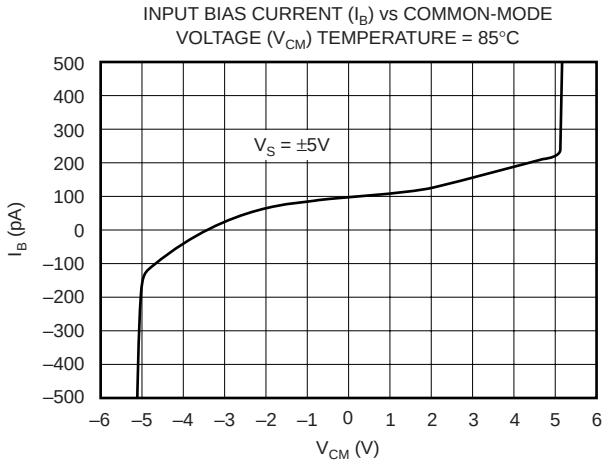


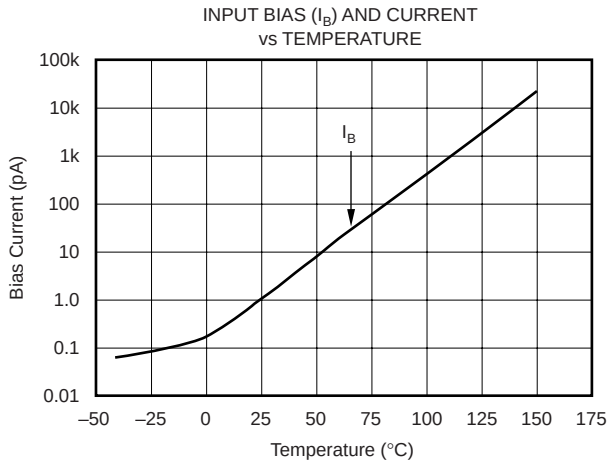


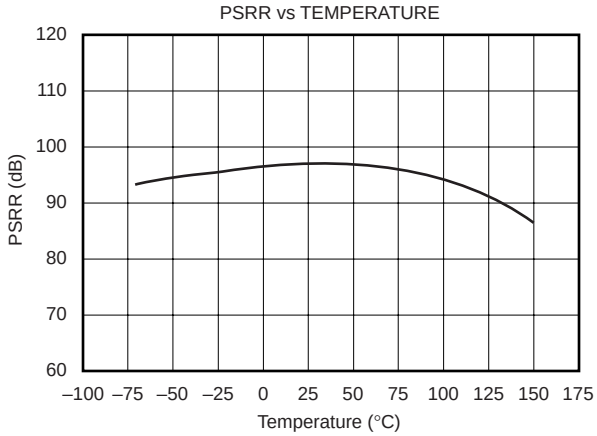
TYPICAL CHARACTERISTICS (Cont.)

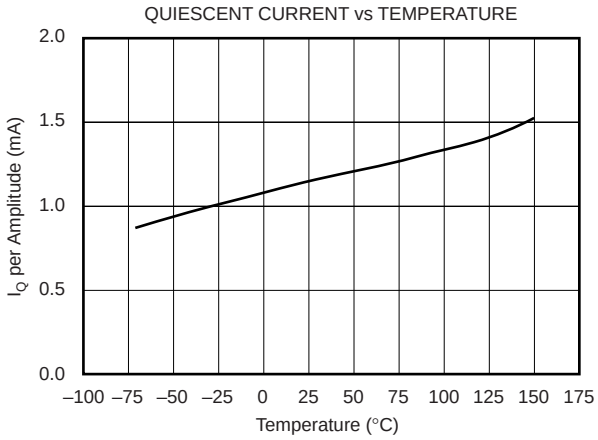
At T_A = +25°C, V_S = ±6V, and R_L = 10kΩ, unless otherwise noted.

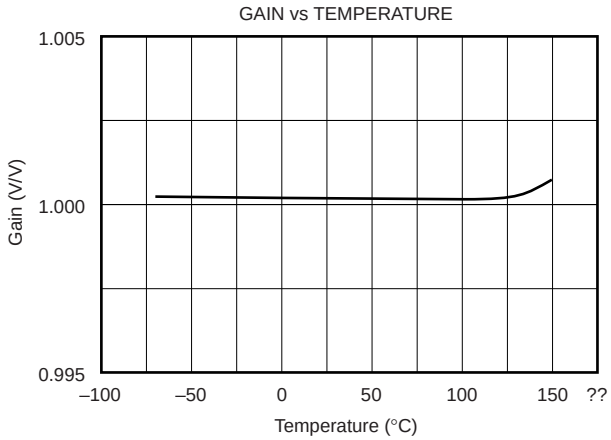






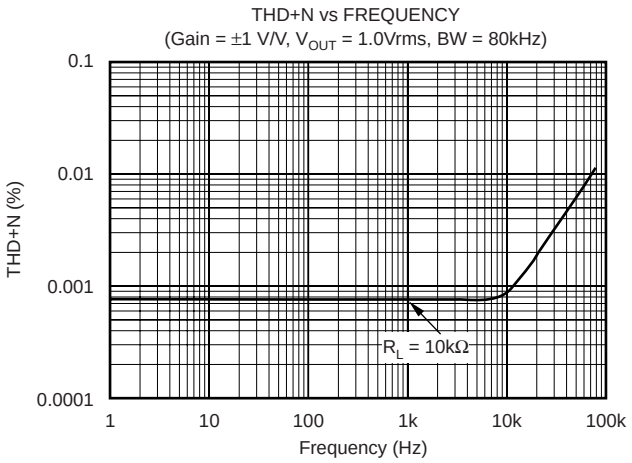


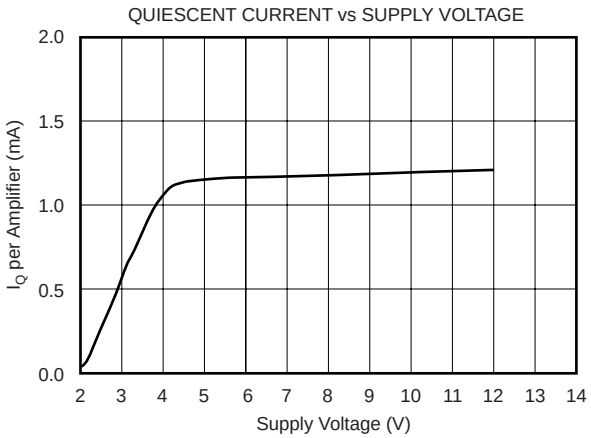


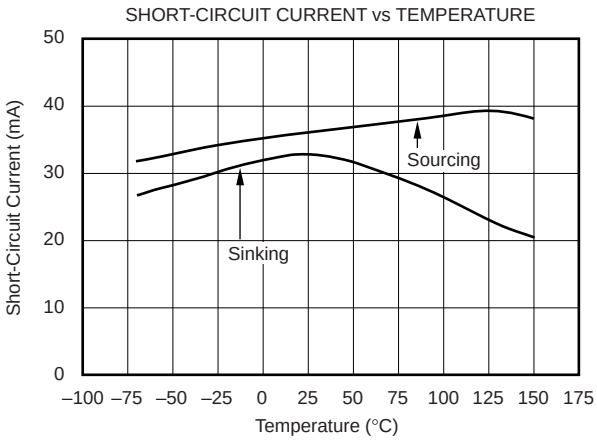


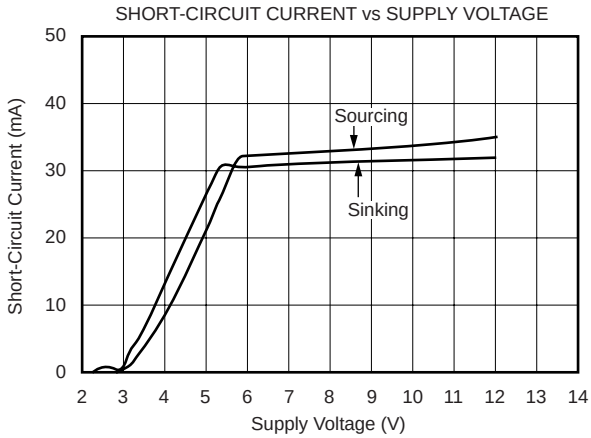
TYPICAL CHARACTERISTICS (Cont.)

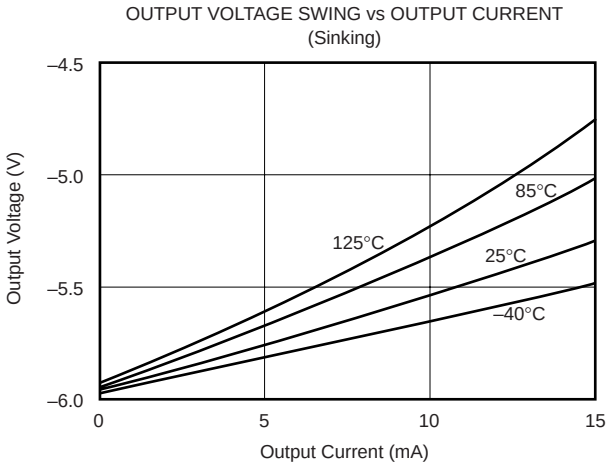
At T_A = +25°C, V_S = ±6V, and R_L = 10kΩ, unless otherwise noted.

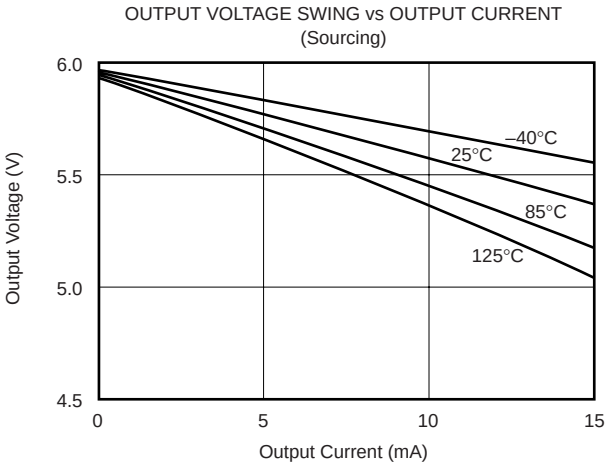








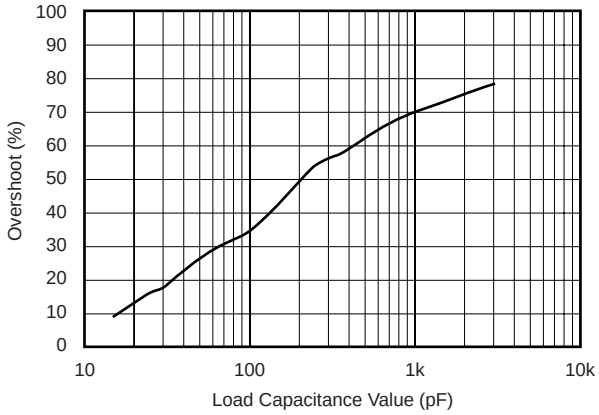




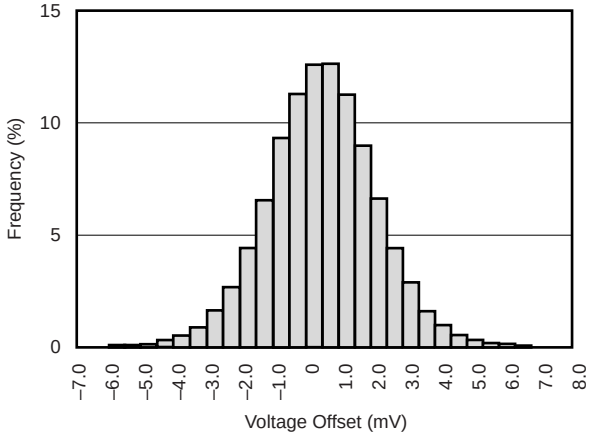
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = ±6V, and R_L = 10kΩ, unless otherwise noted.

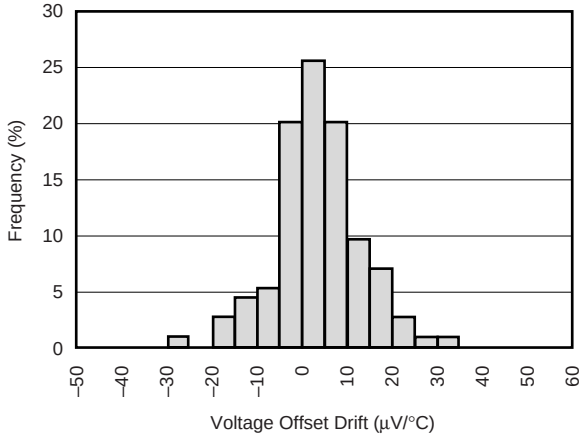
OVERSHOOT (%) vs CAPACITANCE



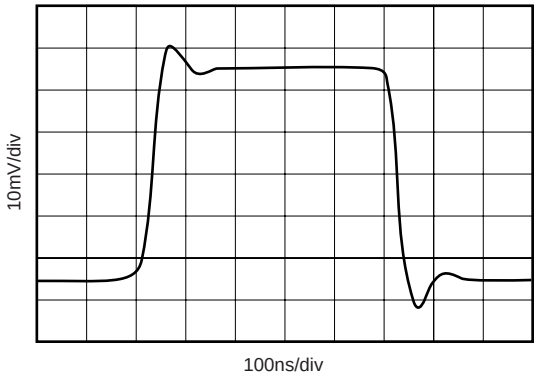
V_{OS} PRODUCTION DISTRIBUTION



V_{OS} DRIFT DISTRIBUTION



SMALL SIGNAL STEP RESPONSE
(G = +1V/V, R_L = 10kΩ, C_L = 15pF)



LARGE SIGNAL STEP RESPONSE
(G = +1V/V, R_L = 10kΩ, C_L = 15pF)

APPLICATIONS INFORMATION

Figure 1 shows the BUF04701 connected as a buffer. Power supplies should be bypassed with capacitors connected close to the device pins. Capacitor values as low as 0.1µF will assure stable operation in most applications, but high output current and fast output slewing can demand large current transients from the power supplies.

Rail-to-rail input and output swing helps maintain dynamic range, especially in low supply applications. Figure 2 shows the input and output waveforms for the BUF04701. On a ±6V supply with a 100kΩ load connected to $V_S/2$, the output is tested to swing within 50mV to the rail.

OPERATING VOLTAGE

The BUF04701 is fully specified and tested from 3.5V to 12V over a temperature range of –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristic Curves.

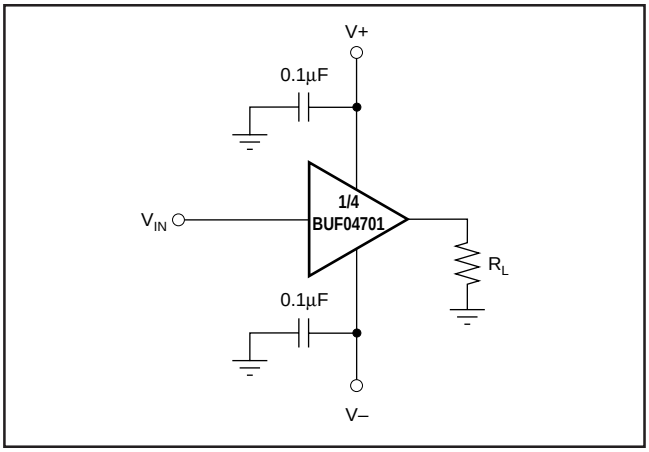


FIGURE 1. Basic Connections.

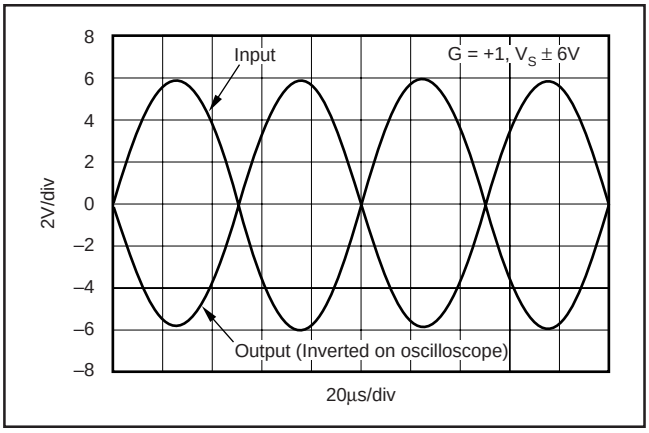


FIGURE 2. Rail-to-Rail Input and Output.

RAIL-TO-RAIL INPUT

The input common-mode voltage range of the BUF04701 extends 100mV beyond the supply rails at room temperature; however, due to the fixed gain at G = 1, the output will limit the useable input range. This wide swing is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 2.0V to 100mV above the positive supply, while the P-channel pair is on for inputs from 100mV below the negative supply to approximately (V+) – 1.5V. There is a small transition region, typically (V+) – 2.0V to (V+) – 1.5V, in which both pairs are on. This 500mV transition region can vary ±100mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 2.1V to (V+) – 1.4V on the low end, up to (V+) – 1.9V to (V+) – 1.6V on the high end.

INPUT PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than approximately 300mV. Momentary voltages greater than 300mV beyond the power supply can be tolerated if the current is limited to 10mA. This is easily accomplished with an input resistor, in series with the buffer input shown in Figure 3. Many input signals are inherently current-limited to less than 10mA; therefore, a limiting resistor is not always required. The BUF04701 features no phase inversion when the inputs extend beyond supplies if the input current is limited, as shown in Figure 4.

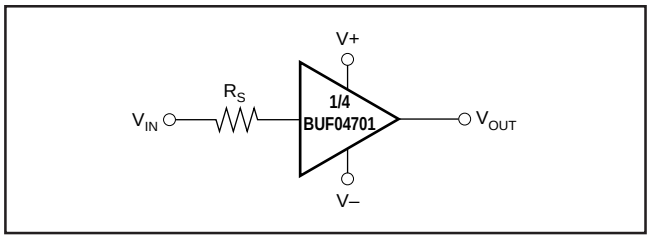


FIGURE 3. Limiting Input Current on the BUF04701.

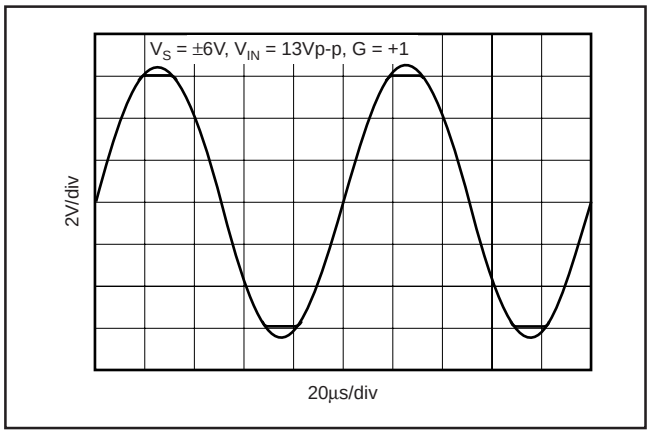


FIGURE 4. BUF04701—No Phase Inversion with Inputs Greater than the Power-Supply Voltage.

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving 1kΩ loads connected to any point between V+ and V–. For light resistive loads (> 100kΩ), the output voltage can swing to 100mV from the supply rail. With 2kΩ resistive loads, the output is specified to swing to within 200mV of the supply rails while maintaining high open-loop gain (see the typical characteristic curve *Output Voltage Swing vs Output Current*).

CAPACITIVE LOAD AND STABILITY

The BUF04701 can drive up to 1000pF pure capacitive load. One method of improving capacitive load drive is to insert a 10 to 20Ω resistor in series with the output, as shown in Figure 5. This reduces ringing with large capacitive loads while maintaining DC accuracy.

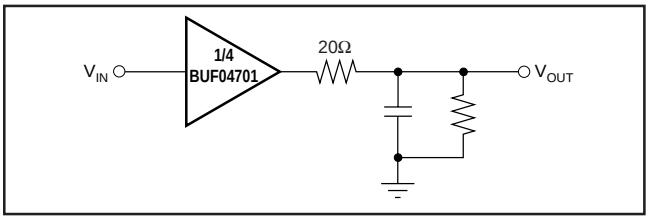


FIGURE 5. Improving Capacitive Load Drive.

APPLICATION CIRCUITS

REFERENCE BUFFER FOR LCD SOURCE DRIVERS

In modern high-resolution TFT-LCD displays, gamma correction must be performed to correct for nonlinearities in the glass transmission characteristics of the LCD panel. The typical LCD source driver for 64 bits of grayscale uses internal Digital-to-Analog Converters (DACs) to convert the 6-bit data into analog voltages applied to the LCD. These DACs typically require external voltage references for proper operation. Normally these external reference voltages are generated using a simple resistive ladder, like the one shown in Figure 6.

Typical laptop or desktop LCD panels require 6 to 8 of the source driver circuits in parallel to drive all columns of the panel. Although the resistive load of one internal string of a DAC is only around 10kΩ to 16kΩ, 6 to 8 strings in parallel represent a very substantial load. The power supply used for the LCD source drivers for laptops is typically in the order of 10V. To maximize the dynamic range of the DAC, rail-to-rail

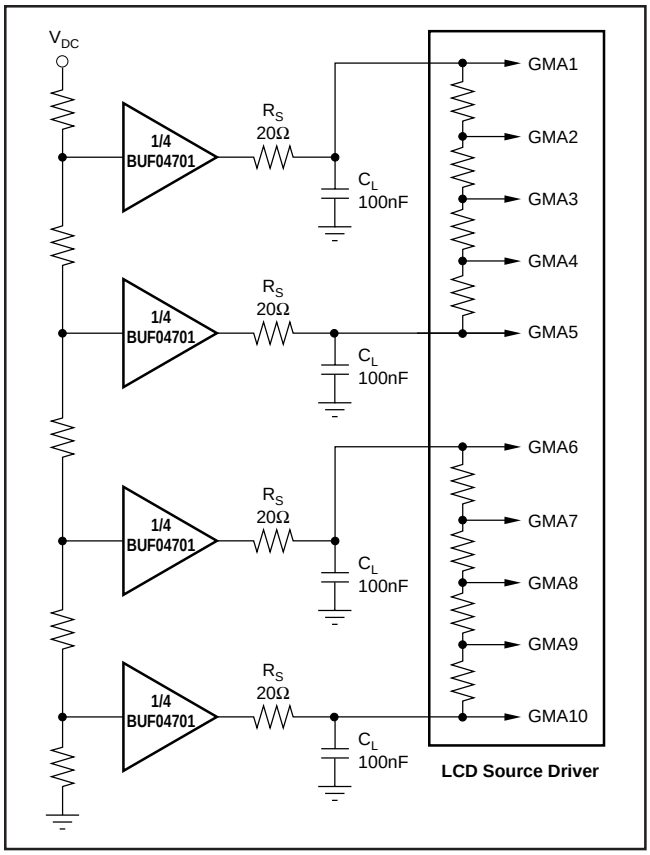


FIGURE 6. BUF04701 as LCD Display Buffer.

output performance is required for the upper and lower buffer. The ability of the BUF04701 to operate on 12V supplies, to drive heavy resistive loads (as low as 2kΩ), and to swing to within 200mV of the supply rails, makes it very well suited as a buffer for the reference voltage inputs of LCD source drivers.

During conversion of the DAC, internal switches create current glitches on the output of the reference buffer. The capacitor C_L (typically 100nF) functions as a charge reservoir that provides/absorbs most of the glitch energy. The series resistor R_S isolates the outputs of the BUF04701 from the heavy capacitive load and helps to improve settling time.

4-POLE LOW-PASS SALLEN-KEY FILTER

The high open-loop gain and wide bandwidth of the BUF04701 make it optimal for active filtering applications. Figure 7 shows the BUF04701 in a 4-pole Butterworth low-pass active filter configuration of 20kHz bandwidth.

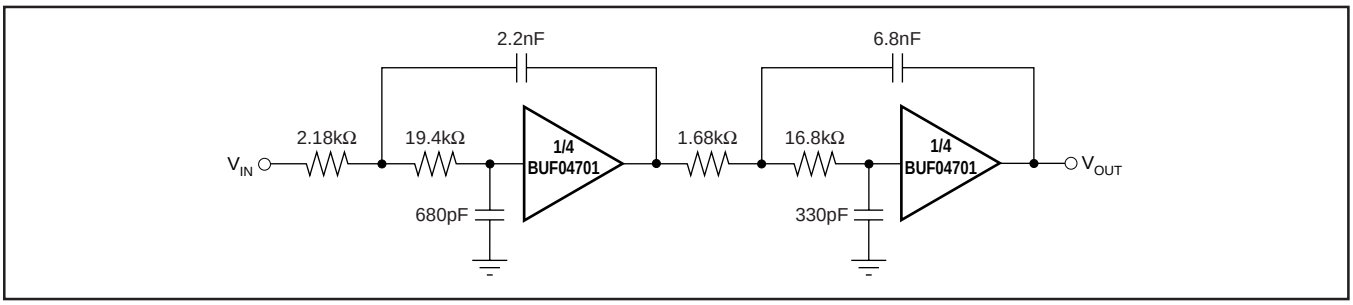


FIGURE 7. BUF04701 Configured as a 4-Pole Sallen-Key Butterworth Low-Pass Filter.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BUF04701AIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	B01	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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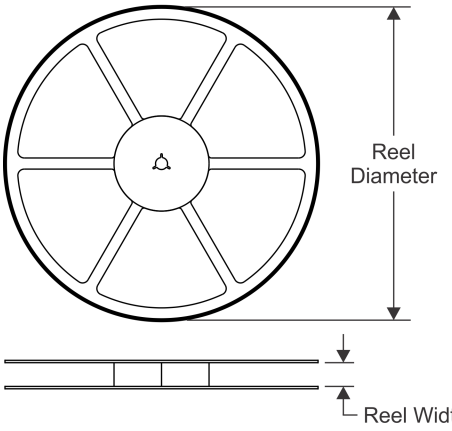
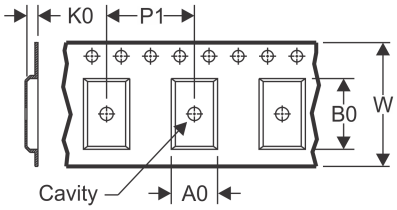
TAPE AND REEL INFORMATION

REEL DIMENSIONS

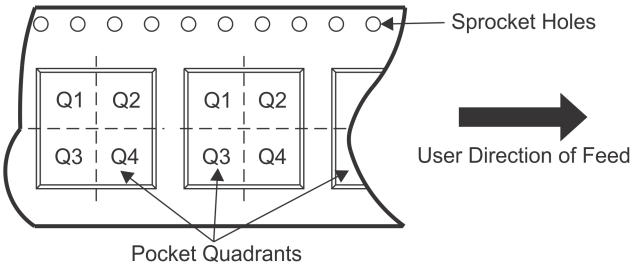


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

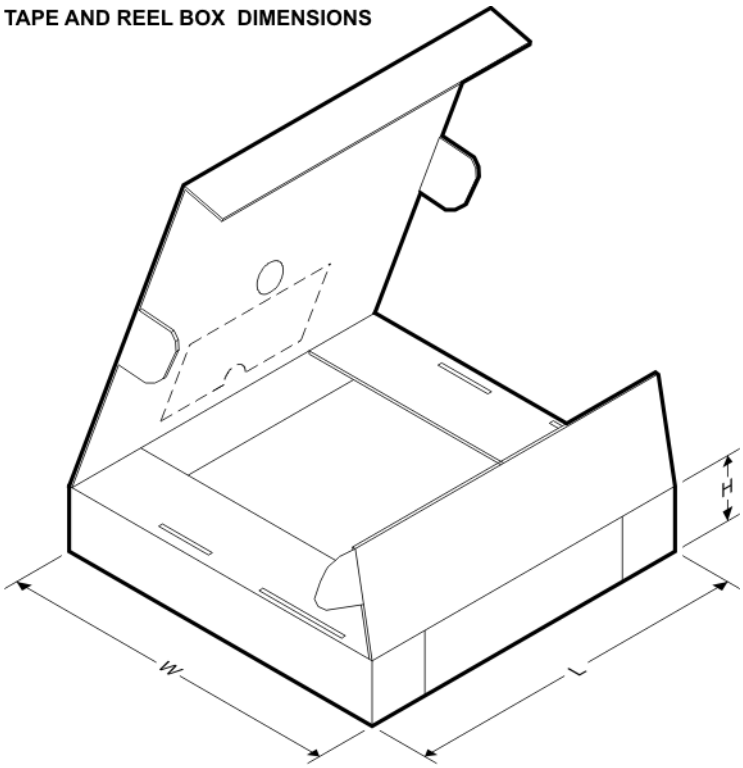
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

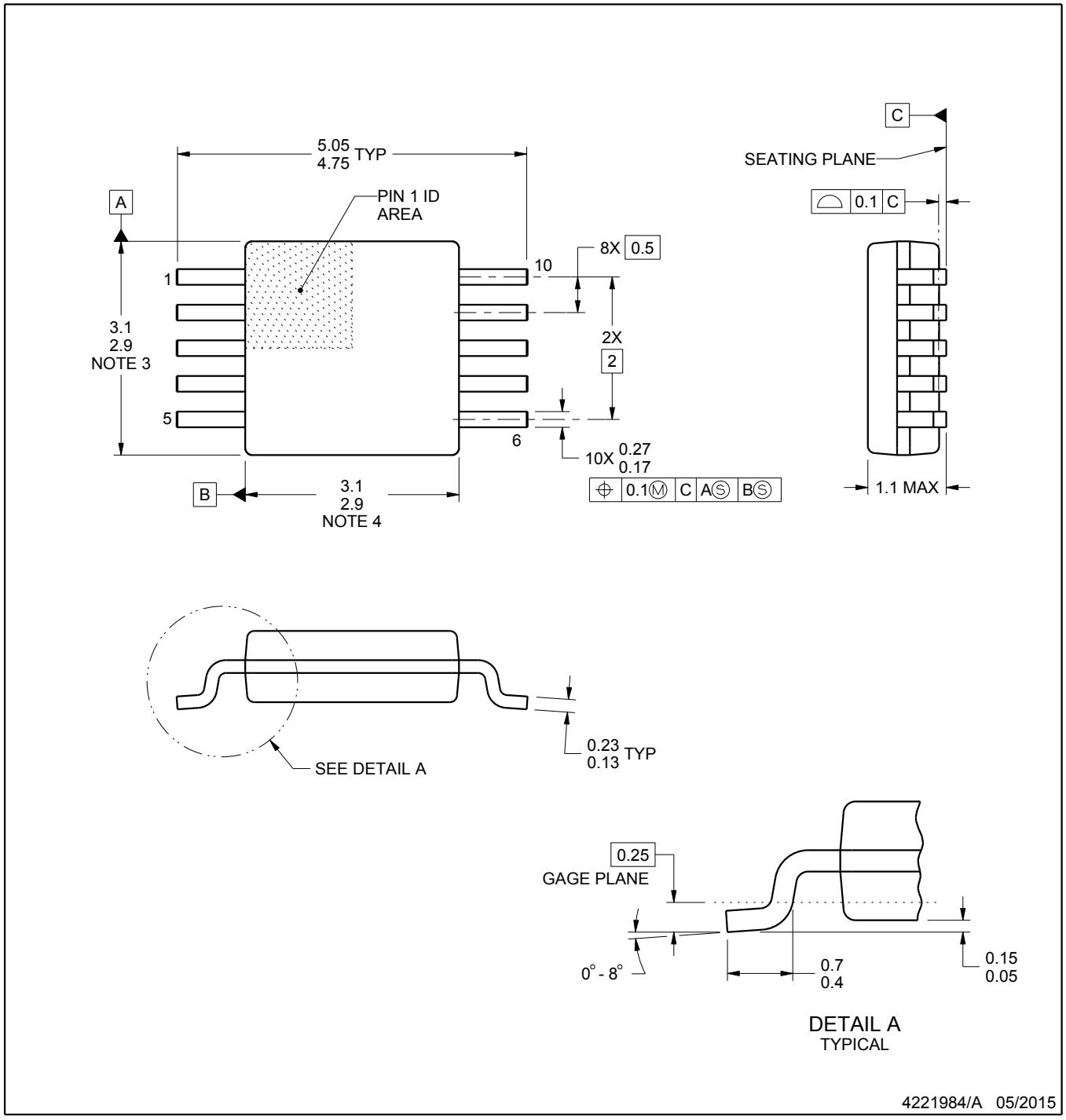
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF04701AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



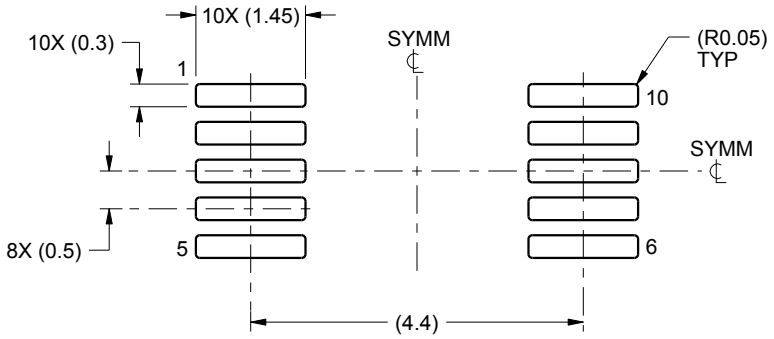
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF04701AIDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0

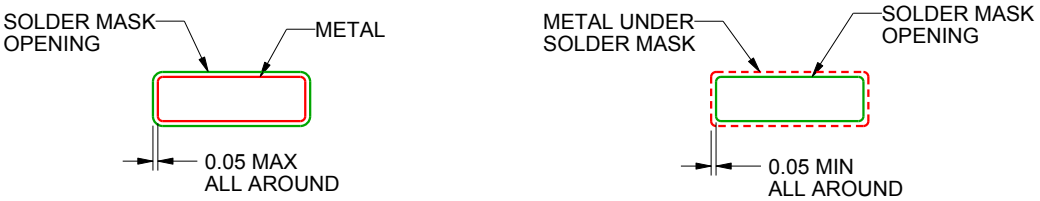


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

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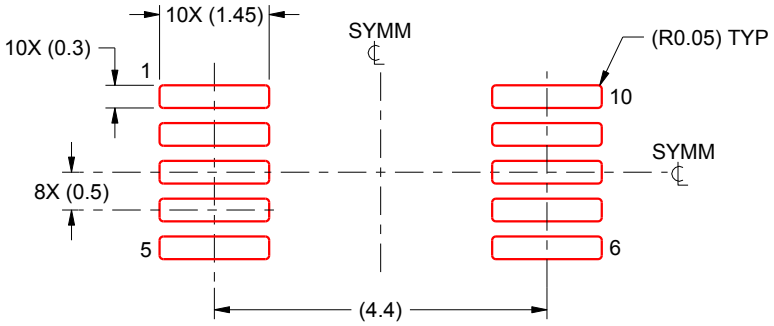
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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