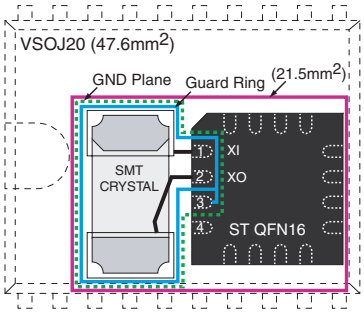
M41T60

Low-power serial real-time clock (RTC)

Datasheet - production data



QFN16
3 mm x 3 mm



Footprint comparison of ST's QFN16 with SMT crystal vs. competing VSOJ20 package

Features

- Counters for seconds, minutes, hours, day, date, month, years, and century
- 32 KHz crystal oscillator integrating load capacitance and high crystal series resistance operation
- Oscillator stop detection monitors clock operation
- Serial interface supports I^2C bus (400 kHz)
- 350 nA timekeeping current at 3 V
- Low operating current of 35 µA (at 400 kHz)
- Timekeeping down to 1.0 V
- 1.3 V to 4.4 V I^2C bus operating voltage
- Software clock calibration to compensate deviation of crystal due to temperature
- Software programmable output (OUT)
- Operating temperature of –40 to 85 °C
- Automatic leap year compensation
- Lead-free 16-pin QFN package
- Li-ion rechargeable operation

This is information on a product in full production. www.st.com

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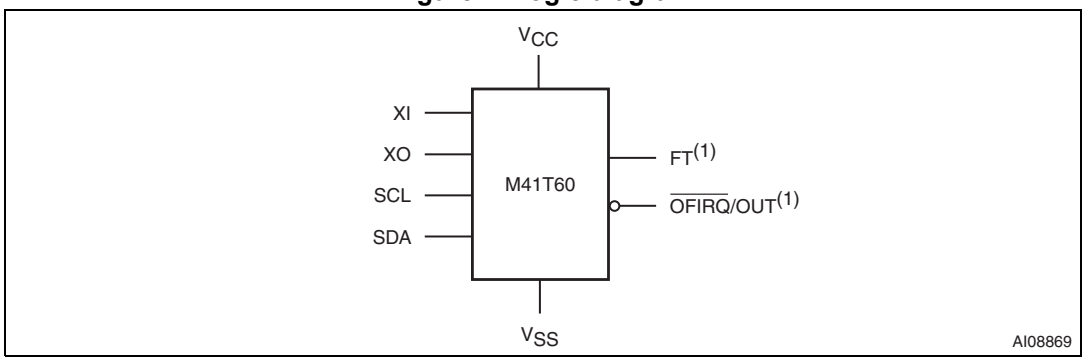
1 Description

The M41T60 is a low-power serial real-time clock (RTC) with a built-in 32.768 kHz oscillator (external crystal controlled). Eight registers are used for the clock/calendar function and are configured in binary-coded decimal (BCD) format. Addresses and data are transferred serially via a two-line, bidirectional bus. The built-in address register is increased automatically after each WRITE or READ data byte.

The eight clock address locations contain the century, year, month, date, day, hour, minute, and second in 24-hour BCD format. Corrections for 28-, 29- (leap year), 30-, and 31-day months are made automatically.

The M41T60 is supplied in a 16-lead QFN package.

Figure 1. Logic diagram



1. Open drain

Table 1. Signal names

XI	Oscillator input
XO	Oscillator output
FT	Frequency test output (open drain)
SDA	Serial data address input/output
SCL	Serial clock
$\overline{\text{OFIRQ}}$/OUT	Oscillator fail interrupt/out output (open drain)
V_{CC}	Supply voltage
V_{SS}	Ground

Figure 2. 16-pin QFN connections

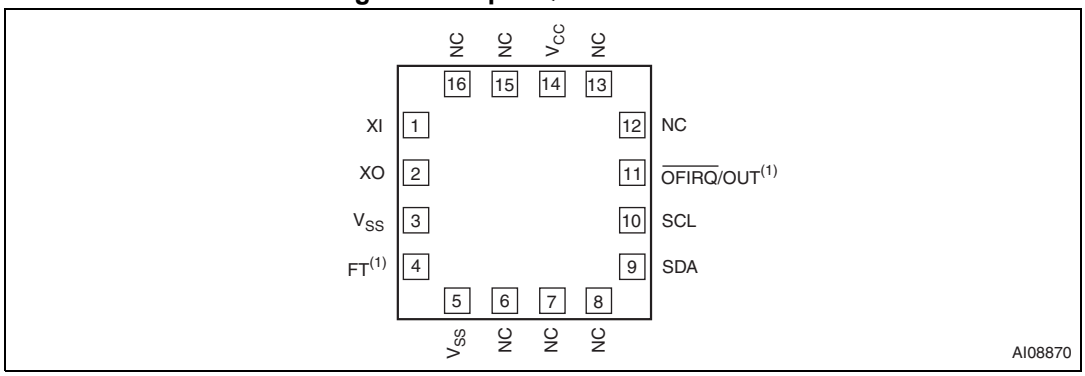
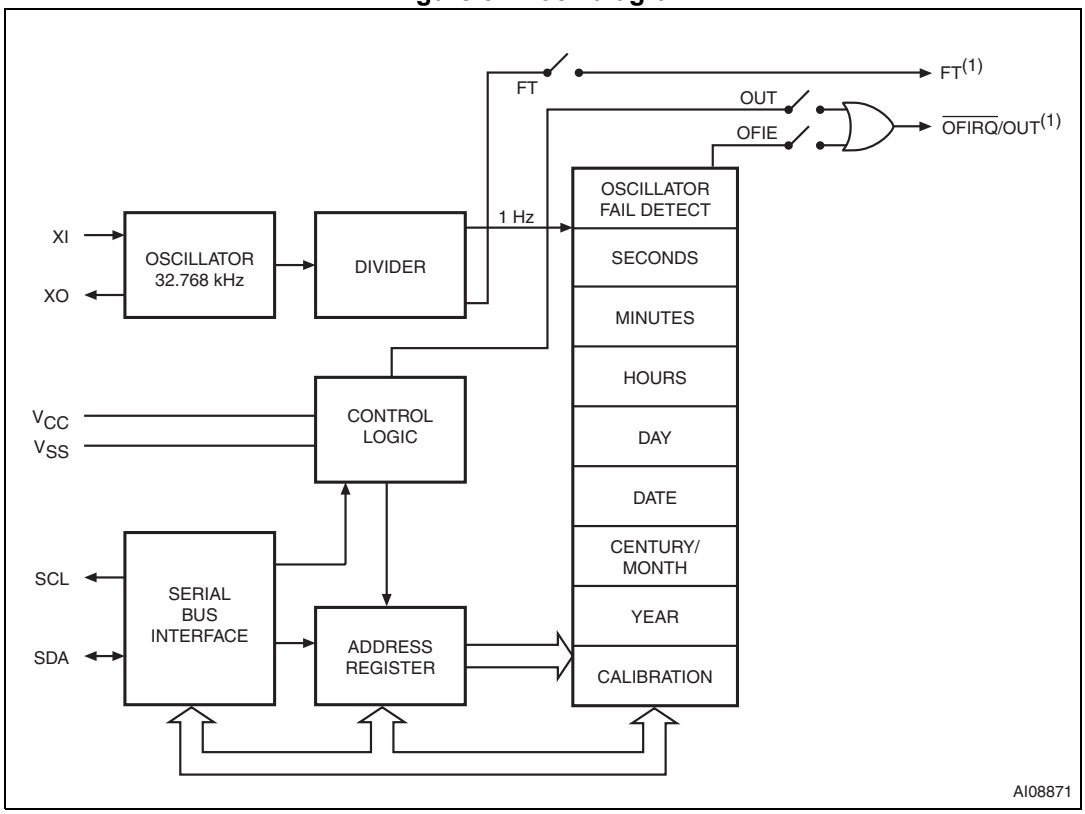
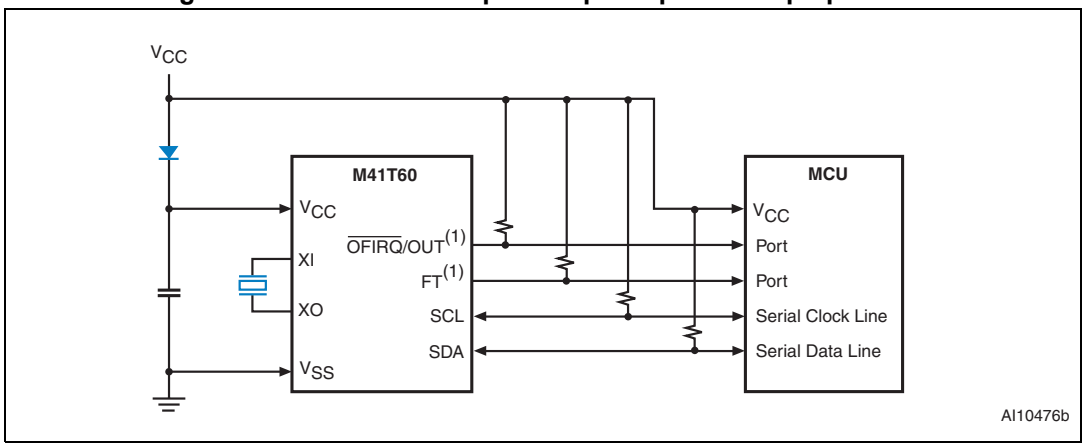


Figure 3. Block diagram



1. Open drain output.

Figure 4. Hardware hookup for SuperCap™ backup operation



1. Open drain output.

2 Operation

The M41T60 clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 8 bytes contained in the device can then be accessed sequentially in the following order:

1. Seconds register
2. Minutes register
3. Hours register
4. Day register
5. Date register
6. Century/month register
7. Years register
8. Calibration register

2.1 2-wire bus characteristics

This bus is intended for communication between different ICs. It consists of two lines: one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

2.1.1 Bus not busy

Both data and clock lines remain high.

2.1.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

2.1.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

2.1.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition, a device that gives out a message is called “transmitter”, the receiving device that gets the message is called “receiver”. The device that controls the message is called “master”. The devices that are controlled by the master are called “slaves”.

2.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 5. Serial bus data transfer sequence

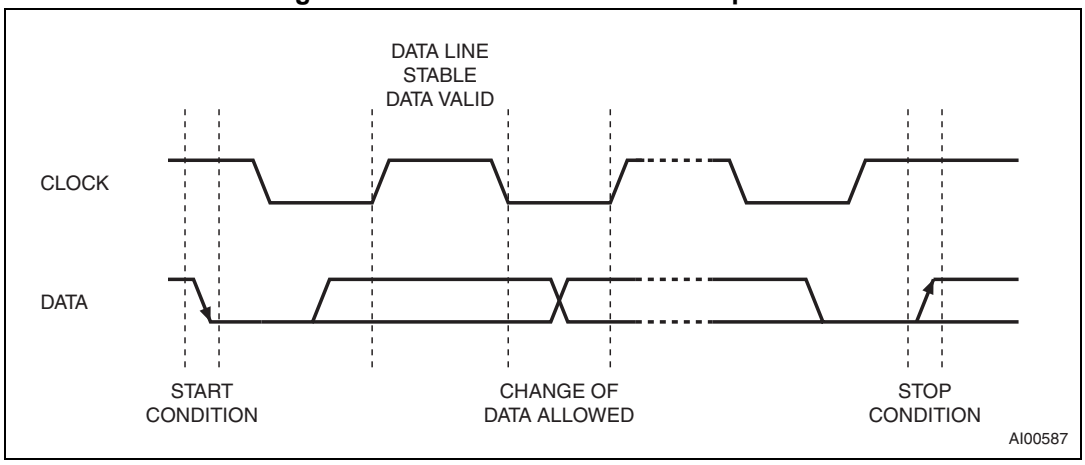
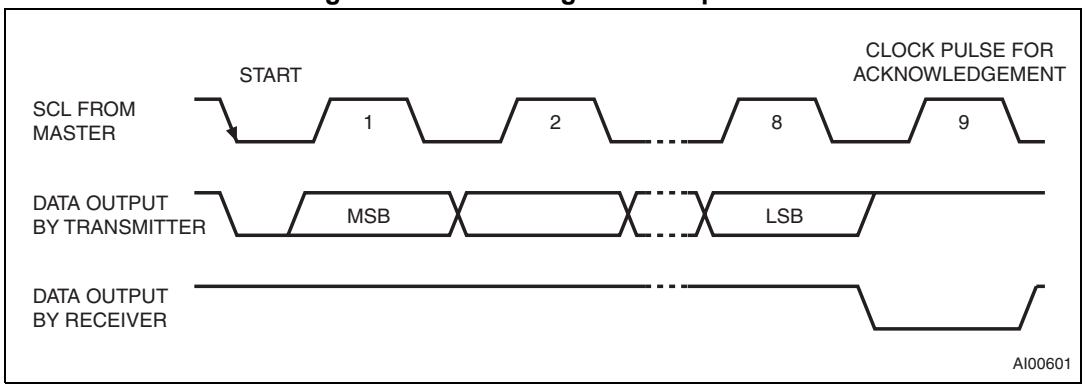


Figure 6. Acknowledgement sequence



2.2 READ mode

In this mode, the master reads the M41T60 slave after setting the slave address (see *Figure 7*). Following the WRITE mode control bit (R/$\overline{W}$ = 0) and the acknowledge bit, the word address An is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit (R/$\overline{W}$ = 1). At this point, the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only increased on reception of an acknowledge bit. The M41T60 slave transmitter will now place the data byte at address A_{n+1} on the bus. The master receiver reads and acknowledges the new byte and the address pointer is increased to A_{n+2}.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (0h to 6h). The update will resume due to a stop condition or when the pointer increments to any non-clock address (7h).

An alternate READ mode may also be implemented, whereby the master reads the M41T60 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 9 on page 11*).

Figure 7. Slave address location

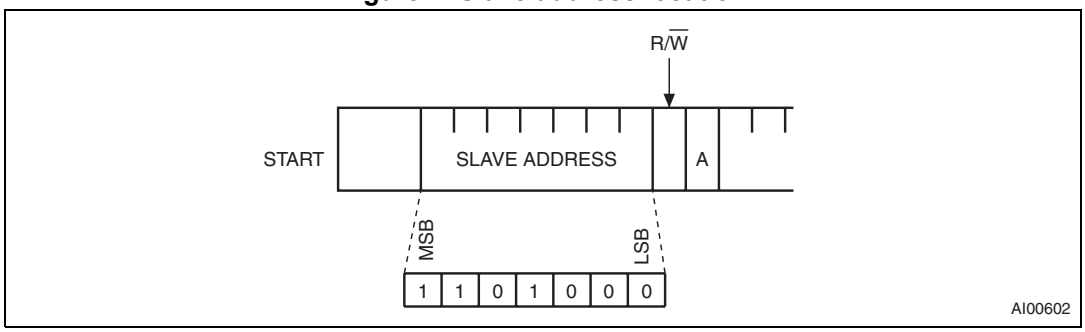


Figure 8. READ mode sequence

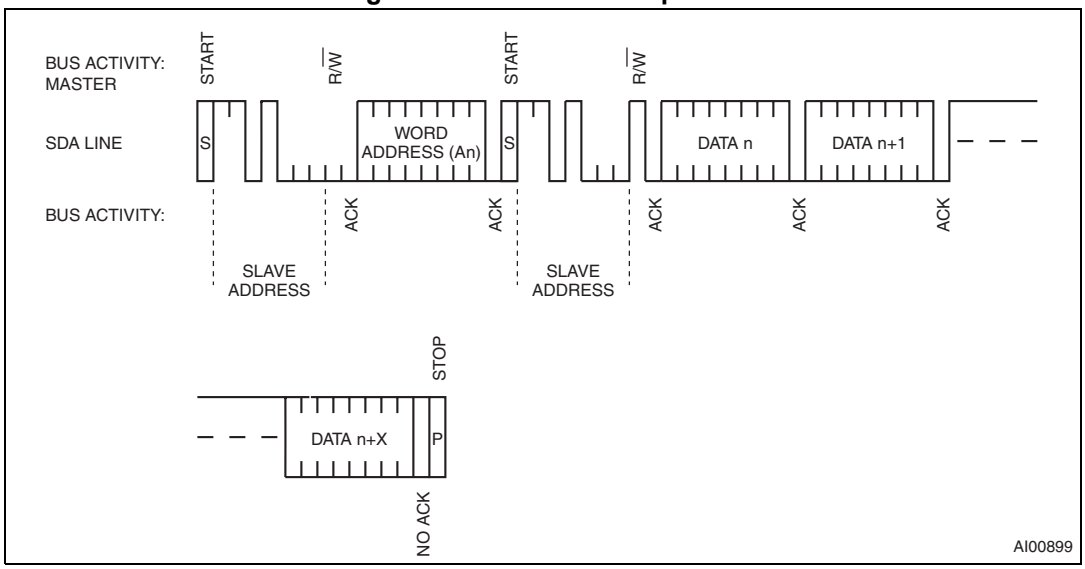
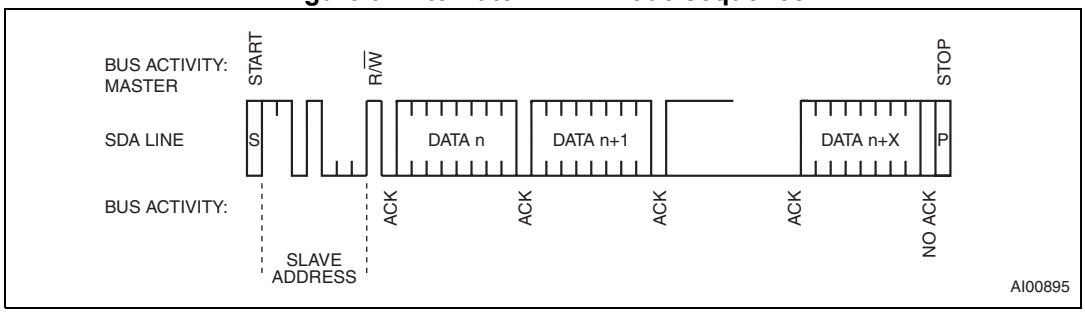


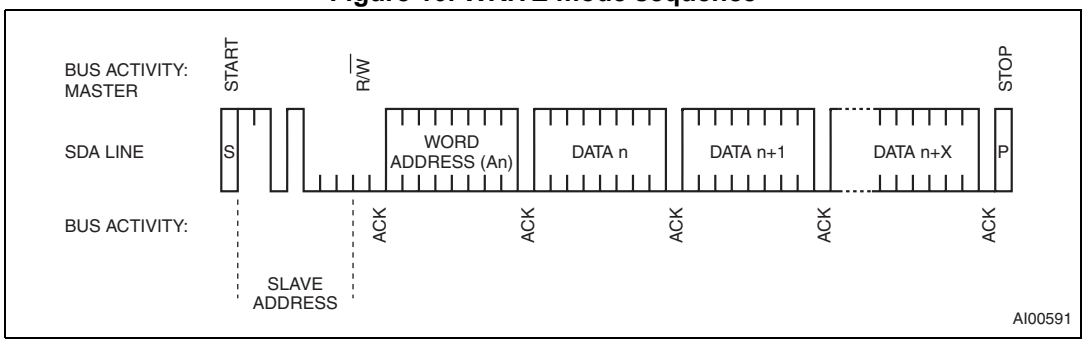
Figure 9. Alternate READ mode sequence



2.3 WRITE mode

In this mode the master transmitter transmits to the M41T60 slave receiver. Bus protocol is shown in *Figure 10 on page 12*. Following the START condition and slave address, a logic '0' (R/$\overline{W}$ = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is increased to the next address location on the reception of an acknowledge clock. The M41T60 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte.

Figure 10. WRITE mode sequence



3 Clock operation

The M41T60 is driven by a quartz-controlled oscillator with a nominal frequency of 32.768 kHz. The accuracy of the real-time clock depends on the frequency of the quartz crystal that is used as the time-base for the RTC. The eight-byte clock register (see *Table 2 on page 15*) is used to both set the clock and to read the date and time from the clock, in a binary-coded decimal format. Seconds, minutes, and hours are contained within the first three registers.

Bits D6 and D7 of clock register 05h (century/month register) contain the century bit 0 (CB0) and the century bit 1 (CB1). See *Table 3 on page 16* for additional explanation. Bits D0 through D2 of register 03h contain the day (day of the week). Registers 04h, 05h, and 06h contain the date (day of the month), century/month, and years. The eighth clock register is the calibration register (this is described in the clock calibration section). Bit D7 of register 00h contains the stop bit (ST). Setting this bit to a '1' will cause the oscillator to stop. When reset to a '0,' the oscillator restarts within one second (typical).

Note: Upon initial power-up, the user should set the ST bit to a '1,' then immediately reset the ST bit to '0.' This provides an additional "kick-start" to the oscillator circuit.

Bit D7 of register 01h contains the oscillator fail interrupt enable bit (OFIE - see the description in the oscillator fail detection section).

Note: A WRITE to ANY location within the first seven bytes of the clock register (0h-6h), including the OFIE and ST bit, will result in an update of the system clock and a reset of the divider chain. This could result in an inadvertent change of the current time. These non-clock related bits should be written prior to setting the clock, and remain unchanged until such time as a new clock time is also written.

The seven clock registers may be read one byte at a time, or in a sequential block. The calibration register (address location 7h) may be accessed independently. A provision has been made to ensure that a clock update does not occur while any of the clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. this will prevent a transition of data during the READ.

3.1 Calibrating the clock

The M41T60 is driven by a quartz-controlled oscillator with a nominal frequency of 32,768 Hz. The accuracy of the clock is dependent upon the accuracy of the crystal, and the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. The M41T60 oscillator is designed for use with a 6 - 7 pF crystal load capacitance. When the calibration circuit is properly employed, accuracy improves to better than ±2 ppm at 25 °C.

The oscillation rate of crystals changes with temperature (see *Figure 11 on page 15*). The M41T60 design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 12 on page 16*. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the calibration register. Adding counts speeds the clock up, subtracting counts slows the clock down. The calibration bits occupy the five lower-order bits (D4-D0) in the calibration register 07h.

These bits can be set to represent any value between 0 and 31 in binary format. Bit D5 is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration.

Calibration occurs within a 64-minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64-minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on. Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles. That is, +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per day which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M41T60 may require:

- The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in application note AN934, “TIMEKEEPER® calibration.” This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the calibration byte.
- The second approach is better suited to a manufacturing environment, and involves the use of the frequency test (FT) pin. The FT pin will toggle at 512 Hz when the ST bit is set to '0,' and the OUT bit and FT bit are set to '1.' Any measured deviation from the 512 Hz frequency indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (XX001010) to be loaded into the calibration byte for correction.

Note: Setting or changing the calibration byte does not affect the frequency test output frequency. the FT pin is an open drain pin which requires a pull-up resistor to V_{CC} for proper operation. A 500-10 k resistor is recommended in order to control the rise time.

Table 2. Register map

Address	Data								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
0	ST	10 seconds			Seconds				Seconds	00-59
1	OFIE	10 minutes			Minutes				Minutes	00-59
2	0	0	10 hours		Hours				Hours	00-23
3	0	0	0	0	0	Day			Day	01-07
4	0	0	10 date		Date				Date	01-31
5	CB1	CB0	0	10 M.	Month				Century/month	0-3/01-12
6	10 Years				Years				Year	00-99
7	OUT	FT	S	Calibration					Calibration	

- 0 = Must be set to '0'
- CB0, CB1 = century bits
- FT = frequency test bits
- OFIE = oscillator fail interrupt enable bit
- OUT = output level
- S = sign bit
- ST = stop bit

Figure 11. Crystal accuracy across temperature

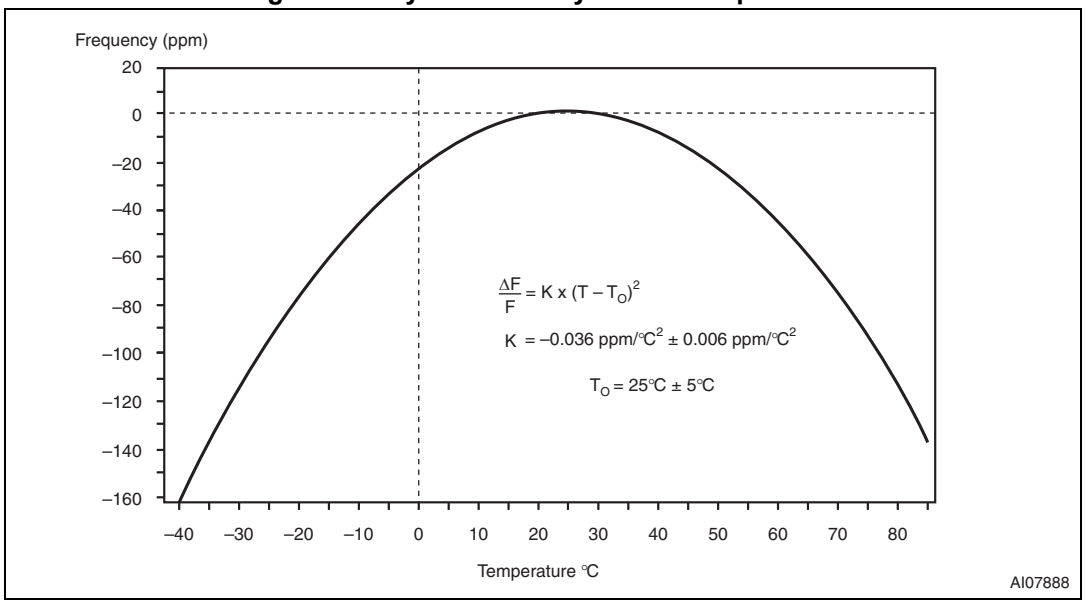
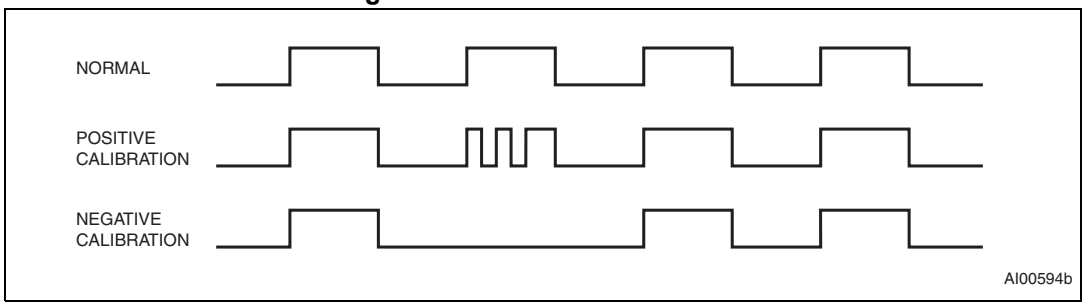


Figure 12. Calibration waveform



3.2 Century bits

The two century bits, CB1 and CB0, are bits D7 and D6, respectively, in the century/month register at address 06h. Together, they comprise a 2-bit counter which increments at the turn of each century. CB1 is the most significant bit.

The user may arbitrarily assign the meaning of CB1:CB0 to represent any century value, but the simplest way of using these bits is to extend the year register (07h) by mapping them directly to bits 9 and 8. (The reader is reminded that the year register is in BCD format.) Higher order year bits can be maintained in the application software.

Figure 13. Century bits CB1 and CB0

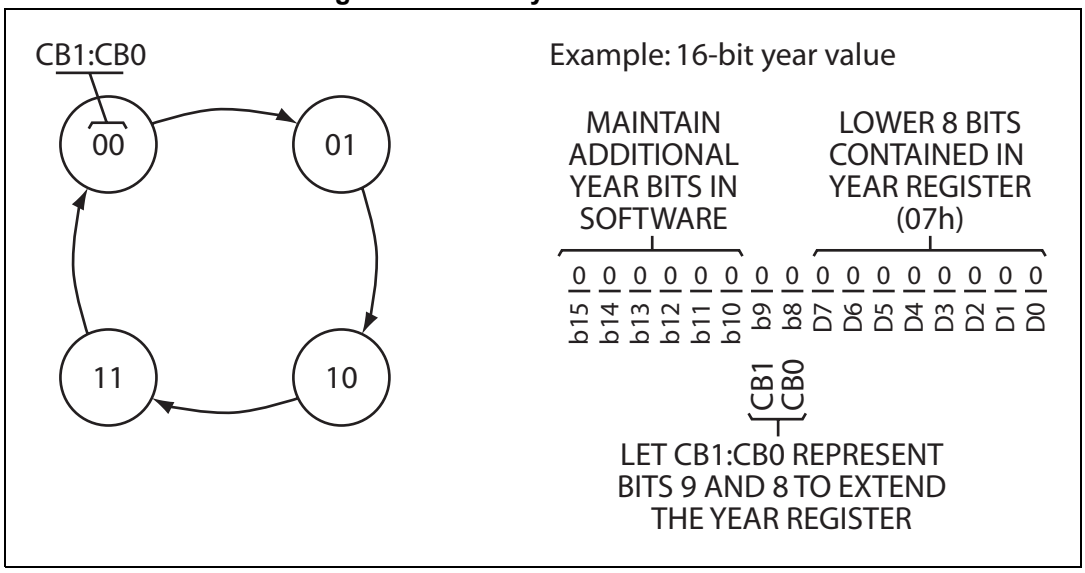


Table 3. Examples using century bits

CB1	CB0	CENTURY
0	0	2000
0	1	2100
1	0	2200
1	1	2300

3.3 Leap year

Leap year occurs every four years, in years which are multiples of 4. For example, 2012 was a leap year. An exception to that is any year which is a multiple of 100. For example, the year 2100 is *not* a leap year. A further exception is that years which are multiples of 400 are indeed leap years. Hence, while 2100 is not a leap year, 2400 is.

During any year which is a multiple of 4, the M41T6x RTC will automatically insert leap day, February 29. Therefore, the application software must correct for this during the exception years (2100, 2200, etc.) as noted above.

3.4 Output driver pin

When the OFIE bit is not set to generate an interrupt, the $\overline{\text{OFIRQ}}$/OUT pin becomes an output driver that reflects the contents of D7 of the calibration register. In other words, when D7 (OUT bit) is a '0,' then the $\overline{\text{OFIRQ}}$/OUT pin will be driven low.

Note: The $\overline{\text{OFIRQ}}$/OUT pin is an open drain which requires an external pull-up resistor.

3.5 Oscillator stop detection

In the event that the oscillator has either stopped, or was stopped for some period of time, and if the oscillator fail interrupt enable (OFIE) bit is set to a '1,' an interrupt will be generated. This interrupt can be used to judge the validity of the clock and date data.

The interrupt will be active any time the oscillator stops while V_{CC} is ≥ 1.0V. The following conditions will cause the $\overline{\text{OFIRQ}}$ pin to be active:

- the ST bit is set to '1.'
- external interference or removal of the crystal.

The oscillator fail interrupt ($\overline{\text{OFIRQ}}$) will remain active until the OFIE bit is reset to '0,' or the oscillator restarts.

The oscillator must start and have run for at least 4 seconds before attempting to set the OFIE bit to '1.'

3.6 Initial power-on defaults

Upon initial application of power to the device, the OUT bit will be set to a '1,' while the ST, OFIE, and FT bits will be set to '0.' All other register bits will initially power-on in a random state.

4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Conditions(1)	Value(2)	Unit
T_{STG}	Storage temperature (V_{CC} off, oscillator off)		–55 to 125	°C
V_{CC}	Supply voltage		–0.3 to 5.0	V
T_{SLD}(3)	Lead solder temperature for 10 seconds		260	°C
V_{IO}	Input or output voltages		–0.2 to Vcc+0.3	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A = 25°C	>1500	V
$V_{ESD(RCDM)}$	Electro-static discharge voltage (Robotic Charged Device Model)	T_A = 25°C	>1000	V

1. Test conforms to JEDEC standard
2. Data based on characterization results, not tested in production
3. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 5. Operating and AC measurement conditions

Parameter	M41T60
Supply voltage (V_{CC})	1.3 V to 4.4 V
Ambient operating temperature (T_A)	–40 to 85 °C
Load capacitance (C_L)	50 pF
Input rise and fall times	≤ 5 ns
Input pulse voltages	0.2 V_{CC} to 0.8 V_{CC}
Input and output timing ref. voltages	0.3 V_{CC} to 0.7 V_{CC}

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 14. AC testing I/O waveform

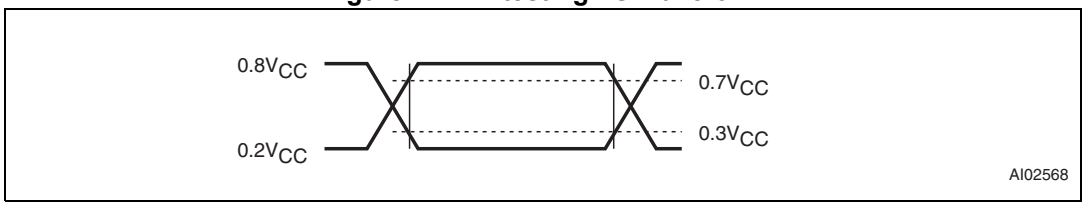
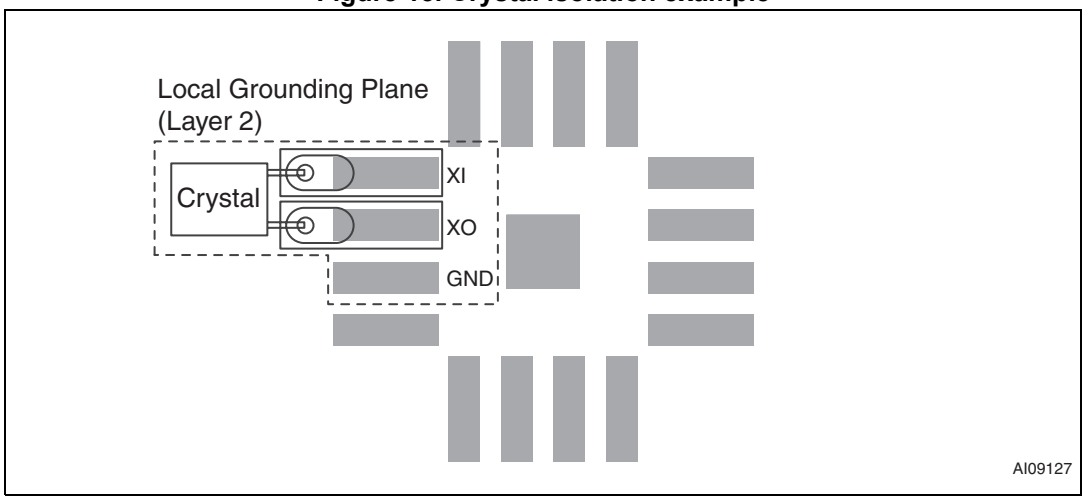


Figure 15. Crystal isolation example



Note: Substrate pad should be tied to V_{SS}.

Table 6. Capacitance

Symbol	Parameter (1)(2)	Min	Max	Unit
C_{IN}	Input capacitance (SCL)	-	7	pF
C_{OUT}(3)	Output capacitance (SDA, OUT)	-	10	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)	-	50	ns

1. Effective capacitance measured with power supply at 3.6 V; sampled only, not 100% tested.
2. At 25 °C, f = 1 MHz.
3. Outputs deselected.

Table 7. DC characteristics

Symbol	Parameter	Test condition(1)		Min	Typ	Max	Unit
V_{CC}(2)	Operating voltage	Clock (3)		1.0		4.4	V
		I^2C bus (400 kHz)		1.3		4.4	V
I_{CC1}	Supply current	SCL = 400 kHz (No load)	V_{CC} = 4.4 V			100	µA
			V_{CC} = 3.6 V		50	70	µA
			V_{CC} = 3.0 V		35		µA
			V_{CC} = 2.5 V		30		µA
			V_{CC} = 2.0 V		20		µA
I_{CC2}	Supply current (Standby)	SCL = 0 Hz All inputs ≥ V_{CC} – 0.2 V ≤ V_{SS} + 0.2 V	4.4 V			950	nA
			3.6 V		375	700	nA
			3.0 V at 25 °C		350		nA
			2.0 V at 25 °C		310		nA
V_{IL}	Input low voltage			–0.2		0.3 V_{CC}	V
V_{IH}	Input high voltage			0.7 V_{CC}		V_{CC} + 0.3	V
V_{OL}	Output low voltage	V_{CC} = 4.4 V, I_{OL} = 3 mA (SDA)				0.4	V
		V_{CC} = 4.4 V, I_{OL} = 1 mA ($\overline{OFIRQ}$/OUT)				0.4	V
	Pull-up supply voltage (open drain)	FT, $\overline{OFIRQ}$/OUT				4.4	V
I_{LI}	Input leakage current	0 V ≤ V_{IN} ≤ V_{CC}		–1.0		+1.0	µA
I_{LO}	Output leakage current	0 V ≤ V_{OUT} ≤ V_{CC}		–1.0		+1.0	µA

1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 1.3 to 4.4 V (except where noted).
2. When using battery backup, V_{CC} fall time should not exceed 10 mV/µs.
3. Oscillator startup guaranteed at 1.5 V only.

Table 8. Crystal electrical characteristics

Symbol	Parameter [1][2]	Min	Typ	Max	Unit
f_O	Resonant frequency	-	32.768		kHz
R_S	Series resistance (T_A = –40 to 70°C, oscillator startup at 2.0 V)	-		75 [3][4]	kΩ
C_L	Load capacitance	-	6		pF

1. For the QFN16 package, user-supplied, external crystals are required. The 6 and 7 pF crystals listed in *Table 9* below have been evaluated by ST and have been found to be satisfactory for use with the M41T6x series RTCs.
2. Load capacitors are integrated within the M41T60. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.
3. Guaranteed by design.
4. $R_{S\ (max)}$ = 65 kΩ for T_A = –40 to 85 °C and oscillator startup at 1.5 V.

Table 9. Crystals suitable for use with M41T6x series RTCs

Vendor	Order number	Package	Manufacturer's specifications			
			ESR max	Temp. range (°C)	Rated tolerance at 25 °C	Rated load cap.
Citizen	CMJ206T-32.768KDZB-UB	8.3 x 2.5 mm leaded SMT	50 kΩ	–40/+85	±20 ppm	6 pF
Citizen	CM315-32.768KDZY-UB	3.2 x 1.5 x 0.9 mm SMT	70 kΩ	–40/+85	±20 ppm	7 pF
Ecliptek	E4WCDA06-32.768K[1]	2.0 x 6.0 mm thru-hole	50 kΩ	–10/+60	±20 ppm	6 pF
Ecliptek	E5WSDC 07 - 32.768K	7 x 1.5 x 1.4 mm SMT	65 kΩ	–40/+85	±20 ppm	7 pF
ECS	ECS-.327-6-17X-TR	3.8 x 8.5 x 2.5 mm SMT	50 kΩ	–10/+60	±20 ppm	6 pF
ECS	ECS-.327-7-34B-TR	3.2 x 1.5 x 0.9 mm SMT	70 kΩ	–40/+85	±20 ppm	7 pF
ECS	ECS-.327-7-38-TR	7 x 1.5 x 1.4 mm SMT	65 kΩ	–40/+85	±20 ppm	7 pF
Epson	MC-146 32.7680KA-AG: ROHS[2]	7 x 1.5 x 1.4 mm SMT	65 kΩ	–40/+85	±20 ppm	7 pF
Fox	298LF-0.032768-19	1.5 x 5.0 mm thru-hole	50 kΩ	–20/+60	±20 ppm	6 pF
Fox	299LF-0.032768-37	2.0 x 6.0 mm thru-hole	50 kΩ	–20/+60	±20 ppm	6 pF
Fox	414LF-0.032768-12	3.8 x 8.5 x 2.5 mm SMT	50 kΩ	–40/+85	±20 ppm	6 pF
Fox	501LF-0.032768-5	7 x 1.5 x 1.4 mm SMT	65 kΩ	–40/+85	±20 ppm	7 pF
Micro Crystal	MS3V-T1R 32.768KHZ 7PF 20PPM	6.7 x 1.4 mm leaded SMT	65 kΩ	–40/+85	±20 ppm	7 pF
Pletronics	SM20S - 32.768K - 6pF	3.8 x 8.5 x 2.5 mm SMT	50 kΩ	–40/+85	±20 ppm	6 pF
Seiko	SSPT7F-7PF20PPM	7 x 1.5 x 1.4 mm SMT	65 kΩ	–40/+85	±20 ppm	7 pF
Seiko	VT200F-6PF20PPM	2.0 x 6.0 mm thru-hole	50 kΩ	–10/+60	±20 ppm	6 pF

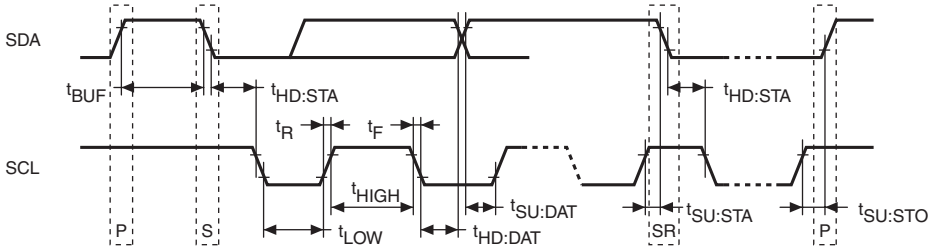
1. ST has been informed that this crystal has been terminated by the vendor.
2. Epson MC-146 32.7680KA-E: ROHS is 6 pF version.

Table 10. Oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{STA}	Oscillator start voltage	≤ 10 seconds	1.5			V
t_{STA}	Oscillator start time	V_{CC} = 3.0 V			1	s
C_g	XIN capacitance			12		pF
C_d	XOUT capacitance			12		pF
	IC-to-IC frequency variation (1)		–10		+10	ppm

1. Reference value. T_A = 25 °C, V_{CC} = 3.0 V, CMJ-145 (C_L = 6 pF, 32,768 Hz) manufactured by Citizen, $C_L = C_g \bullet C_d / (C_g + C_d)$

Figure 16. Bus timing requirements sequence



Note: P = STOP and S = START

Table 11. AC characteristics

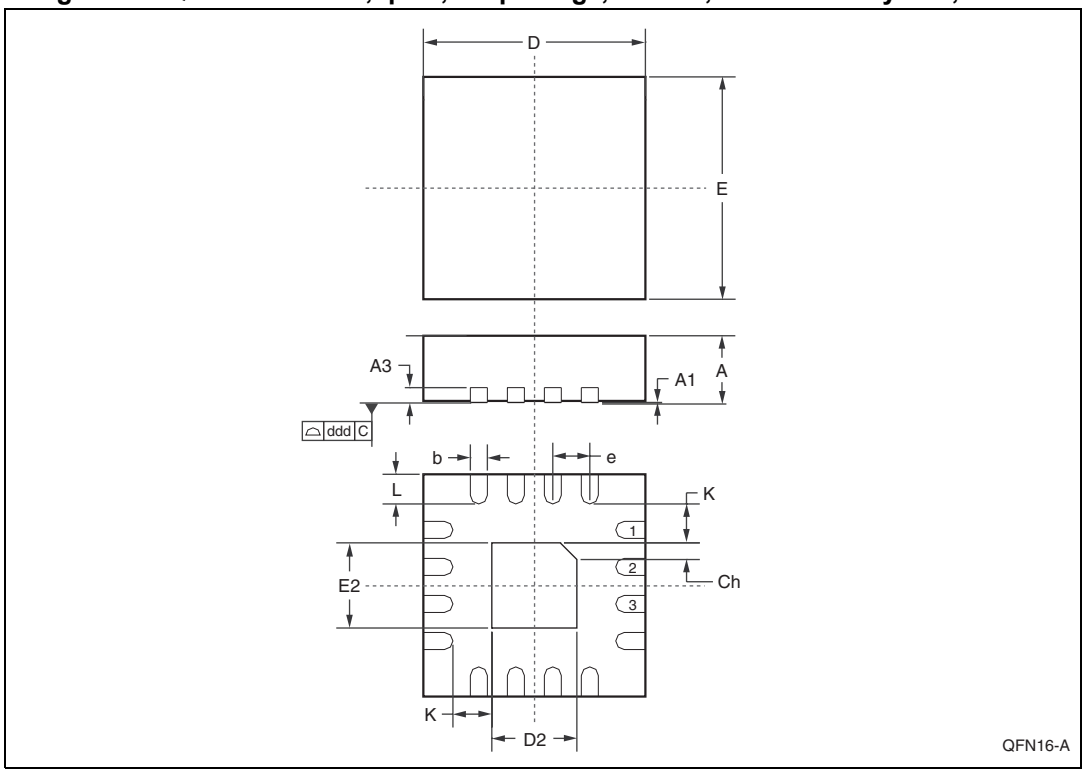
Symbol	Parameter(1)	Min	Max	Unit
f_{SCL}	SCL clock frequency	0	400	kHz
t_{LOW}	Clock low period	1.3		µs
t_{HIGH}	Clock high period	600		ns
t_R	SDA and SCL rise time		300	ns
t_F	SDA and SCL fall time		300	ns
$t_{HD:STA}$	START condition hold time (after this period the first clock pulse is generated)	600		ns
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start condition)	600		ns
$t_{SU:DAT}$	Data setup time	100		ns
$t_{HD:DAT}$(2)	Data hold time	0		µs
$t_{SU:STO}$	STOP condition setup time	600		ns
t_{BUF}	Time the bus must be free before a new transmission can start	1.3		µs

1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 1.3 to 4.4 V (except where noted).
2. Transmitter must internally provide a hold time to bridge the undefined region (300 ns max.) of the falling edge of SCL.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 17. QFN16 – 16-lead, quad, flat package, no lead, 3 x 3 mm body size, outline

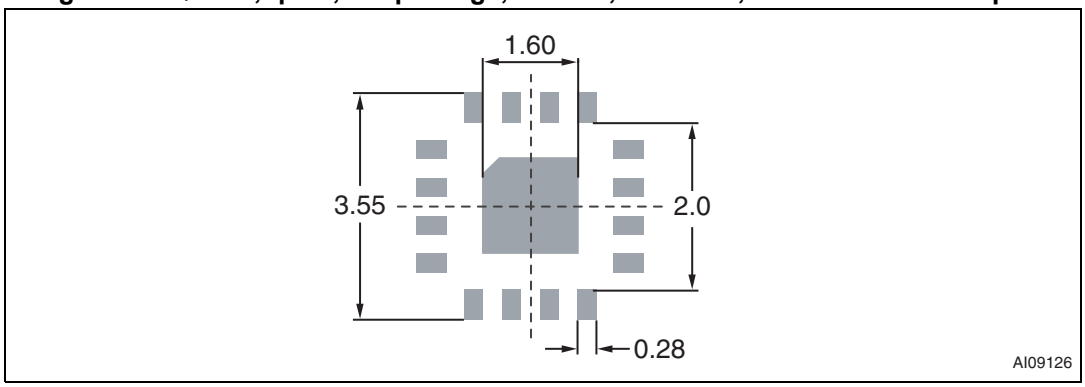


Note: Drawing is not to scale.

Table 12. QFN16 – 16-lead, quad, flat package, no lead, 3 x 3 mm body size, mechanical data

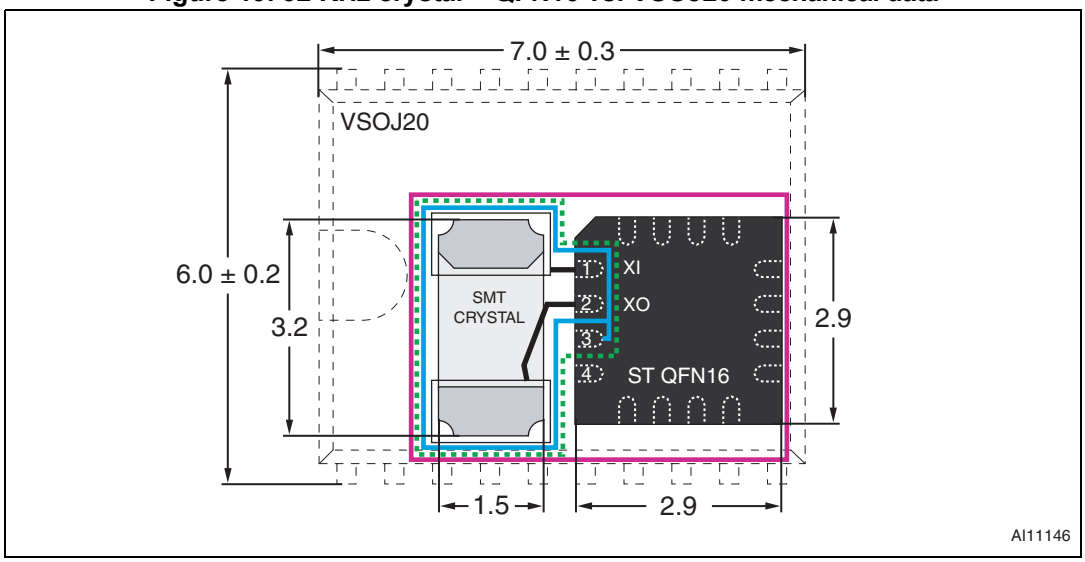
Dim	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.90	0.80	1.00	0.035	0.032	0.039
A1	0.02	0.00	0.05	0.001	0.000	0.002
A3	0.20	–	–	0.008	–	–
b	0.25	0.18	0.30	0.010	0.007	0.012
D	3.00	2.90	3.10	0.118	0.114	0.122
D2	1.70	1.55	1.80	0.067	0.061	0.071
E	3.00	2.90	3.10	0.118	0.114	0.122
E2	1.70	1.55	1.80	0.067	0.061	0.071
e	0.50	–	–	0.020	–	–
K	0.20	–	–	0.008	–	–
L	0.40	0.30	0.50	0.016	0.012	0.020
ddd	–	0.08	–	–	0.003	–
Ch	–	0.33	–	–	0.013	–
N	16			16		

Figure 18. QFN16, quad, flat package, no lead, 3 x 3 mm, recommended footprint



Note: Substrate pad should be tied to V_{SS}.

Figure 19. 32 KHz crystal + QFN16 vs. VSOJ20 mechanical data



Note: Dimensions shown are in millimeters (mm).

7 Part numbering

Table 13. Ordering information scheme

Example: **M41T 60 Q 6 F**

Device family

M41T

Device type and supply voltage

60 = V_{CC} = 1.3 to 4.4 V

Package

Q = QFN16 (3 mm x 3 mm)

Temperature range

6 = –40 to 85 °C

Shipping method

F = ECOPACK® package, tape & reel

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

8 Revision history

Table 14. Revision history

Date	Revision	Changes
13-Nov-2003	1	First issue
20-Nov-2003	1.1	Update characteristics (*Figure 2*, *3*, *4*; *Table 1*, *2*, *5*, *7*, *11*)
25-Dec-2003	2	Reformatted; add crystal isolation, footprint (*Figure 12*)
13-Jan-2004	2.1	Update characteristics (*Figure 9*, *10*, *12*; *Table 7*, *13*)
26-Feb-2004	2.2	Update characteristics and mechanical dimensions (*Figure 15*, *18*; *Table 4* , *7*, *12*)
02-Mar-2004	2.3	Update characteristics (*Table 7*)
26-Apr-2004	3	Reformat and republish
13-May-2004	4	Update characteristics (*Table 7*, *8*; *Figure 15* , *18*)
06-Aug-2004	5	Update characteristics (*Figure 2*; *Table 7*, *10*)
25-Oct-2004	6	Document status promotion; update characteristics (*Figure 1*; *Table 4* ,*7*, *8*, *10*, *12*)
20-Dec-2004	7	Corrected footprint; update characteristics (*Figure 4*, *18*; *Table 7*)
05-May-2005	8	Add package comparison and mechanical data (*Figure 19*)
31-Oct-2005	9	Update: bus operating voltage, characteristics (*Figure 4*; *Table 4*, *7*, *11*, *13*)
30-Nov-2005	10	Update ESD:HBM rating, crystal characteristics (*Table 4*, *8*)
06-Jul-2006	11	New template
26-Jan-2010	12	Minor textual changes; updated footnote *3* of *Table 4*; updated footnote *1* of *Table 8*; added *Table 9*; updated *Table 10*, *11*, *Section 3.1*; added text to *Section 6: Package mechanical data*.
29-Apr-2010	13	Updated *Table 9*; minor textual change in *Section 4*.
21-Feb-2013	14	Updated title of datasheet; updated *Section 3.2: Century bits*; added *Figure 13: Century bits CB1 and CB0*; moved and modified *Table 3: Examples using century bits*; added *Section 3.3: Leap year*; added footnote *1* to *Table 9: Crystals suitable for use with M41T6x series RTCs*.

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