Keywords: AMD K8, MAX1937, active offset, K8 mobile cpu power, low power K8 mobile power supply

**REFERENCE DESIGN 3218 INCLUDES: √Tested Circuit √Schematic √BOM √Description**

# Power Supply Meets AMD K8 Low-Power Mobile Specification

**Apr 30, 2004**

*Abstract: This application note describes a two-phase, synchronous, step-down converter that is fully compliant with the AMD® K8 Low-Power Mobile Specification. It includes details of the circuit operation, schematic, bill of materials, and a 1.2 volt, 27.3 Amp reference design with test data.*

This application note describes a two-phase, synchronous, step-down converter that uses the MAX1937 to achieve a power supply that is fully compliant with the AMD K8 Low-Power Mobile Specification.

The design uses the standard K8 VID table with a -100mV offset from the selected VID voltage. An active offset method implements the required -100mV offset. The specified "droop" or voltage positioning value for this application is 50mV.

Details of the active offset circuit are presented, along with the schematic and bill of materials for the complete power supply. A 1.2 volt, 27.3 Amp reference design along with test data is also presented.

For more details on the 2-phase synchronous step down converter (voltage positioning etc.), please refer to the MAX1937-MAX1939 Data Sheet.

## Active Offset

The active offset circuit is shown in **Figure 1**. It is essentially a precision 1-mA current source. The circuit consists of resistors R51, R52, R53, R54, R55 and the LMX321 op amp U2. The circuit accepts a 2V input from the reference voltage (pin 12) of the MAX1937 and maintains 2V, with the polarity shown, across the 2kΩ resistor R55. The resulting 1mA current in the resistor flows in the 100Ω feedback resistor R8 connected to the FB pin (pin 14) of the MAX1937 and produces a negative offset of -100mV.

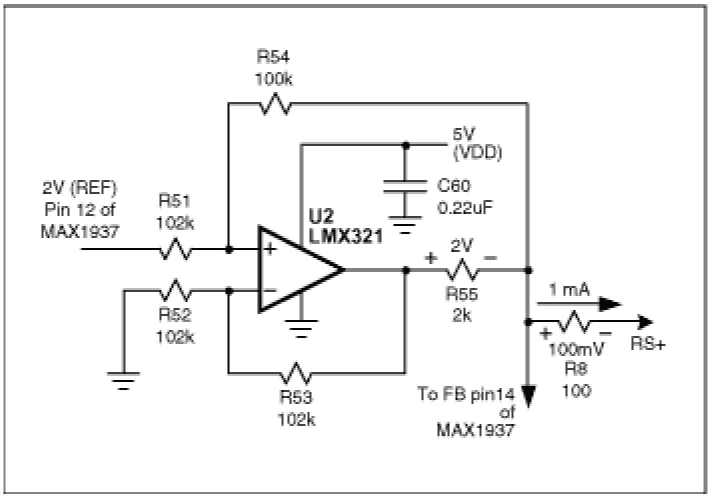



*Figure 1. Active offset circuit.*

It can be shown mathematically that the output impedance of the above current source is much larger than the load resistance (in this case 100Ω) and therefore its effect on the circuit can be neglected. For a -100mV offset, the accuracy of the above circuit depends on the exact values of the 2 Volt reference (±13mV for 0°C to 85°C), the 2k, 1% Resistor R5A and the 100Ω, 1% FB resistor R8. The offset voltage is given by

$$V_{offset} = \frac{V_{Ref}}{R5A} \cdot R8$$

Substituting worst-case values in the above equation yields a ±2.6mV worst-case error in the offset voltage. Test data is presented in Table 1 to show selected VID codes and actual output voltage at no load to demonstrate the performance of the active offset circuit. Table 2 shows load line data for the 1.2 volt, 35 watt application.

**Table 1. VID codes and actual output voltages with -100mV offset**

| VID CODE | $V_{OUT}$ | $V_{OFFSET}$, Target = -100mV |
|---|---|---|
| 1.3 | 1.201 | 0.099 |
| 1.275 | 1.1759 | 0.0991 |
| 1.25 | 1.1507 | 0.0993 |
| 1.225 | 1.1256 | 0.0994 |
| 1.2 | 1.1019 | 0.0981 |
| 1.175 | 1.0768 | 0.0982 |
| 1.15 | 1.051 | 0.099 |
| 1.125 | 1.0265 | 0.0985 |
| 1.1 | 1.0013 | 0.0987 |
| 1.075 | 0.9763 | 0.0987 |
| 1.05 | 0.951 | 0.099 |
| 1.025 | 0.926 | 0.099 |
| 1 | 0.9008 | 0.0992 |
| 0.975 | 0.8759 | 0.0991 |

| | | |
|---|---|---|
| 0.95 | 0.8507 | 0.0993 |
| 0.925 | 0.8256 | 0.0994 |
| 0.9 | 0.8004 | 0.0996 |
| 0.875 | 0.7753 | 0.0997 |
| 0.85 | 0.7501 | 0.0999 |
| 0.825 | 0.7249 | 0.1001 |
| 0.8 | 0.6997 | 0.1003 |

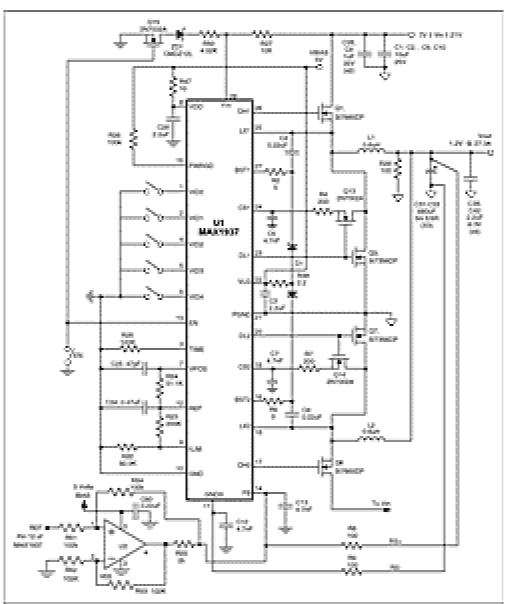
**Table 2. Load line data for 1.2 Volts VID setting**

| $I_{OUT}$ | $V_{OUT}$ | VID CODE | $\Delta V$ = VID - $V_{OUT}$ |
|---|---|---|---|
| 0 | 1.201 | 1.3 | 0.099 |
| 2 | 1.1981 | 1.3 | 0.1019 |
| 5 | 1.1924 | 1.3 | 0.1076 |
| 10 | 1.1806 | 1.3 | 0.1194 |
| 15 | 1.1725 | 1.3 | 0.1275 |
| 20 | 1.1641 | 1.3 | 0.1359 |
| 25 | 1.1577 | 1.3 | 0.1423 |
| 27.3 | 1.152 | 1.3 | 0.148 |

**Table 3. Bill of Materials**

| DESIGNATION | QTY | DESCRIPTION | Vendor |
|---|---|---|---|
| C1, C2, C9, C10 | 4 | 10µF 25V (1812) TMK432BJ106MM | Taiyo Yuden |
| C3, C26, C39-C42 | 6 | 2.2uF 6.3V (0805) JMK107BJ225MA | Taiyo Yuden |
| C4, C6, C60 | 3 | 0.22µF 10V X7R (0603) LMK107BJ224KA | Taiyo Yuden |
| C24 | 1 | 0.47µF 10V X5R (0603) LMK107BJ474KA | Taiyo Yuden |
| C5, C7, C12, C13 | 4 | 4.7nF 50V X7R (0603) GRM39X7F472K50 | Murata |
| C8, C28 | 2 | 1µF 35V (0805) GMK316BJ105ML | Taiyo Yuden |
| C25 | 1 | 47pF 50V C0G (0603) GRM39C0G470J050AD | Murata |
| C31-C33 | 3 | 680µF/2.5V 5mΩ ESR POSCAP Sanyo: 2R5TPD680M | Sanyo |
| R2, R5 | 2 | 0Ω (0603) | |
| R4, R7 | 2 | 200, 5% (0603) | |
| R8, R9, R28 | 3 | 100, 5% (0603) | |
| R23 | 1 | 200k, 1% (0603) | |
| R24 | 1 | 51.1k, 1%, (0603) | |
| | | | |

| | | | |
|---|---|---|---|
| R27 | 1 | 10k, 1% (0603) | |
| R47 | 1 | 10, 5% (0603) | |
| R22 | 1 | 90.9k, 1% (0603) | |
| R25 | 1 | 120k, 1% (0603) | |
| R26 | 1 | 100k, 1% (0603) | |
| R51, R52, R53 | 3 | 102k, 1%(0603) | |
| R54 | 1 | 100k, 1% (0603) | |
| R55 | 1 | 2k, 1% (0603) | |
| R50 | 1 | 4.02k, 1% (0603) | |
| L1, L2 | 2 | 0.6uH ETQP1H0R6BFA | Panasonic |
| D1 | 1 | Dual Schottky Diodes (SOT23) Central: CMPSH-3A Central | |
| ZD1 | 1 | Zener, 12V Central CMDZ12L | Central |
| Q1, Q6 | 2 | N-channel Powerpak SO8 MOSFETs, SI7860DP | VISHAY SILICONIX |
| Q3, Q7 | 2 | N-channel Powerpak SO8 MOSFETs, SI7356DP | VISHAY SILICONIX |
| Q15, Q13, Q14 | 3 | 2N7002A | Central |
| PCB | 1 | 4 Phase MAX1937 Evaluation PCB NPCB 07-03 4.5inch x 3 7/8 | |
| U1 | 1 | MAX1937EEI (QSOP) | **MAXIM** |
| U2 | 1 | LMX321 Opamp SOT-23-5 / SC70-5 | **MAXIM** |



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| Related Parts | | |
|---|---|---|
| LMX321 | Single/Dual/Quad, General-Purpose, Low-Voltage, Rail-to-Rail Output Op Amps | Free Samples |
| MAX1937 | Two-Phase Desktop CPU Core Supply Controllers with Controlled VID Change | Free Samples |
| MAX1938 | Two-Phase Desktop CPU Core Supply Controllers with Controlled VID Change | |
| MAX1939 | Two-Phase Desktop CPU Core Supply Controllers with Controlled VID Change | |

**More Information**
For Technical Support: http://www.maximintegrated.com/support
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REFERENCE DESIGN 3218, AN3218, AN 3218, APP3218, Appnote3218, Appnote 3218