

MAX14595

Low-Power Dual-Channel Logic-Level Translator

General Description

The MAX14595 is a dual-channel, bidirectional logic-level translator designed specifically for low power consumption making it suitable for portable and battery-powered equipment. Externally applied voltages, V_{CC} and V_L , set the logic levels on either side of the device. A logic signal present on the V_L side of the device appears as the same logic signal on the V_{CC} side of the device, and vice-versa.

The device is optimized for the I²C bus as well as the management data input/output (MDIO) bus where often high-speed, open-drain operation is required. When $\overline{TS}$ is high, the device allows the pullup to be connected to the I/O port that has the power. This allows continuous I²C operation on the powered side without any disruption while the level translation function is off.

The part is specified over the extended -40°C to +85°C temperature range, and is available in 8-bump WLP and 8-pin TDFN packages.

- ◆ **Meets Industry Standards**
 - ◇ I²C Requirements for Standard, Fast, and High* Speeds
 - ◇ MDIO Open Drain Above 4MHz*
- ◆ **Allows Greater Design Flexibility**
 - ◇ Down to 0.9V Operation on V_L Side
 - ◇ Supports Above 8MHz Push-Pull Operation
- ◆ **Ultra-Low Power Consumption**
 - ◇ 7 μ A V_{CC} Supply Current
 - ◇ 3 μ A V_L Supply Current
- ◆ **Provides High Level of Integration**
 - ◇ Pullup Resistor Enabled with One Side Power Supply when $\overline{TS}$ Is High
 - ◇ 12k Ω (max) Internal Pullup
 - ◇ Low Transmission Gate R_{ON} : 17 Ω (max)
- ◆ **Saves Space**
 - ◇ 8-Bump, 0.4mm Pitch, 0.8mm x 1.6mm WLP Package
 - ◇ 8-Pin, 2mm x 2mm TDFN Package

Applications

Portable and Battery-Powered Electronics
Devices with I²C Communication
Devices with MDIO Communication
General Logic-Level Translation

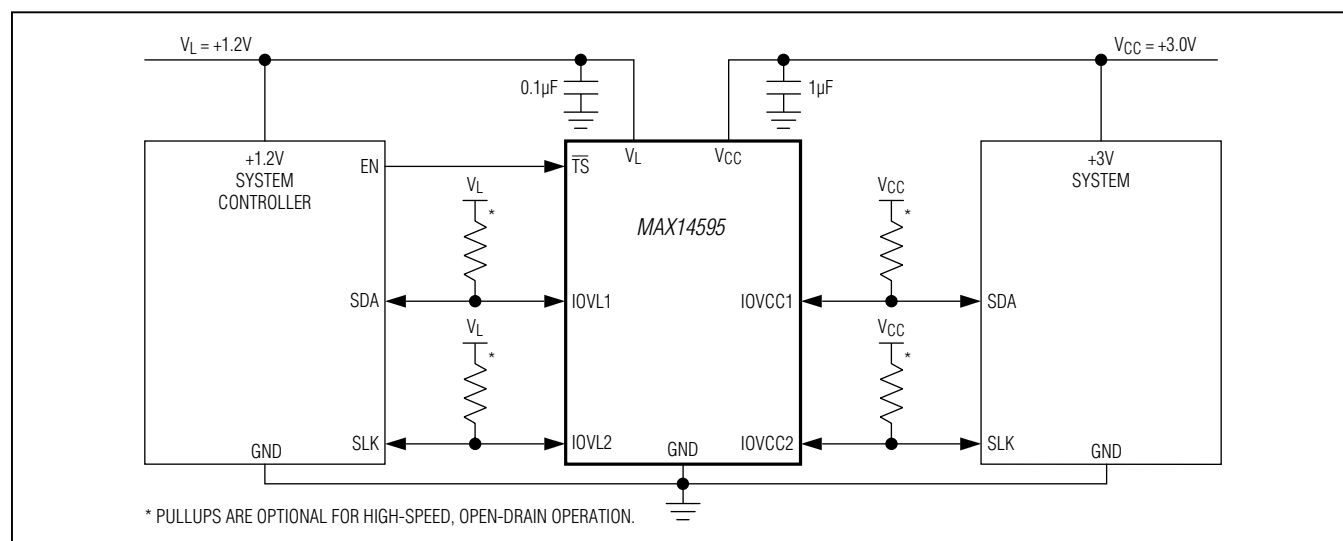
*Requires external pullups.

Ordering Information appears at end of data sheet.

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX14595.related.

Benefits and Features

Typical Operating Circuit



Low-Power Dual-Channel Logic-Level Translator

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to GND.

V_{CC} , V_L , $\overline{TS}$	-0.5V to +6V
IOVCC1, IOVCC2	-0.5V to $+(V_{CC} + 0.5V)$
IOVL1, IOVL2	-0.5V to $+(V_L + 0.5V)$
Short-Circuit Duration IOVCC1, IOVCC2, IOVL1, IOVL2 to GND	Continuous
V_{CC} , IOVCC_ Maximum Continuous Current at +110°C	100mA
V_L IOVL_ Maximum Continuous Current at +110°C	40mA

$\overline{TS}$ Maximum Continuous Current at +110°C	70mA
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
TDFN (derate 6.2mW/°C above +70°C)	496mW
WLP (derate 11.8mW/°C above +70°C)	944mW
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (TDFN only, soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TDFN

Junction-to-Ambient Thermal Resistance (θ_{JA})	162°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	20°C/W

WLP

Junction-to-Ambient Thermal Resistance (θ_{JA})	85°C/W
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Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

($V_{CC} = +1.65V$ to $+5.5V$, $V_L = +0.9V$ to $\min(V_{CC} + 0.3V, +3.6V)$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $V_{CC} = +3V$, $V_L = +1.2V$, and $T_A = +25^\circ\text{C}$.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power Supply Range	V_L		0.9		5.5	V
	V_{CC}		1.65		5.5	
V_{CC} Supply Current	I_{CC}	IOVCC_ = V_{CC} , IOVL_ = V_L , $\overline{TS} = V_{CC}$		7	15	μA
V_L Supply Current	I_L	IOVCC_ = V_{CC} , IOVL_ = V_L , $\overline{TS} = V_{CC}$		3	6	μA
V_{CC} Shutdown Supply Current	$I_{CC-SHDN}$	$\overline{TS} = \text{GND}$		0.4	1	μA
		$\overline{TS} = V_{CC}$, $V_L = \text{GND}$, IOVCC_ = unconnected		0.4	1	
V_L Shutdown Supply Current	I_{L-SHDN}	$\overline{TS} = \text{GND}$		0.1	1	μA
		$\overline{TS} = V_L$, $V_{CC} = \text{GND}$, IOVL_ = unconnected		0.1	1	
IOVCC_, IOVL_ Three-State Leakage Current	I_{LEAK}	$T_A = +25^\circ\text{C}$, $\overline{TS} = \text{GND}$		0.1	1	μA
$\overline{TS}$ Input Leakage Current	I_{LEAK_TS}	$T_A = +25^\circ\text{C}$			1	μA
V_{CC} Shutdown Threshold	V_{TH_VCC}	$\overline{TS} = V_L$, V_{CC} falling		0.8	1.35	V
V_L Shutdown Threshold	V_{TH_VL}	$\overline{TS} = V_{CC}$, V_L falling, $V_L = 0.9V$	0.25	0.6	0.86	V
V_L Above V_{CC} Shutdown Threshold	V_{TH_VL-VCC}	V_L rising above V_{CC} , $V_{CC} = +1.65V$	0.4	0.73	1.1	V
IOVL_ Pullup Resistor	R_{VL_PU}	Inferred from V_{OHL} measurements	3	7.6	12	$k\Omega$
IOVCC_ Pullup Resistor	R_{VCC_PU}	Inferred from V_{OHC} measurements	3	7.6	12	$k\Omega$
IOVL_ to IOVCC_ DC Resistance	$R_{IOVL-IOVCC}$	Inferred from V_{OLx} measurements		6	17	Ω

Low-Power Dual-Channel Logic-Level Translator**ELECTRICAL CHARACTERISTICS (continued)**

($V_{CC} = +1.65V$ to $+5.5V$, $V_L = +0.9V$ to $\min(V_{CC} + 0.3V, +3.6V)$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = +3V$, $V_L = +1.2V$, and $T_A = +25^{\circ}C$.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC LEVELS						
IOVL_ Input-Voltage High	V _{IHL}	IOVL_ rising, V _L = +0.9V, V _{CC} = +1.65V (Note 4)	V _L - 0.2			V
IOVL_ Input-Voltage Low	V _{ILL}	IOVL_ falling, V _L = +0.9V, V _{CC} = +1.65V (Note 4)			0.15	V
IOVCC_ Input-Voltage High	V _{IHC}	IOVCC_ rising, V _L = +0.9V, V _{CC} = +1.65V (Note 4)	V _{CC} - 0.4			V
IOVCC_ Input-Voltage Low	V _{ILC}	IOVCC_ falling, V _L = +0.9V, V _{CC} = +1.65V (Note 4)			0.2	V
$\overline{TS}$ Input-Voltage High	V _{IH}	$\overline{TS}$ rising, V _L = +0.9V or +3.6V, V _{CC} > V _L	V _L - 0.15			V
$\overline{TS}$ Input-Voltage Low	V _{IL}	$\overline{TS}$ falling, V _L = +0.9V or +3.6V, V _{CC} > V _L			0.2	V
IOVL_ Output-Voltage High	V _{OHL}	IOVL_ source current 20μA, V _{IOVCC_} = V _L to V _{CC} (V _{CC} ≥ V _L)	0.7 x V _L			V
IOVL_ Output-Voltage Low	V _{OLL}	IOVL_ sink current 5mA, V _{IOVCC_} ≤ 0.05V			0.2	V
IOVCC_ Output-Voltage High	V _{OHC}	IOVCC_ source current 20μA, V _{IOVL_} = V _L	0.7 x V _{CC}			V
IOVCC_ Output-Voltage Low	V _{OLC}	IOVCC_ sink current 5mA, V _{IOVL_} ≤ 0.05V			0.25	V
RISE/FALL TIME ACCELERATOR STAGE						
Accelerator Pulse Duration		V _L = +0.9V, V _{CC} = +1.65V	9	22	48	ns
IOVL_ Output Accelerator Source Impedance		V _L = +0.9V, IOVL_ = GND, V _{CC} = +1.65V	26			Ω
		V _L = +3.3V, IOVL_ = GND, V _{CC} = +5V	6.8			
IOVCC_ Output Accelerator Source Impedance		V _{CC} = +1.65V, IOVCC_ = GND	26			Ω
		V _{CC} = +5V, IOVCC_ = GND	6.5			
THERMAL PROTECTION						
Thermal Shutdown	T _{SHDN}		+150			°C
Thermal Hysteresis	T _{HYST}		10			°C

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TIMING CHARACTERISTICS

($V_{CC} = +1.65V$ to $+5.5V$, $V_L = +0.9V$ to $+3.6V$, $V_{CC} \geq V_L$, $\overline{TS} = V_L$, $C_{VCC} = 1\mu F$, $C_{VL} = 0.1\mu F$, $C_{IOVL_} \leq 100pF$, $C_{IOVCC_} \leq 100pF$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +3V$, $V_L = +1.2V$ and $T_A = +25^\circ C$. All timing is 10% to 90% for rise time and 90% to 10% for fall time.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Turn-On Time for Q1	t_{ON}	$V_{\overline{TS}} = 0V$ to V_L (see the <i>Block Diagram</i>)		160	400	μs
IOVCC_ Rise Time	t_{RCC}	Push-pull driving, $V_L = +1.2V$, $V_{CC} = +3V$ (Figure 1)		8	22	ns
		Open-drain driving, $V_L = +1.2V$, $V_{CC} = +3V$ (Figure 2)		11		
IOVCC_ Fall Time	t_{FCC}	Push-pull driving, $V_L = +1.2V$, $V_{CC} = +3V$ (Figure 1)		5	15	ns
		Open-drain driving, $V_L = +1.2V$, $V_{CC} = +3V$ (Figure 2)		6		
IOVL_ Rise Time	t_{RL}	Push-pull driving, $V_L = +1.2V$, $V_{CC} = +3V$ (Figure 3)		4	13	ns
		Open-drain driving, $V_L = +1.2V$, $V_{CC} = +3V$ (Figure 4)		16		
IOVL_ Fall Time	t_{FL}	Push-pull driving, $V_L = +1.2V$, $V_{CC} = +3V$ (Figure 3)		2.8	12	ns
		Open-drain driving, $V_L = +1.2V$, $V_{CC} = +3V$ (Figure 4)		3.3		
Propagation Delay (Driving IOVL_)	t_{PD_LCC}	Push-pull driving, $V_L = +1.2V$, $V_{CC} = +3V$ (Figure 1)	Rising	7.6	19	ns
			Falling	3	9	
Propagation Delay (Driving IOVCC_)	t_{PD_CCL}	Push-pull driving, $V_L = +1.2V$, $V_{CC} = +3V$ (Figure 3)	Rising	3	5	ns
			Falling	1.5	7	
Channel-to-Channel Skew	t_{SKEW}	Input rise time/fall time $< 6ns$			1.5	ns
Maximum Data Rate		Push-pull operation	8			MHz
		Open-drain operation (Note 6)	4			

Note 2: All devices are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 3: V_L must be less than or equal to V_{CC} during normal operation. However, V_L can be greater than V_{CC} during startup and shutdown conditions.

Note 4: V_{IHL} , V_{ILL} , V_{IHC} , and V_{ILC} are intended to define the range where the accelerator triggers.

Note 5: Guaranteed by design.

Note 6: External pullup resistors are required.

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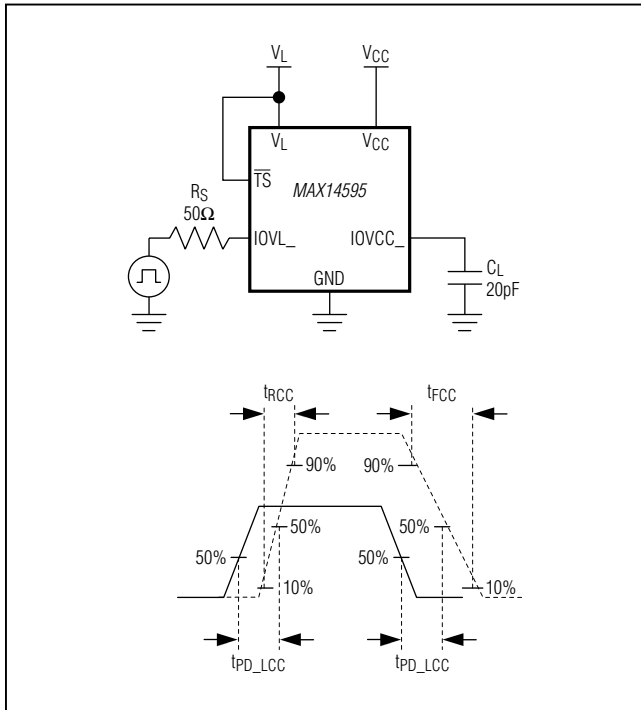


Figure 1. Push-Pull Driving $IOVL_-$

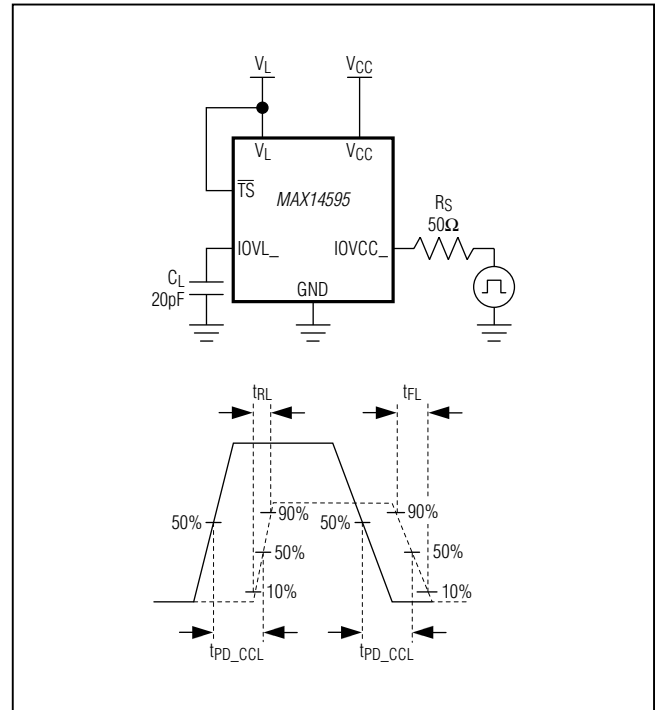


Figure 3. Push-Pull Driving $IOVCC_-$

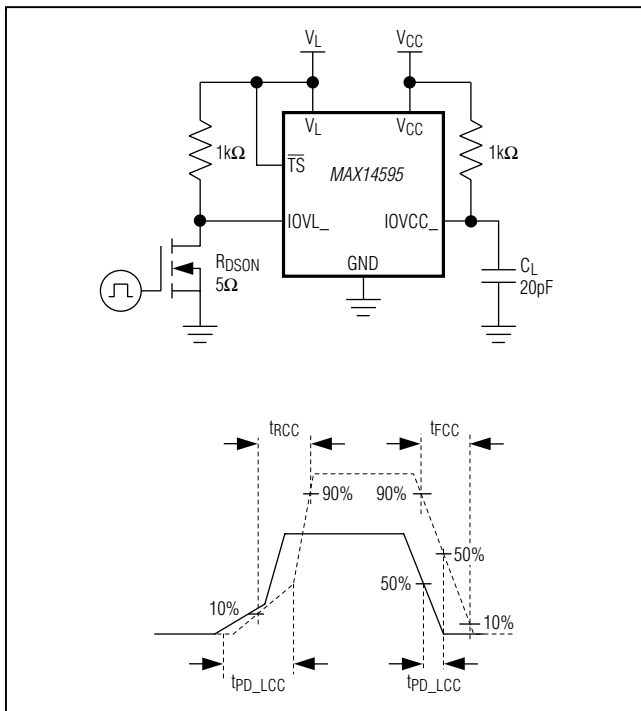


Figure 2. Open-Drain Driving $IOVL_-$

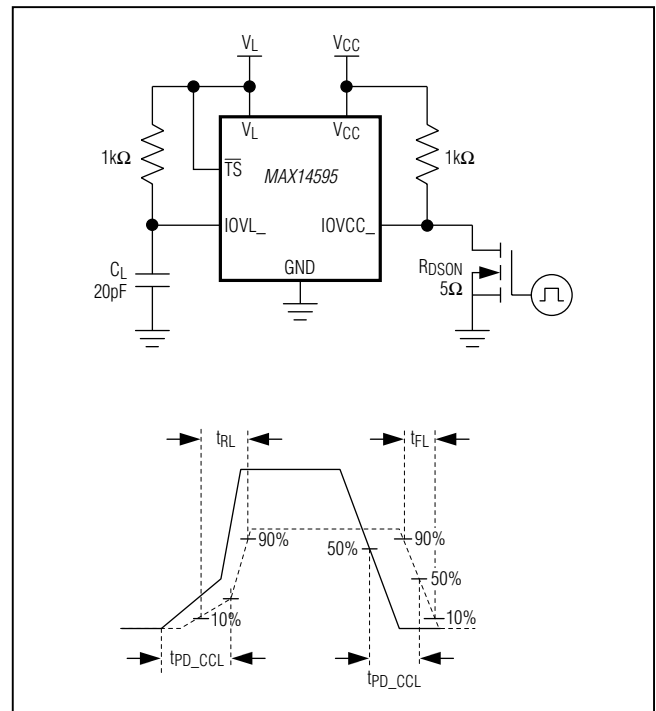


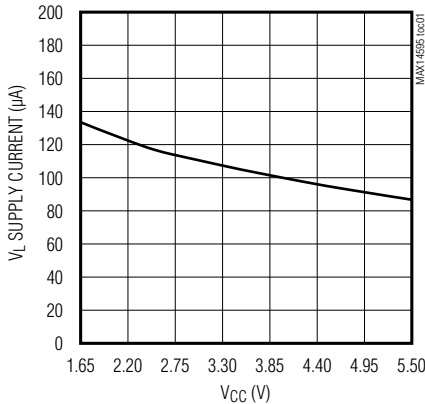
Figure 4. Open-Drain Driving $IOVCC_-$

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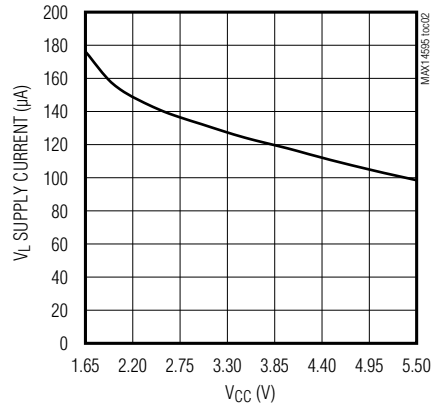
Typical Operating Characteristics

($V_{CC} = +3V$, $V_L = +1.5V$, $R_L = 1M\Omega$, $C_L = 15pF$, push-pull driving data rate = 8Mbps, $T_A = +25^\circ C$, unless otherwise noted.)

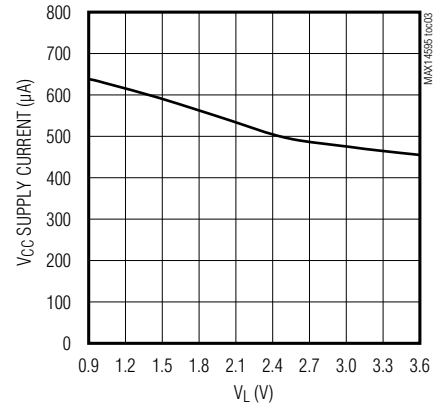
V_L DYNAMIC SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (OPEN-DRAIN DRIVING ONE IOVL_)



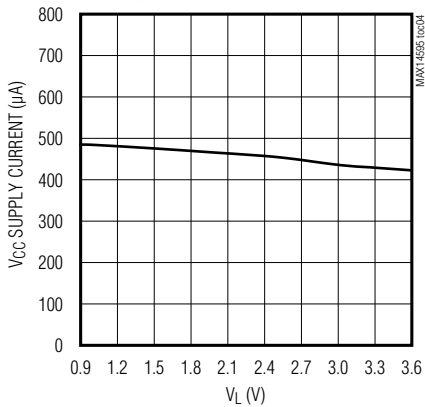
V_L DYNAMIC SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (PUSH-PULL DRIVING ONE IOVCC_)



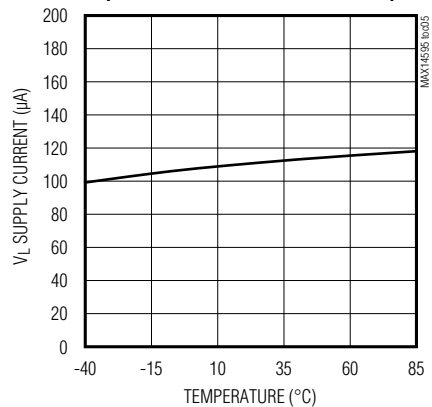
V_{CC} DYNAMIC SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (PUSH-PULL DRIVING ONE IOVL_)



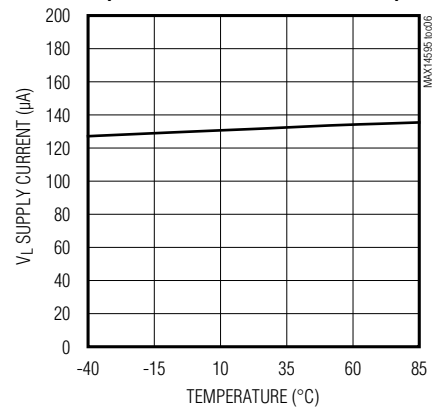
V_{CC} DYNAMIC SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (OPEN-DRAIN DRIVING ONE IOVCC_)



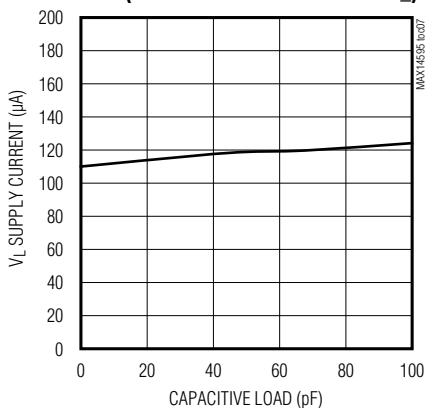
V_L DYNAMIC SUPPLY CURRENT vs. TEMPERATURE (OPEN-DRAIN DRIVING ONE IOVL_)



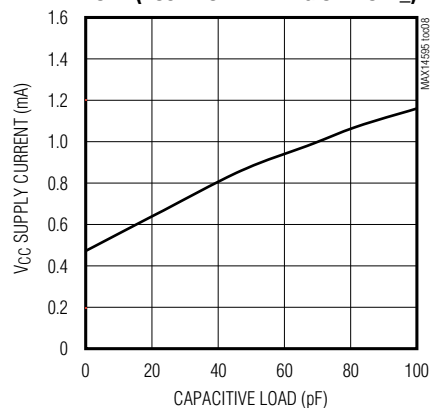
V_L DYNAMIC SUPPLY CURRENT vs. TEMPERATURE (PUSH-PULL DRIVING ONE IOVCC_)



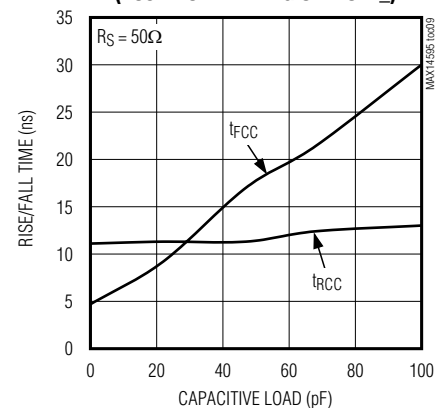
V_L DYNAMIC SUPPLY CURRENT vs. CAPACITIVE LOAD (OPEN-DRAIN DRIVING ONE IOVL_)



V_{CC} DYNAMIC SUPPLY CURRENT vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE IOVL_)



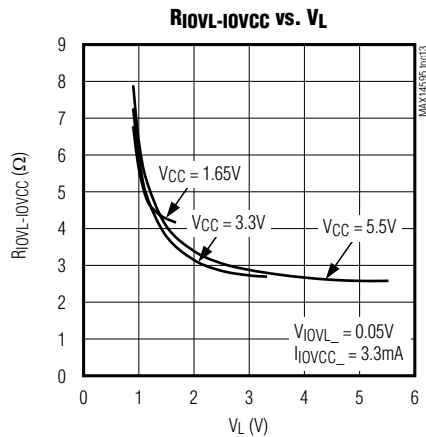
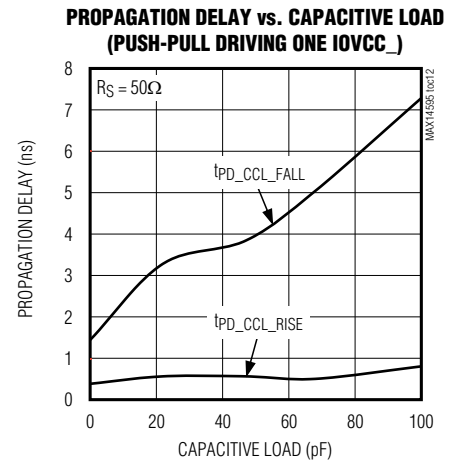
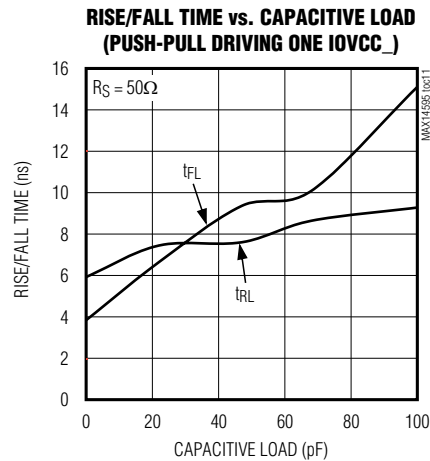
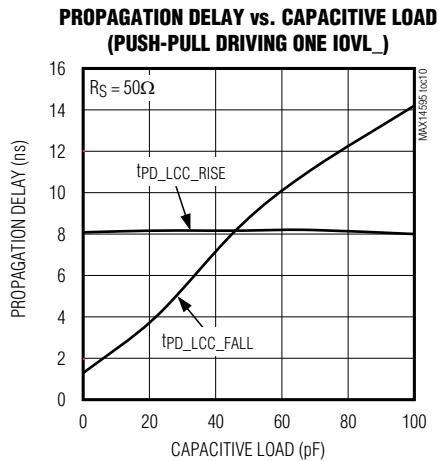
RISE/FALL TIME vs. CAPACITIVE LOAD (PUSH-PULL DRIVING ONE IOVL_)



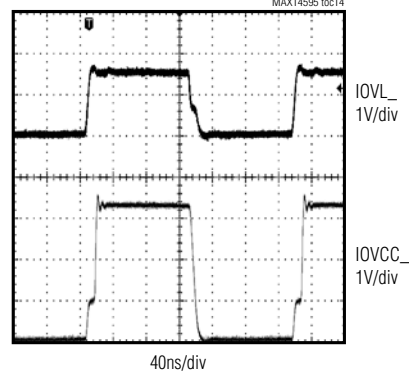
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Typical Operating Characteristics (continued)

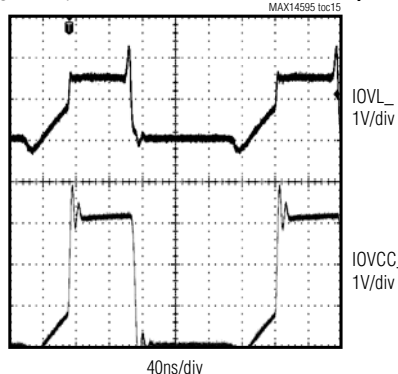
($V_{CC} = +3V$, $V_L = +1.5V$, $R_L = 1M\Omega$, $C_L = 15pF$, push-pull driving data rate = 8Mbps, $T_A = +25^\circ C$, unless otherwise noted.)



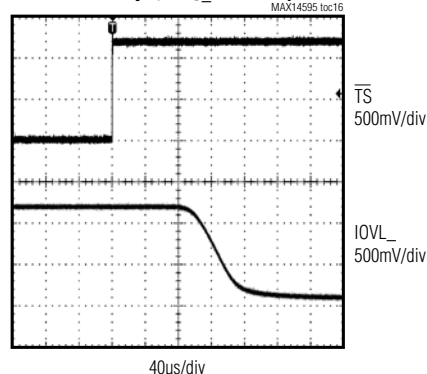
RAIL-TO-RAIL DRIVING (PUSH-PULL DRIVING ONE IOVL₋)
($V_L = +1.5V$, $V_{CC} = +3.3V$, $C_L = 15pF$, $R_L = 1M\Omega$, $R_S = 50\Omega$)



RAIL-TO-RAIL DRIVING (OPEN-DRAIN DRIVING ONE IOVL₋)
($V_L = +1.5V$, $V_{CC} = +3.3V$, $C_L = 100pF$, $R_L = 50\Omega$, $R_S = 50\Omega$, PULLUP ON IOVL₋/IOVCC₋ = 1kΩ)



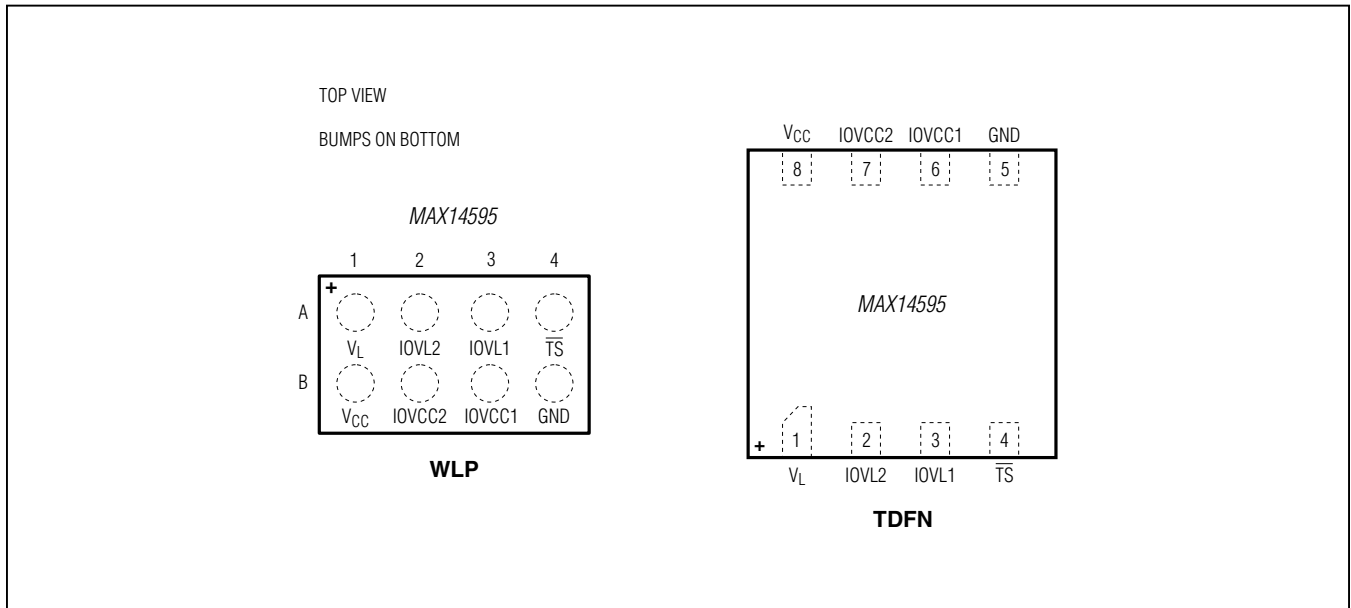
EXITING SHUTDOWN MODE
($V_L = 1.2V$, $V_{CC} = 3.0V$, $IOVCC_- = 0V$, $C_L = 100pF$, $R_{PU_VL} = 50\Omega$)



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Pin Configurations



Pin Description

BUMP/PIN		NAME	FUNCTION
WLP	TDFN		
A1	1	V _L	Logic Supply Voltage, +0.9V to min(V _{CC} + 0.3V, +3.6V). Bypass V _L to GND with a 0.1μF ceramic capacitor as close as possible to the device.
A2	2	IOVL2	Input/Output 2. Reference to V _L .
A3	3	IOVL1	Input/Output 1. Reference to V _L .
A4	4	$\overline{TS}$	Active Low Three-State Input. Drive $\overline{TS}$ low to place the device in shutdown mode with high-impedance output and internal pullup resistors disconnected. Drive $\overline{TS}$ high for normal operation.
B1	8	V _{CC}	Power-Supply Voltage, +1.65V to +5.5V. Bypass V _{CC} to GND with a 1μF ceramic capacitor as close as possible to the device.
B2	7	IOVCC2	Input/Output 2. Reference to V _{CC} .
B3	6	IOVCC1	Input/Output 1. Reference to V _{CC} .
B4	5	GND	Ground

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The schematic diagram illustrates the MAX14595 gate driver circuit. It features two MOSFETs, N and P, which are driven by a GATE DRIVE signal. The N-MOSFET is connected to the load (V_L) and the P-MOSFET is connected to the supply (V_{CC}). The MAX14595 IC is shown as a central block with two ONE-SHOOT BLOCKS and an EN CONTROL BLOCK. The EN CONTROL BLOCK is connected to the GATE DRIVE signal and the MOSFET gates. The ONE-SHOOT BLOCKS are connected to the MOSFET gates and the load/supply lines. The circuit is powered by IOVL₋ and IOVCC₋.

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Ordering Information

PART	TOP MARK	PIN-PACKAGE
MAX14595ETA+T	BNT	8 TDFN
MAX14595EWA+T	AAE	8 WLP

Note: All devices are specified over -40°C to +85°C operating temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 TDFN	T822CN+1	21-0487	90-0349
8 WLP	W80A1+1	21-0555	Refer to Application Note 1891

MAX14595

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/11	Initial release	—



Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

Maxim Integrated 160 Rio Robles, San Jose, CA 95134 USA 1-408-601-1000

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