12-Rail Sequencer and System Health Monitor With Fan Control

Check for Samples: UCD90124

FEATURES

- **Monitor and Sequence 12 Voltage Rails**
  - **All Rails Sampled Every 400 μs**
  - **12-bit ADC With 2.5-V, 0.5% Internal V_{REF}**
  - **Sequence Based on Time, Rail and Pin Dependencies**
  - **Four Programmable Undervoltage and Overvoltage Thresholds per Monitor**
- **Fan Control and Monitoring**
  - **Supports Four Fans With Five User-Defined Speed-vs-Temperature Setpoints**
  - **Supports Two-, Three-, and Four-Wire Fans**
- **Nonvolatile Error and Peak-Value Logging per Monitor (up to 10 Fault Detail Entries)**
- **Closed-Loop Margining for 10 Rails**
  - **Margin Output Adjusts Rail Voltage to Match User-Defined Margin Thresholds**
- **Programmable Watchdog Timer and System Reset**
- **Flexible Digital I/O Configuration**
- **Multiphase PWM Clock Generator**
  - **Clock Frequencies From 15.259 kHz to 125 MHz**
  - **Capability to Configure Independent Clock Outputs for Synchronizing Switch-Mode Power Supplies**
- **Internal Temperature Sensor**
- **JTAG and I²C/SMBus/ PMBus™ Interfaces**

APPLICATIONS

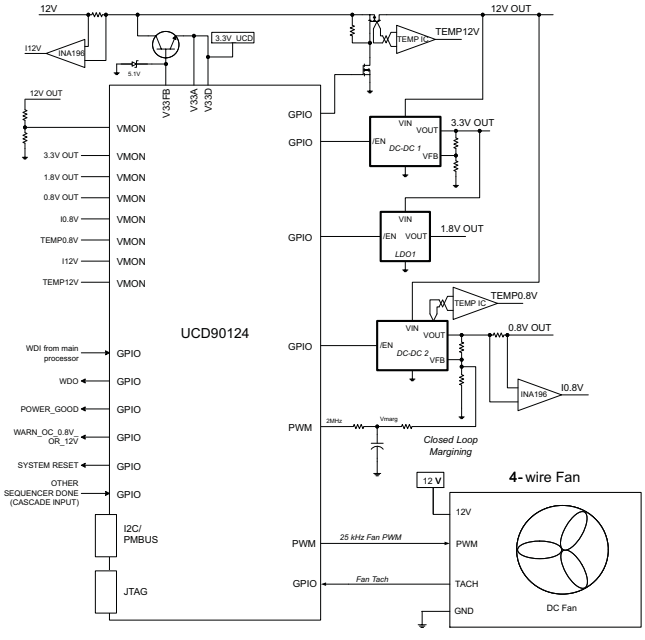
- **Industrial / ATE**
- **Telecommunications and Networking Equipment**
- **Servers and Storage Systems**
- **Embedded Computing**
- **Any System Requiring Sequencing and Monitoring of Multiple Power Rails**

DESCRIPTION

The UCD90124 is a 12-rail PMBus/I²C addressable power-supply sequencer and system-health monitor. The device integrates a 12-bit ADC for monitoring up to 13 power-supply voltage, current, or temperature inputs. Twenty-six GPIO pins can be used for power supply enables, power-on reset signals, external interrupts, cascading, or other system functions. Twelve of these pins offer PWM functionality. Using these pins, the UCD90124 offers support for fan control, margining, and general-purpose PWM functions.

Fan-control signals can be sent using PMBus commands or generated from one of two built-in fan-control algorithms. PWM outputs combined with temperature and fan-speed measurements provide a complete fan-control solution for up to four independent fans.

The TI Fusion Digital Power™ designer software is provided for device configuration. This PC-based graphical user interface (GUI) offers an intuitive interface for configuring, storing, and monitoring all system operating parameters.



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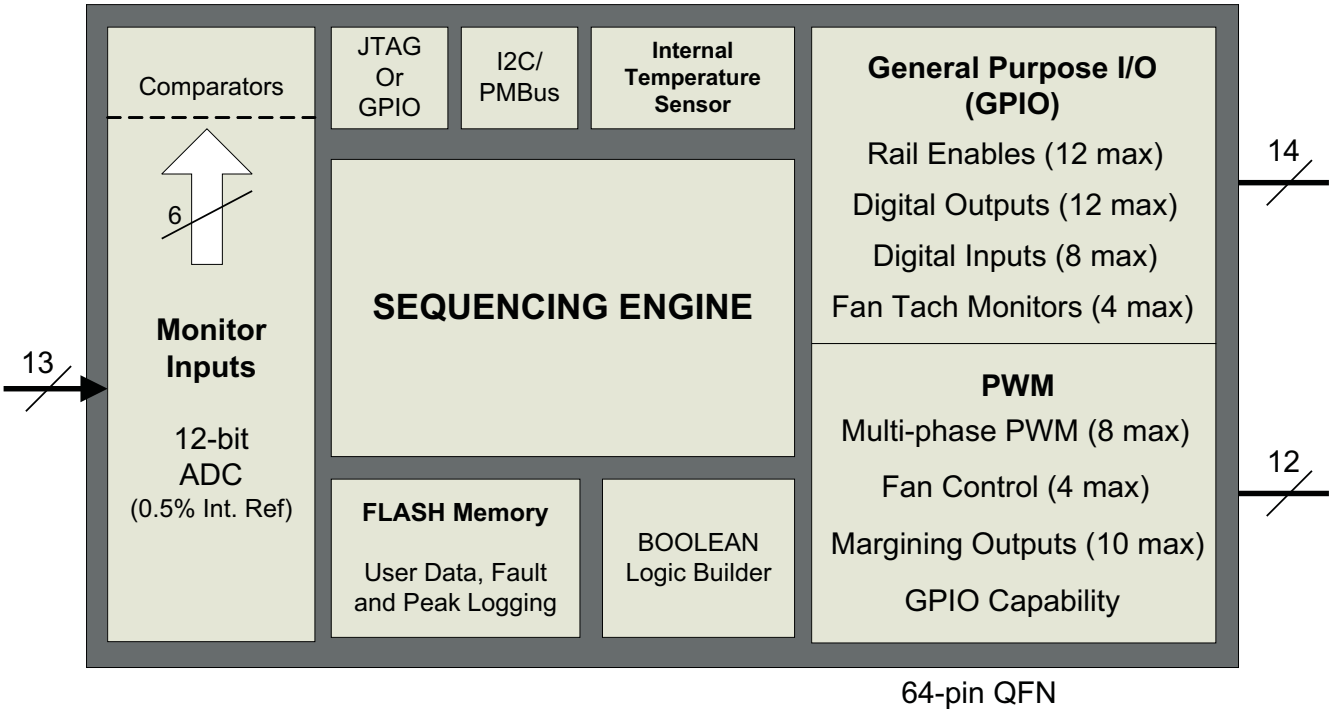
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
Voltage applied at V33D to DV_{SS}		–0.3 V to 3.8	V
Voltage applied at V33A to AV_{SS}		–0.3 V to 3.8	V
Voltage applied at V33FB to AV_{SS}		–0.3 V to 5.5	V
Voltage applied to any other pin (2)		–0.3 V to (V33A + 0.3 V)	V
Storage temperature (T_{stg})		–55 to 150	°C
ESD rating	Human-body model (HBM)	2.5	kV
	Charged-device model (CDM)	750	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}

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THERMAL INFORMATION

THERMAL METRIC(1)		UCD90124 RGC 64 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	26.4	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (3)	21.2	
θ_{JB}	Junction-to-board thermal resistance (4)	1.7	
ψ_{JT}	Junction-to-top characterization parameter (5)	0.7	
ψ_{JB}	Junction-to-board characterization parameter (6)	8.8	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance (7)	1.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage during operation (V_{33D}, V_{33DIO}, V_{33A})	3	3.3	3.6	V
Operating free-air temperature range, T_A	–40		110	°C
Junction temperature, T_J			125	°C

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ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SUPPLY CURRENT						
I_{V33A}	Supply current(1)	V_{V33A} = 3.3 V		8		mA
I_{V33DIO}		V_{V33DIO} = 3.3 V		2		mA
I_{V33D}		V_{V33D} = 3.3 V		40		mA
I_{V33D}		V_{V33D} = 3.3 V, storing configuration parameters in flash memory		50		mA
INTERNAL REGULATOR CONTROLLER INPUTS/OUTPUTS						
V_{V33}	3.3-V linear regulator	Emitter of NPN transistor	3.25	3.3	3.35	V
V_{V33FB}	3.3-V linear reg feedback			4	4.6	V
I_{V33FB}	Series pass base drive	V_{VIN} = 12 V		10		mA
Beta	Series NPN pass device		40			
EXTERNALLY SUPPLIED 3.3V POWER						
V_{V33D}, V_{V33DIO}	Digital 3.3-V power	T_A = 25°C	3		3.6	V
V_{V33A}	Analog 3.3-V power	T_A = 25°C	3		3.6	V
ANALOG INPUTS (MON1–MON13)						
V_{MON}	Input voltage range	MON1–MON9	0		2.5	V
		MON10–MON13	0.2		2.5	V
INL	ADC integral nonlinearity		–2.5		2.5	mV
I_{lkg}	Input leakage current	3 V applied to pin			100	nA
I_{OFFSET}	Input offset current	1-kΩ source impedance	–5		5	µA
R_{IN}	Input impedance	MON1–MON9, ground reference	8			MΩ
		MON10–MON13, ground reference	0.5	1.5	3	MΩ
C_{IN}	Input capacitance				10	pF
$t_{CONVERT}$	ADC sample period	14 voltages sampled, 3.89 µsec/sample		400		µsec
V_{REF}	ADC 2.5 V, internal reference accuracy	0°C to 125°C	–0.5		0.5	%
		–40°C to 125°C	–1		1	%
ANALOG INPUT (PMBUS_ADDRx, INTERNAL TEMP SENSE)						
I_{BIAS}	Bias current for PMBus Addr pins		9		11	µA
V_{ADDR_OPEN}	Voltage – open pin	PMBus_ADDR0, PMBus_ADDR1 open	2.26			V
V_{ADDR_SHORT}	Voltage – shorted pin	PMBus_ADDR0, PMBus_ADDR1 short to ground			0.124	V
$T_{Internal}$	Internal temperature-sense accuracy	Over range from 0°C to 100°C	–5		5	°C
DIGITAL INPUTS AND OUTPUTS						
V_{OL}	Low-level output voltage	I_{OL} = 6 mA(2), V_{33DIO} = 3 V			Dgnd + 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –6 mA(3), V_{33DIO} = 3 V	V_{33DIO} – 0.6V			V
V_{IH}	High-level input voltage	V_{33DIO} = 3 V	2.1		3.6	V
V_{IL}	Low-level input voltage	V_{33DIO} = 3.5 V			1.4	V

(1) Typical supply current values are based on device programmed but not configured, and no peripherals connected to any pins.
(2) The maximum total current, I_{OL}max, for all outputs combined, should not exceed 12 mA to hold the maximum voltage drop specified.
(3) The maximum total current, I_{OH}max, for all outputs combined, should not exceed 48 mA to hold the maximum voltage drop specified.

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
FAN CONTROL INPUTS AND OUTPUTS						
T_{PWM_FREQ}	FAN-PWM frequency	FPWM1-8	15.259		125000	kHz
		PWM1		10		
		PWM2		1		
		PWM3-4	0.001		7800	
$DUTY_{PWM}$	FAN-PWM duty cycle range		0		100	%
$Tach_{RANGE}$	FAN-TACH range	For 1 Tach pulse per revolution. At 2, 3 or 4 pulse/rev, divide by the value	30		300k	RPM
$Tach_{RES}$	FAN-TACH resolution	For 1 Tach pulse per revolution		30		RPM
t_{MIN}	FAN-TACH minimum pulse width	Either positive or negarive polarity	200			µs
MARGINING OUTPUTS						
T_{PWM_FREQ}	MARGINING-PWM frequency	FPWM1-8	15.260		125000	kHz
		PWM3-4	0.001		7800	
$DUTY_{PWM}$	MARGINING-PWM duty cycle range		0		100	%
SYSTEM PERFORMANCE						
V_{DD}Slew	Minimum V_{DD} slew rate	V_{DD} slew rate between 2.3 V and 2.9 V	0.25			V/ms
V_{RESET}	Supply voltage at which device comes out of reset	For power-on reset (POR)			2.4	V
t_{RESET}	Low-pulse duration needed at $\overline{RESET}$ pin	To reset device during normal operation	2			µS
f(PCLK)	Internal oscillator frequency	T_A = 125°C, T_A = 25°C	240	250	260	MHz
$t_{retention}$	Retention of configuration parameters	T_J = 25°C	100			Years
Write_Cycles	Number of nonvolatile erase/write cycles	T_J = 25°C	20			K cycles

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PMBus/SMBus/I²C

The timing characteristics and timing diagram for the communications interface that supports I²C, SMBus and PMBus is shown below.

I²C/SMBus/PMBus TIMING REQUIREMENTS

T_A = –40°C to 85°C, 3 V < V_{DD} < 3.6 V; typical values at T_A = 25°C and V_{CC} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FSMB	SMBus/PMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		400	kHz
FI2C	I²C operating frequency	Slave mode, SCL 50% duty cycle	10		400	kHz
$t_{(BUF)}$	Bus free time between start and stop		4.7			µs
$t_{(HD:STA)}$	Hold time after (repeated) start		0.26			µs
$t_{(SU:STA)}$	Repeated-start setup time		0.26			µs
$t_{(SU:STO)}$	Stop setup time		0.26			µs
$t_{(HD:DAT)}$	Data hold time	Receive mode	0			ns
$t_{(SU:DAT)}$	Data setup time		50			ns
$t_{(TIMEOUT)}$	Error signal/detect	See (1)			35	ms
$t_{(LOW)}$	Clock low period		0.5			µs
$t_{(HIGH)}$	Clock high period	See (2)	0.26		50	µs
$t_{(LOW:SEXT)}$	Cumulative clock low slave extend time	See (3)			25	ms
t_f	Clock/data fall time	See (4)			120	ns
t_r	Clock/data rise time	See (5)			120	ns

(1) The device times out when any clock low exceeds $t_{(TIMEOUT)}$.
(2) $t_{(HIGH)}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0] = 0).
(3) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) Fall time t_f = 0.9 VDD to (V_{IL}MAX – 0.15)
(5) Rise time t_r = (V_{IL}MAX – 0.15) to (V_{IH}MIN + 0.15)

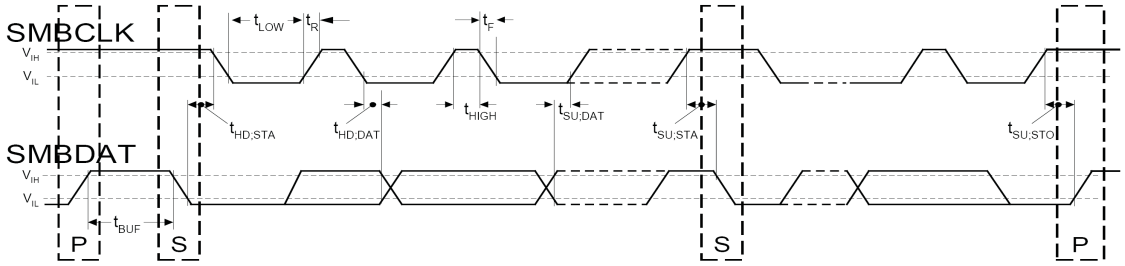


Figure 1. I²C/SMBus Timing Diagram

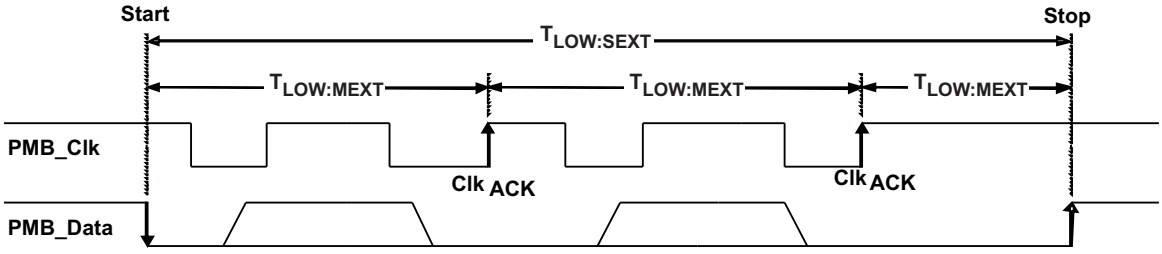


Figure 2. Bus Timing in Extended Mode

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DEVICE INFORMATION

UCD90124 PIN ASSIGNMENT

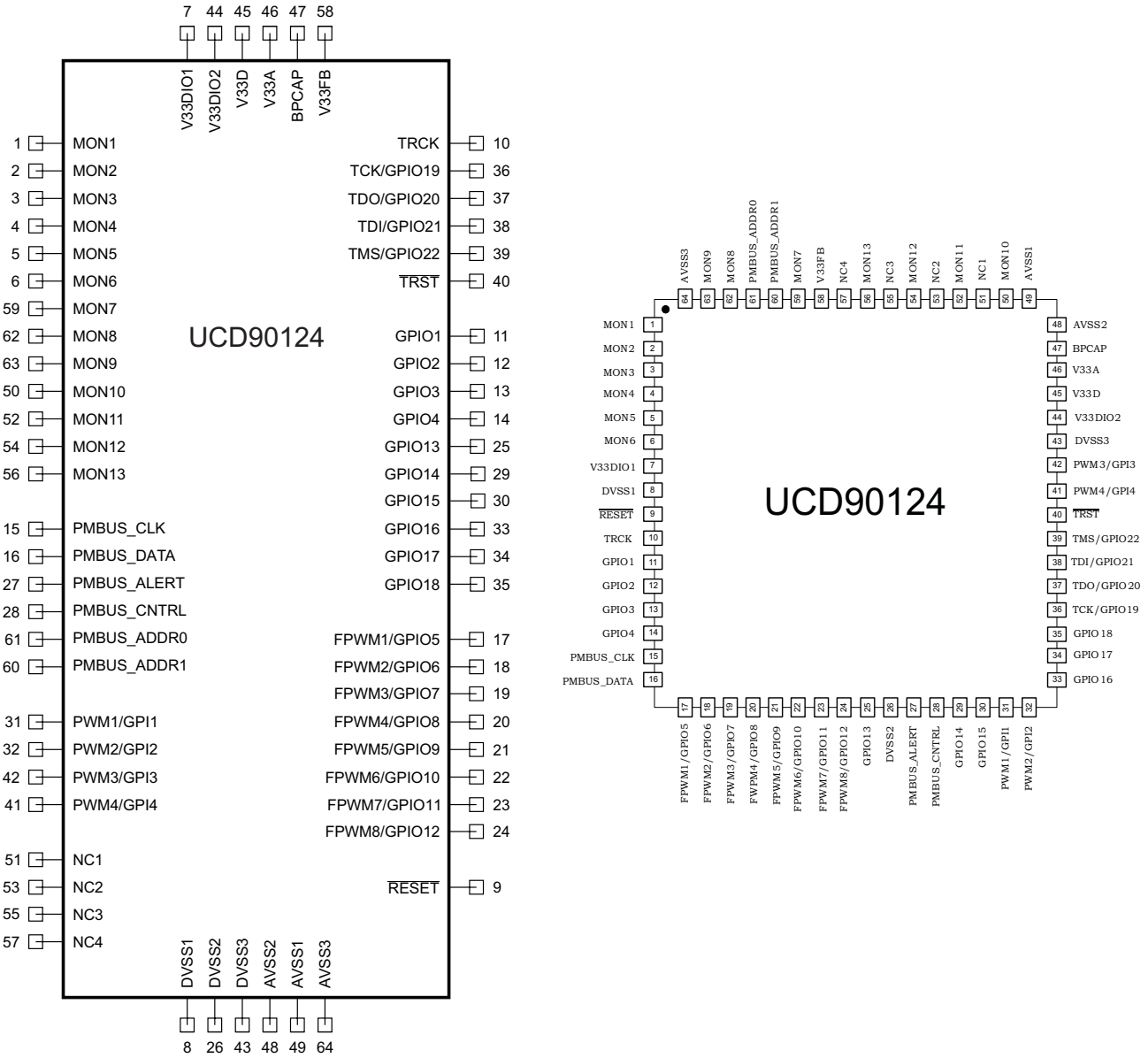


Table 1. PIN FUNCTIONS

PIN NAME	PIN NO.	I/O TYPE	DESCRIPTION
ANALOG MONITOR INPUTS			
MON1	1	I	Analog input (0 V–2.5 V)
MON2	2	I	Analog input (0 V–2.5 V)
MON3	3	I	Analog input (0 V–2.5 V)
MON4	4	I	Analog input (0 V–2.5 V)
MON5	5	I	Analog input (0 V–2.5 V)
MON6	6	I	Analog input (0 V–2.5 V)
MON7	59	I	Analog input (0 V–2.5 V)

Table 1. PIN FUNCTIONS (continued)

PIN NAME	PIN NO.	I/O TYPE	DESCRIPTION
MON8	62	I	Analog input (0 V–2.5 V)
MON9	63	I	Analog input (0 V–2.5 V)
MON10	50	I	Analog input (0.2 V–2.5 V)
MON11	52	I	Analog input (0.2 V–2.5 V)
MON12	54	I	Analog input (0.2 V–2.5 V)
MON13	56	I	Analog input (0.2 V–2.5 V)
GPIO			
GPIO1	11	I/O	General-purpose discrete I/O
GPIO2	12	I/O	General-purpose discrete I/O
GPIO3	13	I/O	General-purpose discrete I/O
GPIO4	14	I/O	General-purpose discrete I/O
GPIO13	25	I/O	General-purpose discrete I/O
GPIO14	29	I/O	General-purpose discrete I/O
GPIO15	30	I/O	General-purpose discrete I/O
GPIO16	33	I/O	General-purpose discrete I/O
GPIO17	34	I/O	General-purpose discrete I/O
GPIO18	35	I/O	General-purpose discrete I/O
PWM OUTPUTS			
FPWM1/GPIO5	17	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM2/GPIO6	18	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM3/GPIO7	19	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM4/GPIO8	20	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM5/GPIO9	21	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM6/GPIO10	22	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM7/GPIO11	23	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM8/GPIO12	24	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
PWM1/GPI1	31	I/PWM	Fixed 10-kHz PWM output or GPI
PWM2/GPI2	32	I/PWM	Fixed 1-kHz PWM output or GPI
PWM3/GPI3	42	I/PWM	PWM (0.93 Hz to 7.8125 MHz) or GPI
PWM4/GPI4	41	I/PWM	PWM (0.93 Hz to 7.8125 MHz) or GPI
PMBus COMM INTERFACE			
PMBUS_CLK	15	I/O	PMBus clock (must have pullup to 3.3 V)
PMBUS_DATA	16	I/O	PMBus data (must have pullup to 3.3 V)
PMBALERT#	27	O	PMBus alert, active-low, open-drain output (must have pullup to 3.3 V)
PMBUS_CNTRL	28	I	PMBus control
PMBUS_ADDR0	61	I	PMBus analog address input. Least-significant address bit
PMBUS_ADDR1	60	I	PMBus analog address input. Most-significant address bit
JTAG			
TRCK	10	O	Test return clock
TCK/GPIO19	36	I/O	Test clock or GPIO
TDO/GPIO20	37	I/O	Test data out or GPIO
TDI/GPIO21	38	I/O	Test data in (tie to V_{dd} with 10-kΩ resistor) or GPIO
TMS/GPIO22	39	I/O	Test mode select (tie to V_{dd} with 10-kΩ resistor) or GPIO
$\overline{\text{TRST}}$	40	I	Test reset – tie to ground with 10-kΩ resistor

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Table 1. PIN FUNCTIONS (continued)

PIN NAME	PIN NO.	I/O TYPE	DESCRIPTION
INPUT POWER AND GROUNDS			
$\overline{\text{RESET}}$	9		Active-low device reset input. Hold low for at least 2 μs to reset the device.
V33FB	58		3.3-V linear regulator feedback connection
V33A	46		Analog 3.3-V supply
V33D	45		Digital core 3.3-V supply
V33DIO1	7		Digital I/O 3.3-V supply
V33DIO2	44		Digital I/O 3.3-V supply
BPCap	47		1.8-V bypass capacitor – tie 0.1-μF capacitor to analog ground.
AVSS1	49		Analog ground
AVSS2	48		Analog ground
AVSS3	64		Analog ground
DVSS1	8		Digital ground
DVSS2	26		Digital ground
DVSS3	43		Digital ground
QFP ground pad	NA		Thermal pad – tie to ground plane.

FUNCTIONAL DESCRIPTION

TI FUSION GUI

The Texas Instruments *Fusion Digital Power Designer* is provided for device configuration. This PC-based graphical user interface (GUI) offers an intuitive I^2C/PMBus interface to the device. It allows the design engineer to configure the system operating parameters for the application without directly using PMBus commands, store the configuration to on-chip nonvolatile memory, and observe system status (voltage, temperature, etc). Fusion is referenced throughout the data sheet and many sections include screenshots.

PMBUS INTERFACE

The PMBus is a serial interface specifically designed to support power management. It is based on the SMBus interface that is built on the I^2C physical specification. The UCD90124 supports revision 1.1 of the PMBus standard. Wherever possible, standard PMBus commands are used to support the function of the device. For unique features of the UCD90124, MFR_SPECIFIC commands are defined to configure or activate those features. These commands are defined in the UCD90xxx Sequencer and System Health Controller PMBUS Command Reference (SLVU352).

This document makes frequent mention of the PMBus specification. Specifically, this document is *PMBus Power System Management Protocol Specification Part II – Command Language*, Revision 1.1, dated 5 February 2007. The specification is published by the Power Management Bus Implementers Forum and is available from www.pmbus.org.

The UCD90124 is PMBus compliant, in accordance with the *Compliance* section of the PMBus specification. The firmware is also compliant with the SMBus 1.1 specification, including support for the SMBus ALERT function. The hardware can support either 100-kHz or 400-kHz PMBus operation.

THEORY OF OPERATION

Modern electronic systems often use numerous microcontrollers, DSPs, FPGAs, and ASICs. Each device can have multiple supply voltages to power the core processor, analog-to-digital converter or I/O. These devices are typically sensitive to the order and timing of how the voltages are sequenced on and off. The UCD90124 can sequence supply voltages to prevent malfunctions, intermittent operation, or device damage caused by improper power up or power down. Appropriate handling of under- and overvoltage faults, overcurrent faults and overtemperature faults can extend system life and improve long term reliability. The UCD90124 stores power supply faults to on-chip nonvolatile flash memory for aid in system failure analysis.

Tach monitor inputs, PWM outputs and temperature measurements can be combined with a choice between two built-in fan-control algorithms to provide a stand-alone fan controller for independent operation of up to four fans.

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System reliability can be improved through four-corner testing during system verification. During four-corner testing, the system is operated at the minimum and maximum expected ambient temperature and with each power supply set to the minimum and maximum output voltage, commonly referred to as margining. The UCD90124 can be used to implement accurate closed-loop margining of up to 10 power supplies.

The UCD90124 12-rail sequencer can be used in a PMBus- or pin-based control environment. The TI Fusion GUI provides a powerful but simple interface for configuring sequencing solutions for systems with between one and 12 power supplies using 13 analog voltage-monitor inputs, four GPIs and 22 highly configurable GPIOs. A rail can include voltage, temperature, current, a power-supply enable and a margining output. At least one must be included in a rail definition. Once the user has defined how the power-supply rails should operate in a particular system, analog input pins and GPIOs can be selected to monitor and enable each supply (Figure 3).

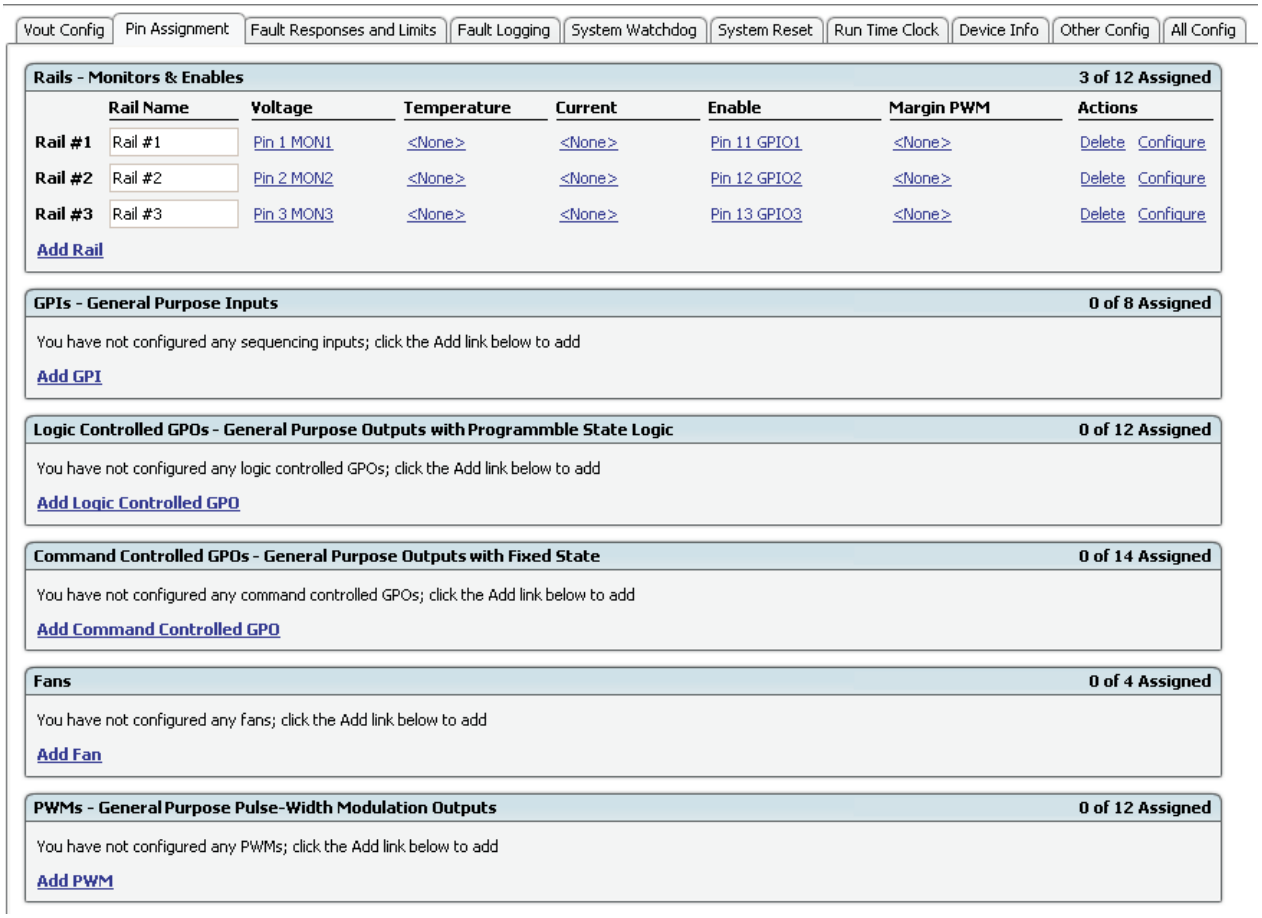


Figure 3. Fusion Pin-Assignment Tab

After the pins have been configured, other key monitoring and sequencing criteria are selected for each rail from the Vout Config tab (Figure 4):

- Nominal operating voltage (Vout)
- Undervoltage (UV) and overvoltage (OV) warning and fault limits
- Margin-low and margin-high values
- Power-good on and power-good off limits
- PMBus or pin-based sequencing control (On/Off Config)
- Rails that must achieve power good, or input pins that must be at a defined logic state before a rail is enabled (rail and input-pin sequence-on dependencies)
- Turn-on and turn-off delay timing
- Maximum time allowed for a rail to reach POWER_GOOD_ON or POWER_GOOD_OFF after being enabled or disabled

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- Other rails to turn off in case of a fault on a rail (fault-shutdown slaves)

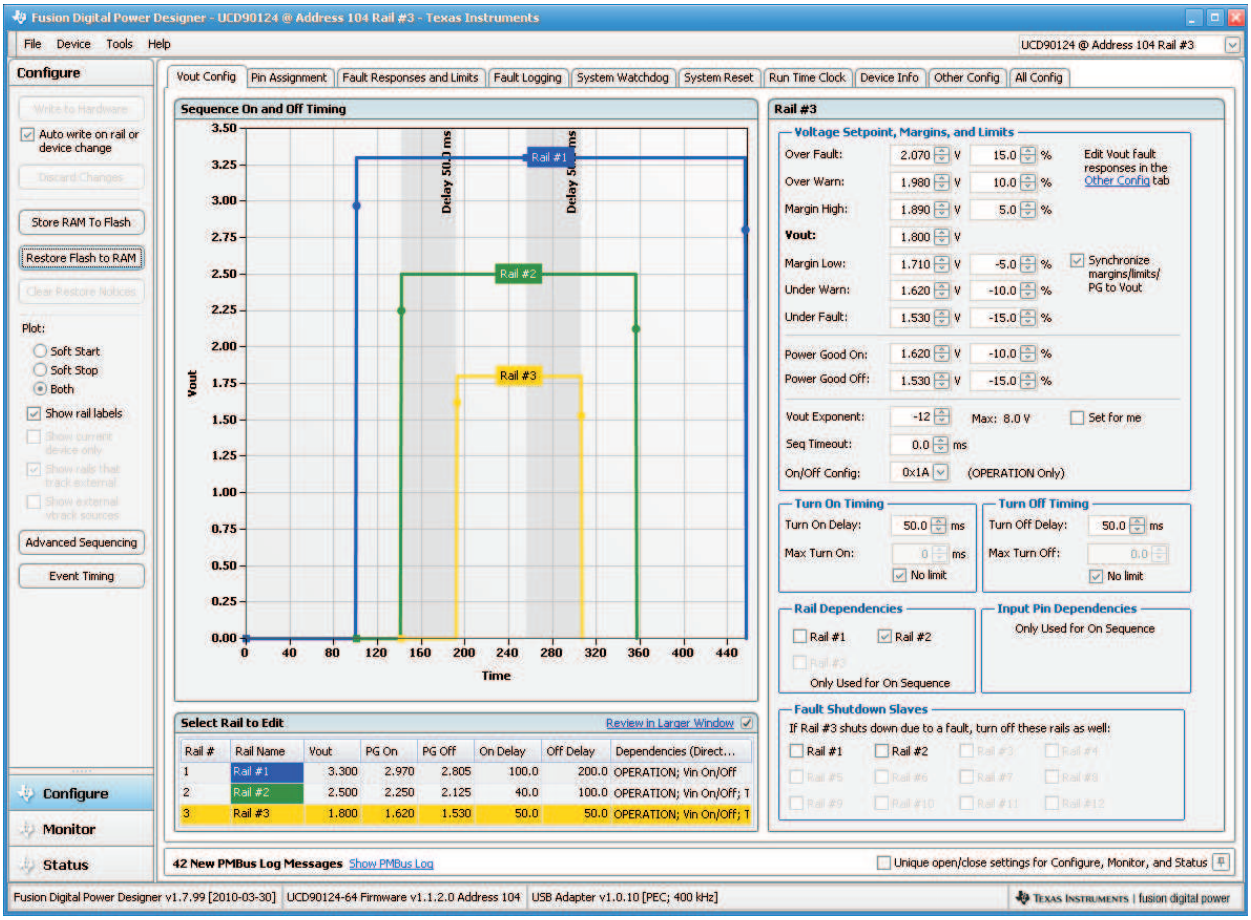


Figure 4. Fusion V_{OUT}-Config Tab

The **Synchronize margins/limits/PG to Vout** checkbox is an easy way to change the nominal operating voltage of a rail and also update all of the other limits associated with that rail according to the percentages shown to the right of each entry.

The plot in the upper left section of Figure 4 shows a simulation of the overall sequence-on and sequence-off configuration, including the nominal voltage, the turn-on and turn-off delay times, the power-good on and power-good off voltages and any timing dependencies between the rails.

After a rail voltage has reached its POWER_GOOD_ON voltage and is considered to be in regulation, it is compared against two UV and two OV thresholds in order to determine if a warning or fault limit has been exceeded. If a fault is detected, the UCD90124 responds based on a variety of flexible, user-configured options. Faults can cause rails to restart, shut down immediately, sequence off using turn-off delay times or shut down a group of rails and sequence them back on. Different types of faults can result in different responses.

Fault responses, along with a number of other parameters including user-specific manufacturing information and external scaling and offset values, are selected in the different tabs within the Configure funciton of Fusion software. Once the configuration satisfies the user requirements, it can be written to device SRAM if Fusion is connected to a UCD90124 using an I^2C/PMBus. SRAM contents can then be stored to data flash memory so that the configuration remains in the device after a reset or power cycle.

The Fusion Monitor page has a number of options, including a device dashboard and a system dashboard, for viewing and controlling device and system status.

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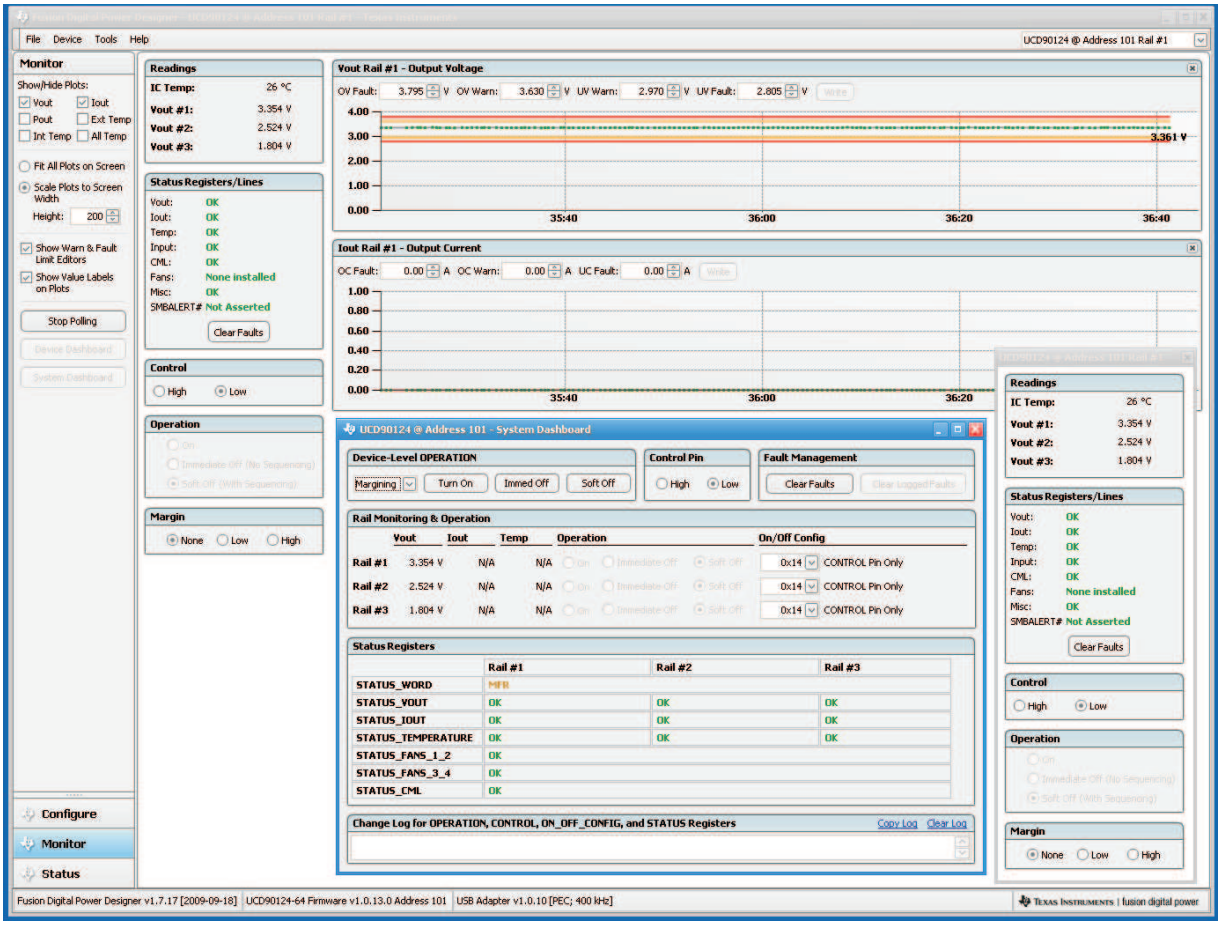


Figure 5. Fusion Monitor Page with Device Dashboard and System Dashboard

The UCD90124 also has status registers for each rail and the capability to log faults to flash memory for use in system troubleshooting. This is helpful in the event of a power-supply or system failure. The status registers (Figure 6) and the fault log (Figure 7) are available in Fusion. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference and the PMBus Specification* for detailed descriptions of each status register and supported PMBus commands.

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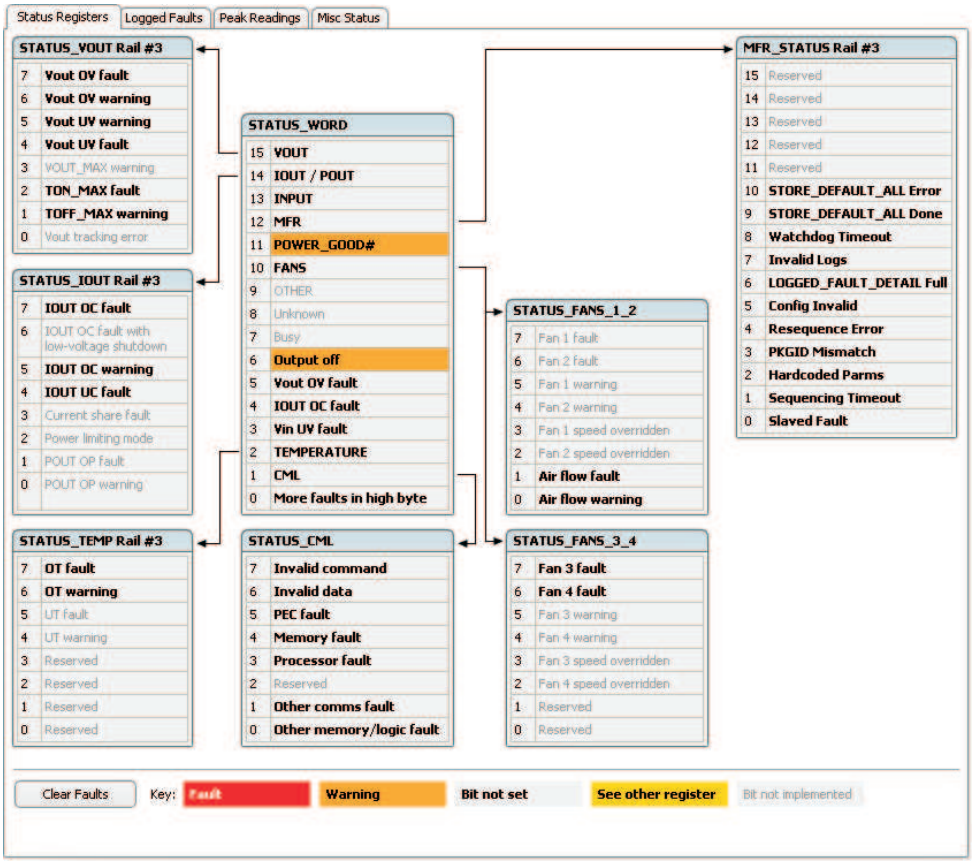


Figure 6. Fusion Rail-Status Register

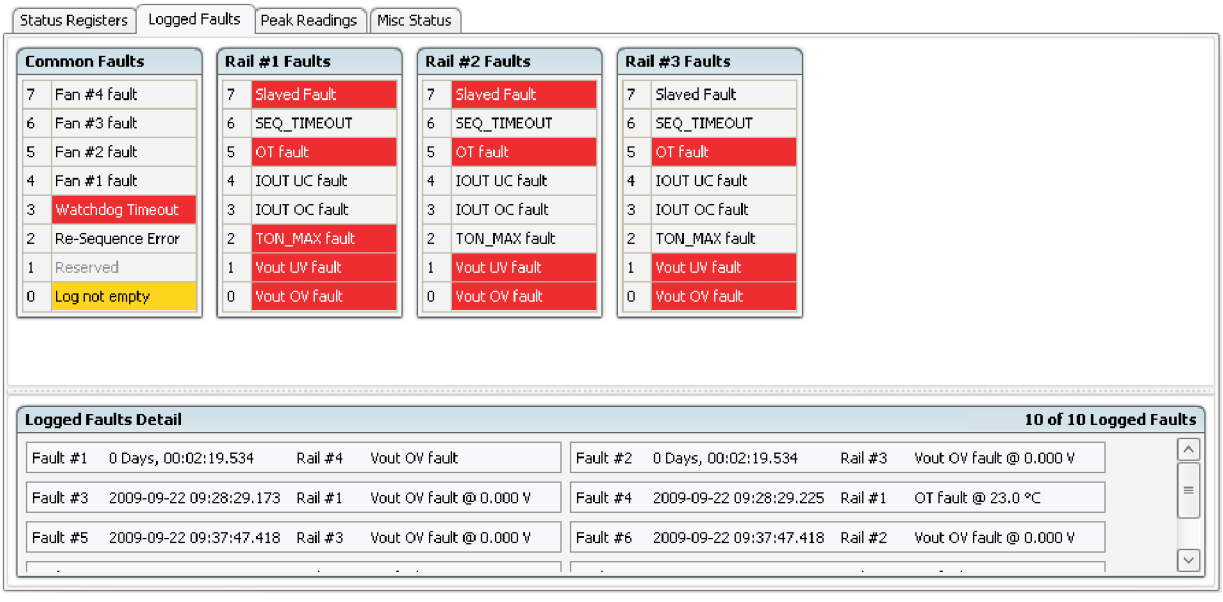


Figure 7. Fusion Flash-Error Log (Logged Faults)

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POWER-SUPPLY SEQUENCING

The UCD90124 can control the turn-on and turn-off sequencing of up to 12 voltage rails by using a GPIO to set a power-supply enable pin high or low. In PMBus-based designs, the system PMBus master can initiate a sequence-on event by asserting the PMBUS_CNTRL pin or by sending the OPERATION command over the I^2C serial bus. In pin-based designs, the PMBUS_CNTRL pin can also be used to sequence-on and sequence-off.

The auto-enable setting ignores the OPERATION command and the PMBUS_CNTRL pin. Sequence-on is started at power up after any dependencies and time delays are met for each rail. A rail is considered to be on or within regulation when the measured voltage for that rail crosses the power-good on (POWER_GOOD_ON(1)) limit. The rail is still in regulation until the voltage drops below power-good off (POWER_GOOD_OFF).

(1) In this document configuration parameters such as Power Good On are referred to using Fusion GUI names. The UCD90xxx Sequencer and System Health Controller PMBus Command Reference name is shown in parentheses (POWER_GOOD_ON) the first time the parameter appears.

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Turn-on Sequencing

The following sequence-on options are supported for each rail:

- Monitor only – do not sequence-on
- Fixed delay time after a PMBus OPERATION command to turn on
- Fixed delay time after assertion of the PMBUS_CNTRL pin
- Fixed time after one or a group of parent rails achieves regulation
- Fixed time after a designated GPI has reached a user-specified state
- Any combination of the previous options

The maximum TON_DELAY time is 3276 ms.

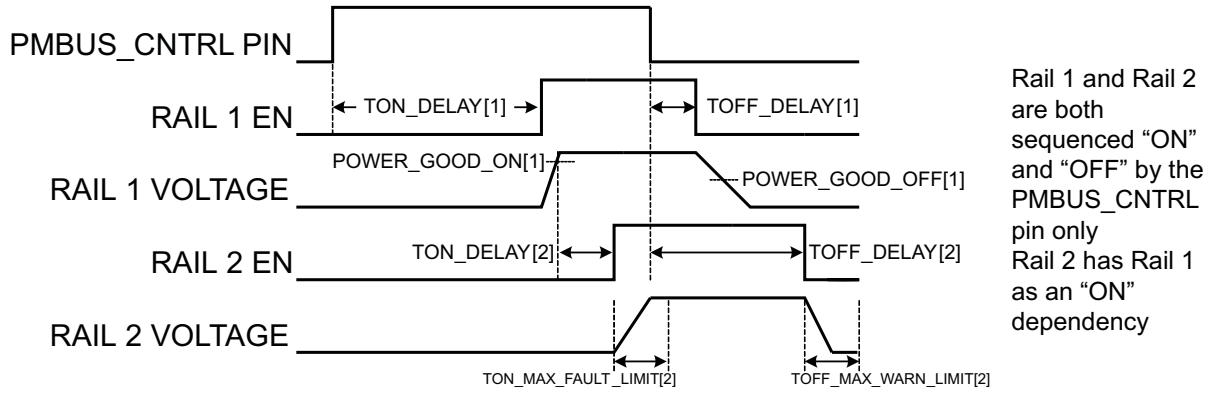


Figure 8. Sequence-on and Sequence-off Timing

Turn-off Sequencing

The following sequence-off options are supported for each rail:

- Monitor only – do not sequence-off
- Fixed delay time after a PMBus OPERATION command to turn off
- Fixed delay time after deassertion of the PMBUS_CNTRL pin
- Fixed delay time in response to an undervoltage, overvoltage, undercurrent, overcurrent, undertemperature, overtemperature, or max turn-on fault on the rail
- Fixed delay time in response to a fault on a different rail when set as a fault shutdown slave to the faulted rail

The maximum TOFF_DELAY time is 3276 ms.

Sequencing Configuration Options

In addition to the turn-on and turn-off sequencing options, the time between when a rail is enabled and when the monitored rail voltage must reach its power-good-on setting can be configured using max turn-on (TON_MAX_FAULT_LIMIT). Max turn-on can be set in 1-ms increments. A value of 0 ms means that there is no limit and the device can try to turn on the output voltage indefinitely.

Rails can be configured to turn off immediately or to sequence-off according to user-defined delay times. A sequenced shutdown is configured by selecting the appropriate turn-off delay (TOFF_DELAY) times for each rail. The turn-off delay times begin when the PMBUS_CNTRL pin is deasserted, when the PMBus OPERATION command is used to give a soft-stop command, or when a fault occurs on a rail that has other rails set as fault-shutdown slaves.

Shutdowns on one rail can initiate shutdowns of other rails or controllers. In systems with multiple UCD90124s, it is possible for each controller to be both a master and a slave to another controller.

VOLTAGE MONITORING

Up to 13 voltages can be monitored using the analog input pins. The input voltage range is 0 V–2.5 V for MON pins 1–6, 59, 62 and 63. Pins 50, 52, 54, and 56 can measure down to 0.2 V. Any voltage between 0 V and 0.2 V on these pins is read as 0.2 V. External resistors can be used to attenuate voltages higher than 2.5 V.

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The ADC operates continuously, requiring 3.89 μs to convert a single analog input and 54.5 μs to convert all 14 of the analog inputs, including the onboard temperature sensor. Each rail is sampled by the sequencing and monitoring algorithm every 400 μs. The maximum source impedance of any sampled voltage should be less than 4 kΩ. The source impedance limit is particularly important when a resistor-divider network is used to lower the voltage applied to the analog input pins.

MON1 - MON6 can be configured using digital hardware comparators, which can be used to achieve faster fault responses. Each hardware comparator has four thresholds (two UV (Fault and Warning) and two OV (Fault and Warning)). The hardware comparators respond to UV or OV conditions in about 80 μs (faster than 400 μs for the ADC inputs) and can be used to disable rails or assert GPOs. The only fault response available for the hardware comparators is to shut down immediately.

An internal 2.5-V reference is used by the ADC. The ADC reference has a tolerance of ±0.5% between 0°C and 125°C and a tolerance of ±1% between –40°C and 125°C. An external voltage divider is required for monitoring voltages higher than 2.5 V. The nominal rail voltage and the external scale factor can be entered into the Fusion GUI and are used to report the actual voltage being monitored instead of the ADC input voltage. The nominal voltage is used to set the range and precision of the reported voltage according to Table 2.

Table 2. Voltage Range and Resolution

VOLTAGE RANGE (Volts)	RESOLUTION (millivolts)
0 to 63.99805	1.95313
0 to 31.99902	0.97656
0 to 15.99951	0.48828
0 to 7.99976	0.24414
0 to 3.99988	0.12207

Although the monitor results can be reported with a resolution of about 15 μV, the real conversion resolution of 610 μV is fixed by the 2.5-V reference and the 12-bit ADC.

The MON pins can directly measure voltages, but each input can be defined as a voltage, current, or temperature. A single rail can include all three measurement types, each monitored on separate MON pins. If a rail has both voltage and current assigned to it, then power can be calculated and reported for the rail. Digital filtering applied to each MON input depends on the type of signal. Voltage inputs have no filtering. Current and temperature inputs have a low-pass filter.

CURRENT MONITORING

Current can be monitored using the analog inputs. External circuitry, see Figure 9, must be used in order to convert the current to a voltage within the range of the UCD90124 MONx input being used.

If a monitor input is configured as a current, the measurements are smoothed by a sliding-average digital filter. The current for 1 rail is measured every 200μs. If the device is programmed to support 10 rails (independent of current not being monitored at all rails), then each rail's current will get measured every 2ms. The current calculation is done with a sliding average using the last 4 measurements. The filter reduces the probability of false fault detections, and introduces a small delay to the current reading. If a rail is defined with a voltage monitor and a current monitor, then monitoring for undercurrent warnings begins once the rail voltage reaches POWER_GOOD_ON. If the rail does not have a voltage monitor, then current monitoring begins after TON_DELAY.

The device supports multiple PMBus commands related to current, including READ_IOUT, which reads external currents from the MON pins; IOUT_OC_FAULT_LIMIT, which sets the overcurrent fault limit; IOUT_OC_WARN_LIMIT, which sets the overcurrent warning limit; and IOUT_UC_FAULT_LIMIT, which sets the undercurrent fault limit. The *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* contains a detailed description of how current fault responses are implemented using PMBus commands.

IOUT_CAL_GAIN is a PMBus command that allows the scale factor of an external current sensor and any amplifiers or attenuators between the current sensor and the MON pin to be entered by the user in milliohms. IOUT_CAL_OFFSET is the current that results in 0 V at the MON pin. The combination of these PMBus commands allows current to be reported in amperes. The example below using the INA196 would require programming IOUT_CAL_GAIN to Rsense(mΩ)×20.

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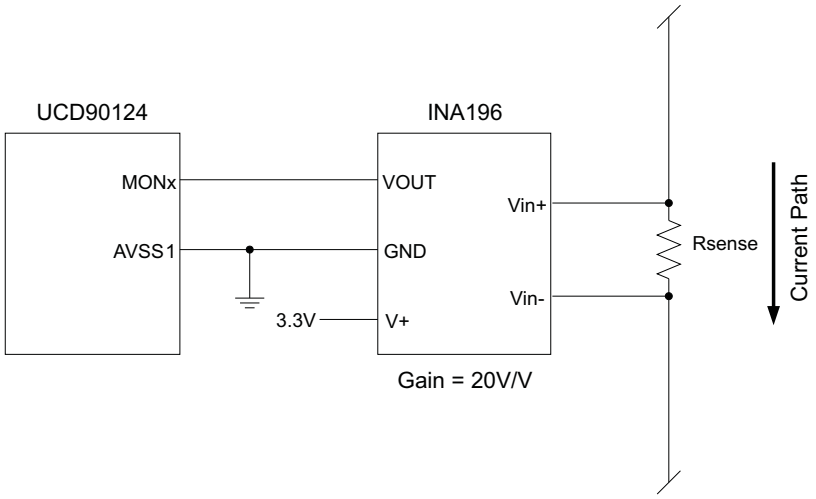


Figure 9. Current Monitoring Circuit Example Using the INA196

REMOTE TEMPERATURE MONITORING AND INTERNAL TEMPERATURE SENSOR

The UCD90124 has support for internal and remote temperature sensing. The internal temperature sensor requires no calibration and can report the device temperature via the PMBus interface. The remote temperature sensor can report the remote temperature by using a configurable gain and offset for the type of sensor that is used in the application such as a linear temperature sensor (LTS) connected to the analog inputs.

External circuitry must be used in order to convert the temperature to a voltage within the range of the UCD90124 MONx input being used.

If an input is configured as a temperature, the measurements are smoothed by a sliding average digital filter. The temperature for 1 rail is measured every 100ms. If the device is programmed to support 10 rails (independent of temperature not being monitored at all rails), then each rail's temperature will get measured every 1s. The temperature calculation is done with a sliding average using the last 16 measurements. The filter reduces the probability of false fault detections, and introduces a small delay to the temperature reading. The internal device temperature is measured using a silicon diode sensor with an accuracy of ±5°C and is also monitored using the ADC. Temperature monitoring begins immediately after reset and initialization.

The device supports multiple PMBus commands related to temperature, including READ_TEMPERATURE_1, which reads the internal temperature; READ_TEMPERATURE_2, which reads external temperatures; and OT_FAULT_LIMIT and OT_WARN_LIMIT, which set the overtemperature fault and warning limit. The *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* contains a detailed description of how temperature-fault responses are implemented using PMBus commands.

TEMPERATURE_CAL_GAIN is a PMBus command that allows the scale factor of an external temperature sensor Figure 10and any amplifiers or attenuators between the temperature sensor and the MON pin to be entered by the user in °C/V. TEMPERATURE_CAL_OFFSET is the temperature that results in 0 V at the MON pin. The combination of these PMBus commands allows temperature to be reported in degrees Celsius.

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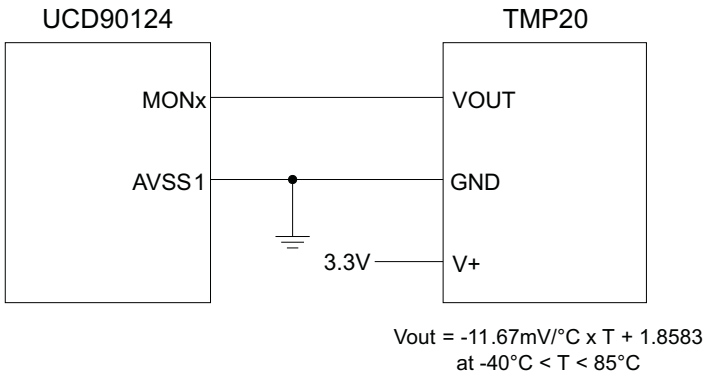


Figure 10. Remote Temperature Monitoring Circuit Example Using the TMP20

FAULT RESPONSES AND ALERT PROCESSING

Software monitors that the rail stays within a window of normal operation. There are two programmable warning levels (under and over) and two programmable fault levels (under and over). When any monitored voltage, current, or temperature goes outside of the warning or fault window, the PMBALERT# pin is asserted immediately, and the appropriate bits are set in the PMBus status registers (see Figure 6). Detailed descriptions of the status registers are provided in the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* and the *PMBus Specification.*

A programmable glitch filter can be enabled or disabled for each MON input. A glitch filter for an input defined as a voltage can be set between 0 and 102 ms with 400-µs resolution. A glitch filter for an input defined as a current or temperature can be between 0 and 25.5 seconds with 100-ms resolution. The longer time constants are due to the fixed low-pass digital filters associated with current and temperature inputs.

Fault-response decisions are based on results from the 12-bit ADC. The device cycles through the ADC results and compares them against the programmed limits. The time to respond to an individual event is determined by when the event occurs within the ADC conversion cycle and the selected fault response.

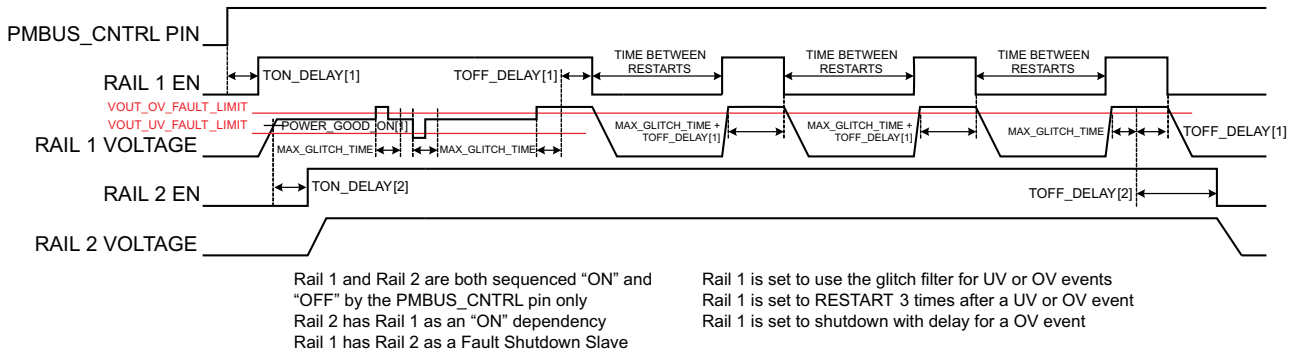


Figure 11. Sequencing and Fault-Response Timing

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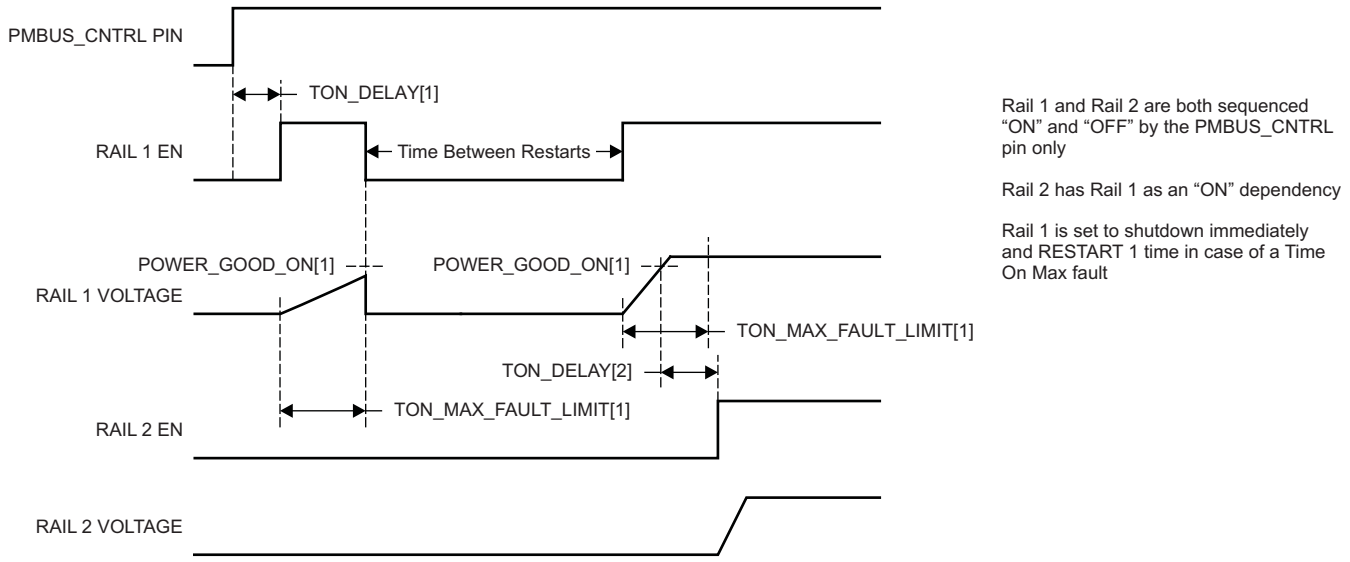


Figure 12. Maximum Turn-on Fault

The configurable fault limits are:

Maximum turn-on fault – Flagged if a rail that is enabled does not reach the POWER_GOOD_ON limit within the configured time

Undervoltage warning – Flagged if a voltage rail drops below the specified UV warning limit after reaching the POWER_GOOD_ON setting

Undervoltage fault – Flagged if a rail drops below the specified UV fault limit after reaching the POWER_GOOD_ON setting

Overvoltage warning – Flagged if a rail exceeds the specified OV warning limit at any time during startup or operation

Overvoltage fault – Flagged if a rail exceeds the specified OV fault limit at any time during startup or operation

Maximum turn-off warning – Flagged if a rail that is commanded to shut down does not reach 12.5% of the nominal rail voltage within the configured time

Faults are more serious than warnings. The PMBALERT# pin is always asserted immediately if a warning or fault occurs. If a warning occurs, the following takes place:

Warning Actions

- Immediately assert the PMBALERT# pin
- Status bit is flagged
- Assert a GPIO pin (optional)
- Warnings are not logged to flash

A number of fault response options can be chosen from:

Fault Responses

- *Continue Without Interruption:* Flag the fault and take no action
- *Shut Down Immediately:* Shut down the faulted rail immediately and restart according to the rail configuration

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— *Shut Down using TOFF_DELAY:* If a fault occurs on a rail, exhaust whatever retries are configured. If the rail does not come back, schedule the shutdown of this rail and all fault-shutdown slaves. All selected rails, including the faulty rail, are sequenced off according to their T_OFF_DELAY times. If Do Not Restart is selected, then sequence off all selected rails when the fault is detected.

Restart

— *Do Not Restart:* Do not attempt to restart a faulted rail after it has been shut down.

— *Restart Up To N Times:* Attempt to restart a faulted rail up to 14 times after it has been shut down. The time between restarts is measured between when the rail enable pin is deasserted (after any glitch filtering and turn-off delay times, if configured to observe them) and then reasserted. It can be set between 0 and 1275 ms in 5-ms increments.

— *Restart Continuously:* Same as *Restart Up To N Times* except that the device continues to restart until the fault goes away, it is commanded off by the specified combination of PMBus OPERATION command and PMBUS_CNTRL pin status, the device is reset, or power is removed from the device.

— *Shut Down Rails and Sequence On (Re-sequence):* Shut down selected rails immediately or after continue-operation time is reached and then sequence-on those rails using turn-on delay times

SHUT DOWN ALL RAILS AND SEQUENCE ON (RE-SEQUENCE)

In response to a fault, the UCD90124 can be configured to turn off a set of rails and then sequence them back on. To sequence all rails in the system, then all rails must be selected as fault-shutdown slaves of the faulted rail. If the faulted rail is set to stop immediately or stop with delay, then the rails designated as fault-shutdown slaves behave the same way. Shut-down-all-rails and sequence-on are not performed until retries are exhausted for a given fault.

While waiting for the rails to turn off, an error is reported if any of the rails reaches its TOFF_MAX_WARN_LIMIT. There is a configurable option to continue with the resequencing operation if this occurs. After the faulted rail and fault-shutdown slaves sequence-off, the UCD90124 waits for a programmable delay time between 0 and 1275 ms in increments of 5 ms and then sequences-on the faulted rail and fault-shutdown slaves according to the start-up sequence configuration. This is repeated until the faulted rail and fault-shutdown slaves successfully achieve regulation or for a user-selected 1, 2, 3, or 4 times. If the resequence operation is successful, the resequence counter is reset if all of the rails that were resequenced maintain normal operation for one second.

Once shut-down-all-rails and sequence-on begin, any faults on the fault-shutdown slave rails are ignored. If there are two or more simultaneous faults with different fault-shutdown slaves, the more conservative action is taken. For example, if a set of rails is already on its second resequence and the device is configured to resequence three times, and another set of rails enters the resequence state, that second set of rails is only resequenced once. Another example – if one set of rails is waiting for all of its rails to shut down so that it can resequence, and another set of rails enters the resequence state, the device now waits for all rails from both sets to shut down before resequencing.

GPIOs

The UCD90124 has 22 GPIO pins that can function as either inputs or outputs. Each GPIO has configurable output mode options including open-drain or push-pull outputs that can be actively driven to 3.3 V or ground. There are an additional four pins that can be used as either inputs or PWM outputs but not as GPOs. Table 3 lists possible uses for the GPIO pins and the maximum number of each type for each use. GPIO pins can be dependents in sequencing and alarm processing. They can also be used for system-level functions such as external interrupts, power-goods, resets, or for the cascading of multiple devices. GPOs can be sequenced up or down by configuring a rail without a MON pin but with a GPIO set as an enable.

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Table 3. GPIO Pin Configuration Options

PIN NAME	PIN	RAIL EN (12 MAX)	GPI (8 MAX)	GPO (12 MAX)	FAN TACH (4 MAX)	FAN PWM (4 MAX)	PWM OUT (12 MAX)	MARGIN PWM (10 MAX)
FPWM1/GPIO5	17	X	X	X	X	X	X	X
FPWM2/GPIO6	18	X	X	X	X	X	X	X
FPWM3/GPIO7	19	X	X	X	X	X	X	X
FPWM4/GPIO8	20	X	X	X	X	X	X	X
FPWM5/GPIO9	21	X	X	X	X	X	X	X
FPWM6/GPIO10	22	X	X	X	X	X	X	X
FPWM7/GPIO11	23	X	X	X	X	X	X	X
FPWM8/GPIO12	24	X	X	X	X	X	X	X
FANTAC1/GPI1/PWM1	31		X		X	X	X	
FANTAC2/GPI2/PWM2	32		X		X	X	X	
FANTAC3/GPI3/PWM3	42		X		X	X	X	X
FANTAC4/GPI4/PWM4	41		X		X	X	X	X
GPIO1	11	X	X	X	X			
GPIO2	12	X	X	X	X			
GPIO3	13	X	X	X	X			
GPIO4	14	X	X	X	X			
GPIO13	25	X	X	X	X			
GPIO14	29	X	X	X	X			
GPIO15	30	X	X	X	X			
GPIO16	33	X	X	X	X			
GPIO17	34	X	X	X	X			
GPIO18	35	X	X	X	X			
TCK/GPIO19	36	X	X	X	X			
TDO/GPIO20	37	X	X	X	X			
TDI/GPIO21	38	X	X	X	X			
TMS/GPIO22	39	X	X	X	X			

GPO Control

The GPIOs when configured as outputs can be controlled by PMBus commands or through logic defined in internal Boolean function blocks. Controlling GPOs by PMBus commands (GPIO_SELECT and GPIO_CONFIG) can be used to have control over LEDs, enable switches, etc. with the use of an I2C interface. See the UCD90xxx Sequencer and System Health Controller PMBus Command Reference for details on controlling a GPO using PMBus commands.

GPO Dependencies

GPIOs can be configured as outputs that are based on Boolean combinations of up to four ANDs all ORed together (Figure 13). Inputs to the logic blocks can include GPIs and rail-status flags. One rail status type is selectable as an input for each AND gate in a Boolean block. For a selected rail status, the status flags of all active rails can be included as inputs to the AND gate. *_LATCH* rail-status types stay asserted until cleared by a MFR PMBus command or by a specially configured GPI pin. The different rail-status types are shown in Figure 15. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for complete definitions of rail-status types.

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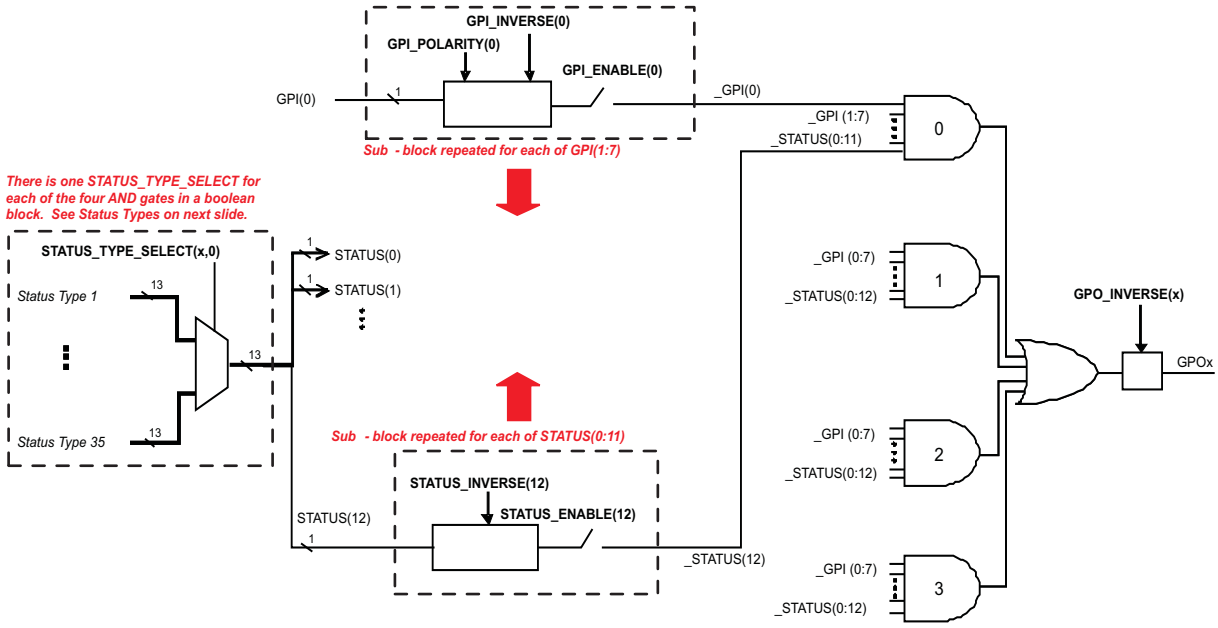


Figure 13. Boolean Logic Combinations

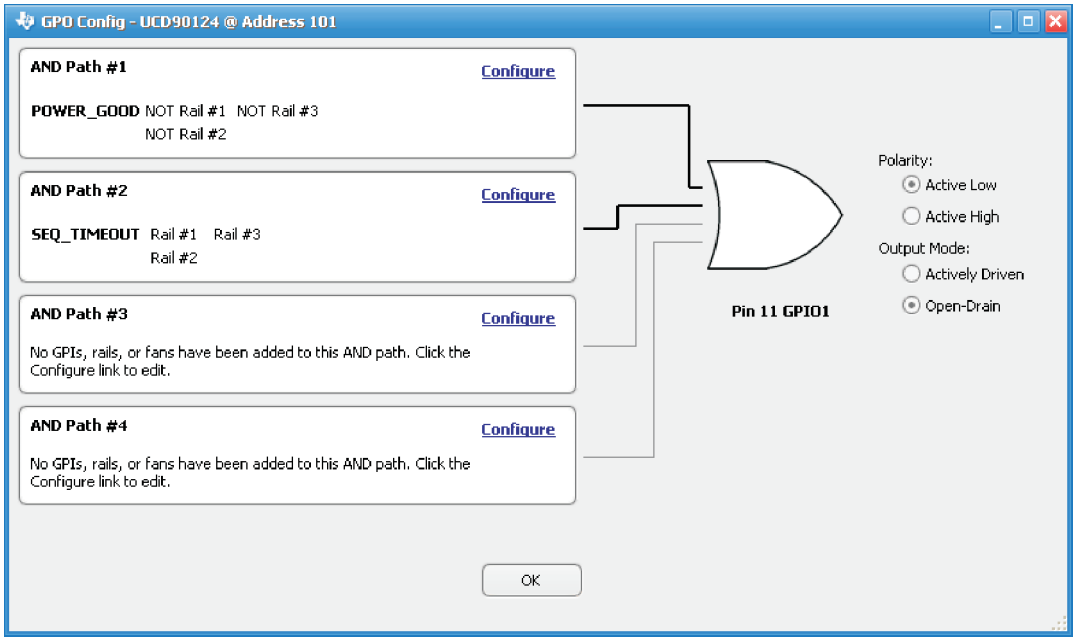


Figure 14. Fusion Boolean Logic Builder

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1.	POWER_GOOD(0:12)
2.	VOUT_OV_FAULT(0:12)
3.	VOUT_OV_FAULT_LATCH(0:12)
4.	VOUT_OV_WARN(0:12)
5.	VOUT_OV_WARN_LATCH(0:12)
6.	VOUT_UV_WARN(0:12)
7.	VOUT_UV_WARN_LATCH(0:12)
8.	VOUT_UV_FAULT(0:12)
9.	VOUT_UV_FAULT_LATCH(0:12)
10.	VOUT_TON_FAULT(0:12)
11.	VOUT_TON_FAULT_LATCH(0:12)
12.	VOUT_TOFF_WARN(0:12)
13.	VOUT_TOFF_WARN_LATCH(0:12)
14.	IOUT_OC_FAULT(0:12)
15.	IOUT_OC_FAULT_LATCH(0:12)
16.	IOUT_OC_WARN(0:12)
17.	IOUT_OC_WARN_LATCH(0:12)
18.	IOUT_UC_FAULT(0:12)
19.	IOUT_UC_FAULT_LATCH(0:12)

20.	TEMP_OT_FAULT(0:12)
21.	TEMP_OT_FAULT_LATCH(0:12)
22.	TEMP_OT_WARN(0:12)
23.	TEMP_OT_WARN_LATCH(0:12)
24.	INPUT_VIN_OV_FAULT(0:12)
25.	INPUT_VIN_OV_FAULT_LATCH(0:12)
26.	INPUT_VIN_OV_WARN(0:12)
27.	INPUT_VIN_OV_WARN_LATCH(0:12)
28.	INPUT_VIN_UV_WARN(0:12)
29.	INPUT_VIN_UV_WARN_LATCH(0:12)
30.	INPUT_VIN_UV_FAULT(0:12)
31.	INPUT_VIN_UV_FAULT_LATCH(0:12)
32.	MFR_SEQ_TIMEOUT(0:12)
33.	MFR_SEQ_TIMEOUT_LATCH(0:12)

Figure 15. Rail-Status Types

GPI Special Functions

There are five special input functions for which GPIs can be used. There can be no more than one pin assigned to each of these functions.

- **Sequencing Timeout Source** - If SEQ_TIMEOUT is non-zero on any rail, a fault will occur if this GPI pin does not go active within SEQ_TIMEOUT time after the rail reaches its power good state.
- **Latched Statuses Clear Source** - When a GPO uses a latched status type (_LATCH), you can configure a GPI that will clear the latched status.
- **Input Source for Margin Enable** - When this pin is asserted, all rails with margining enabled will be put in a margined state (low or high).
- **Input Source for Margin Low/Not-High** - When this pin is asserted all margined rails will be set to Margin Low as long as the Margin Enable is asserted. When this pin is de-asserted the rails will be set to Margin High.
- **Fans Installed** - Fan control is enabled while this pin is asserted.

The polarity of GPI pins can be configured to be either Active Low or Active High.

Power-Supply Enables

Each GPIO can be configured as a rail-enable pin with either active-low or active-high polarity. Output mode options include open-drain or push-pull outputs that can be actively driven to 3.3 V or ground. During reset, the GPIO pins are high-impedance except for FPWM/GPIO pins 17–24, which are driven low. External pulldown or pullup resistors can be tied to the enable pins to hold the power supplies off during reset. The UCD90124 can support a maximum of 12 enable pins.

Cascading Multiple Devices

A GPIO pin can be used to coordinate multiple controllers by using it as a power good-output from one device and connecting it to the PMBUS_CNTRL input pin of another. This imposes a master/slave relationship among multiple devices. During startup, the slave controllers initiate their start sequences after the master has completed its start sequence and all rails have reached regulation voltages. During shutdown, as soon as the master starts to sequence-off, it sends the shut-down signal to its slaves.

A shutdown on one or more of the master rails can initiate shutdowns of the slave devices. The master shutdowns can be initiated intentionally or by a fault condition. This method works to coordinate multiple controllers, but it does not enforce interdependency between rails within a single controller.

The PMBus specification implies that the power-good signal is active when ALL the rails in a controller are regulating at their programmed voltage. The UCD90124 allows GPIOs to be configured to respond to a desired subset of power-good signals.

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PWM Outputs

FPWM1-8

Pins 17–24 can be configured as fast pulse-width modulators (FPWMs). The frequency range is 15.260 kHz to 125 MHz. FPWMs can be configured as closed-loop margining outputs , fan controllers or general-purpose PWMs.

Any FPWM pin not used as a PWM output can be configured as a GPIO. One FPWM in a pair can be used as a PWM output and the other pin can be used as a GPO. The FPWM pins are actively driven low from reset when used as GPOs.

The frequency settings for the FPWMs apply to pairs of pins:

- FPWM1 and FPWM2 – same frequency
- FPWM3 and FPWM4 – same frequency
- FPWM5 and FPWM6 – same frequency
- FPWM7 and FPWM8 – same frequency

If an FPWM pin from a pair is not used while its companion is set up to function, it is recommended to configure the unused FPWM pin as an active-low open-drain GPO so that it does not disturb the rest of the system. By setting an FPWM, it automatically enables the other FPWM within the pair if it was not configured for any other functionality.

The frequency for the FPWM is derived by dividing down a 250MHz clock. To determine the actual frequency to which an FPWM can be set, must divide 250MHz by any integer between 2 and (2^{14}-1).

The FPWM duty cycle resolution is dependent on the frequency set for a given FPWM. Once the frequency is known the duty cycle resolution can be calculated as Equation 1.

$$\text{Change per Step } (\%)_{FPWM} = \text{frequency} \div (250 \times 10^6 \times 16) \quad (1)$$

Take for an example determining the actual frequency and the duty cycle resolution for a 75MHz target frequency.

1. Divide 250MHz by 75MHz to obtain 3.33.
2. Round off 3.33 to obtain an integer of 3.
3. Divide 250MHz by 3 to obtain actual closest frequency of 83.333MHz.
4. Use Equation 1 to determine duty cycle resolution to obtain 2.0833% duty cycle resolution.

PWM1-4

Pins 31, 32, 41, and 42 can be used as GPIs or PWM outputs.

If configured as PWM outputs, then limitations apply:

- PWM1 has a fixed frequency of 10 kHz
- PWM2 has a fixed frequency of 1 kHz
- PWM3 and PWM4 frequencies can be 0.93 Hz to 7.8125 MHz.

The frequency for PWM3 and PWM4 is derived by dividing down a 15.625MHz clock. To determine the actual frequency to which these PWMs can be set, must divide 15.625MHz by any integer between 2 and (2^{24}-1). The duty cycle resolution will be dependent on the set frequency for PWM3 and PWM4.

The PWM3 or PWM4 duty cycle resolution is dependent on the frequency set for the given PWM. Once the frequency is known the duty cycle resolution can be calculated as Equation 2

$$\text{Change per Step } (\%)_{PWM3/4} = \text{frequency} \div 15.625 \times 10^6 \quad (2)$$

To determine the closest frequency to 1MHz that PWM3 can be set to calculate as the following:

1. Divide 15.625MHz by 1MHz to obtain 15.625.
2. Round off 15.625 to obtain an integer of 16.
3. Divide 15.625MHz by 16 to obtain actual closest frequency of 976.563kHz.
4. Use Equation 2 to determine duty cycle resolution to obtain 6.25% duty cycle resolution.

All frequencies below 238Hz will have a duty cycle resolution of 0.0015%.

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Programmable Multiphase PWMs

The FPWMs can be aligned with reference to their phase. The phase for each FPWM is configurable from 0° to 360°. This provides flexibility in PWM-based applications such as power-supply controller, digital clock generation, and others. See an example of four FPWMs programmed to have phases at 0°, 90°, 180° and 270° (Figure 16).

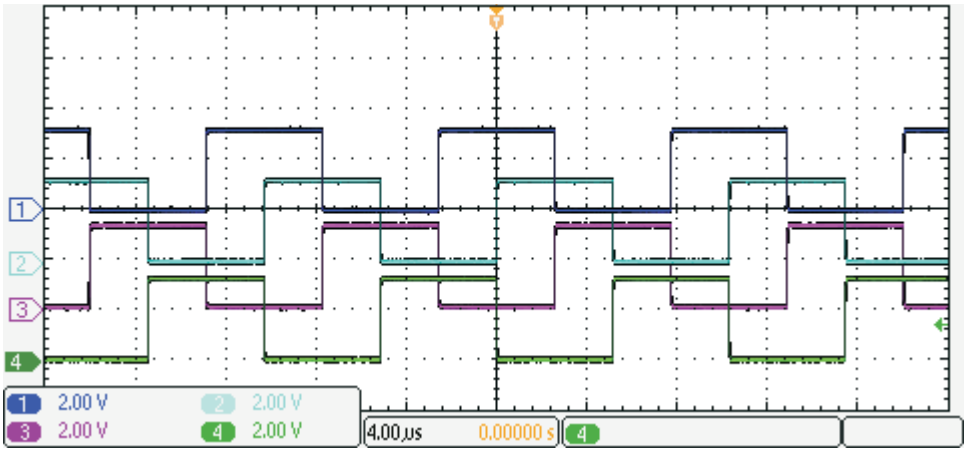


Figure 16. Multiphase PWMs

MARGINING

Margining is used in product validation testing to verify that the complete system works properly over all conditions, including minimum and maximum power-supply voltages, load range, ambient temperature range, and other relevant parameter variations. Margining can be controlled over PMBus using the OPERATION command or by configuring two GPIO pins as margin-EN and margin-UP/DOWN inputs. The MARGIN_CONFIG command in the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* describes different available margining options, including ignoring faults while margining and using closed-loop margining to trim the power-supply output voltage one time at power up.

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Open-loop margining is done by connecting a power-supply feedback node to ground through one resistor and to the margined power supply output (V_{OUT}) through another resistor. The power-supply regulation loop responds to the change in feedback node voltage by increasing or decreasing the power-supply output voltage to return the feedback voltage to the original value. The voltage change is determined by the fixed resistor values and the voltage at V_{OUT} and ground. Two GPIO pins must be configured as open-drain outputs for connecting resistors from the feedback node of each power supply to V_{OUT} or ground.

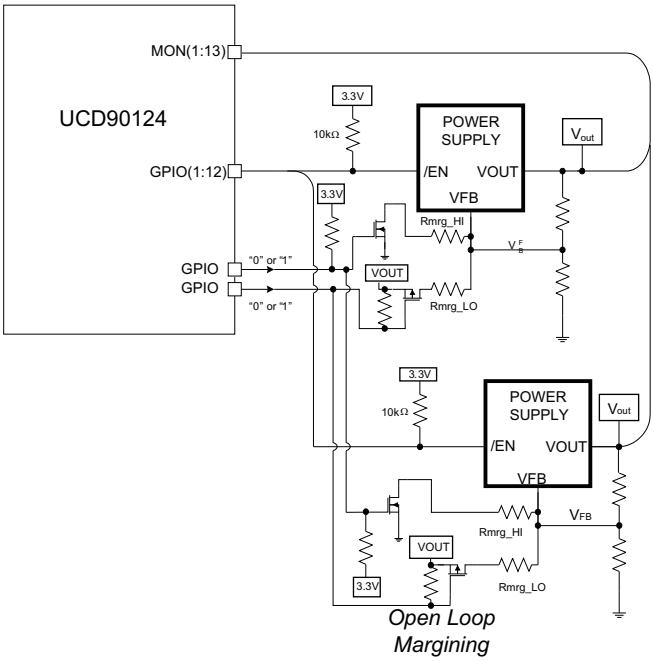


Figure 17. Open-Loop Margining

Closed-loop margining uses a PWM or FPWM output for each power supply that is being margined. An external RC network converts the FPWM pulse train into a DC margining voltage. The margining voltage is connected to the appropriate power-supply feedback node through a resistor. The power-supply output voltage is monitored, and the margining voltage is controlled by adjusting the PWM duty cycle until the power-supply output voltage reaches the margin-low and margin-high voltages set by the user. The voltage setting resolutions will be the same that applies to the voltage measurement resolution (Table 2). When using a closed-loop margining configuration it is important to determine the default duty cycle that is necessary to maintain the margined power-supply at the nominal operation voltage. Make note that if margining is configured, and the rail is not set to Margin High or Margin Low then the PWM used for margining will stay active and operate at the default duty cycle which will control the operation of the power supply. Given that this closed-loop system has feed back through the ADC, the closed-loop margining accuracy will be dominated by the ADC measurement. For more details on configuring the UCD90124 for margining, see the *Voltage Margining Using the UCD9012x* application note (SLVA375).

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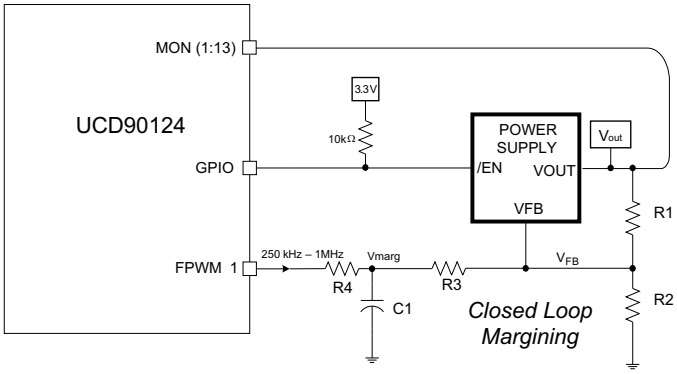


Figure 18. Closed-Loop Margining

FAN CONTROL

The UCD90124 can control and monitor up to four two-, three- or four-wire fans. Up to four GPIO pins can be used as tachometer inputs. The number of fan tach pulses per revolution for each fan can be entered using the Fusion GUI. A fan speed-fault threshold can be set to trigger an alarm if the measured speed drops below a user-defined value.

The two- and three-wire fans are controlled by connecting the positive input of the fan to the specified supply voltage for the fan. The negative input of the fan is connected to the collector or drain of a transistor. The transistor is turned off and on using a GPIO pin. Four-wire fans can be controlled the same way. However, four-wire fans should use the fan PWM input (the fourth wire). It can be driven directly by one of the eight FPWM or the two adjustable PWM outputs. The normal frequency range for the PWM input is 15 kHz to 40 kHz, but the specifications for the fan confirm the interface procedure.

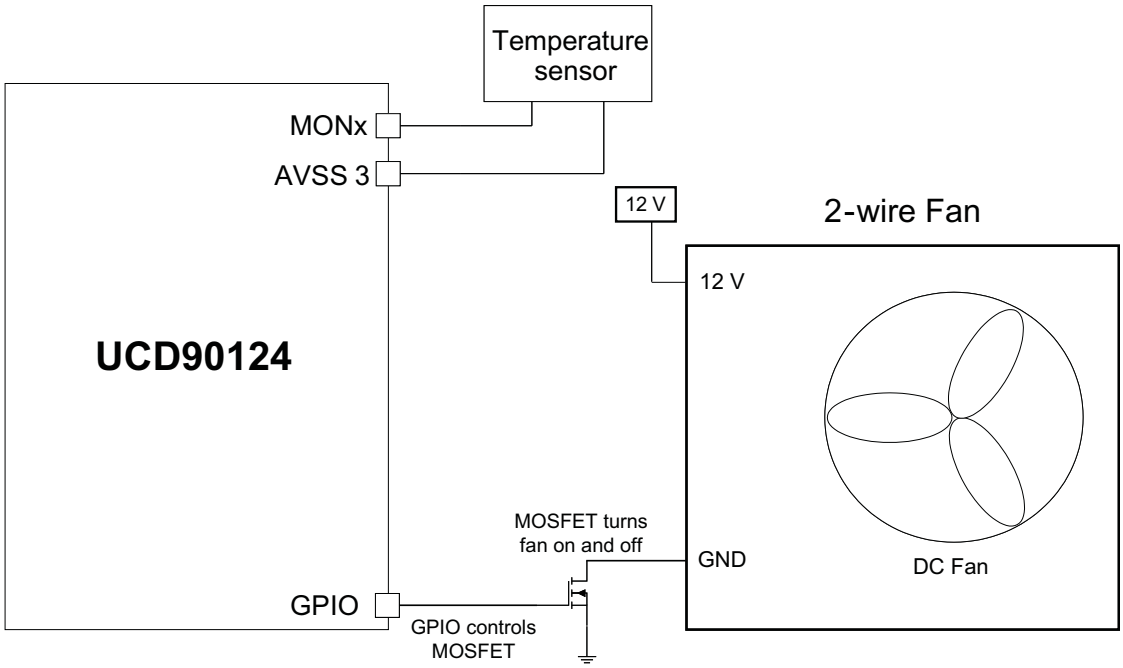


Figure 19. Two-Wire Fan Connection

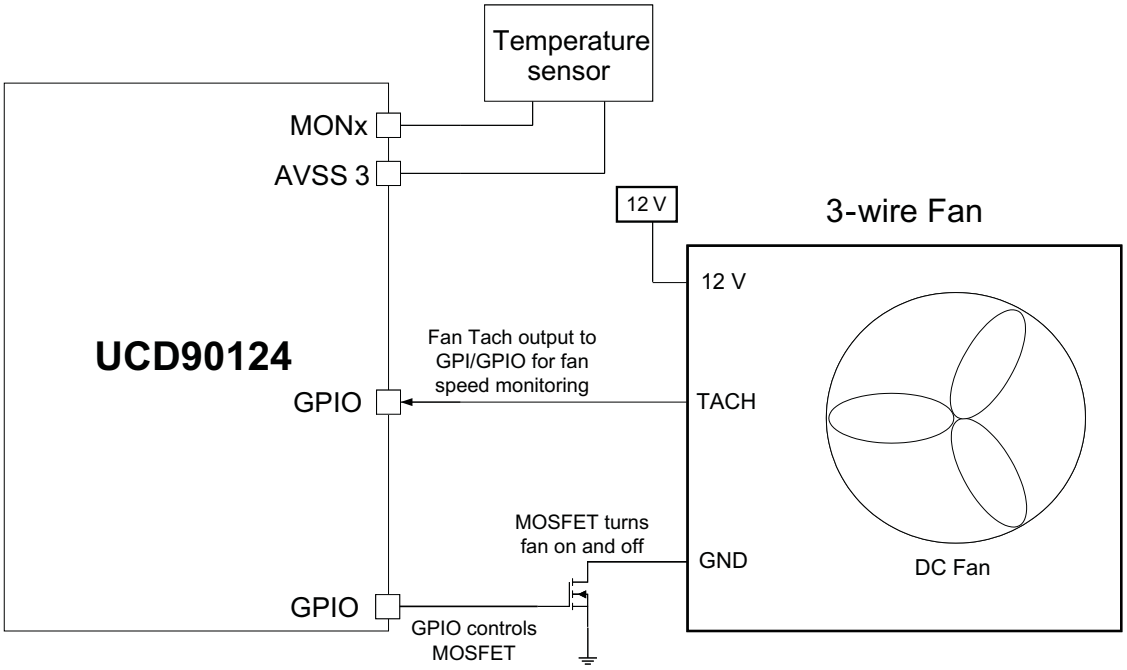


Figure 20. Three-Wire Fan Connection

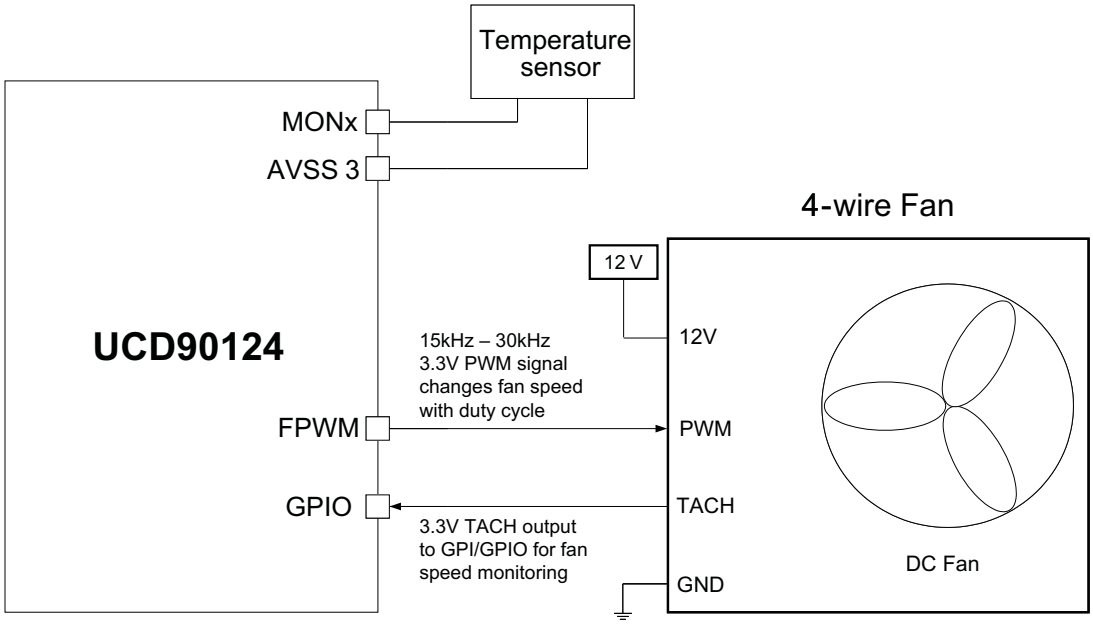


Figure 21. Four-Wire Fan Connection

The UCD90124 autocalibrate feature automatically finds and records the turn-on, turn-off and maximum speeds and duty cycles for any fan. Fans have a minimum speed at which they turn on, a turn-off speed that is usually slightly lower than the turn-on speed, and a maximum speed that occurs at slightly less than 100% duty cycle. Each speed has a PWM duty cycle that goes with it. Every fan is slightly different, even if the model numbers are the same. The built-in temperature control algorithms use the actual measured operating speed range instead of 0 RPM to rated speed of the fan to improve the fan control algorithms. The user can choose whether to use autocalibrate or to manually enter the fan data.

The UCD90124 can control up to four independent fans as defined in the PMBus standard. When enabled, the

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FAN-PWM control output provides a digital signal with a configurable frequency and duty cycle, with a duty cycle that is set based on the FAN_COMMAND_1 PMBus command. The PWM can be set to frequencies between 1 Hz and 125 MHz based on the UCD90124 PWM type selected for the fan control. The duty cycle can be set from 0% to 100% with 1% resolution. The FAN-TACH fan-control input counts the number of transitions in the tachometer output from the fan in each 1-second interval. The tachometer can be read by issuing the READ_FAN_SPEED_1 command. The speed is returned in RPMs.

Fault limits can also be set for the tachometer speed by issuing the FAN_SPEED_FAULT_LIMIT command and the status checked by issuing the STATUS_FAN_1_2 command. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for a complete description of each command.

The UCD90124 also supports two fan control algorithms.

Hysteretic Fan Control

$Temp_{ON}$ and $Temp_{OFF}$ levels are input by the user. $Temp_{ON}$ is higher than $Temp_{OFF}$. A GPIO pin is used to turn the fan or fans on at full speed when the monitored temperature reaches $Temp_{ON}$ and to turn the fans off when the temperature drops below $Temp_{OFF}$.

Inputs: T_{ON}, T_{OFF}, T_{OT}, Update Interval, Rail where MEAS_TEMP is monitored, GPOx pin

- System starts up at t = 0 seconds
- MEAS_TEMP = 25°C → ambient temp
- GPO/PWM is low and Fan is off
- Check MEAS_TEMP every 1 second (or 250 msec)
- When MEAS_TEMP = T_{ON}, set GPO/PWM = 1 → turn fan on
- Leave GPO/PWM = 1 unless MEAS_TEMP < T_{OFF}
- If MEAS_TEMP is > T_{ON}, declare a fault and take the prescribed action.

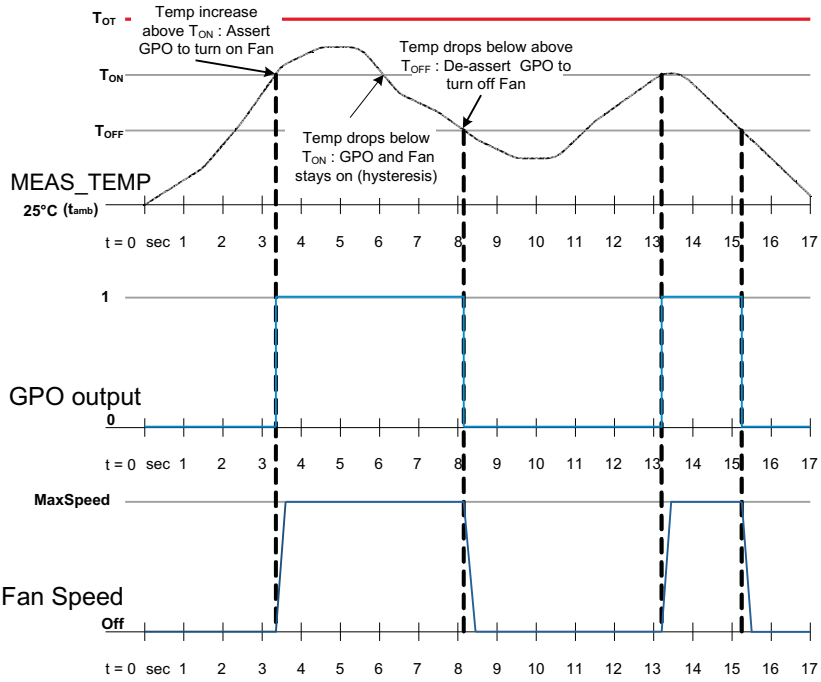


Figure 22. Hysteretic Temperature Control for 2- or 3-wire Fans

Set Point Fan Control

The second algorithm (Figure 23) uses five control set points that each have a temperature and a fan speed. When the monitored temperature increases above one of the set point temperatures, the fan speed is increased to the corresponding set point value. When the monitored temperature drops below a set point temperature, the fan speed is reduced to the corresponding set point value. The ramp rate for speed can be selected, allowing the user to optimize fan performance and minimize audible noise.

The fan speed is varied by changing the duty cycle of a PWM output. For two- and three-wire fans, as the fan is turned on and off, the inertia of the fan smoothes out the fan speed changes, resulting in variable speed operation. This approach can be taken with any fan, but would most likely be used with two- or three-wire fans at a PWM frequency in the 40-Hz to 80-Hz range. Four-wire fans would use the PWM input as described earlier in this section.

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Inputs: T_{OT}, Updates Interval, Rail that MEAS_TEMP is being monitored on, PWM pin, PWM freq, PWM temp rate, FANTAC pin, 5x (TEMPn, SPEEDn) setpoints.

- System starts up at t = 0 seconds
- MEAS_TEMP = 25°C at ambient temp
- PWM DUTY_CYCLE = 0% and fan is off
- Check MEAS_TEMP every 250 ms (or 1 s)
- When MEAS_TEMP > TEMP1:
  - set SPEED_TARGET = SPEED1
  - increase DUTY_CYCLE to DUTY_CYCLE_ON
  - increase DUTY_CYCLE by ramp rate (10%/second) until SPEED = SPEED_TARGET

  When MEAS_TEMP > TEMP2:
  - set SPEED_TARGET = SPEED2
  - increase DUTY_CYCLE by ramp rate until SPEED = SPEED_TARGET
- Repeat as temperature is increased for each new setpoint
- If MEAS_TEMP > T_{OT}, declare a fault and take the prescribed action

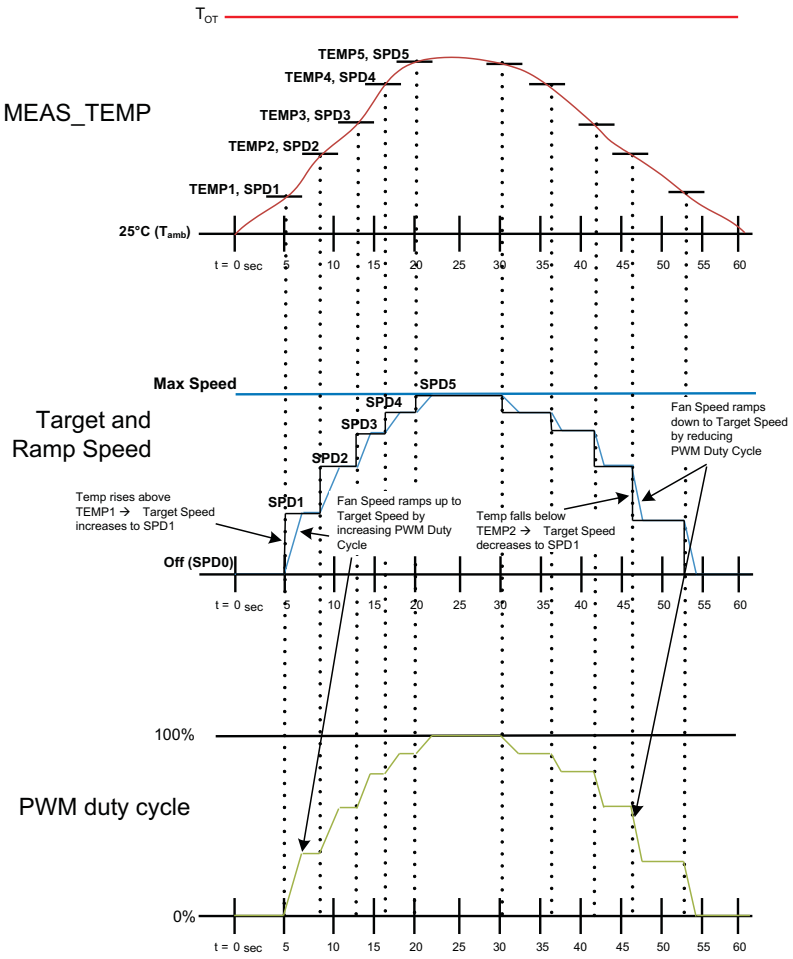


Figure 23. Temperature and Speed Set Point PWM Control for Four-Wire Fans

- If temperature drops - above TEMP4 to below TEMP3 for example
  - when MEAS_TEMP drops below TEMP4, maintain SPEED4 → do not change the DUTY_CYCLE
  - when MEAS_TEMP drops below TEMP3, set SPEED_TARGET = SPEED3
  - decrease DUTY_CYCLE by ramp rate (10%/second) until SPEED = SPEED_TARGET
- To turm the fan off when MEAS_TEMP < TEMP1, set SPEED1 = 0 RPM

EXAMPLE: MEAS_TEMP = 25°C at ambient temp:

- t = 0 to 5 sec: MEAS_TEMP increases from ambient to TEMP1 → increases SPEED_TARGET from SPD0 (Off) to SPD1 → increases DUTY_CYCLE from 0% to DUTYON (30%) → ACTUAL fan speed ramps up from 0 RPM to SPD1.
- t = 5 to 10 sec: MEAS_TEMP increases > TEMP2 → increases SPEED_TARGET from SPD1 to SPD2 → increases DUTY_CYCLE → ACTUAL fan speed ramps up from SPD1 to SPD2.
- t = 10 to 25 sec: MEAS_TEMP increases to > TEMP5 → SPEED_TARGET increases from SPD2 to SPD5 → DUTY_CYCLE ramps to DUTYMAX → ACTUAL fan speed increases SPD5.
- t = 25 to 30 sec: MEAS_TEMP stays > TEMP5 → SPEED_TARGET and DUTY_CYCLE do not change → ACTUAL fan speed stays at SPD5.
- t = 30 to 35 sec: MEAS_TEMP decreases to < TEMP4 → SPEED_TARGET drops to SPD4 and then to SPD3 → decreases DUTY_CYCLE → ACTUAL fan speed ramps down from SPD5 to SPD3.
- t = 35 to 60 sec: MEAS_TEMP decreases to < TEMP1 → SPEED_TARGET drops to SPD0 → decreases DUTY_CYCLE to DUTYOFF → ACTUAL fan speed ramps down from SPD3 to SPD0 (Off).

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SYSTEM RESET SIGNAL

The UCD90124 can generate a programmable system-reset signal as part of sequence-on. The signal is created by programming a GPIO to remain deasserted until the voltage of a particular rail or combination of rails reach their respective POWER_GOOD_ON levels plus a programmable delay time Figure 24. The system-reset delay duration can be programmed as shown in Table 4.

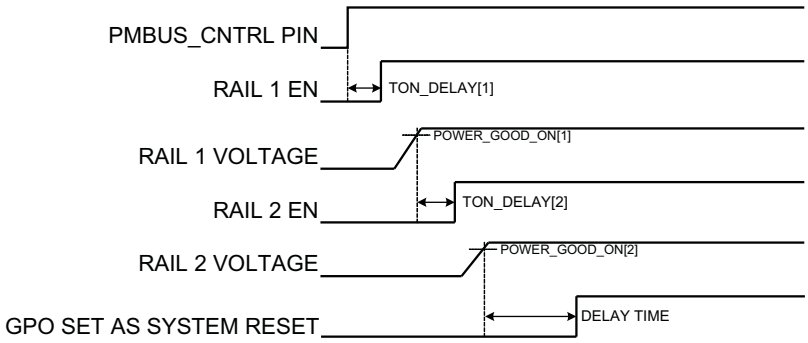


Figure 24. SYSTEM RESET Timing for a 2-Rail System

Table 4. System-Reset Delay Duration

Delay Duration
0 ms
1 ms
2 ms
4 ms
8 ms
16 ms
32 ms
64 ms
128 ms
256 ms
512 ms
1.02 s
2.05 s
4.10 s
8.19 s
16.38 s
32.8 s

WATCH DOG TIMER

A GPI and GPO can be configured as a watchdog timer (WDT). The WDT can be independent of power-supply sequencing or tied to a GPIO configured to provide a system-reset signal. The WDT can be reset by toggling a watchdog input (WDI) pin or by writing to SYSTEM_WATCHDOG_RESET over I^2C.

The WDT can be active immediately at power up or set to wait while the system initializes. Table 5 lists the programmable wait times before the initial timeout sequence begins.

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Table 5. WDT Initial Wait Time

WDT INITIAL WAIT TIME
0 ms
100 ms
200 ms
400 ms
800 ms
1.6 s
3.2 s
6.4 s
12.8 s
25.6 s
51.2 s
102 s
205 s
410 s
819 s
1638 s

The watchdog timeout is programmable from 0 to 2.55 s with a 10-ms step size. If the WDT times out, the UCD90124 can assert a GPIO pin configured as WDO that is separate from a GPIO defined as system-reset pin, or it can generate a system-reset pulse. After a timeout, the WDT is restarted by toggling the WDI pin or by writing to SYSTEM_WATCHDOG_RESET over I^2C.

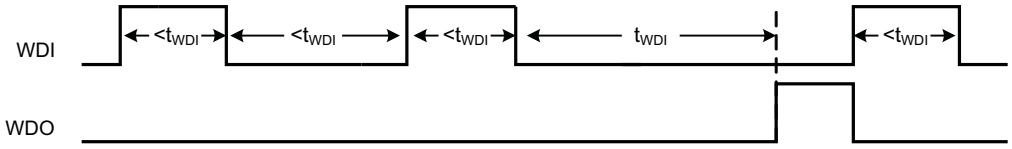


Figure 25. Timing of GPIOs Configured for Watchdog Timer Operation

DATA AND ERROR LOGGING TO FLASH MEMORY

The UCD90124 can log faults and the number of device resets to flash memory. Peak voltage, current, and temperature measurements are also stored for each rail. To reduce stress on the flash memory, a 30-second timer is started if a measured value exceeds the previously logged value. Only the highest value from the 30-second interval is written from RAM to flash.

Multiple faults can be stored in flash memory and can be accessed over PMBus to help debug power-supply bugs or failures. Each logged fault includes:

- Rail number
- Fault type
- Fault time since previous device reset
- Last measured rail voltage

The total number of device resets is also stored to flash memory. The value can be reset using PMBus.

With the brownout function enabled, the run-time clock value, peak monitor values, and faults are only logged to flash when a power-down is detected. The device run-time clock value is stored across resets or power cycles unless the brownout function is disabled, in which case the run-time clock is returned to zero after each reset.

It is also possible to update and calibrate the UCD90124 internal run-time clock via a PMBus host. For example, a host processor with a real-time clock could periodically update the UCD90124 run-time clock to a value that corresponds to the actual date and time. The host must translate the UCD90124 timer value back into the appropriate units, based on the usage scenario chosen. See the REAL_TIME_CLOCK command in the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for more details.

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BROWNOUT FUNCTION

The UCD90124 can be enabled to turn off all nonvolatile logging until a brownout event is detected. A brownout event occurs if V_{CC} drops below 2.9 V. In order to enable this feature, the user must provide enough local capacitance to deliver up to 80 mA (consider additional load based on GPOs sourcing external circuits such as LEDs) on for 5 ms while maintaining a minimum of 2.6 V at the device. If using the brownout circuit (Figure 26), then a schottky diode should be placed so that it blocks the other circuits that are also powered from the 3.3V supply.

With this feature enabled, the UCD90124 saves faults, peaks, and other log data to SRAM during normal operation of the device. Once a brownout event is detected, all data is copied from SRAM to Flash. Use of this feature allows the UCD90124 to keep track of a single run-time clock that spans device resets or system power down (rather than resetting the run time clock after device reset). It can also improve the UCD90124 internal response time to events, because Flash writes are disabled during normal system operation. This is an optional feature and can be enabled using the MISC_CONFIG command. For more details, see the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference*.

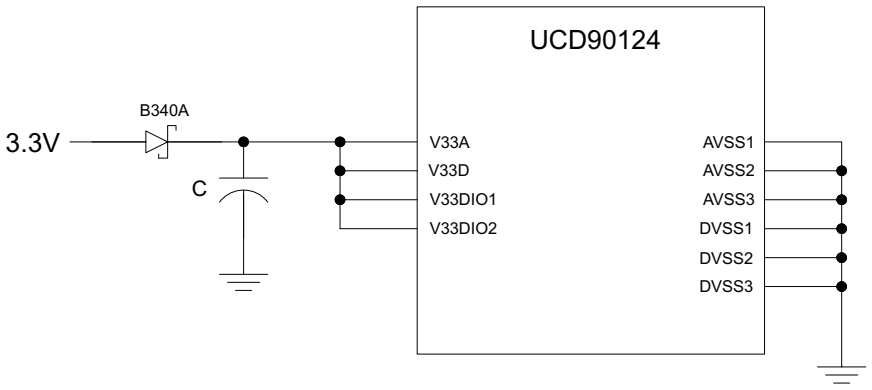


Figure 26. Brownout Circuit

PMBUS ADDRESS SELECTION

Two pins are allocated to decode the PMBus address. At power up, the device applies a bias current to each address-detect pin, and the voltage on that pin is captured by the internal 12-bit ADC. The PMBus address is calculated as follows.

$$\text{PMBus Address} = 12 \times \text{bin}(V_{AD01}) + \text{bin}(V_{AD00})$$

Where $\text{bin}(V_{AD0x})$ is the address bin for one of eight addresses as shown in Table 6. The address bins are defined by the MIN and MAX VOLTAGE RANGE (V). Each bin is a constant ratio of 1.25 from the previous bin. This method maintains the width of each bin relative to the tolerance of standard 1% resistors.

Table 6. PMBus Address Bins

ADDRESS BIN	VPMBus PMBus VOLTAGE RANGE (V)		RPMBus PMBus RESISTANCE (kΩ)
	MIN	MAX	
open	2.226	3.300	
11	1.747	2.225	210
10	1.342	1.746	158
9	1.031	1.341	115
8	0.793	1.030	84.5
7	0.609	0.792	63.4
6	0.468	0.608	47.5
5	0.359	0.467	36.5
4	0.276	0.358	27.4
short	0	0.097	

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A low impedance (short) on either address pin that produces a voltage below the minimum voltage causes the PMBus address to default to address 126 (0x7E). A high impedance (open) on either address pin that produces a voltage above the maximum voltage also causes the PMBus address to default to address 126 (0x7E).

Address 0 is not used because it is the PMBus general-call address. Addresses 11 and 127 can not be used by this device or any other device that shares the PMBus with it, because those are reserved for manufacturing programming and test. It is recommended that address 126 not be used for any devices on the PMBus, because this is the address that the UCD90124 defaults to if the address lines are shorted to ground or left open. Table 7 summarizes which PMBus addresses can be used. Other SMBus/PMBus addresses have been assigned for specific devices. For a system with other types of devices connected to the same PMBus, see the SMBus device address assignments table in Appendix C of the latest version of the System Management Bus (SMBus) specification. The SMBus specification can be downloaded at http://smbus.org/specs/smbus20.pdf.

Table 7. PMBus Address Assignment Rules

Address	STATUS	Reason
0	Prohibited	SMBus general address call
1-10	Available	
11	Avoid	Causes conflicts with other devices during program flash updates.
12	Prohibited	PMBus alert response protocol
13-125	Available	
126	Avoid	Default value; may cause conflicts with other devices. Enables JTAG mode.
127	Prohibited	Used by TI manufacturing for device tests.

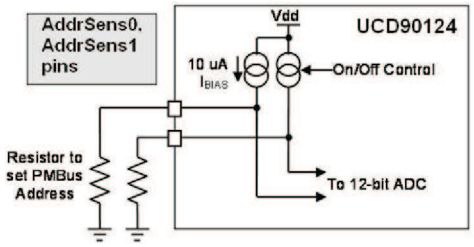


Figure 27. PMBus Address-Detection Method

CAUTION

Leaving the address in default state as 126 (0x7E) will enable the JTAG and not allow using the JTAG compatible pins (36-39) as GPIOs.

HIGH VOLTAGE SUPPLY VOLTAGE REGULATOR

The UCD90124 requires 3.3 V to operate. It can be provided directly on the various V_{33x} pins using an external 3.3-V regulator, or it can be generated from a higher voltage using a built-in series regulator and an external transistor. The external transistor must be an NPN device with a beta of at least 40 and a V_{CE} rating appropriate for the high supply voltage. Figure 28 shows a typical circuit using the external series pass transistor. The NPN emitter output becomes the 3.3-V supply for the chip. A 4.7-µF bypass capacitor is required to stabilize the series regulator.

To design this circuit, Q must be selected first. Two things are important about this NPN transistor: rated power and beta value (ß or h_{FE}). A higher beta allows R to be larger, which results in a more efficient circuit. Also, Q must be able to dissipate the power lost in it, as it is the pass element in this linear regulator. This power can be calculated from Equation 3:

$$P_{diss_Q} = (V_{in_max} - 3.3\ V) \times I_{UCD90124} \quad (3)$$ (3)

$I_{UCD90124}$ is the maximum current drawn by the controller on the V33A and V33D pins and is 50 mA for the UCD90124.

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Once a transistor is selected, R must be sized based on the maximum input voltage. At V_{in_max}, the current through R is highest, because the base voltage is still held at ~4 V. At high V_{in}, the base current is also constant, as the emitter current is still the same. Thus at V_{in_max}, more current must be sunk by the V33FB pin. Good design practice dictates keeping the current sink required by the V33FB pin at high input voltage to half of the maximum rating for the V33FB pin, thus, 5 mA. This corresponds to a minimum value for R. Therefore R must be set by Equation 4:

$$R = \frac{V_{in_max} - 4\ V}{5\ mA + \left(\frac{I_{UCD90124}}{\beta + 1}\right)} \quad (4)$$

A maximum value of R corresponds to the minimum input voltage. This assumes that the V33FB pin is sinking no current and all the current through R flows into the base of the BJT. R must be below this value, or else the linear regulator does not operate reliably at low input voltage:

$$R < \frac{V_{in_min} - 4\ V}{\frac{I_{UCD90124}}{\beta + 1}} \quad (5)$$

If the value of R from Equation 5 is less than the value of R from Equation 4, then a transistor with a larger beta must be chosen. For completion, the power lost in R can be calculated from Equation 6:

$$P_{diss_R} = \frac{(V_{in_max} - 4\ V)^2}{R} \quad (6)$$

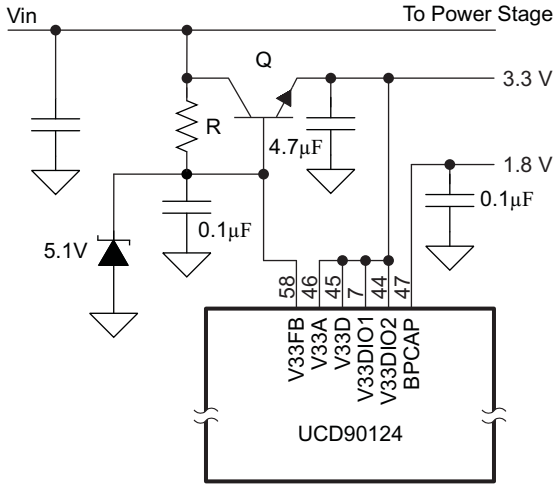


Figure 28. High-Voltage Supply With External Transistor

Some circuits in the device require 1.8 V, which is generated internally from the 3.3-V supply. This voltage requires a 0.1-µF to 1-µF bypass capacitor from BPCAP to ground.

An external LDO, such as the TPS715A33, may be used to provide the needed 3.3 V instead of the previously described regulator. In this case, the V33FB pin may simply be left floating.

DEVICE RESET

The UCD90124 has an integrated power-on reset (POR) circuit which monitors the supply voltage. At power up, the POR detects the V_{33D} rise. When V_{33D} is greater than V_{RESET}, the device comes out of reset.

The device can be forced into the reset state by an external circuit connected to the $\overline{\text{RESET}}$ pin. A logic-low voltage on this pin for longer than t_{RESET} holds the device in reset. It comes out of reset within 1 ms after $\overline{\text{RESET}}$is released and can return to a logic-high level. To avoid an erroneous trigger caused by noise, a pullup resistor to 3.3 V is recommended.

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Any time the device comes out of reset, it begins an initialization routine that lasts about 20 ms. During the initialization routine, the FPWM pins are held low, and all other GPIO and GPI pins are open-circuit. At the end of initialization, the device begins normal operation as defined by the device configuration.

DEVICE CONFIGURATION AND PROGRAMMING

From the factory, the device contains the sequencing and monitoring firmware. It is also configured so that all GPOs are high-impedance (except for FPWM/GPIO pins 17-24, which are driven low), with no sequencing or fault-response operation. See *Configuration Programming of UCD Devices*, available from the *Documentation & Help Center* that can be selected from the *Fusion GUI* Help menu, for full UCD90124 configuration details.

After the user has designed a configuration file using *Fusion GUI*, there are three general device-configuration programming options:

1. Devices can be programmed in-circuit by a host microcontroller using PMBus commands over I^{2}C (see the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference*). Each parameter write replaces the data in the associated memory (RAM) location. After all the required configuration data has been sent to the device, it is transferred to the associated nonvolatile memory (data flash) by issuing a special command, STORE_DEFAULT_ALL. This method is how the *Fusion GUI* normally reads and writes a device configuration.
2. The *Fusion GUI* (Figure 29) can create a PMBus or I^{2}C command script file that can be used by the I^{2}C master to configure the device.

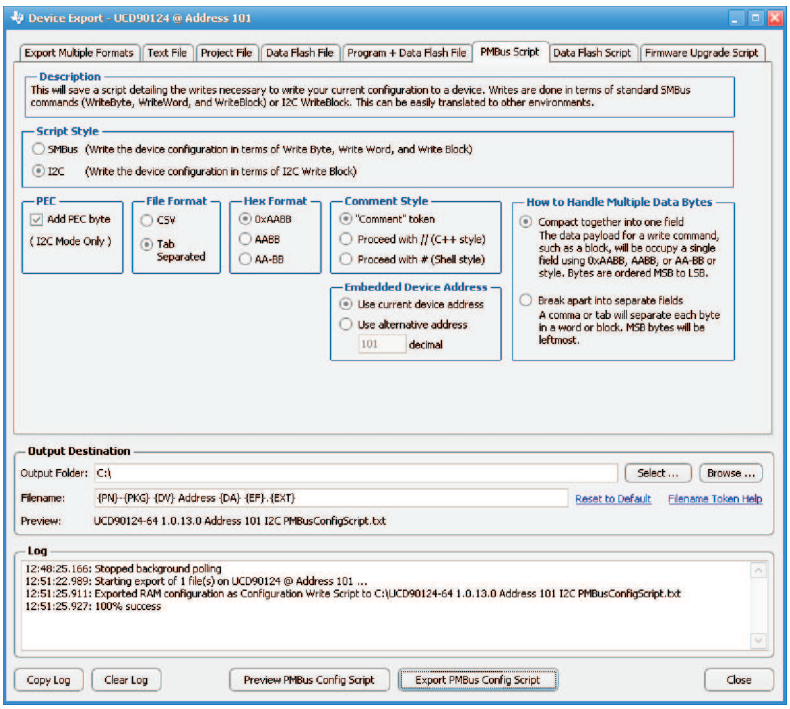


Figure 29. Fusion GUI PMBus Configuration Script Export Tool

3. Another in-circuit programming option is for the *Fusion GUI* to create a data flash image from the configuration file (Figure 30). The configuration files can be exported in Intel Hex, Serial Vector Format (SVF) and S-record. The image file can be downloaded into the device using I^{2}C or JTAG. The *Fusion GUI* tools can be used on-board if the *Fusion GUI* can gain ownership of the target board I^{2}C bus.

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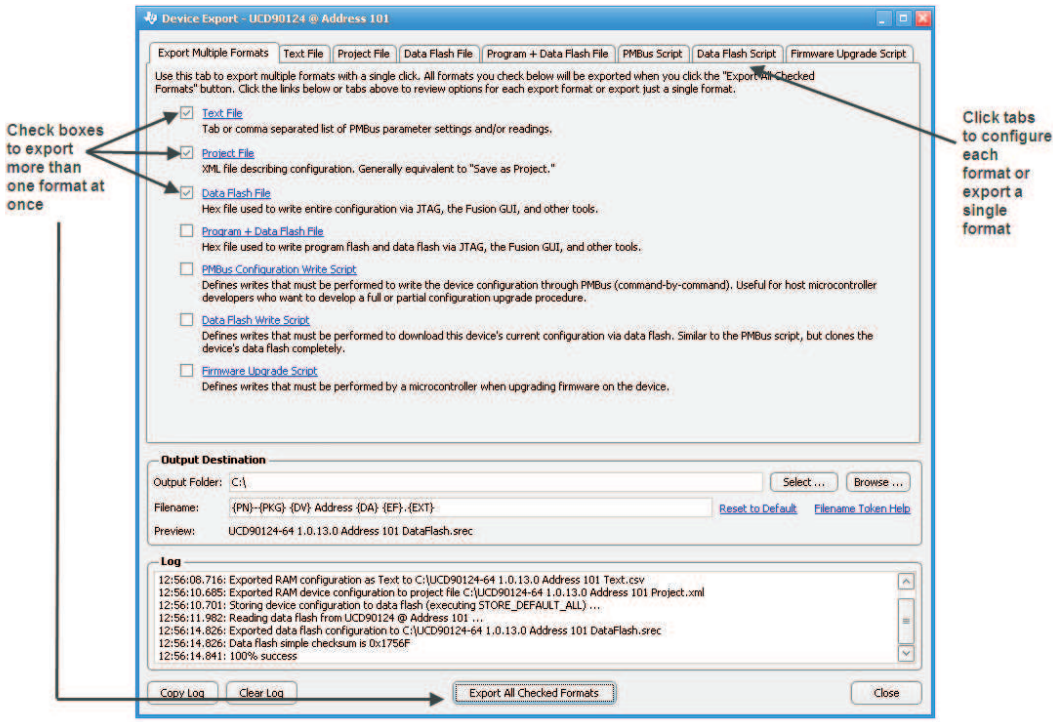


Figure 30. Fusion GUI Device Configuration Export Tool

Devices can be programmed off-board using the *Fusion GUI* tools or a dedicated device programmer. For small runs, a ZIF socketed board with an I²C header can be used with the standard *Fusion GUI* or manufacturing GUI. The *Fusion GUI* can also create a data flash file that can then be loaded into the UCD90124 using a dedicated device programmer.

To configure the device over I²C or PMBus, the UCD90124 must be powered. The PMBus clock and data pins must be accessible and must be pulled high to the same V_{DD} supply that powers the device, with pullup resistors between 1 kΩ and 2 kΩ. Care should be taken to not introduce additional bus capacitance (<100 pF). The user configuration can be written to data flash using a gang programmer via JTAG or I²C before the device is installed in circuit. To use I²C, the clock and data lines must be multiplexed or the device addresses must be assigned by socket. The *Fusion GUI* tools can be used for socket addressing. Pre-programming can also be done using a single device test fixture.

Table 8. Configuration Options

	Data Flash via JTAG	Data Flash via I²C	PMBus Commands via I²C
Off-Board Configuration	Data Flash Export (.svf type file)	Data Flash Export (.srec or hex type file)	Project file I²C/PMBus script
	Dedicated programmer	Fusion GUI tools (with exclusive bus access via USB to I²C adapter)	Fusion GUI tools (with exclusive bus access via USB to I²C adapter)
On-Board Configuration	Data flash export	Fusion GUI tools (with exclusive bus access via USB to I²C adapter)	Fusion GUI tools (with exclusive bus access via USB to I²C adapter)
	IC		

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The advantages of off-board configuration include:

- Does not require access to device I^2C bus on board.
- Once soldered on board, full board power is available without further configuration.
- Can be partially reconfigured once the device is mounted.

JTAG INTERFACE

The JTAG port can be used for production programming. Four of the six JTAG pins can also be used as GPIOs during normal operation. See the *Pin Functions* table at the beginning of the document and Table 3 for a list of the JTAG signals and which can be used as GPIOs. The JTAG port is compatible with the IEEE Standard 1149.1-1990, IEEE Standard Test-Access Port and Boundary Scan Architecture specification. Boundary scan is not supported on this device.

The JTAG interface can provide an alternate interface for programming the device. It is disabled by default in order to enable the GPIO pins with which it is multiplexed. There are two conditions under which the JTAG interface is enabled:

1. On power-up if the data flash is blank, allowing JTAG to be used for writing the configuration parameters to a programmed device with no PMBus interaction
2. When address 126 (0x7E) is detected at power up. A short to ground or an open condition on either address pin will cause an address 126 (0x7E) to be generated which enables JTAG mode.

The Fusion GUI can create SVF files (See DEVICE CONFIGURATION AND PROGRAMMING section) based on a given data flash configuration which can be used to program the desired configuration by JTAG. For Boundary Scan Description Language (BSDL) file that supports the UCD90124 see the product folder in www.ti.com.

INTERNAL FAULT MANAGEMENT AND MEMORY ERROR CORRECTION (ECC)

The UCD90124 verifies the firmware checksum at each power up. If it does not match, then the device waits for I^2C commands but does not execute the firmware. A device configuration checksum verification is also performed at power up. If it does not match, the factory default configuration is loaded. The PMBALERT# pin is asserted and a flag is set in the status register. The error-log checksum validates the contents of the error log to make sure that section of flash is not corrupted.

There is an internal firmware watchdog timer. If it times out, the device resets so that if the firmware program is corrupted, the device goes back to a known state. This is a normal device reset, so all of the GPIO pins are open-drain and the FPWM pins are driven low while the device is in reset. Checks are also done on each parameter that is passed, to make sure it falls within the acceptable range.

Error-correcting code (ECC) is used to improve data integrity and provide high-reliability storage of Data Flash contents. ECC uses dedicated hardware to generate extra check bits for the user data as it is written into the Flash memory. This adds an additional six bits to each 32-bit memory word stored into the Flash array. These extra check bits, along with the hardware ECC algorithm, allow for any single-bit error to be detected and corrected when the Data Flash is read.

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APPLICATION INFORMATION

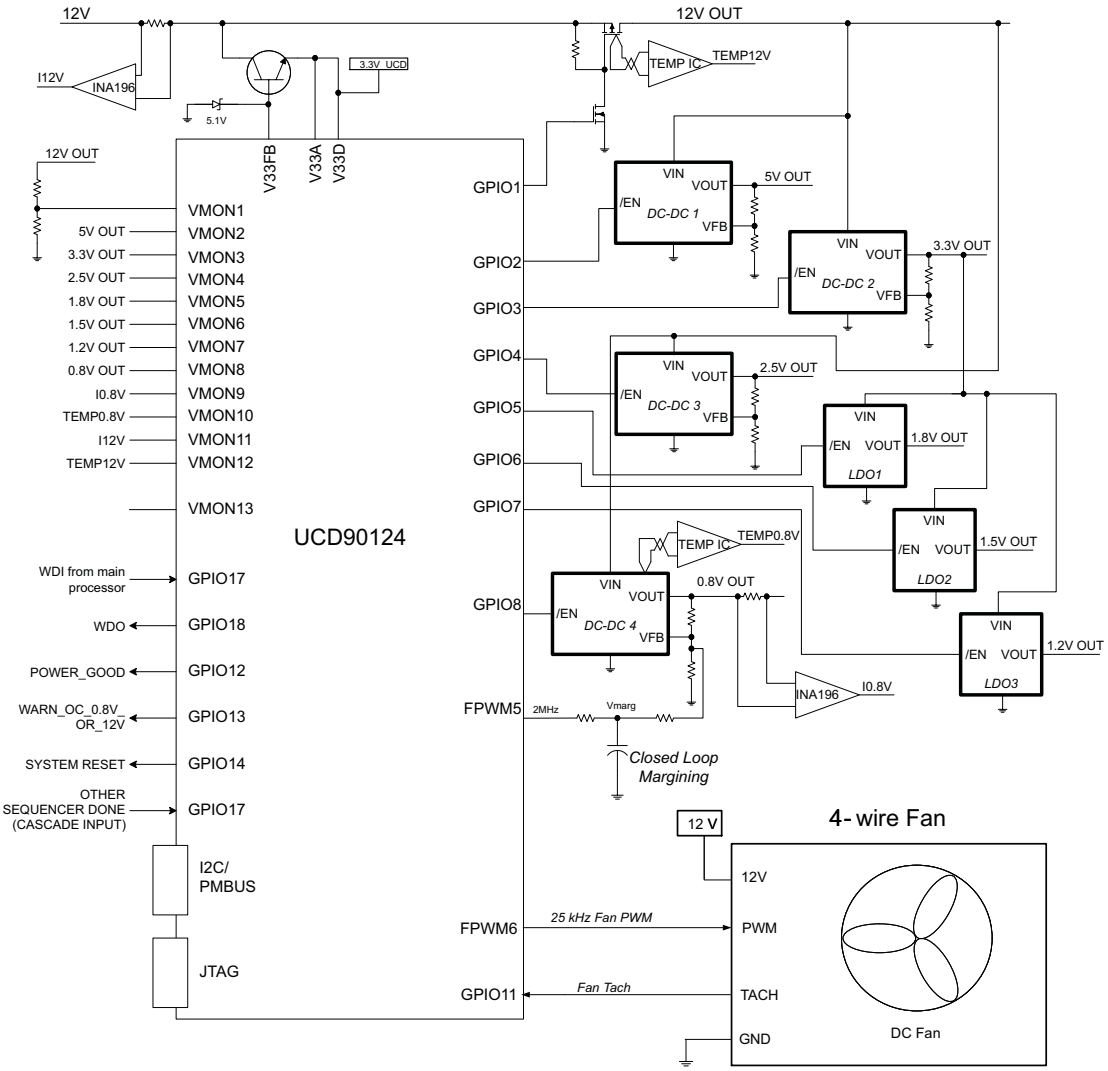


Figure 31. Typical Application Schematic

NOTE

Figure 31 is a simplified application schematic. Voltage dividers such as the ones placed on VMON1 input have been ommited for simplifying the schematic. All VMONx pins which are configured to measure a voltage that exceeds the 2.5V ADC reference are required to have a voltage divider.

Layout guidelines

The thermal pad provides a thermal and mechanical interface between the device and the printed circuit board (PCB). While device power dissipation is not of primary concern, a more-robust thermal interface can help the internal temperature sensor provide a better representation of PCB temperature. Connect the exposed thermal pad of the PCB to the device V_{SS} pins and provide at least a 4 × 4 pattern of PCB vias to connect the thermal pad and V_{SS} pins to the circuit ground on other PCB layers.

For supply-voltage decoupling, provide power-supply pin bypass to the device as follows:

- 0.1-µF, X7R ceramic in parallel with 0.01-µF, X7R ceramic at pin 47 (BPCAP)
- 0.1-µF, X7R ceramic in parallel with 4.7-µF, X5R ceramic at pins 44 (V_{33DIO2}) and 45 (V_{33D})
- 0.1-µF, X7R ceramic at pin 7 (V_{33DIO1})
- 0.1-µF, X7R ceramic in parallel with 4.7-µF, X5R ceramic at pin 46 (V_{33A})

Depending on use and application of the various GPIO signals used as digital outputs, some impedance control may be desired to quiet fast signal edges. For example, when using the FPWM pins for fan control or voltage margining, the pin is configured as a digital *clock* signal. Route these signals away from sensitive analog signals. It is also good design practice to provide a series impedance of 20 Ω to 33 Ω at the signal source to slow fast digital edges.

Estimating ADC Reporting Accuracy

The UCD90124 uses a 12-bit ADC and an internal 2.5-V reference (V_{REF}) to convert MON pin inputs into digitally reported voltages. The least significant bit (LSB) value is $V_{LSB} = V_{REF}/2^N$ where N = 12, resulting in a VLSB = 610 µV. The error in the reported voltage is a function of the ADC linearity errors and any variations in VREF. The total unadjusted error (E_{TUE}) for the UCD90124 ADC is ±5 LSB, and the variation of VREF is ±0.5% between 0°C and 125°C and ±1% between –40°C and 125°C. V_{TUE} is calculated as $V_{LSB} \times E_{TUE}$. The total reported voltage error is the sum of the reference-voltage error and V_{TUE}. At lower monitored voltages, V_{TUE} dominates reported error, wheereas at higher monitored voltages, the tolerance of V_{REF} dominates the reported error. Reported error can be calculated using Equation 7, where REFTOL is the tolerance of V_{REF}, V_{ACT} is the actual voltage being monitored at the MON pin, and V_{REF} is the nominal voltage of the ADC reference.

$$RPT_{ERR} = \left(\frac{1+REFTOL}{V_{ACT}}\right) \times \left(\frac{V_{REF} \times E_{TUE}}{4096} + V_{ACT}\right) - 1 \quad (7)$$

From Equation 7, for temperatures between 0°C and 125°C, if V_{ACT} = 0.5 V, then RPT_{ERR} = 1.11%. If V_{ACT} = 2.2 V, then RPT_{ERR} = 0.64%. For the full operating temperature range of –40°C to 125°C, if VACT = 0.5 V, then RPT_{ERR} = 1.62%. If V_{ACT} = 2.2 V, then RPT_{ERR} = 1.14%.

REVISION HISTORY

Changes from Original (November 2009) to Revision A — **Page**

- Changed Timing requirements table (t_f) From: See (Note Rise Time) To: See (Note Fall Time) 6
- Changed Timing requirements table (t_r) From: See (Note Fall Time) To: See (Note Rise Time) 6

Changes from Revision A (December 2009) to Revision B — **Page**

- Changed the FUNCTIONAL BLOCK DIAGRAM 2
- Added FAN CONTROL INPUTS AND OUTPUTS to the Electrical Characteristics table 5
- Added Figure 9 17
- Changed text From: [P-N junction or To: such as 17
- Deleted Information and Figure 10 pertinent to remote diode temp sensing 17
- Added GPO Control subsection 21
- Added Note regarding what happens when margining is configured but turned off 26
- Added brownout circuit figure. 33

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCD90124RGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD90124	Samples
UCD90124RGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD90124	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

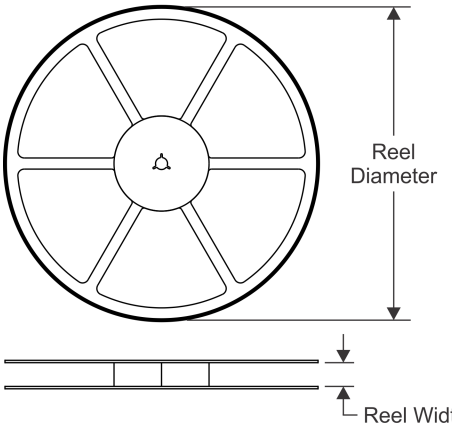
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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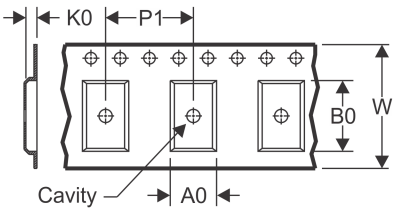
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

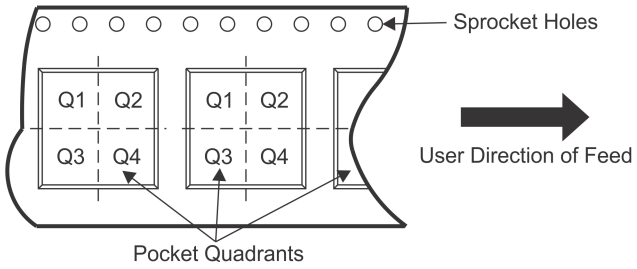


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

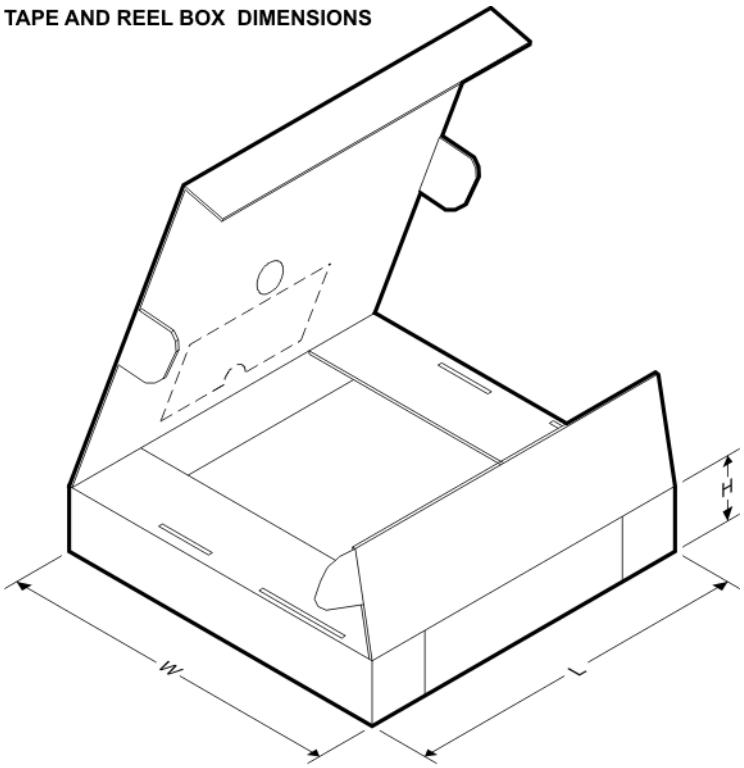
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD90124RGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
UCD90124RGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
UCD90124RGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
UCD90124RGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD90124RGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
UCD90124RGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
UCD90124RGCT	VQFN	RGC	64	250	210.0	185.0	35.0
UCD90124RGCT	VQFN	RGC	64	250	210.0	185.0	35.0

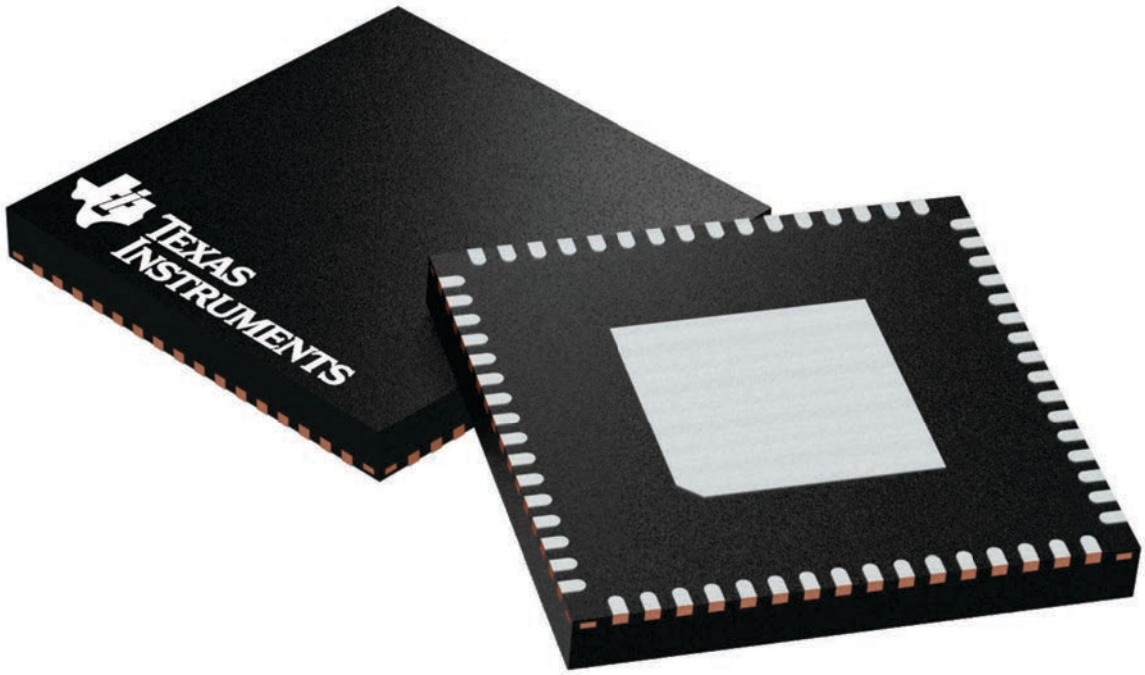
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

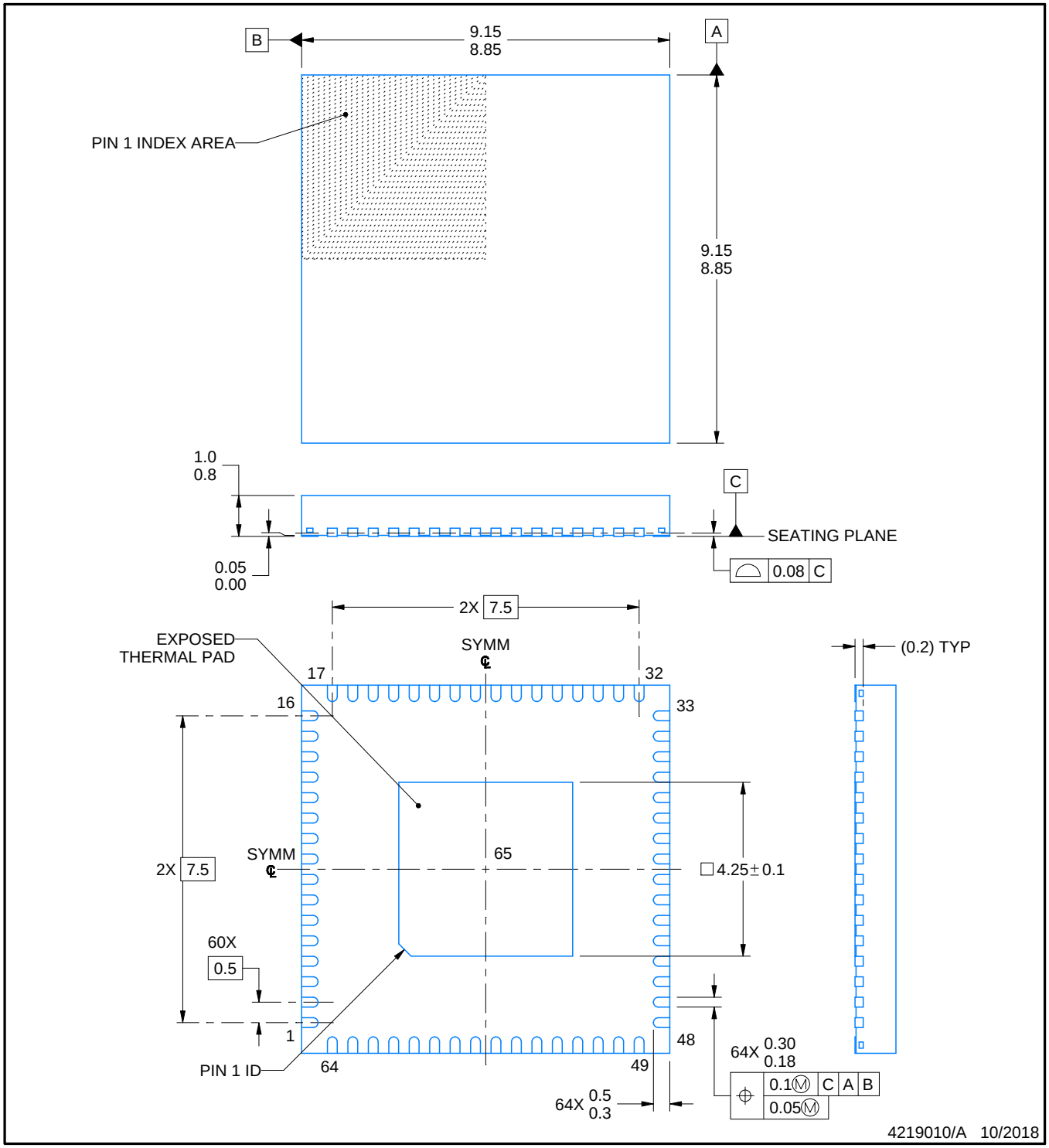
4224597/A

PACKAGE OUTLINE

RGC0064B

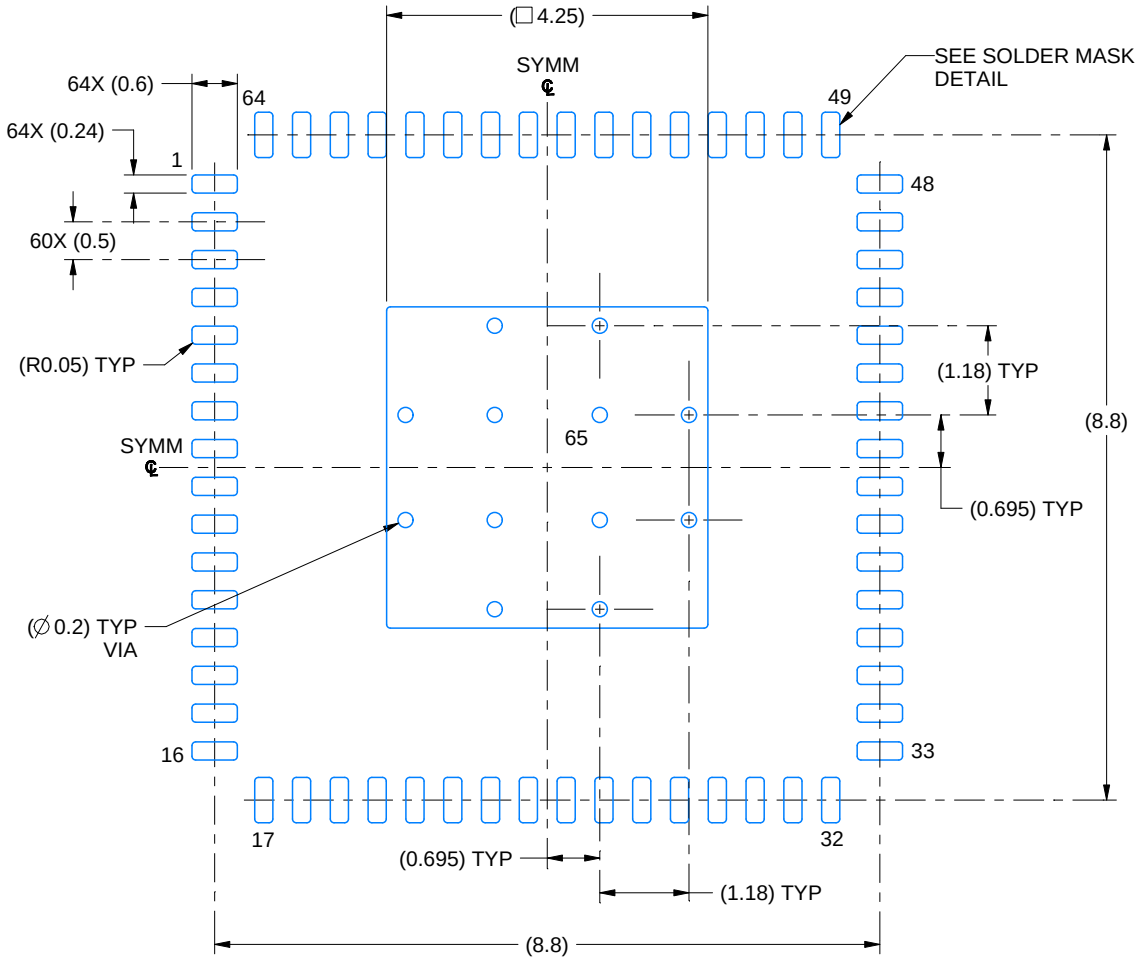
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

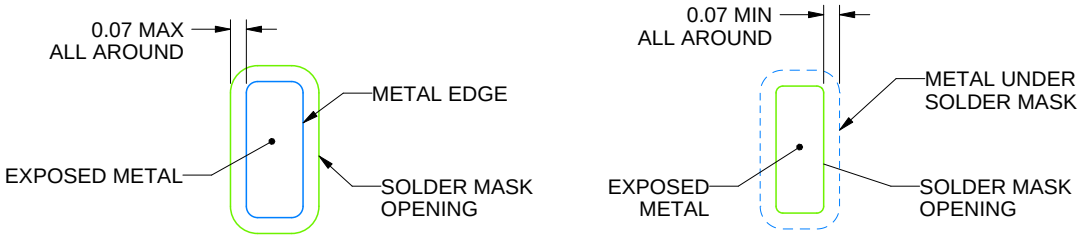


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

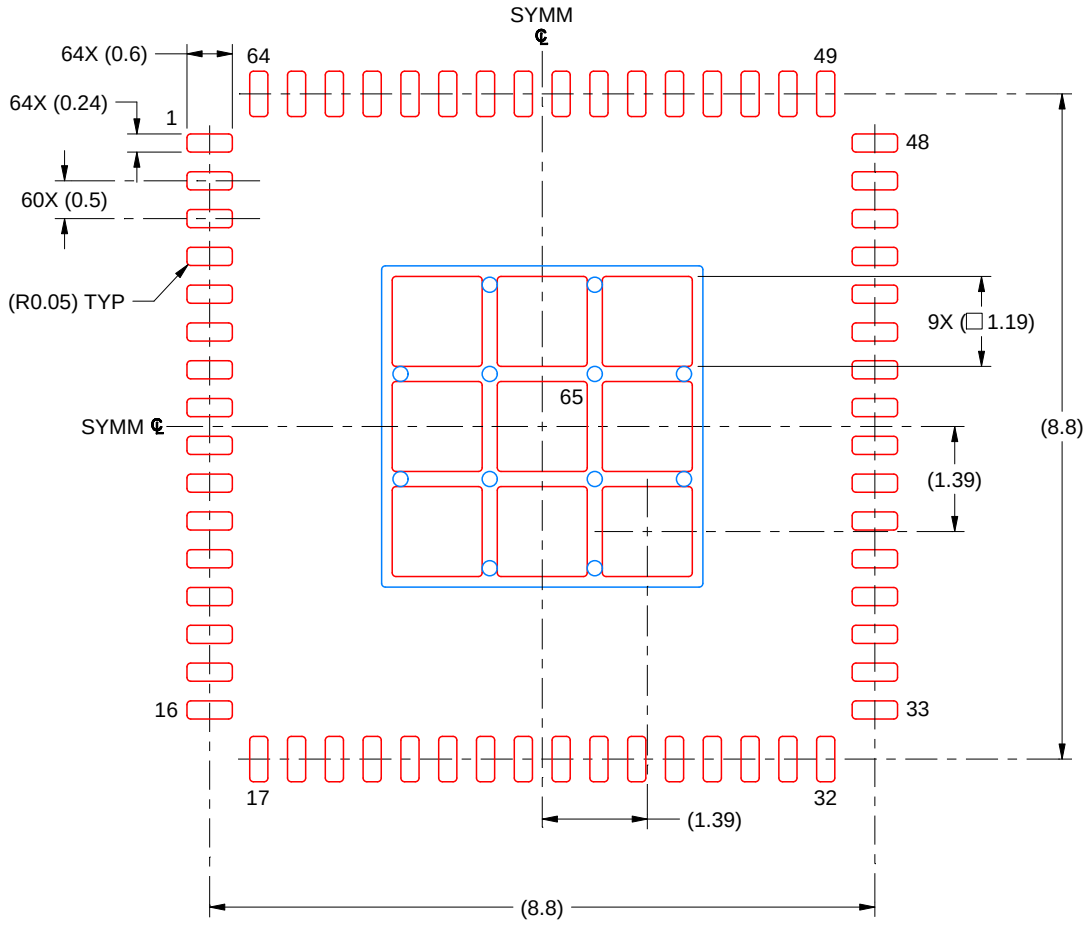


SOLDER MASK DETAILS

4219010/A 10/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219010/A 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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