VT-803

Temperature Compensated Crystal Oscillator
Voltage Controlled Temperature Compensated Crystal Oscillator

Description

Vectron's VT-803 Temperature Compensated Crystal Oscillator (TCXO) is a quartz stabilized, clipped sine wave or CMOS output, 5th order analog temperature compensated oscillator, operating off a 2.8 to 5.0 volt supply in a hermetically sealed 3.2x5 mm ceramic package.

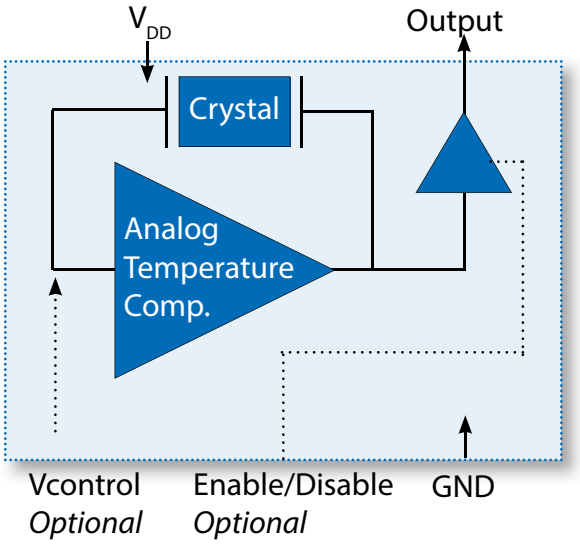
Features

- Clipped Sine Wave or CMOS Output
- 10.000-52.000 MHz Output
- ±100 ppb Temperature Stability
- Optional Enable/Disable Function
- Optional VCXO
- Fundamental Crystal Design
- Gold over nickel contact pads
- Hermetically Sealed Ceramic SMD package
- Product is compliant to RoHS directive and fully compatible with lead free assembly

Applications

- Stratum 3
- SyncE
- 1588
- Femto Cells
- Base Stations
- IP Networking
- GPS
- Point to Point Radio
- Manpack Radio
- Test and Measurement

Block Diagram



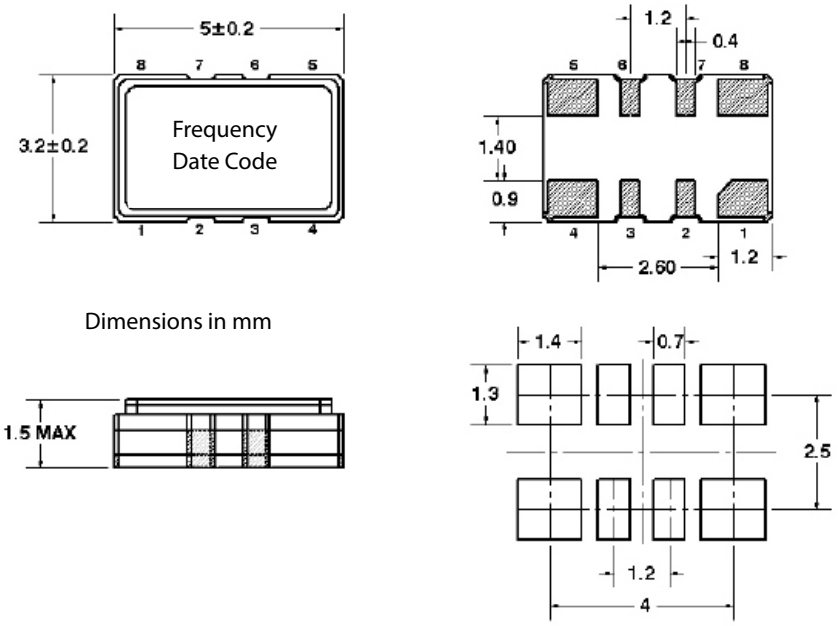
Specifications

Table 1. Electrical Performance, Clipped Sine Wave Option

Parameter	Symbol	Min	Typ	Max	Units
Output Frequency,[1] *Ordering Option*	f_O	10		52	MHz
Supply Voltage[2], *Ordering Option*	V_{DD}	+2.8, +3.0, +3.3, +5.0			V
Supply Current, 10-20.000MHz 20.001-52.000MHz	I_{DD}			2.0 3.4	mA
Operating Temperature, *Ordering Option*	T_{OP}	-20/70, -40/85			°C
Stability Over Operating Temperature[3], *Ordering Option*		±0.100, ±0.200, ±0.280, ±1.0			ppm
Initial Accuracy, "No Adjust" Option[4]				±1.5	ppm
Power Supply Stability, ±5% change				±0.05	ppm
Load Stability, ±10% change				±0.05	ppm
Aging				±0.5	ppm 1st yr
Stability, temperature and 24 hours[5]				±0.37	ppm
Total Stability[5]				±4.6	ppm
Pull Range, *Ordering Option*	PR	±5, ±10			ppm
Control Voltage to reach Pull Range		0.5		2.5	V
Control Voltage Impedance		100			Kohm
Output Enable/Disable[6], *Ordering Option* Output Enabled Output Disabled (high impedance output)	 V_{IH} V_{IL}	 $0.2*V_{DD}$		 $0.8*V_{DD}$	 V V
Output Level	V_O p/p	0.8			V
Output Load				10K II 10pF	
Phase Noise, 26.000MHz 10Hz 100Hz 1kHz 10kHz 100kHz	$Ø_N$		 -91 -117 -136 -150 -158		dBc/Hz
Start Up Time	t_{SU}			2	ms

1. The Output is DC coupled.
2. The VT-803 power supply pin should be filtered, eg, a 10uF, 0.1uF and 0.01uf capacitor.
3. Not all stabilities are available over all temperature ranges. Measured at mid Vc for parts with frequency tuning.
4. After 2 IR reflows and 24 hours.
5. ±100, ±200 and ±280 ppb temp stability parts, all inclusive with 10 years aging.
6. Output is Enabled if E/D is left open.

Outline Drawing



Dimensions in mm

Table 2. Pinout

Pin #	Symbol	Function
1	NC or V_C	No Connection or TCXO Control Voltage
2	NC	Make No Connection
3	NC	Make No Connection
4	GND	Ground
5	OUT	Output
6	NC or E/D	No Connection or Enable/Disable
7	NC	Make No Connection
8	V_{DD}	Supply Voltage

Table 3. Enable Disable Function (optional)

Pin 6	Pin 5 Output
High	Clock Output
Open	Clock Output
Low	High Impedance

Specifications

Table 4. Electrical Performance, CMOS Option					
Parameter		Min	Typ	Max	Units
Output Frequency[1], *Ordering Option*	fo	10		52	MHz
Supply Voltage[2], *Ordering Option*	V_{DD}	+2.8, +3.0, +3.3, +5.0			V
Supply Current, 10-24.999MHz 25.000-39.000MHz 40.000- 49.999MHz 50.000- 52.000MHz	I_{DD}			3.0 3.5 5.0 6.0	mA
Operating Temperature, *Ordering Option*	T_{OP}	-20/70, -40/85			°C
Stability Over Operating Temperature[3], *Ordering Option*		±0.100, ±0.200, ±0.280, ±1.0			ppm
Initial Accuracy, "No Adjust" Option[4]				±1.5	ppm
Power Supply Stability, ±5% change 10MHz-27MHz, 2.8V, 3.0V, and3.3V >27MHz-52MHz, 2.8V, 3.0V, and3.3V 10MHz-27MHz, 5V >27MHz-52MHz, 5V		I		 ±0.10 ±0.20 ±0.20 ±0.30	ppm
Load Stability, ±10% change				±0.10	ppm
Aging				±0.5	ppm 1st yr
Stability, temperature and 24 hours[5]				±0.37	ppm
Total Stability[5]				±4.6	ppm
Pull Range, *Ordering Option*		±5, ±10			ppm
Control Voltage to reach Pull Range		0.5		2.5	V
Control Voltage Impedance		100			Kohm
Output Enable/Disable[6], *Ordering Option* Output Enabled Output Disabled (high impedance output)	 V_{IH} V_{IL}		 $0.2*V_{DD}$	 $0.8*V_{DD}$	 V V
Output Level Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive	 V_{OH} V_{OL}	 $0.9*V_{DD}$ 4		 $0.1*V_{DD}$ -4	 V V mA mA
Output Load				15	pF
Phase Noise, 26.000MHz 10Hz 100Hz 1kHz 10kHz 100kHz			 -91 -117 -139 -153 -157		dBc/Hz
Period Jitter[7] rms peak-peak			 2.5 21.0		 ps ps
Start Up Time	t_{SU}			2	ms

1. The Output is DC coupled.
2. The VT-803 power supply pin should be filtered, eg, a 10uF, 0.1uF and 0.01uf capacitor.
3. Not all stabilities are available over all temperatures. Measured at mid Vc for parts with frequency tuning
4. After 2 IR reflows and 24 hours.
5. ±100, ±200 and ±280 ppb temp stability parts, all inclusive with 10 years aging.
6. Output is Enabled if E/D is left open.
7. Measured using a Wavecrest SIA3300C, 90K samples.

Warm Up Time

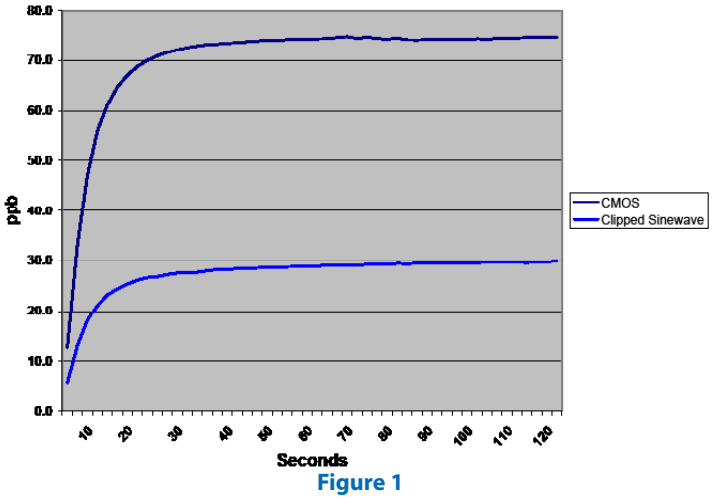


Figure 1

The VT-803 start up time is rated at 2ms. Figure 1 shows the Output Frequency versus time in seconds which shows the output reaching a steady state frequency within 60 seconds.

Frequency versus Vc Over Temperature

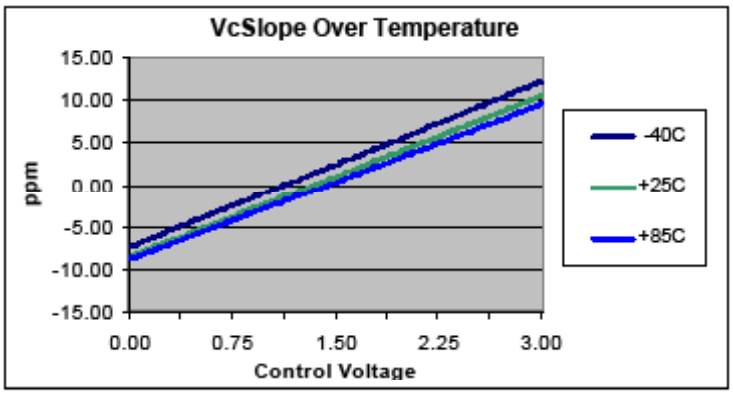


Figure 2

The VT-803 output frequency change versus control voltage is very linear and Figure 2 show the typical performance over temperature.

Allan Deviation, Clipped Sine Wave Output

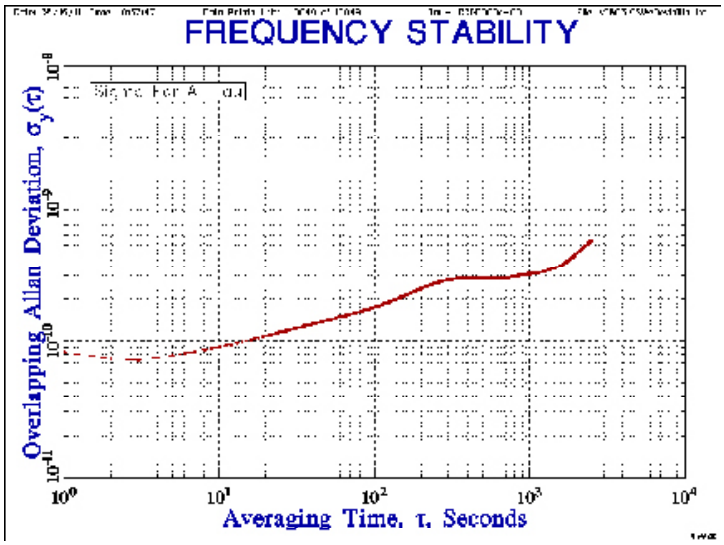


Figure 3

Test Conditions are under room ambient air flow (non insulated conditions).

Allan Deviation, CMOS Output

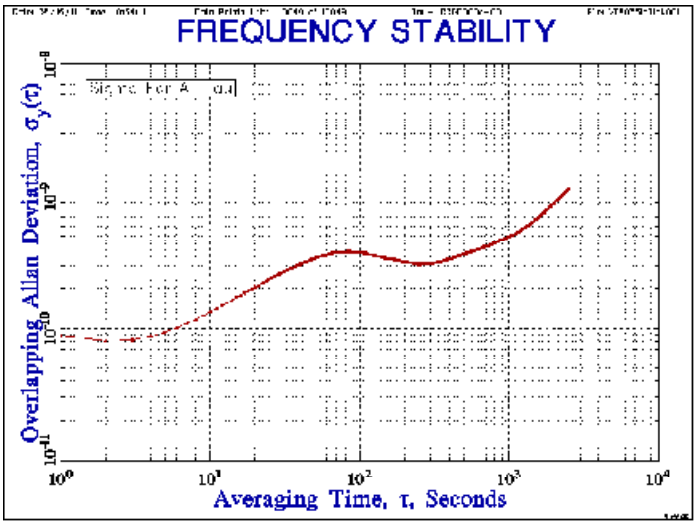


Figure 4

Test Conditions are under room ambient air flow (non insulated conditions).

Aging

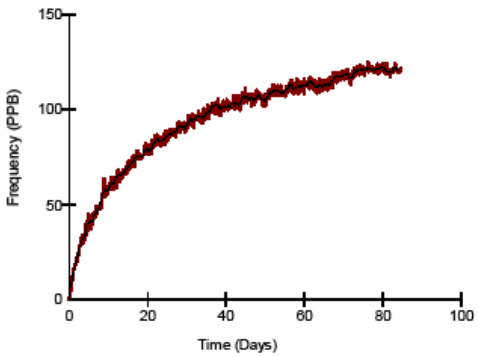


Figure 5

Figure 5 shows an output frequency change of 125ppb typical over 85 days at 85°C which would be equivalent to 125ppb over 2.25 years at 40°C.

Temperature Stability Graph

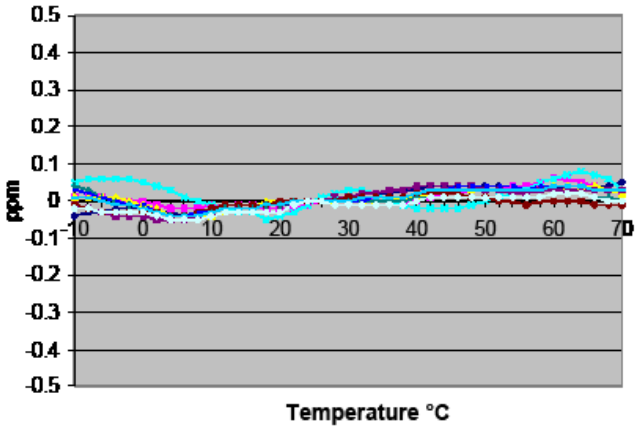


Figure 6

Delta Frequency vs. Temperature

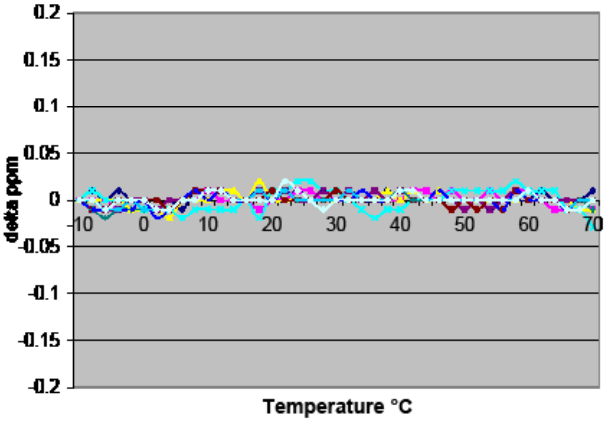


Figure 7

Figure 7 shows the change in frequency reading between every adjacent 2°C readings.

Phase Noise Performance, Clipped Sine Wave

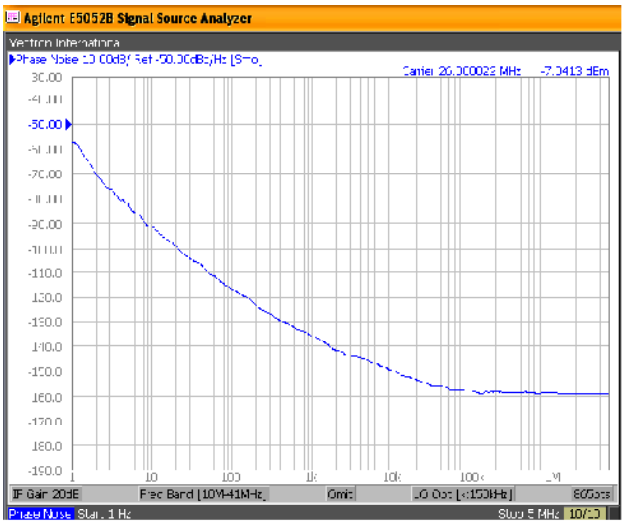


Figure 8

Phase Noise Performance, CMOS

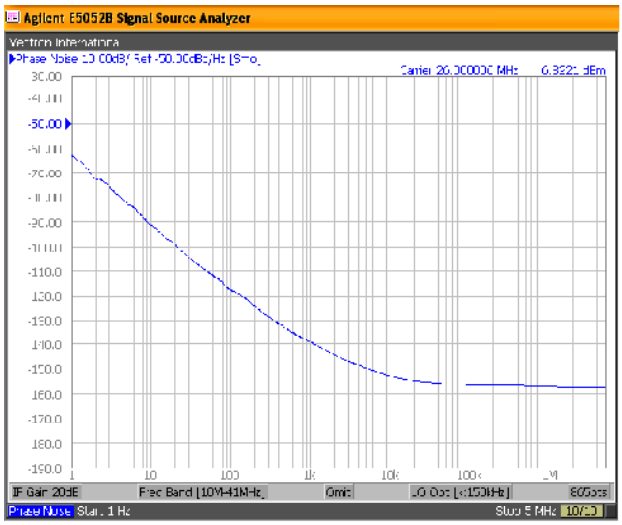


Figure 9

Phase Noise Over Temperature

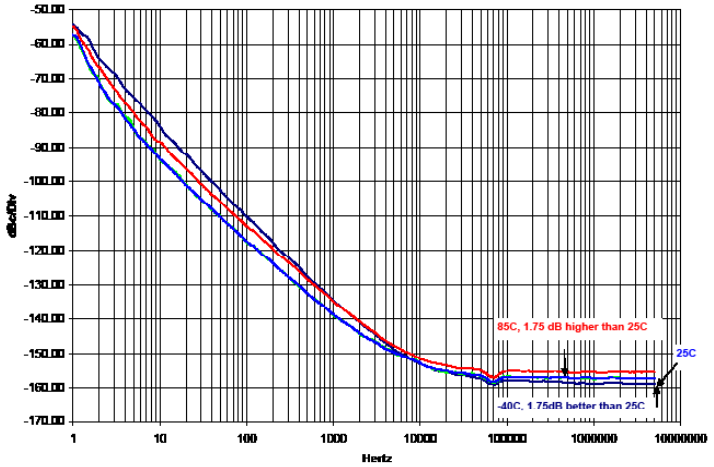


Figure 10

Figure 10 shows the difference in the phase noise at 85°C, 25°C and -40°C.

Phase Noise Over Power Supply Variation

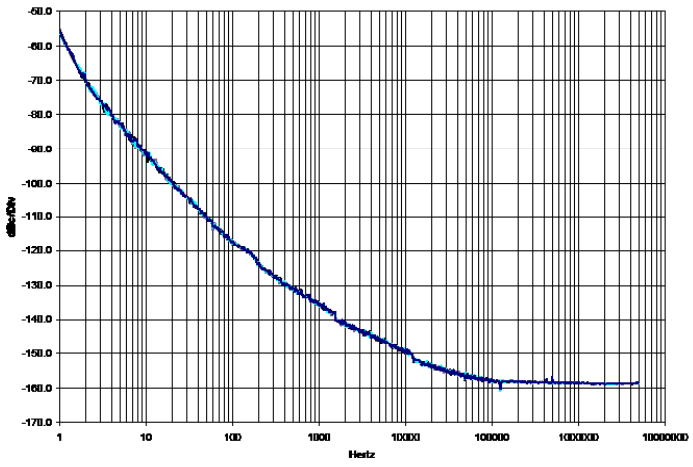


Figure 11

Figure 11 is a phase noise plot at a 2.8, 3.0, 3.3 and 3.6 volt power supply which demonstrates there is no significant change in performance.

VCXO Function

VCXO Feature: The VT-803 is supplied with a VCXO function for applications were it will be used in a PLL, or the output frequency needs fine tune or calibration adjustments. This is a high impedance input , 100 Kohm, and can be driven with an op-amp or terminated with adjustable resistors etc. **Pin 1 should not be left floating on the VCXO optional device.**

Maximum Ratings

Absolute Maximum Ratings and Handling Precautions
Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Although ESD protection circuitry has been designed into the VT-803, proper precautions should be taken when handling and mounting, Vectron employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation.
ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5kOhms and capacitance of 100pF is widely used and therefor can be used for comparison purposes.

Table 5. Maximum Ratings

Parameter	Symbol	Rating	Unit
Storage Temperature	T_{STORE}	-55/125	°C
Supply Voltage	V_{DD}	-0.6/6	V
Control Voltage	V_C	-0.6/V_{DD}+0.6	V
Enable/Disable Voltage	E/D	-0.6/V_{DD}+0.6	V
ESD, Human Body Model		1500	V
ESD, Charged Device Model		1000	V

Reliability

Table 6. Environmental Compliance

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002 (1500 G, 0.5 msec)
Mechanical Vibration	MIL-STD-883 Method 2007 (20 G Peak Acceleration)
Temperature Cycle	MIL-STD-883 Method 1010 (-55/85°C)
Solderability	MIL-STD-883 Method 2003 (Lead free solder)
Fine and Gross Leak	MIL-STD-883 Method 1014 (Crystal)
Resistance to Solvents	MIL-STD-883 Method 2015 (IPA solvent)
Moisture Sensitivity Level	MSL1
Termination Finish	Gold (0.3-1.0um) over Nickel
Weight	70 mg
ThetaJC	6 °C/W

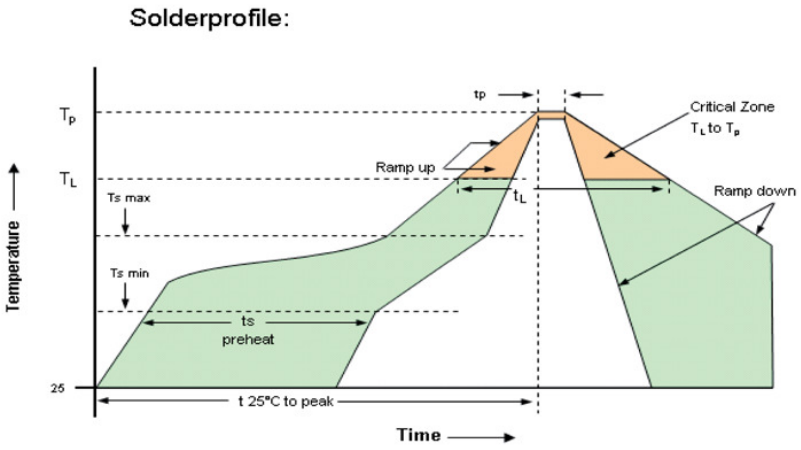
Test conditions: ±2.0 ppm change limit.

IR Reflow

Suggested IR Profile

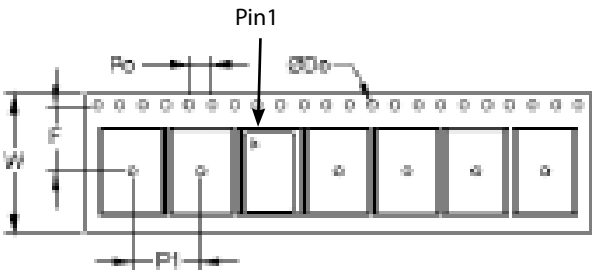
Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 7. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220°C.

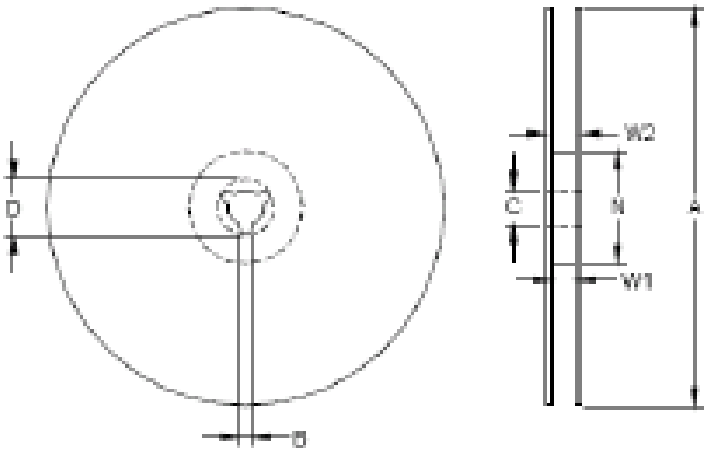
Table 7 Reflow Profile		
Parameter	Symbol	Value
PreHeat Time Ts-min Ts-max	t_s	200 sec Max 150°C 200°C
Ramp Up	R_{UP}	3°C/sec Max
Time above 217C	t_L	150 sec Max
Time to Peak Temperature	$t_{25C\ to\ peak}$	480 sec Max
Time at 260C	t_P	30 sec Max
Time at 240C	t_{P2}	60 sec Max
Ramp down	R_{DN}	6°C/sec Max



Tape & Reel

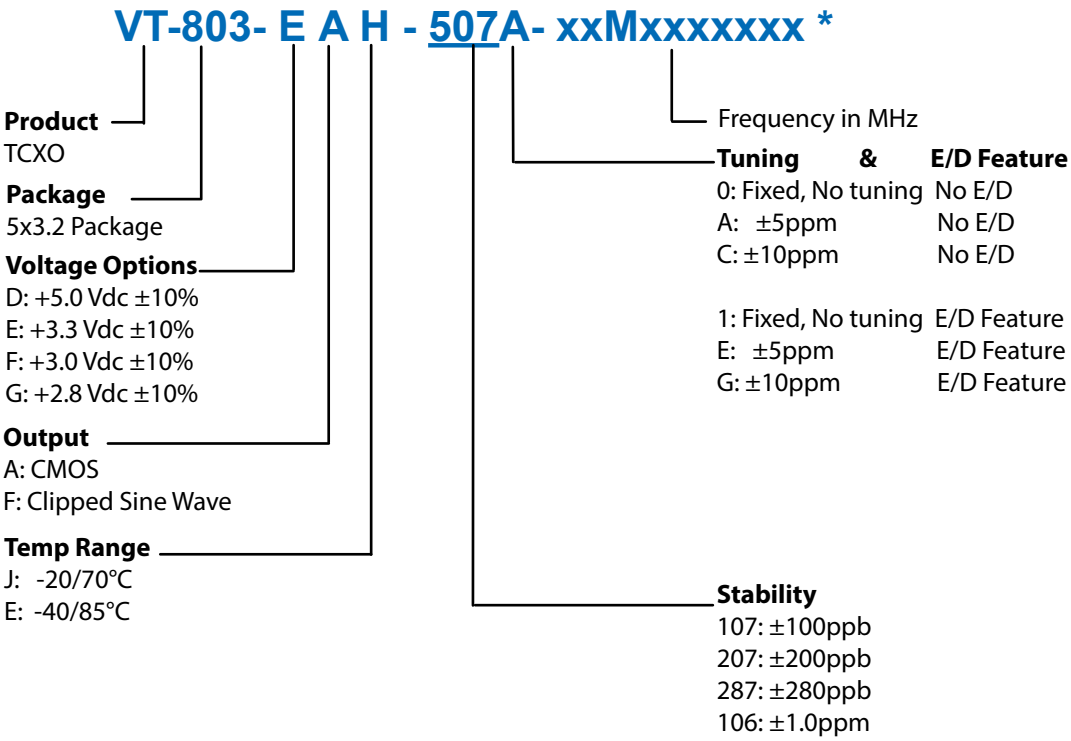
Table 8. Tape and Reel Information												
Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
12	5.5	1.5	4	8	254	2.5	13	21	100	13.5	17.5	2000





Ordering Information

Table 9. Standard Frequencies (MHz)									
10.000	12.800	16.000	16.384	16.800	19.200	19.440	20.000	20.480	24.000
24.576	25.000	26.000	27.000	28.800	29.792	30.000	30.720	31.250	32.000
33.333	36.000	38.400	38.880	39.000	40.000	48.000	49.152	50.000	52.000



* Add _SNPB for tin lead solder dip

Example: VT-803-EAE-2870-40M0000000_SNPB

Revision Date	Description
Nov 4, 2013	Updated product capability chart (Table 9 & 10). Changed VI Asia contact information.
Jan 7, 2014	Added "temperature stability measurement at Mid Vc for parts with frequency tuning option". Removed Delta 1s Frequency Plot.
Feb 18, 2014	Added temp stability measurement condition on parts with Vc feature. Changed Vectron logo and Hudson contact information.
Sep 3, 2014	Modified Package Drawing Orientation, added tuningl slope (positive), red bullet in Capability Chart
June 28, 2018	Add: E/D function, E/D specifications, E/D Table. New Frequencies,Stratum3/SyncE, ±4.6ppm overall stability, ±0.37ppm temperature plus 24 hours (for stabilities <= ±280ppb), weight and thetaJC. Updated CMOS load and power supply stability. Update test conditions and clipped sine wave current limit >26MHz to 52MHz. Add new Table 3; Enable/Disable Table. Deleted Capabilities Tables 9 and 10. Add _SNPBDIP ordering option and example. Change Vectron logo to Microsemi/Microchip.
May 24, 2019	Update logo, contact information and ordering options.

Contact Information

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