ADSP-BF609 EZ-KIT Lite®
Evaluation System Manual

Revision 1.1, May 2014

Part Number
82-000269-01

Analog Devices, Inc.
One Technology Way
Norwood, Mass. 02062-9106

ANALOG DEVICES

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Regulatory Compliance

The ADSP-BF609 EZ-KIT Lite is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The ADSP-BF609 EZ-KIT Lite has been certified to comply with the essential requirements of the European EMC directive 2004/108/EC and therefore carries the "**CE**" mark.

The ADSP-BF609 EZ-KIT Lite has been appended to Analog Devices, Inc EMC Technical File (EMC TF) referenced **DSPTOOLS1**, issue 2 dated June 4, 2008 and was declared CE compliant by an appointed Notified Body (No.0673) as listed below.

Notified Body Statement of Compliance: Z600ANA2.043 dated August 24, 2012.

Issued by: Technology International (Europe) Limited
56 Shrivenham Hundred Business Park
Shrivenham, Swindon, SN6 8TY, UK

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

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PREFACE

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ADSP-BF609 EZ-KIT LITE HARDWARE REFERENCE

PREFACE

Thank you for purchasing the ADSP-BF609 EZ-KIT Lite®, Analog Devices, Inc. low-cost evaluation system for the ADSP-BF60x Blackfin® processors.

The ADSP-BF609 processor is a member of the Blackfin family of products, incorporating the Analog Devices/Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

ADSP-BF60x Blackfin processors embody a new type of embedded processor designed specifically to meet the computational demands and power constraints of today's automotive systems, embedded industrial, instrumentation, and power/motor control applications.

The evaluation board is designed to be used in conjunction with the CrossCore® Embedded Studio (CCES) development tools to test capabilities of the ADSP-BF60x Blackfin processors. The CCES development environment aids advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory

- Read and write core and peripheral registers
- Plot memory

Access to the processor from a personal computer (PC) is achieved through a USB port (when a debug agent is mounted on the EZ-KIT Lite board) or an external JTAG emulator. The USB interface provides unrestricted access to the ADSP-BF609 processor and evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to: http://www.analog.com/processors/tools/.

The ADSP-BF609 EZ-KIT Lite provides example programs to demonstrate the product capabilities.

The ADSP-BF609 EZ-KIT Lite software is part of the EZ-Board® BSP (Board Support Package) for the Blackfin ADSP-BF60x family which needs to be installed after CrossCore Embedded Studio. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for 90 days after activation. For more information, refer to Evaluation License in this manual and the *Installation Quick Reference Card*.

Product Overview

The board features:

- Analog Devices ADSP-BF609 Blackfin processor
  - 349-pin LFBGA package
  - 25 MHz CLKIN oscillator
  - 48 MHz USB CLKIN

- Double Data Rate Synchronous Dynamic Random-Access Memory (DDR2 SDRAM)
    - Micron MT47H64M16HR-3
    - 64M x 16 bit (1 Gb)
- Burst flash memory
    - Micron PC28F128P33T85B
    - 16M x 16-bit (32 MB) flash memory
- Quad Serial Peripheral Interface (SPI)
    - Winbond W25Q32
    - 32 Mb serial flash memory
- Ethernet PHY
    - National Semiconductor
    - DP83848C 10/100 PHY
    - Two LEDs integrated into the RJ-45 connector: link/activity
- Universal Asynchronous Receiver/Transmitter (UART)
    - ADM3315 RS-232 line driver/receiver
    - DB9 female connector
- Temp sensor
    - On Semiconductor
    - ADM1032 two-wire sensor

- Controller Area Network (CAN)
    - NXP TJA1041
    - RJ-11 connector
- Debug interface
    - JTAG header for use with ADI emulators
    - Standalone debug agent
- LEDs
    - Eight LEDs: one power (green), one board reset (red), one temperature limit (amber), Ethernet speed (green), and four general-purpose (amber)
- Push buttons
    - Four push buttons: one reset, one wake, and two IRQ/flag
- Expansion Interface 3 (EI3)
    - Next generation of the expansion interface design, provides access to most of the processor signals
- Power supply
    - CE approved
    - 5V @ 3.6 Amps
- Other features
    - Link port connectors
    - SD/MMC memory connector
    - Rotary encoder
    - MP JTAG in and out connectors
    - 0.05-ohm resistors for processor current measurement

- JTAG ICE 14-pin header
- USB cable

Traditional mechanical switches for changing the board's factory setup have been removed in favor of I^2C controlled software switches. The only remaining mechanical switches are the JTAG switches, boot mode switch, and push buttons. The JTAG switches are provided for setting up single-processor JTAG communications or multiple-processor configurations.

For information about the hardware components of the EZ-KIT Lite, refer to ADSP-BF609 EZ-KIT Lite Bill Of Materials.

Purpose of This Manual

The *ADSP-BF609 EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes operation and configuration of the board components and provides guidelines for running your own code on the ADSP-BF609 EZ-KIT Lite. Finally, a schematic and a bill of materials are provided for reference.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture, instruction set, and C/C++ programming languages.

Programmers who are unfamiliar with Analog Devices processors can use this manual, but should supplement it with other texts (such as the *ADSP-BF60x Blackfin Processor Hardware Reference* and *Blackfin Processor Programming Reference*) that describe your target architecture.

Programmers who are unfamiliar with CrossCore Embedded Studio should refer to the CCES online help.

Manual Contents

The manual consists of:

- Chapter 1, Using ADSP-BF609 EZ-KIT Lite.
  Describes EZ-KIT Lite functionality from a programmer's perspective and provides a simplified memory map of the processor.
- Chapter 2, ADSP-BF609 EZ-KIT Lite Hardware Reference.
  Provides information about the EZ-KIT Lite hardware components.
- Appendix A, ADSP-BF609 EZ-KIT Lite Bill Of Materials.
  Provides a list of hardware components used to manufacture the EZ-KIT Lite board.
- Appendix B, ADSP-BF609 EZ-KIT Lite Schematic.
  Lists the resources for board-level debugging.

What's New in This Manual

This is Revision 1.1 of the *ADSP-BF609 EZ-KIT Lite Evaluation System Manual*. Changes to this manual from the previous revision (Revision 1.0) include compliance certification and a revised Figure 1-2, Processor Memory Map.

Technical Support

You can reach Analog Devices processors and DSP technical support in the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:
  http://ez.analog.com/community/dsp
- Submit your questions to technical support directly at:
  http://www.analog.com/support
- E-mail your questions about processors, DSPs, and tools development software from **CrossCore Embedded Studio** or **VisualDSP++®**:

  Choose **Help > Email Support**. This creates an e-mail to processor.tools.support@analog.com and automatically attaches your **CrossCore Embedded Studio** or **VisualDSP++** version information and `license.dat` file.
- E-mail your questions about processors and processor applications to:
  processor.support@analog.com or
  processor.china@analog.com (Greater China support)
- In the **USA only**, call **1-800-ANALOGD** (1-800-262-5643)
- Contact your Analog Devices sales office or authorized distributor. Locate one at:
  www.analog.com/adi-sales

- Send questions by mail to:
  Processors and DSP Technical Support
  Analog Devices, Inc.
  Three Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Supported Processors

This evaluation system supports Analog Devices ADSP-BF609 Blackfin embedded processors.

Product Information

Product information can be obtained from the Analog Devices Web site and the CCES online help system.

Analog Devices Web Site

The Analog Devices Web site, www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, myAnalog.com is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest

information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. myAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Visit myAnalog.com (found on the Analog Devices home page) to sign up. If you are a registered user, just log on. Your user name is your e-mail address.

EngineerZone

EngineerZone is a technical support forum from Analog Devices. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

Related Documents

For additional information about the product, refer to the following publications.

Table 1. Related Processor Publications

Title	Description
ADSP-BF606/ADSP-BF607/ADSP-BF608/ ADSP-BF609 Blackfin Dual Core Embedded Processor Data Sheet	General functional description, pinout, and timing of the processor
ADSP-BF60x Blackfin Processor Hardware Reference	Description of the internal processor architecture and all register functions
Blackfin Processor Programming Reference	Description of all allowed processor assembly instructions

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
File > Close	Titles in reference sections indicate the location of an item within the CCES environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.

Example	Description
.SECTION	Commands, directives, keywords, and feature names are in text with letter gothic font.
filename	Non-keyword placeholders appear in text with italic style format.
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

1 USING ADSP-BF609 EZ-KIT LITE

This chapter provides information to assist you with development of programs for the ADSP-BF609 EZ-KIT Lite evaluation system.

The following topics are covered.

- UART Interface
- Rotary Encoder Interface
- Temperature Sensor Interface
- Link Ports Interface
- General-Purpose I/O (GPIO)
- JTAG Interface
- Power-On-Self Test
- Expansion Interface III
- Power Architecture
- Power Measurements
- Example Programs
- Reference Design Information

For information about the CCES graphical user interface (GUI), including the boot loading, target options, and other facilities of the EZ-KIT Lite system, refer to the online help.

For detailed information about the ADSP-BF609 Blackfin processor, see documents referred to as Related Documents.

Package Contents

Your ADSP-BF609 EZ-KIT Lite package contains the following items.

- ADSP-BF609 EZ-KIT Lite board
- Standalone debug agent (SADA2)

- USB cable
- 5 in 1 USB cable kit
- CE approved power supply
- Ethernet cable
- 2 GB memory card
- 4 nylon standoffs
- 4 nylon hex nuts

With the standalone debug agent removed, the board can connect to an Analog Devices emulator: USB, HP-USB, or ICE-100B.

Contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc. if any item is missing.

ADSP-BF609 EZ-Board

The product ADSP-BF609 EZ-KIT Lite with the Stand Alone Debug Agent removed is referred to as the ADSP-BF609 EZ-Board.

The EZ-Board requires an Analog Devices USB-based emulator (USB, HP-USB, or ICE-100B).

Default Configuration

The ADSP-BF609 EZ-KIT Lite board is designed to run as a standalone unit.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which can damage some components.

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

Figure 1-1 shows the default jumper and switch settings and LED used in installation. There are four nylon standoffs in a bag included in the box. They can be installed in the four corner mounting holes (MH1, MH7, MH8, MH9) if desired. Place the nylon standoff in the hole and tighten a hex nut on each. Confirm that your board is in the default configuration before using the board.

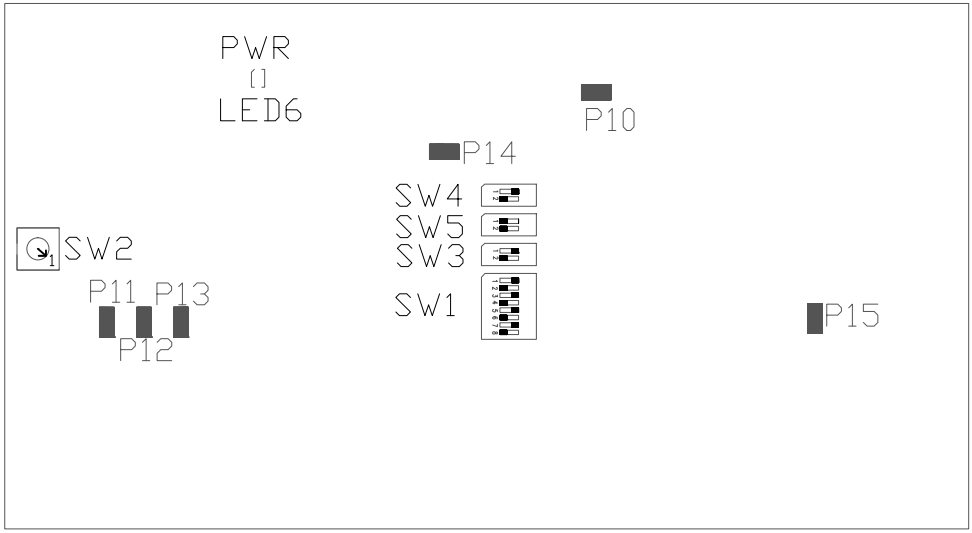


Figure 1-1. EZ-KIT Lite Hardware Setup

Supported Operating Systems

CCES 1.0.0 is supported on the following operating systems:

- Windows® XP Professional SP3 (32-bit only)
- Windows Vista™ Business, Enterprise, or Ultimate SP2 (32-bit only)
- Windows 7 Professional, Enterprise, or Ultimate (32- and 64-bit)

Windows Vista and Windows 7 users may experience User Access Control (UAC) related errors if the software is installed into a protected location, such as `Program Files` or `Program Files (x86)`. We recommend installing the software in a non-UAC-protected location.

System Requirements

Verify that your PC has these minimum requirements for the CCSE 1.0.0 installation:

- 2 GHz single-core processor
- 1 GB RAM
- 8 GB available disk space
- One open USB port

A faster disk drive decreases the build time, especially for a large amount of source files .

EZ-KIT Lite Installation

Follow these instructions to ensure correct operation of the product software and hardware.

Step 1: Attach the provided USB plugs (labeled `Mini` and `Male`) to the provided USB cable.

Step 2: Connect the EZ-KIT Lite board to a personal computer (PC) running CCES.

There are two connection options: using an Analog Devices emulator or using the standalone debug agent.

Using an Emulator:

1. Plug one side of the assembled USB cable into the USB connector of the emulator. Plug the other side into a USB port of the PC running CCES.
2. Attach the emulator to the header connector `P1` (labeled `JTAG`) on the EZ-KIT Lite board.

Using the Debug Agent:

1. Attach the standalone debug agent to connectors `P1` and `ZP1` of the EZ-KIT Lite board.
2. Plug one side of the provided USB cable into the USB connector of the debug agent `ZP1` (labeled `USB`). Plug the other side of the cable into a USB port of the PC running CCES.

Step 3: Attach the provided cord and appropriate plug to the 5V power adaptor.

1. Plug the jack-end of the assembled power adaptor into the power connector P18 (labeled 5V) on the EZ-KIT Lite board.
2. Plug the other side of the power adaptor into a power outlet. The power LED (labeled LED6) lights green when power is applied to the board.
3. Power the emulator. Plug the jack-end of the assembled power adaptor into the emulator and plug the other side of the power adaptor into a power outlet. The ENABLE/POWER indicator lights green.

Step 4 (if connected through the debug agent): Verify that the yellow USB monitor LED and the green power LED on the debug agent are both on. This signifies that the board is communicating properly with the host PC and ready to run CCES.

EZ-KIT Lite Session Startup

It is assumed that the CrossCore Embedded Studio software is installed and running on your PC.

Note: If you connect the board or emulator first (before installing CCES) to the PC, the Windows driver wizard may not find the board drivers.

1. Navigate to the CCES environment via the **Start** menu.

   Note that CCES is not connected to the target board.

2. Use the system configuration utility to connect to the EZ-KIT Lite board.

   If a debug configuration exists already, select the appropriate configuration and click **Apply and Debug** or **Debug**. Go to step 8.

   To create a debug configuration, do one of the following:

   - Click the down arrow next to the little bug icon, select **Debug Configurations**
   - Choose **Run > Debug Configurations**.

   The **Debug Configuration** dialog box appears.

3. Select **CrossCore Embedded Studio Application** and click  (**New launch configuration**).

   The **Select Processor** page of the **Session Wizard** appears.

4. Ensure **Blackfin** is selected in **Processor family**. In **Processor type**, select **ADSP-BF609**. Click **Next**.

   The **Select Connection Type** page of the **Session Wizard** appears.

5. Select one of the following:

   - For standalone debug agent connections, **EZ-KIT Lite** and click **Next**.
   - For emulator connections, **Emulator** and click **Next**.

   The **Select Platform** page of the **Session Wizard** appears.

6. Do one of the following:
    - For standalone debug agent connections, ensure that the selected platform is **ADSP-BF609 EZ-KIT Lite via Debug Agent**.
    - For emulator connections, choose the type of emulator that is connected to the board.
7. Click **Finish** to close the wizard.

   The new debug configuration is created and added to the program(s) to load list.
8. In the **Program(s) to load** section, choose the program to load when connecting to the board. If not loading any program upon connection to the target, do not make any changes.

   Note that while connected to the target, there is no way to choose a program to download. To load a program once connected, terminate the session.

To delete a configuration, go to the **Debug Configurations** dialog box and select the configuration to delete. Click ✖ and choose **Yes** when asked if you wish to delete the selected launch configuration. Then **Close** the dialog box.

To disconnect from the target board, click the terminate button (red box) or choose **Run > Terminate**.

To delete a session, choose **Target > Session > Session List**. Select the session name from the list and click **Delete**. Click **OK**.

Evaluation License

The ADSP-BF609 EZ-KIT Lite software is part of the Board Support Package (BSP) for the Blackfin ADSP-BF60x family. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for 90 days after activation. Once the evaluation period ends, the evaluation license becomes permanently disabled. If the evaluation license is installed but not activated, it allows 10 days of unrestricted use and then becomes disabled. The license can be re-enabled by activation.

An evaluation license can be upgraded to a full license. Licenses can be purchased from:

- Analog Devices directly. Call (800) 262-5645 or 781-937-2384 or go to:
  `http://www.analog.com/buyonline`.
- Analog Devices, Inc. local sales office or authorized distributor. To locate one, go to:
  `http://www.analog.com/salesdir/continent.asp`.

The EZ-KIT Lite hardware must be connected and powered up to use CCES with a valid evaluation or full license.

Memory Map

The ADSP-BF609 processor has a single unified 4G memory space for instructions and data storage. See Figure 1-2. The processor's memory details can be found in the *ADSP-BF60x Blackfin Processor Hardware Reference*.

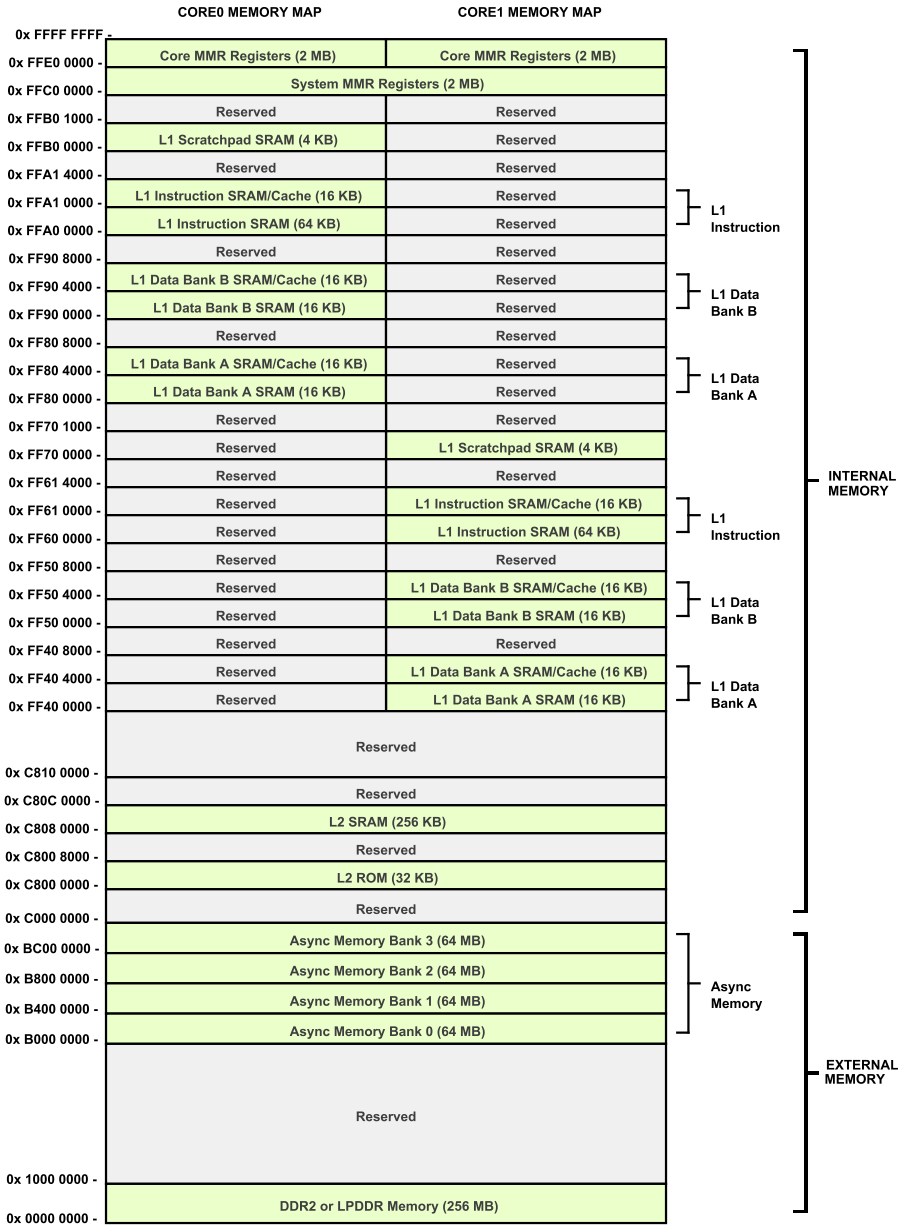


Figure 1-2. ADSP-BF609 Processor Memory Map

The board has a 16M x 16-bit burst flash memory connected to the processor's Static Memory Controller (SMC). The processor also is connected to a 32 Mb quad serial flash memory via the Serial Peripheral Interface (SPI). Both flash memories can be used for non-volatile data storage and processor boot.

DDR2 SDRAM

The ADSP-BF609 processor connects to a 128 MB Micron MT47H64M16HR-3 chip through the Double Data Rate Synchronous Dynamic Random-Access Memory (DDR2 SDRAM) controller. The DDR2 memory controller on the processor and DDR2 memory chip are powered by the on-board 1.8V regulator. Data is transferred between the processor and DDR2 on both the rising and falling edges of the DDR2 clock. The DDR2 controller on the processor can operate at a maximum clock frequency of 250 MHz.

With a CCES session running and connected to the EZ-KIT Lite via the USB standalone debug agent, the DDR2 registers are configured automatically each time the processor is reset. The values are used whenever DDR2 is accessed through the debugger (for example, when viewing memory or loading a program).

To disable the automatic setting of the DDR2 registers, select **Target > Settings > Target Options** in CCES and disable **Use XML reset values**.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to setup and access the DDR2 interface. For more information on how to initialize the registers after a reset, refer to the hardware reference manual.

SPI Interface

The ADSP-BF609 processor has two SPI interfaces, SPI0 and SPI1. SPI0 is connected to a Winbond W25Q32BV 32 Mb serial flash memory with dual and quad SPI support.

Quad mode is enabled by default. The processor flag signals, PD00 and PD01 (SPI0 D2 and D3), can be disconnected by using SoftConfig. Refer to Software-Controlled Switches (SoftConfig) for more information. By default, the SPI0 chip select 1 is connected to the memory device. This can also be disconnected by using SoftConfig.

SMC Interface

The Static Memory Controller (SMC) interface of the ADSP-BF609 EZ-KIT Lite contains a 32 MB (16M x 16) Numonyx PC28F128P33B parallel flash chip. Flash memory is connected to the 16-bit data bus and address lines 1-23. Chip enable is decoded by using $\overline{\text{SMC0\_AMS0}}$.

The flash memory is bottom boot and provides One-Time-Programmable (OTP) memory.

Flash memory is preloaded with boot code for the POST program. For more information, refer to Power-On-Self Test.

Ethernet Interface

The ADSP-BF609 processor has two Reduced Media Independent Interfaces (RMIIs), one of which connects to an external Ethernet PHY device. The EZ-KIT Lite provides a National DP83848C, Auto-MDIX, fully compliant PHY with IEEE 802.2/802.2u standards. The PHY supports 10BASE-T and 100BASE-TX operations.

The PHY and processor support IEEE 1588 time stamping, available on the EZ-KIT Lite via a standard RJ-45 connector. For more information, see Ethernet Connector (J1).

The MAC address is stored in parallel flash (U44) at address 0x0106 0000, and can be found on a sticker on the bottom side of the board.

If a program is written over this area of the flash, the MAC address will be lost.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate how to use the Ethernet interface.

USB OTG HS Interface

The ADSP-BF609 processor has an integrated USB PHY, and the EZ-KIT Lite provides a mini AB connector. A 48 MHz oscillator provides the clocking for the high-speed USB 2.0 On-the-Go (OTG) interface.

The board allows 5V at 500 mA to a peripheral by enabling the FET switch `U50`. The USB controller has native support for controlling the FET through the `USB_VBC` signal.

A test point also is provided for the USB clock input of the processor. A user can remove the series resistor and feed an external clock from a function generator.

Use the example programs in the EZ-KIT Lite installation directory to learn about the processor's device and host modes. For more information, refer to the *ADSP-BF60x Blackfin Processor Hardware Reference*.

CAN Interface

The Controller Area Network (CAN) interface of the EZ-KIT Lite is connected to the NXP TJA1041 high-speed CAN transceiver. The transceiver is attached to the CAN0 port of the ADSP-BF609 processor via an RJ-11 connector. See CAN Connector (J4).

The PE02 programmable flag connects to the error and power on indication output of the CAN transceiver, CAN0. The transmit and receive pins of the transceiver are connected to the dedicated CAN0 transmit and receive pins of the processor.

To disconnect the CAN IC signals CAN0RX and CAN0_ERR, change the appropriate settings via SoftConfig. See Software-Controlled Switches (SoftConfig).

Example programs are included in the EZ-KIT Lite installation directory to demonstrate CAN circuit operation.

UART Interface

The ADSP-BF609 processor has two built-in universal asynchronous transmitters (UARTs), with only UART0 connected to a UART line transmitter. UART0 has full RS-232 functionality via the Analog Devices ADM3315 line driver and receiver (U39).

Pin PD07/$\overline{\text{UART0\_TX}}$/TM0_ACI3 of the processor is connected to the ADM3315 device directly. Pin PD08/$\overline{\text{UART0\_RX}}$/TM0_ACI0 is connected as well by the default setting of SoftConfig. (This can be changed by the SoftConfig switch).

By default, UART0 RTS and CTS signals are not connected (but can be through SoftConfig). The SoftConfig switches also allow the loopback of CTS and RTS. UART CTS can be added as an input to the reset circuit

through SoftConfig. Pins 1, 4 and 6 of the UART connector (J2) can be enabled as an input to the on-board reset circuit through SoftConfig.

Refer to Software-Controlled Switches (SoftConfig) for more information.

An example program demonstrating UART0 in POST is included in the EZ-KIT Lite installation directory. Note that the loopback of TX and RX data is done through an external connector.

SD Interface

The ADSP-BF609 processor has a secure digital (SD) interface. The SD interface consists of a clock pin, command pin, card detect pin, write protect pin, and an 8-bit data bus. SoftConfig controls the connection of processor pins PG10 and PG13 to the card detect and write protect features of the SD interface. Refer to Software-Controlled Switches (SoftConfig) and SD Connector (J5)for more details.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to set up and access the SD interface.

Rotary Encoder Interface

The ADSP-BF609 processor has a built-in, up-down counter with support for a rotary encoder. The three-wire rotary encoder interface connects to the rotary switch (SW9). The rotary encoder can be turned clockwise for the up function, counter clockwise for the down function, or can be pushed towards the center of the board to clear the counter.

The rotary switch is a two-bit quadrature (gray code) counter with detent, meaning that both the down signal (CNT0_DG) and up signal (CNT0_UD) toggle when the count register increases on a rotation to the right.

Upon rotating to the left, CNT0_DG and CNT0_UD toggle, and the overall count decreases.

If the processor pins are needed on the expansion interface III, disconnect the rotary encoder switch via SoftConfig. See Software-Controlled Switches (SoftConfig) for details.

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to set up and access the rotary encoder.

Temperature Sensor Interface

Two external pins (SYS_TDA and SYS_TDK) of the processor are connected to an internal thermal diode. The EZ-KIT Lite uses ON Semiconductor ADM1032 digital thermometer and under/over temperature alarm to monitor the processor's temperature as well as the thermal diodes inside the ADM1032 device. The thermometer uses the I^2C bus and flag pins of the processor. The following software-controlled signals are used for temperature monitoring.

- TEMP_IRQ_EN (programmable flag pin PG9)
- TEMP_THERM_EN (programmable flag pin PB15)

The thermal limit flag is connected to an LED (LED5) for a visual alarm if the temp exceeds the limit. The thermal limit flag and ADM1032 IRQ connect to flag pins of the processor, but are nonessential for temperature monitoring. Consequently, the software-controlled switches have these signals disconnected from the ADSP-BF609 processor by default.

See Thermal Limit LED (LED5) and Software-Controlled Switches (SoftConfig) for more information.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate temperature sensor operations.

Link Ports Interface

The ADSP-BF609 processor has four dedicated link ports. Each link port has a clock pin, an acknowledgment pin, and eight data pins. The ports can operate at up to 83 MHz and act as either a receiver or a transmitter. The ports are used to interface gluelessly to other ADSP-BF609 processors which also have the link ports pins brought out.

The EZ-KIT Lite enables access to link ports 0 and 1 (referred to as LP0 and LP1 in schematics) via connectors P8 and J3, respectively. Two ADSP-BF609 EZ-KIT Lites can mate gluelessly via the link port connectors. The processors communicate via the link ports, all while performing independent tasks on each of the EZ-KIT Lite. To loopback the link port connectors on one EZ-KIT Lite or connect three or more EZ-KIT Lites, obtain a standard, off the shelf connector from Samtec. For more information, see Link Port /JTAG Connectors (J3 and P8).

By default, the EZ-KIT Lite boots from the parallel flash memory. Link port 0 can be selected as the boot source by setting the boot mode select switch (SW2) to position 6. See Boot Mode Select Switch (SW2).

General-Purpose I/O (GPIO)

Four LEDs are available via programmable pins PG14, PG15, PE14, and PB11. The connections are on by default and can be shut off through SoftConfig.

Two push buttons are available on programmable flags PB10 and PE01. The push buttons are connected to the processor by default. Use SoftConfig to disconnect the push buttons. Refer to Software-Controlled Switches (SoftConfig) for more information.

JTAG Interface

The EZ-KIT Lite design enables a multi-processor JTAG session using connectors P8 and J3. By default, the board is set up in single-processor mode. In single-processor mode, create a CCES session based on a standalone debug agent or an external emulator. To use the EZ-KIT Lite in multi-processor mode, install an external emulator. Only one external emulator is required for the main EZ-KIT Lite; other EZ-KIT Lites in the JTAG chain do not require an emulator. In this mode, create a CCES platform based on the number of JTAG devices in the JTAG chain using the CCES Target Configurator. Then create a session for the EZ-KIT Lite based on the newly created platform.

For a dual ADSP-BF609 EZ-KIT Lite session, connect two EZ-KIT Lites via connectors J3 and P8. Flip one of the two EZ-KIT Lites by 180 degrees to allow the boards to mate. To switch between single- and multi-processor modes, use DIP switches SW1 and SW3-5. The switch settings can be found in JTAG Interface Switches (SW1, SW3–5).

For three or more ADSP-BF609 EZ-KIT Lite sessions, connect each of the boards with JTAG cables. The cables connect JTAG pins of each board and put the EZ-KIT Lites in a JTAG serial chain. For three EZ-KIT Lites, three JTAG cables are required. Similarly, for four EZ-KIT Lites, four JTAG cables are required. Note that each respective EZ-KIT Lite board also requires its own power supply.

The standalone debug agent can be replaced by an external emulator, such as the Analog Devices high-performance USB-based emulator. Be careful not to damage the connectors when removing the debug agent. The emulator is connected to P1 on the top side of the board. See EZ-KIT Lite Installation for more information.

Part numbers for Samtec standard, off the shelf link port cables can be found in Link Port /JTAG Connectors (J3 and P8).

For more information about emulators, contact Analog Devices or go to: http://www.analog.com/processors/tools.

Power-On-Self Test

The Power-On-Self-Test Program (POST) tests all EZ-KIT Lite peripherals and validates functionality as well as connectivity to the processor. Once assembled, each EZ-KIT Lite if fully tested for an extended period of time with POST. All EZ-KIT Lite boards are shipped with POST preloaded into one of their on-board flash memories. The POST is executed by resetting the board and pressing the proper push button(s). The POST also can be used as a reference for a custom software design or hardware troubleshooting. Note that the source code for the POST program is included in the EZ-KIT Lite installation directory along with the `readme.txt` file, which describes how the board is configured to run POST.

Expansion Interface III

The Expansion Interface III (EI3) allows an Analog Devices EZ-Extender® or a custom-design daughter board to be tested across various hardware platforms that have the same expansion interface.

The EI3 implemented on the ADSP-BF609 EZ-KIT Lite consists of five connectors, `P1A`, `P1B`, `P1C`, `P2A`, and `P3A`. The connectors contain a majority of the processor's signals. For pinout information, go to ADSP-BF609 EZ-KIT Lite Schematic. The mechanical dimensions of the expansion connectors can be obtained by contacting Technical Support.

For more information about daughter boards, visit the Analog Devices Web site at: http://www.analog.com/processors/tools.

Limits to current and interface speed must be taken into consideration when using the EI3. Current for the EI3 can be sourced from the EZ-KIT Lite; therefore, the current should be limited to 200 mA for 5V and 300 mA for the 3.3V planes. If more current is required, then a separate power connector and a regulator must be designed on the daughter card. Additional circuitry can add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

Power Architecture

The ADSP-BF609 EZ-KIT Lite has three primary voltage domains: 3.3V, 1.25V and 1.8V.

The Analog Devices ADP1864 controller provides 3.3V for the VDD_USB, VDD_EXT, and the 3.3V power requirements of the board. The Analog Devices ADP1715 regulator provides 1.8V for VDD_DMC. The processor's VDD_INT is regulated to 1.25V by the ADP2119 controller.

Power Measurements

Locations are provided for measuring the current draw from various power planes. Precision 0.05 ohm shunt resistors are available on the VDD_EXT, VDD_INT, VDD_DDR2, VDD_USB, 3.3V, and USB_VBUS voltage domains. For current draw, the jumper is removed, voltage across the resistor can be measured using an oscilloscope, and the value of the resistor can be measured using a precision multi-meter. Once voltage and resistance are measured, the current can be calculated by dividing the voltage by the resistance. For the highest accuracy, a differential probe should be used for measuring the voltage across the resistor. For more information, refer to Power Jumpers.

Example Programs

Example programs are provided with the ADSP-BF609 EZ-KIT Lite to demonstrate various capabilities of the product. The programs are installed with CCES and can be found in the CrossCore Embedded Studio directory. Refer to a readme file provided with each example for more information.

Reference Design Information

A reference design info package is available for download on the Analog Devices Web site. The package provides information on the design, layout, fabrication, and assembly of the EZ-KIT Lite.

The information can be found at:
http://www.analog.com/board-design-database.

2 ADSP-BF609 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-BF609 EZ-KIT Lite board.

The following topics are covered.

- System Architecture
  Describes the board's configuration and explains how the board components interface with the processor.
- Software-Controlled Switches (SoftConfig)
  Lists and describes the processor signals routed through the software-controlled switches.
- Push Buttons and Switches
  Shows the locations and describes the push buttons and switches.
- Power Jumpers
  Shows the locations and describes the configuration jumpers.
- LEDs
  Shows the locations and describes the LEDs.
- Connectors
  Shows the locations and provides part numbers for the on-board connectors. In addition, the manufacturer and part number information is provided for the mating parts.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board (Figure 2-1).

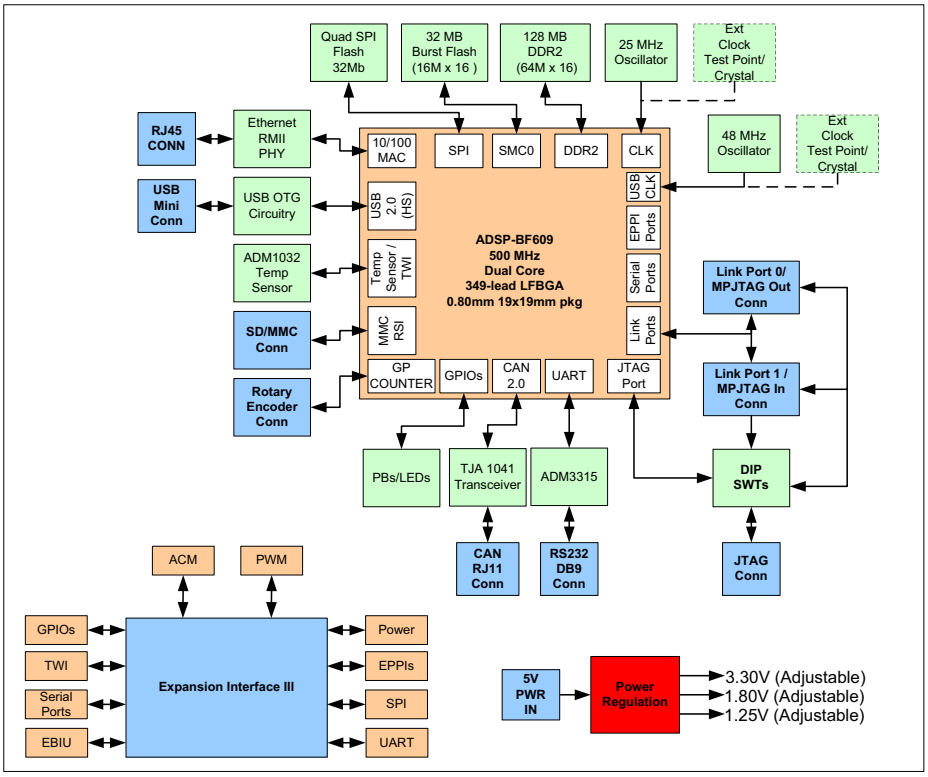


Figure 2-1. EZ-KIT Lite Block Diagram

The EZ-KIT Lite is designed to demonstrate the ADSP-BF609 Blackfin processor's capabilities.

The clock rate can be set up on the fly by the processor. The input clock is 25 MHz. The core clock runs at a maximum of 500 MHz. The default boot mode for the processor is parallel flash boot.

See Boot Mode Select Switch (SW2) for information on how to change the default boot mode.

Software-Controlled Switches (SoftConfig)

On the ADSP-BF609 EZ-KIT Lite, most of the traditional mechanical switches have been replaced by I^2C software-controlled switches. The remaining mechanical switches are provided for setting up a single- or multiprocessor JTAG session, changing the boot mode, and push buttons. Reference any `SoftConfig*.c` file found in the installation directory of CCES for an example of how to set up the SoftConfig feature of the ADSP-BF609 EZ-KIT Lite through software.

The SoftConfig section of this manual serves as a reference to any user that intends to modify an existing software example. If software provided from ADI is used there should be little need to reference this section.

Care should be taken when changing SoftConfig settings not to create a conflict with interfaces. This is especially true when connecting extender cards. There is one possible conflict on the EZ-KIT Lite when using SoftConfig—the wake push button must be disconnected when using the SD card interface. The wake push button is disabled by default, but if making changes, the signal `~WAKE_PUSHBUTTON_EN` must be set to high if the SD card function is desired.

Overview of SoftConfig

In order to further clarify the use of electronic single FET switches and multi-channel bus switches, an example of each is illustrated and compared to a traditional mechanical switching solution. This is a generic example that uses the same FET and bus switch components that are on

the EZ-KIT Lite. After this generic discussion there is a detailed explanation of the SoftConfig interface specific to the ADSP-BF609 EZ-KIT Lite.

Figure 2-2 shows two individual FET switches (Pericom PI3A125CEX) with reference designators UA and UB. Net names ENABLE_A and ENABLE_B control UA and UB. The default FET switch enable settings in this example are controlled by resistors RA and RB which pull the enable pin 1 of UA and UB to ground (low). In a real example, these enable signals are controlled by the Microchip IO expander. The default pull-down resistors connects the signals EXAMPLE_SIGNAL_A and EXAMPLE_SIGNAL_B and also connects signals EXAMPLE_SIGNAL_C and EXAMPLE_SIGNAL_D. To disconnect EXAMPLE_SIGNAL_A from EXAMPLE_SIGNAL_B, the Microchip IO expander is used to change ENABLE_A to a logic 1 through software that interfaces with the Microchip. The same procedure for ENABLE_B would disconnect EXAMPLE_SIGNAL_C from EXAMPLE_SIGNAL_D.

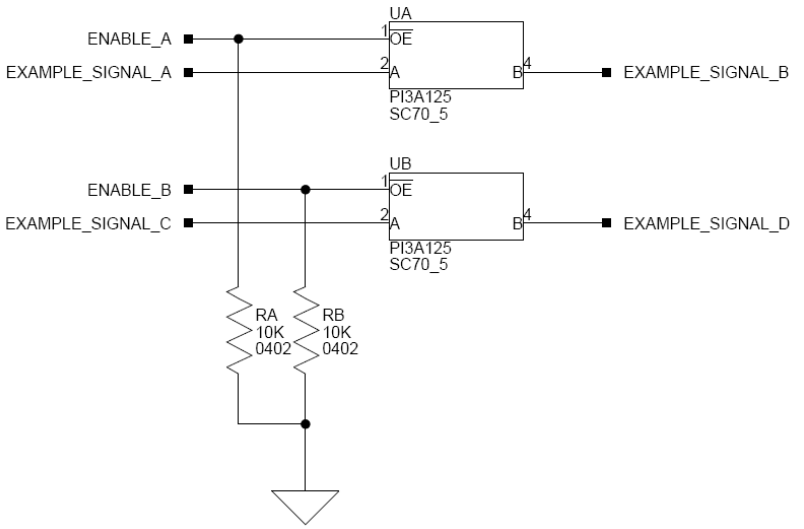


Figure 2-2. Example of Individual FET Switches

Figure 2-3 shows the equivalent circuit to Figure 2-2 but utilizes mechanical switches that are in the same package. Notice the default is shown by black boxes located closer to the ON label of the switches. In order to disconnect these switches, physically move the switch to the OFF position.

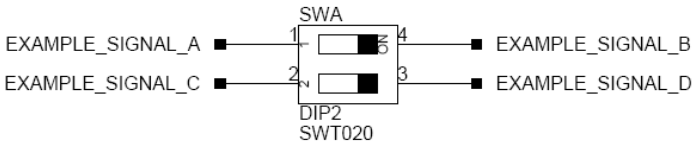


Figure 2-3. Example of Mechanical Switch Equivalent to Figure 2-2

Figure 2-4 shows a bus switch example, reference designator UC (Pericom PI3LVD512ZHE), selecting between lettered functionality and numbered functionality. The signals on the left side are multiplexed signals with naming convention letter_number. The right side of the circuit shows the signals separated into letter and number, with the number on the lower group (eg. OB1) and the letter on the upper group (eg. OB2). The default setting is controlled by the signal CONTROL_LETTER_NUMBER which is pulled low. This selects the number signals on the right to be connected to the multiplexed signals on the left by default. In this example, the Microchip IO expander is not shown but controls the signal CONTROL_LETTER_NUMBER and allows the user to change the selection through software.

Figure 2-5 shows the equivalent circuit to Figure 2-4 but utilizes mechanical switches. Notice the default for reference designators SWC and SWD is illustrated by black boxes located closer to the ON label of the switches to enable the number signals by default. Also notice the default setting for reference designators SWE and SWF is OFF. In order to connect the letters instead of the numbers, the user physically changes all switches on SWC and SWD to the OFF position and all switches on SWE and SEF to the ON position.

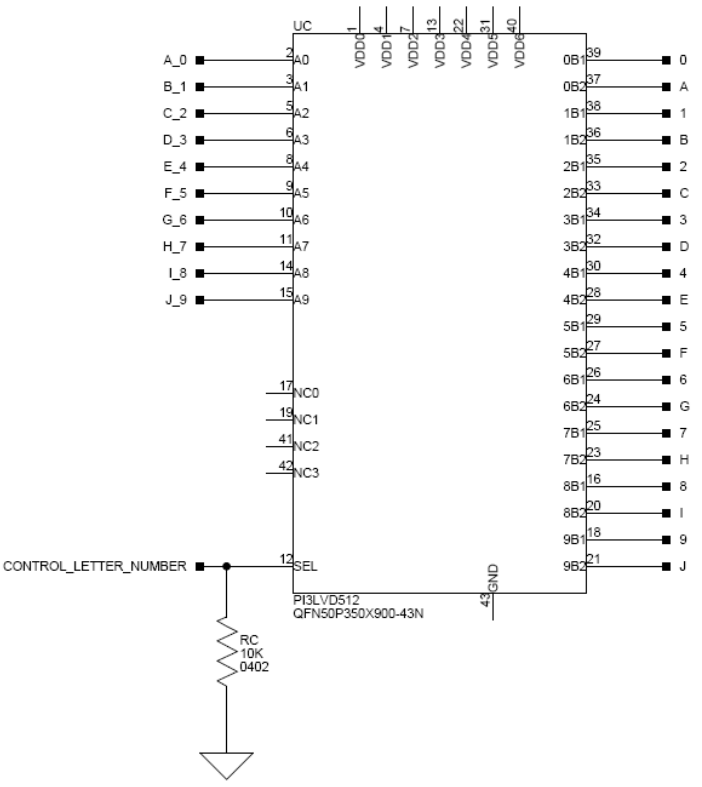


Figure 2-4. Example of Bus Switch

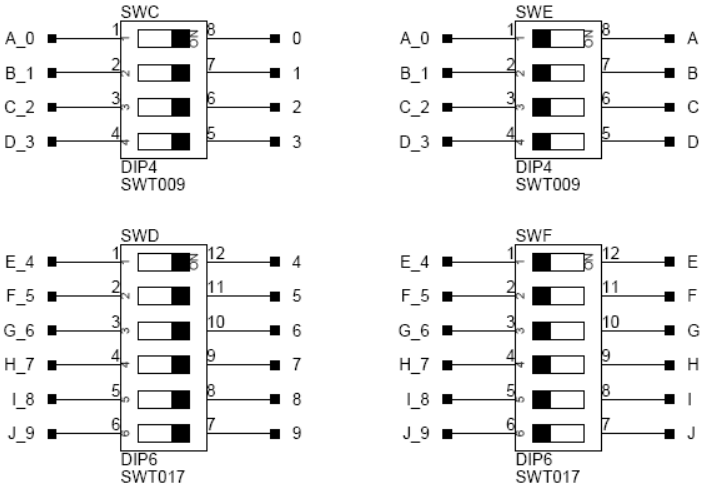


Figure 2-5. Example of Mechanical Switch Equivalent to Figure 2-4

SoftConfig on the ADSP-BF609 EZ-KIT LITE

The Microchip MCP23017 GPIO expander provides control for individual and 10-bit electronic switches. The TWI0 interface of the processor communicates with the Microchip device. Two 10-bit switches, `U40-41` are connected to the link port 1 and 0 interfaces, respectively. There are an additional 27 individual switches with default settings that enable basic board functionality.

Table 2-1 lists the ADSP-BF609 processor and EZ-KIT Lite interfaces that are available by default. Note that only interfaces affected by software switches are listed in Table 2-1.

Table 2-1. Default ADSP-BF609 Processor Interface Availability

Interface	Availability by Default
EMAC0	Fully connected, need SoftConfig to enable RMII clock
Rotary encoder	Enabled
Link port 0	Enabled with selection of the boot mode 6 setting, or by configuring SoftConfig
CAN	Enabled, the CAN0_ERR connection to the processor is disabled
UART	TX, RX and RTS are enabled by default, use SoftConfig to enable other features listed in the UART0 section and Table 2-5
SMC (parallel flash)	Enabled with selection of boot mode 1, can be changed with SoftConfig
SPI Flash	Fully connected for quad mode by default
Temperature sensor	Enabled, requires SoftConfig to connect interrupts
Push buttons	Enabled (except for wake push button)
LEDs	Enabled

Programming SoftConfig Switches

On the ADSP-BF609 EZ-KIT Lite, three Microchip MCP23017 devices exist. Each of these devices have the following programming characteristics:

- Each switch has two programmable GPIO registers.

GPIO Register	Register Address
GPIOA	0x12
GPIOB	0x13

- Each GPIO register controls eight signals (software switches).

- By default, the Microchip MCP23017 GPIO signals function as input signals.

  The signals must be programmed as output signals to override their default values. The following table shows the Microchip register addresses and the values that must be written to them to program the signals as output signals.

IODIR Register	IODIR Register Address	Value to be Written to Program Signals as Outputs
IODIRA	0x00	0
IODIRB	0x01	0

Each of the examples in Cross Core Embedded Studio include source files that program the soft switches, even if the default settings are being used. The `README` for each example identifies only the signals that are being changed from their default values. The code that programs the soft switches is located in the `SoftConfig_BF609.c` file in each example.

The following tables (Table 2-2, Table 2-3, and Table 2-4) outline the default values for each of the three Microchip MCP23017 devices.

Table 2-2. I^2C Hardware Address 0x21

GPIO	MCP23017 Register Address	Default Value
GPIOA	0x12	0x07
GPIOB	0x13	0xFC

Table 2-3. I^2C Hardware Address 0x22

GPIO	MCP23017 Register Address	Default Value
GPIOA	0x12	0x0A
GPIOB	0x13	0x00

Table 2-4. I^2C Hardware Address 0x23

GPIO	MCP23017 Register Address	Default Value
GPIOA	0x12	0x00
GPIOB	0x13	0x00

Page 12 of the ADSP-BF609 EZ-KIT Lite Schematic shows how the three Microchip GPIO expanders are connected to the board's ICs.

U41, a 10-bit bus switch, connects the link port 0 processor interface to J3 (link port connector) when the select input signal (pin 12) is high. By default, the U41 select input is controlled by the boot mode switch (SW2). When the boot mode switch is set to 1 (parallel flash boot), the select line is high, enabling the system memory controller (SMC) signals, connected through pins PA0-7 and PB0-1 of the processor. Setting the boot mode switch to 6 (link port boot) drives the select line low and enables the link port 0 connection to the J3 connector.

The U41 output selection, which is based on the boot mode selection, can be overridden by the Microchip (U46) signal GPA0. This override is useful in a case where the application needs to boot from parallel flash but then use the link port 0 afterwards. After setting the signal high (to disable U29), use GPA3 to control the output of U41.

The processor signals connected to U41 can be disconnected from the link port to support other features. The selection line must be low in order to disconnect the signals from the link port connector J3. This allows the signals to connect to the on-board parallel flash memory and EI3 connectors. See ADSP-BF609 EZ-KIT Lite Schematic for details.

U40, a 10-bit bus switch, controls the link port 1 connection to P8 (link port connector), EI3 (expansion interface), and SMC address signals. The default setting is high, which connects the SMC address bus to the parallel flash memory and connects the link port pins PA8-15 and PB2-3 to the expansion interface. The link port 1 can be selected by setting U46 signal GPA1 low.

Table 2-5 and Table 2-6 show the output signals of the Microchip GPIO expander (U45), with a TWI address of 0100 001X, where X represents the read or write bit. The signals that control an individual FET have an entry under the **FET** column. The **Component Connected** column shows the board IC that is connected if the FET is enabled. Note that some of the Microchip (U45) output signals are connected directly to components on the board. However, in most cases, the Microchip (U45) is controlling the enable signal of a FET switch. Also note that if a particular functionality of the processor signal is being used, it will be in **bold font** under the **Processor Signal** column.

Table 2-5. Output Signals of Microchip GPIO Expander (U45 Port A)

Bit	Signal Name	Description	FET	Processor Signal (if applicable)	Component Connected	Default
0	CAN_EN	Enable CAN IC, enabled by default			U55	High
1	$\overline{\text{CAN\_STB}}$	CAN standby control input			U55	High
2	$\overline{\text{CAN0\_ERR\_EN}}$	GPIO PE02 for CAN0 error	U33	**PE02**/SPI1_RDY/PPI0_D22/SPT1_ACLK	U55	High
3	$\overline{\text{CAN0RX\_EN}}$	CAN0RX connected to CAN IC U55	U34	PG04/SPT2_ACLK/TM0_TMR1/**CAN0_RX**/TM0_ACI2	U55	Low
4	$\overline{\text{CNTOUD\_EN}}$	Rotary counter 0 count up connected to rotary connector	U30	PG11/SPT2_BD1/TM0_TMR6/**CNT0_UD**	SW9	Low

Table 2-5. Output Signals of Microchip GPIO Expander (U45 Port A) (Cont'd)

Bit	Signal Name	Description	FET	Processor Signal (if applicable)	Component Connected	Default
5	CNT0DG_EN	Rotary counter 0 count down connected to rotary connector	U31	PG12/SPT2_BD0/TM0_TMR7/CNT0_DG	SW9	Low
6	CNT0ZM_EN	Rotary counter 0 count zero connected to rotary connector	U32	PG07/SPT2_BFS/TM0_TMR5/CNT0_ZM	SW9	Low
7	RMII_CLK_EN	RMII clock for EMAC0 disabled			U43	Low

Table 2-6. Output Signals of Microchip GPIO Expander (U45 Port B)

Bit	Signal Name	Description	FET	Processor Signal (if applicable)	Component Connected	Default
0	UART0RTS_EN	UART0 RTS connected to UART transceiver U39	U21	PD09/SPI0_SEL5/UART0_RTS/SPI1_SEL4	U39	Low
1	UART0RX_EN	UART0 RX connected to UART transceiver U39	U20	PD08/UART0_RX/TM0_ACI0	U39	Low
2	UART0CTS_EN	UART0 CTS disconnected from UART transceiver U39 by default	U19	PD10/SPI0_RDY/UART0_CTS/SPI1_SEL3	U39	High
3	UART0CTS_RTS_LPBK	UART0 CTS and RTS not connected. Change to low for looping back UART0 CTS and RTS signals	U18			High
4	UART0CTS_RST_EN	UART0 CTS signal not connected to input of reset IC (U48)	U17			High

Table 2-6. Output Signals of Microchip GPIO Expander (U45 Port B) (Cont'd)

Bit	Signal Name	Description	FET	Processor Signal (if applicable)	Component Connected	Default
5	UARTOCTS_146_EN	Allows pins 1, 4 and 6 of UART connector (J2) to be connected together and used as input to reset IC (U48). This is disabled by default.	U16			High
6	TEMP_IRQ_EN	PG09 can be used as TEMP interrupt, disconnected by default	U9	**PG09**/SPT2_ ADO/TMO_TMR4	U54	High
7	TEMP_THERM_EN	PB15 can be used as TEMP thermal limit, disconnected by default	U10	**PB15**/ETHO_ PTPPPS/PPI1_FS3	U54	High

Table 2-7 and Table 2-8 show the output signals of the Microchip GPIO expander (U46), with a TWI address of 0100 010X, where X represents the read or write bit. The signals that control an individual FET have an entry under the **FET** column. The **Component Connected** column shows the board IC that is connected if the FET is enabled. Note that some of the Microchip (U46) output signals are connected directly to components on the board. However, in most cases, the Microchip (U46) is controlling the enable signal of a FET switch. Also note that if a particular functionality of the processor signal is being used, it will be in **bold font** under the **Processor Signal** column.

Table 2-7. Output Signals of Microchip GPIO Expander (U46 Port A)

Bit	Signal Name	Description	FET	Processor Signal (if applicable)	Component Connected	Default
0	OVERRIDE_SMC0_LP0_BOOT	Overrides U41 select	U29			Low
1	SMC0_EPPI2_LP1_SWITCH	Controls U40 select line	U28			High
3	SMC0_LP0_EN	Controls U41 select if Override High	U28			High
4	$\overline{\text{LED1\_GPIO\_EN}}$	PG14 is used as GPIO output for LED1, enabled by default	U27	PG14/$\overline{\text{UART1\_RX}}$/SYS_$\overline{\text{IDLE1}}$/TM0_ACI1	LED1	Low
5	$\overline{\text{LED2\_GPIO\_EN}}$	PG15 is used as GPIO output for LED2, enabled by default	U26	PG15/$\overline{\text{UART1\_TX}}$/SYS_$\overline{\text{IDLE0}}$/SYS_SLEEP/TM0_ACI4	LED2	Low
6	$\overline{\text{LED3\_GPIO\_EN}}$	PE14 is used as GPIO output for LED3, enabled by default	U25	PE14/ETH1_RXERR/SPT2_ATDV/TM0_TMR0	LED3	Low
7	$\overline{\text{LED4\_GPIO\_EN}}$	PB11 is used as GPIO output for LED4, enabled by default	U24	PB11/SMC0_A25/SPT0_BD0/TM0_ACLK3	LED4	Low

Table 2-8. Output Signals of Microchip GPIO Expander (U46 Port B)

Bit	Signal Name	Description	FET	Processor Signal (if applicable)	Component Connected	Default
0	PUSHBUTTON1_EN	PB10 is used as GPIO input for push button 1, enabled by default	U23	PB10/SMC0_A24/SPT0_BD1/TM0_ACLK0	SW6	Low
1	PUSHBUTTON2_EN	PE01 is used as GPIO input for push button 2, enabled by default	U22	PE01/SPI1_D2/PPI0_D19/SPT1_BD0	SW7	Low
2	SD_CD_EN	SD memory card detect connected to GPIO PG10, enabled by default	U15	PG10/UART1_RTS/SPT2_BCLK	J5	Low
3	SD_WP_EN	SD memory write protect connected to GPIO PG10, enabled by default	U14	PG13/UART1_CTS/TM0_CLK	J5	Low
4	SPIFLASH_CS_EN	SPI flash chip select SPI0SEL1 connection to U38 SPI flash, connected by default	U13	PD11/SPI0_SEL1/SPI0_SS	U38	Low
5	SPI0D2_EN	SPI flash data 2 connection to U38 SPI flash, connected by default. This is needed for quad access mode.	U12	PD00/SPI0_D2/PPI1_D16/SPI0_SEL3	U38	Low
6	SPI0D3_EN	SPI flash data 3 connection to U38 SPI flash, connected by default. This is needed for quad access mode.	U16	PD01/SPI0_D3/PPI1_D17/SPI0_SEL2	U38	Low

Table 2-9 and Table 2-10 show the output signals of the Microchip GPIO expander (U47), with a TWI address of 0100 011X, where X represents the read or write bit. The signals that control an individual FET have an entry under the **FET** column. The **Component Connected** column shows the board IC that is connected if the FET is enabled.Note that some of the Microchip (U47) output signals are connected directly to components on the board. However, in most cases, the Microchip (U47) is controlling the enable signal of a FET switch. Also note that if a particular functionality of the processor signal is being used, it will be in **bold font** under the **Processor Signal** column.

Table 2-9. Output Signals of Microchip GPIO Expander (U47 Port A)

Bit	Signal Name	Description	FET	Processor Signal (if applicable)	Component Connected	Default
0	PHYINT_EN[1]	Connects Ethernet 0 interrupt signal to Ethernet PHY, connected by default	U35	PD06/ETH0_PHYINT/PPI1_FS2/TM0_ACI5	U49	Low
1	PHY_PWR_DWN_INT[2]	Controls power down of the Ethernet PHY if PHYINT_EN high			U49	High-Z
2	PHYAD0[3]	Allows the PHY to be placed in isolate mode			U49	High-Z
3	ETHERNET_EN	Disconnects EMAC0 signals from U49			U4/U5	Low
4	WAKE_PUSHBUTTON_EN	Enables push button input to processor	U7	PE12/ETH1_PHYINT/PWM1_CL/RSI0_D5	U1	High
5	PD0_SPI0D2_EPPI1D16_SPI0SEL3_EI3_EN	Connects processor signal to EI3 connectors, disabled by default	U36	PD00/SPI0_D2/PPI1_D16/SPI0_SEL3	EI3	High

Table 2-9. Output Signals of Microchip GPIO Expander (U47 Port A) (Cont'd)

Bit	Signal Name	Description	FET	Processor Signal (if applicable)	Component Connected	Default
6	PD1_SPIOD3_EPPI1D17_SPIOSEL2_EI3_EN	Connects processor signal to EI3 connectors, disabled by default	U51	PD01/SPIO_D3/PPI1_D17/SPIO_SEL2	EI3	High
7	PD2_SPIOMISO_EI3_EN	Connects processor signal to EI3 connectors, disabled by default	U57	PD02/SPIO_MISO	EI3	High

1 This is an active low signal but the signal name does not show this.
2 This signal defaults to an input setting, putting the signal in High-Z. Must be used in concert with PHYINT_EN. Set PHYINT_EN high first and then control PHY_PWR_DWN_INT.
3 This signal defaults to an input setting, putting the signal in High-Z. There is a 2.21k resistor pull-up, which sets the PHY address appropriately. If isolate mode is desired, the signal needs to be set as an output and driven appropriately.

Table 2-10. Output Signals of Microchip GPIO Expander (U47 Port B)

Bit	Signal Name	Description	FET	Processor Signal (if applicable)	Component Connected	Default
0	PD3_SPIOMOSI_EI3_EN	Connects processor signal to EI3 connectors, disabled by default	U56	PD03/SPIO_MOSI	EI3	High
1	PD4_SPIOCK_EI3_EN	Connects processor signal to EI3 connectors, disabled by default	U58	PD04/SPIO_CLK	EI3	High

Push Buttons and Switches

This section describes operation of the push buttons and switches. The push button and switch locations are shown in Figure 2-6.

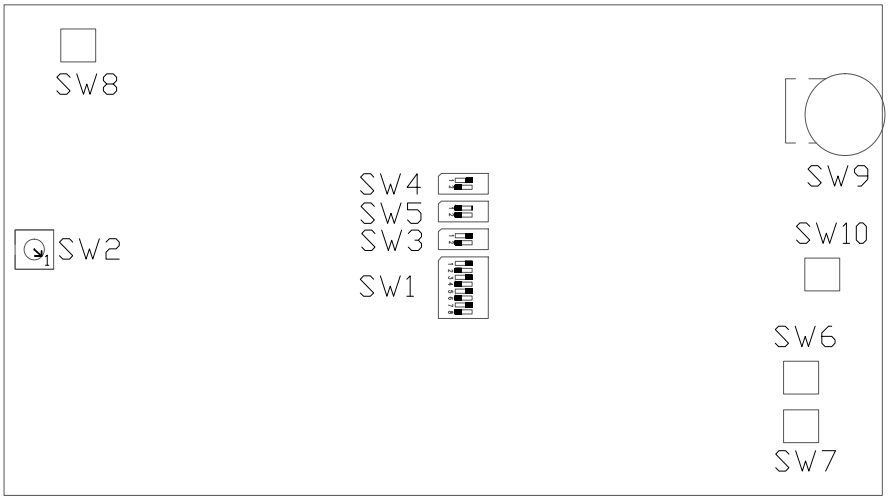


Figure 2-6. Push Button and Switch Locations

JTAG Interface Switches (SW1, SW3–5)

The JTAG switches (SW1, SW3, SW4, and SW5) select between a single-processor (one board) and multi-processor (more than one board) configurations. By default, the four DIP switches are set up for a single EZ-KIT Lite configuration. See Table 2-11.

The default configuration applies to either a debug agent or an external emulator, such as the Analog Devices high-performance USB-based emulator (HP-USB) or ICE-100B emulator.

To use an external emulator and multiple EZ-KIT Lites simultaneously in one CrossCore Embedded Studio (CCES) multi-processor session, set up

the boards as shown in Table 2-12. Attach the boards to each other via connectors J3 and P8. For two EZ-KIT Lites, no external cables are required. For three or more EZ-KIT Lites, obtain Samtec JTAG cables described in Link Port /JTAG Connectors (J3 and P8).

Table 2-11. Single-Processor Configuration

Switch Position	Single EZ-KIT Lite Use (Default)
SW1.1	ON
SW1.2	OFF
SW1.3	ON
SW1.4	OFF
SW1.5	ON
SW1.6	OFF
SW1.7	ON
SW1.8	OFF
SW3.1	ON
SW3.2	OFF
SW4.1	ON
SW4.2	OFF
SW5.1	OFF
SW5.2	OFF

Table 2-12. Multiple-Processor Configuration

Switch Position	Main EZ-KIT Lite Attached to Emulator	EZ-KIT Lite Not Attached to Emulator
SW1.1	ON	OFF
SW1.2	ON	ON
SW1.3	ON	OFF
SW1.4	ON	ON

Table 2-12. Multiple-Processor Configuration (Cont'd)

Switch Position	Main EZ-KIT Lite Attached to Emulator	EZ-KIT Lite Not Attached to Emulator
SW1.5	ON	OFF
SW1.6	ON	ON
SW1.7	ON	OFF
SW1.8	ON	ON
SW3.1	ON	OFF
SW3.2	OFF	OFF
SW4.1	OFF	OFF
SW4.2	ON	ON
SW5.1	OFF	ON
SW5.2	ON	OFF

Boot Mode Select Switch (SW2)

The rotary boot mode select switch (SW2) determines the boot mode of the processor. Table 2-13 shows the available boot mode settings. By default, the ADSP-BF609 processor boots from 8-bit flash memory (parallel flash boot).

Table 2-13. Boot Mode Select Switch (SW2)

SW2 Position	Processor Boot Mode
0	Idle—no boot
1	**Parallel flash boot (default)**
2	RSI master boot
3	SPI0 master boot
4	SPI0 slave boot
5	Reserved

Table 2-13. Boot Mode Select Switch (SW2) (Cont'd)

SW2 Position	Processor Boot Mode
6	Link port 0 slave boot
7	UART0 slave boot

IRQ/Flag Enable Switches (SW6–7)

The IRQ/flag enable switches (SW6-7) are push buttons which provide a momentary low signal on processor signals PB10_A24_SP1D1 and PE1_SPI1D2_EPPI0D19_SP3D0 when enabled through the software-controlled switch.

Reset Switch (SW8)

The reset switch (SW8) is a push button which provides a reset pulse to the ADSP-BF609 processor (U1), Ethernet PHY (U49), GPIO extenders (U45-47), and the expansion interface (EI3) connectors.

Rotary Encoder With Momentary Switch (SW9)

The rotary encoder (SW9) can be turned clockwise for an up count or counter-clockwise for a down count. The encoder also features a momentary switch, activated by pushing the switch towards the center of the board, that can be used to set the counter to zero. The rotary encoder is a two-bit quadrature (Gray code) encoder.

The rotary encoder can be disconnected from the processor by setting SoftConfig, see Software-Controlled Switches (SoftConfig) for more information.

Wake Push Switch (SW10)

One of the wake input signals (PE12/~ETH1_PHYINT/PWM1_CL/RSIO_D5) is connected to a push button switch (SW10). This feature is disabled by default and can be enabled through SoftConfig. Refer to Software-Controlled Switches (SoftConfig) for more details.

Power Jumpers

This section describes functionality of the power jumpers (P10-15). Figure 2-7 shows the jumper locations.

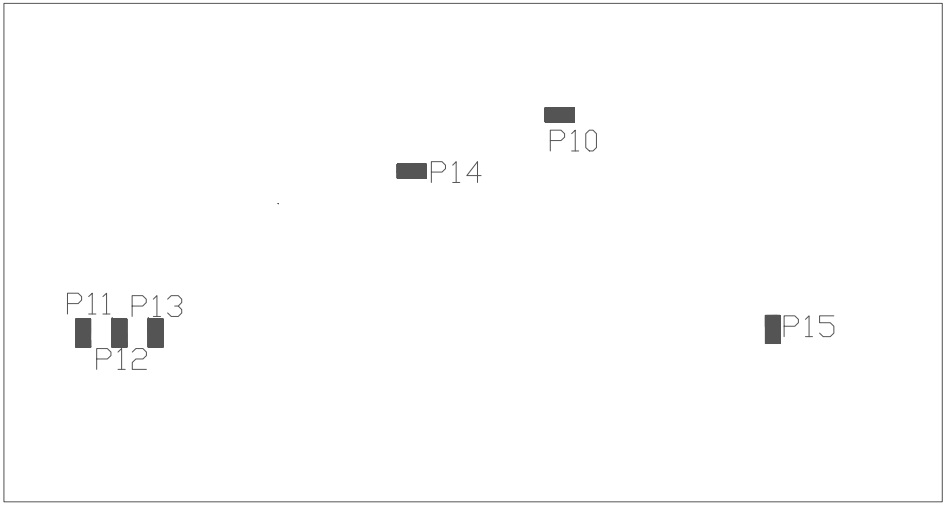


Figure 2-7. Configuration Jumper Locations

Remove jumpers listed in Table 2-14 to measure the respective voltage domain.

Table 2-14. Power Jumpers (P10-15)

Jumper	Power Domain
P15	VDD_DMC
P14	VDD_INT
P13	3.3V
P12	VDD_EXT
P11	VDD_USB
P10	USB_VBUS

LEDs

This section describes the on-board LEDs. Figure 2-8 shows the LED locations.

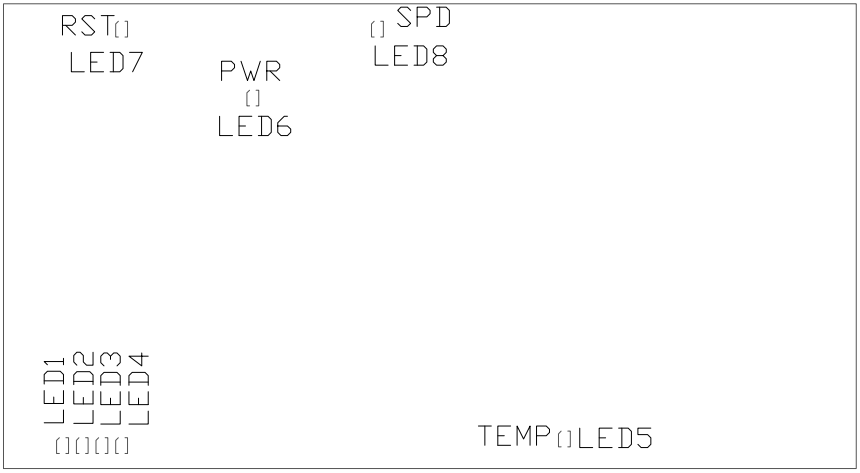


Figure 2-8. LED Locations

GPIO LEDs (LED1–4)

Four LEDs (LED1, LED2, LED3, and LED4) are connected to four general-purpose I/O pins of the processor (see Table 2-15). The LEDs are active high and lit (amber) by writing a "1" to the corresponding programmable flag signal.

Table 2-15. GPIO LEDs

LED Reference Designator	Processor Programmable Flag Pin
LED1	PG14
LED2	PG15
LED3	PE14
LED4	PB11

Thermal Limit LED (LED5)

The thermal limit LED (LED5) reports the status of the thermal sensor, ADM1032 (U54). The thermal sensor monitors the processor's temperature. When the high temperature limit set by the IC is violated, LED5 is turned on (amber) as a visual indicator. The ADM1032 device has built-in hysteresis, which causes the LED to deactivate only when the temperature is significantly within the limit. For more information, see Temperature Sensor Interface.

Power LED (LED6)

When LED6 is lit solid (green), it indicates that power is being supplied to the board properly.

Reset LED (LED7)

When LED4 is lit (red), it indicates that the master reset of the processor is active. The reset signal is controlled by the Analog Devices ADM13305 supervisory reset circuit.

SPD LED (LED6)

SPD LED indicates the speed of the Ethernet port. When LED6 is lit (green), the speed is 100 Mb/s and when not lit, the speed is 10 Mb/s.

Connectors

This section describes connector functionality and provides information about mating connectors. The connector locations are shown in Figure 2-9. Components with dotted outlines are on the board's back side.

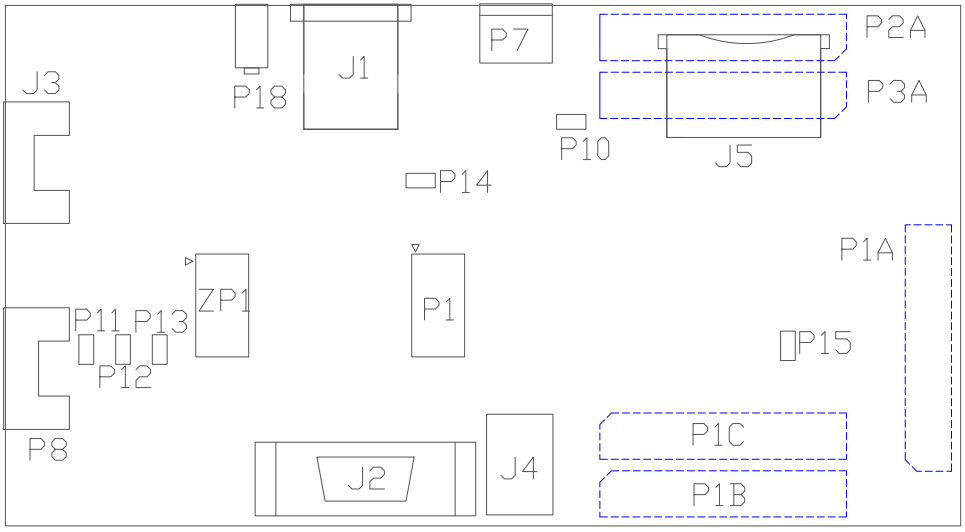


Figure 2-9. Connector Locations

DCE UART Connector (J2)

The pinout of the J2 connector can be found in ADSP-BF609 EZ-KIT Lite Schematic.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-410HLF
Mating Connector		
IDC socket	DIGI-KEY	S4205-ND

Link Port /JTAG Connectors (J3 and P8)

The J3 and P8 connectors provide access to the Link Port and JTAG signals of the ADSP-BF609 processor. J3 supports link port 0 and the P8 connector is for link port 1.

Part Description	Manufacturer	Part Number
ERF8 10X2, RA female (J3)	SAMTEC	ERF8-010-01-S-D-RA-L
ERm8 10x2, RA male (P8)	SAMTEC	ERM8-010-01-S-D-RA-TR
Mating Cable		
6" cable ERF8 to ERM8 10X2	SAMTEC	ERCD-010-06.00-TBL-SBR-1

JTAG Connector (P1)

The JTAG interface of the ADSP-BF609 processor is connected to the 14-pin 0.1" header, P1. Pin 3 is missing to provide keying. Pin 3 in the mating connector must have a plug. For more information, see JTAG Interface.

Remove the standalone debug agent when an emulator is used with the board. Follow the installation instructions provided in EZ-KIT Lite Installation, using P1 as the JTAG connection point.

JTAG Connector (ZP1)

ZP1 is the connecting point for the SADA2 debug interface and is a 14-pin 0.1" header.

Expansion Interface III Connectors (P1A–C, P2A, P3A)

Five board-to-board connectors (P1A, P1B, P1C, P2A, and P3A) provide signals from the SPI, TWI, UART, SPORT, and GPIO interfaces of the processor. The connectors are located on the bottom side of the board. For more information, see Expansion Interface III.

Part Description	Manufacturer	Part Number
120-pin, 0.6 mm	HIROSE	FX8-120P-SV1(91)
Mating Connector		
120-pin, 0.6 mm	HIROSE	FX8-120S-SV(21)

USB Connector (P7)

Part Description	Manufacturer	Part Number
USB mini-Ab	MOLEX	56579-0576

Power Connector (P18)

Part Description	Manufacturer	Part Number
0.65 mm power jack	CUI	045-0883R
Mating Connector		
5.0VDC@3.6A power supply	GLOBETEK	GS-1750(R)

CAN Connector (J4)

Part Description	Manufacturer	Part Number
RJ-11 4-pin modular jack	TYCO	5558872-1
Mating Cable		
4-conductor modular jack cable	L-COM	TSP3044

SD Connector (J5)

Part Description	Manufacturer	Part Number
SD 8-bit, 2 GB	SANDISK	MHC-W21-601
Memory Card		
2 GB	SANDISK	SDSDB-2048-A11

Ethernet Connector (J1)

Part Description	Manufacturer	Part Number
RJ-45 Ethernet jack	Pulse Engineer	PN J0011D21BNL
Mating Cable		
Standard Ethernet cable		

Ethernet Connectors (P16-17)

`P16` and `P17` allow connection to the Ethernet port IEEE 1588 signals. They are 6-pin 0.1” headers. The pinout of the `P16` and `P17` connectors can be found in ADSP-BF609 EZ-KIT Lite Schematic.

A ADSP-BF609 EZ-KIT LITE BILL OF MATERIALS

The bill of materials corresponds to ADSP-BF609 EZ-KIT Lite Schematic.

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
1	1	ADM708SARZ SOIC8	U48	ANALOG DEVICES	ADM708SARZ
2	1	ADM3315 TSSOP24	U39	ANALOG DEVICES	ADM3315EARUZ
3	1	ADSP-BF609 BGA349C80P22X22_1900X1900	U1	ANALOG DEVICES	ADSP-BF609-ENG
4	1	ADP1864AUJZ SOT23-6	VR1	ANALOG DEVICES	ADP1864AUJZ-R7
5	1	ADP1715 MSOP8	VR3	ANALOG DEVICES	ADP1715ARMZ-1.8-R7
6	1	74LVC14A SOIC14	U3	TI	74LVC14AD
7	1	IDT74FCT3244APY SSOP20	U8	IDT	IDT74FCT3244APYG
8	2	SN74LVC1G08 SOT23-5	U52-U53	TI	SN74LVC1G08DBVR
9	1	TJA1041 SOIC14	U55	NXP	TJA1041T/VM,512
10	1	SN74LVC1G04 SOT23-5	U59	TI	SN74LVC1G04DBVT
11	2	SN74CB3Q3245 TSSOP20	U4-U5	DIGI-KEY	296-19130-1-ND

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
12	1	MIC2025-1 SOIC8	U50	DIGI-KEY	576-1057-ND
13	1	MT47H64M16 FBGA84	U37	MICRON	MT47H64M16HR-3 L
14	1	ADM1032 SOIC_N8	U54	ON SEMI	ADM1032ARZ
15	1	DP83848 LQFP48	U49	NATIONAL SEMI	DP83848CVV/NOPB
16	1	50MHZ OSC012	U43	DIGI-KEY	300-8264-2-ND
17	33	PI3A125 SC70_5	U7,U9-U36,U51, U56-U58	PERICOM	PI3A125CEX
18	3	MCP23017 QFN65P600X600-29N	U45-U47	DIGI-KEY	MCP23017-E/ML-ND
19	2	PI3LVD512 QFN50P350X900-43N	U40-U41	PERICOM	PI3LVD512ZHE
20	1	BF609 PC28F128P33B U44	U44	MICRON	PC28F128P33BF60D
21	1	BF609 W25Q32 U38	U38	WINBOND	W25Q32BVSSIG
22	1	SI7403BDN ICS010	U6	VISHAY	SI7403BDN
23	1	25MHZ OSC003	U42	DIGI-KEY	SG-8002CA-SCB-ND
24	1	48MHZ OSC003	U2	DIGI-KEY	SG-8002CA-SCB-ND(48.00M)
25	1	ADP2119ACPZ-R7 DFN50P300X300-11N	VR2	ANA00	ADP2119ACPZ-R7
26	1	DIP8 SWT016	SW1	C&K	TDA08H0SB1
27	2	IDC 3X2 IDC3X2_SMT	P16-P17	SAMTEC	TSM-103-01-T-DV

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
28	1	DB9 9PIN CON038	J2	NORCOMP	191-009-213-L-571
29	1	RJ11 4PIN CON039	J4	TYCO	5558872-1
30	3	DIP2 SWT020	SW3-SW5	C&K	CKN9064-ND
31	6	IDC 2X1 IDC2X1	P10-P15	FCI	90726-402HLF
32	1	3A RESETABLE FUS004	F1	TYCO	SMD300F-2
33	6	IDC 2PIN_-JUMPER_SHORT	SJ1-SJ6	DIGI-KEY	S9001-ND
34	1	PWR .65MM CON045	P18	DIG	CP1-023-ND
35	1	USB_MINI-AB 5PIN CON052	P7	MOLEX	56579-0576
36	4	MOMENTARY SWT024	SW6-SW8,SW10	PANASO-NIC	EVQ-Q2K03W
37	1	ROTA-RY_ENC_EDGE SWT025	SW9	PANASO-NIC	EVQ-WKA001
38	2	IDC 7x2 IDC7x2_SMTA	P1,ZP1	SAMTEC	TSM-107-01-T-DV-A
39	1	ROTARY SWT027	SW2	COPAL	S-8110
40	1	ERM8 10X2 ERM8_10X2_SMT	P8	SAMTEC	ERM8-010-01-S-D-RA-TR
41	1	ERF8 10X2 ERF8_10X2_SMT	J3	SAMTEC	ERF8-010-01-S-D-RA-L-TR
42	1	RJ45 W/LEDS CON065	J1	PULSE ENG.	J0011D21BNL
43	1	SD_CONN 8-BIT CON067	J5	MORETHA-NALL	MHC-W21-601-LF

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
44	5	.6MM 120PIN HIROSE_FX8-120P -SV1(91)	P1A,P1B,P1C,P2A, P3A	HIROSE	FX8-120P-SV1(91)
45	1	TEST LOOP LOOP_2838	GP1	KEYSTONE	5016
46	5	YELLOW LED001	LED1-LED5	DIGI-KEY	P512TR-ND
47	3	600 100MHZ 500MA 1206	FER1-FER3	STEWARD	HZ1206B601R-10
48	2	1UF 16V 10% 0805	C87-C88	DIGI-KEY	399-1284-2-ND
49	2	0 1/8W 5% 0805	R200,R211	VISHAY	CRCW08050000Z0EA
50	1	190 100MHZ 5A FER002	FER4	MURATA	DLW5BSN191SQ2
51	7	10UF 6.3V 10% 0805	C39,C117-C118, C163-C164, C177-C178	AVX	08056D106KAT2A
52	1	4.7UF 6.3V 10% 0805	C90	AVX	08056D475KAT2A
53	40	0.1UF 10V 10% 0402	C17-C18, C41-C45,C84, C95,C100, C115-C116, C135-C142, C153-C162, C173-C176,C186, C188-C191,C200	AVX	0402ZD104KAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
54	124	0.01UF 16V 10% 0402	C1-C15,C19, C22-C24, C26-C38,C40, C46-C61, C64-C83,C94, C96-C98, C104-C107, C111-C113, C119-C134, C143-C152, C165-C172, C179-C185,C192, C198-C199	AVX	0402YC103KAT2A
55	102	10K 1/16W 5% 0402	R9-R12,R17-R18, R20-R33,R39-R48, R50-R52,R56-R63, R65-R67,R69-R72, R80-R84,R89-R96, R100-R101,R104-R105,R107-R111, R113,R118-R119, R133-R135,R142, R146,R148-R149, R158-R160,R167, R169-R170,R174, R188,R205-R206, R210,R218-R221, R230-R235,R239	VISHAY	CRCW040210K0FKED
56	1	4.7K 1/16W 5% 0402	R64	VISHAY	CRCW04024K70JNED
57	13	0 1/16W 5% 0402	R5-R6,R53,R120, R136,R161-R162, R165,R168,R228-R229,R238,R240	PANASO-NIC	ERJ-2GE0R00X

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
58	17	33 1/16W 5% 0402	R8,R13,R34,R37-R38,R54-R55,R85-R86,R137-R138, R140,R172-R173, R227,R244-R245	VISHAY	CRCW040233R0JNEA
59	1	1.5UH 20% IND003	L2	COIL CRAFT	DO1608C-152MLC
60	1	150UF 10V 10% D	CT1	DIGI-KEY	478-3321-2-ND
61	2	2.2UF 10V 10% 0805	C99,C101	AVX	0805ZD225KAT2A
62	1	1A SK12 DO-214AA	D8	DIODES INC	B120B-13-F
63	2	107.0 1/10W 1% 0805	R190,R192	DIGI-KEY	311-107CRTR-ND
64	1	4.7UF 25V 20% 0805	C25	AVX	0805ZD475KAT2A
65	1	68PF 50V 5% 0603	C91	AVX	06035A680JAT2A
66	1	470PF 50V 5% 0603	C92	AVX	06033A471JAT2A
67	1	220UF 6.3V 20% D2E	CT3	SANYO	10TPE220ML
68	1	1M 1/10W 5% 0603	R19	VISHAY	CRCW06031M00FNEA
69	5	0.0 1/10W 1% 0603	R129,R214-R217	PHYCOMP	232270296001L
70	3	10 1/10W 5% 0603	R151-R152,R237	VISHAY	CRCW060310R0JNEA
71	1	4700PF 16V 10% 0603	C110	DIGI-KEY	311-1083-2-ND
72	2	100PF 50V 5% 0603	C108-C109	AVX	06035A101JAT2A
73	10	2.21K 1/10W 1% 0603	R186-R187,R191, R199,R201-R204, R207-R208	DIGI-KEY	311-2.21KHRTR-ND

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
74	2	62.0 1/10W 1% 0603	R153-R154	DIGI-KEY	311-62.0HRTR-ND
75	3	1UF 6.3V 20% 0402	C62-C63,C93	PANASO-NIC	ECJ-0EB0J105M
76	3	100 1/16W 5% 0402	R87-R88,R141	DIGI-KEY	311-100JRTR-ND
77	1	24.9K 1/10W 1% 0603	R132	DIGI-KEY	311-24.9KHTR-ND
78	3	10UF 10V 10% 0805	C16,C114,C187	PANASO-NIC	ECJ-2FB1A106K
79	6	0.05 1/2W 1% 1206	R121,R124-R126, R144-R145	SEI	CSF 1/2 0.05 1%R
80	2	10UF 16V 10% 1210	C86,C103	AVX	1210YD106KAT2A
81	2	GREEN LED001	LED6,LED8	PANASO-NIC	LN1361CTR
82	1	RED LED001	LED7	PANASO-NIC	LN1261CTR
83	2	1000PF 50V 5% 1206	C85,C89	AVX	12065A102JAT2A
84	1	255.0K 1/10W 1% 0603	R130	VISHAY	CRCW06032553FK
85	1	80.6K 1/10W 1% 0603	R131	VISHAY	CRCW060380K6FKEA
86	3	5A MBRS540T3G SMC	D5-D7	ON SEMI	MBRS540T3G
87	1	VARISTOR V5.5MLA 30A 0603	R1	LITTLE-FUSE	V5.5MLA0603
88	1	THERM 0.5A 0.4 1206	R209	LITTLE-FUSE	1206L050-C

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
89	1	2.5UH 30% IND013	L1	COIL-CRAFT	MSS1038-252NL_
90	7	330.0 1/16W 1% 0402	R73-R79	DIGI-KEY	541-330LCT-ND
91	5	1.0K 1/16W 1% 0402	R2-R3,R155-R157	PANASO-NIC	ERJ-2RKF1001X
92	3	1.50K 1/16W 1% 0402	R15-R16,R175	PANASO-NIC	ERJ-2RKF1501X
93	13	0 1/16W 5% RNS005	RN1-RN13	PANASO-NIC	EXB-28VR000X
94	3	22UF 16V 10% 1210	C201-C203	YAIYO YUDEN	EMK325BJ226KM-T
95	1	33 1/16W 5% RNS003	RN14	PANASO-NIC	EXB-2HV330JV
96	1	100.0 1/16W 1% 0402	R4	DIGI-KEY	541-100LCT-ND
97	2	0.036 1/2W 1% 1206	R127-R128	SUSUMU	RL1632S-R036-F
98	1	30A GSOT05 SOT23-3	D2	VISHAY	GSOT05-GS08
99	2	30A GSOT03 SOT23-3	D3-D4	VISHAY	GSOT03-GS08
100	1	40A ESD5Z2.5T1 SOD-523	D1	ON SEMI	ESD5Z2.5T1G
101	2	165.0 1/10W 1% 0603	R197-R198	DIGI-KEY	P165HTR-ND
102	1	220.0 1/10W 1% 0603	R185	DIGI-KEY	P220HTR-ND
103	1	4.87K 1/10W 1% 0402	R189	DIGI-KEY	541-4.87KHCT-ND

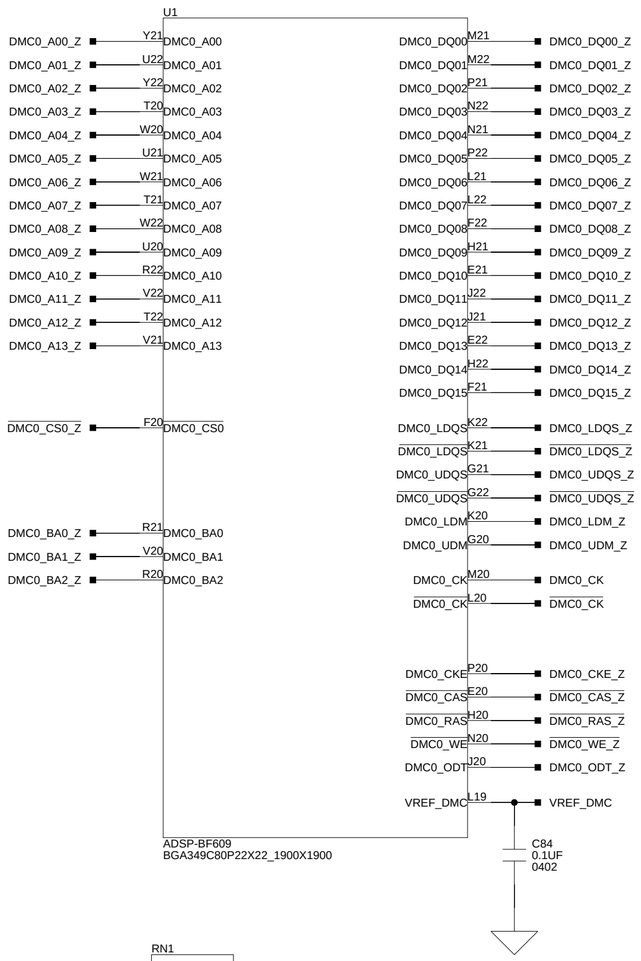
Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
104	13	49.9 1/16W 1% 0402	R176-R184,R193-R196	STACK-POLE	RMCF0402FT49R9
105	1	15KV ESD7004 DFN50P250X100-10N	D10	ON SEMI	ESD7004MUTAG
106	1	15KV ESDA6V1SC SOT95P280-6N	D9	DIGI-KEY	497-6637-1-ND
107	1	30K 1/10W 1% 0402	R242	PANASONIC	ERJ-2RKF3002X
108	1	32.4K 1/10W 1% 0402	R243	PANASONIC	ERJ-2RKF3242X

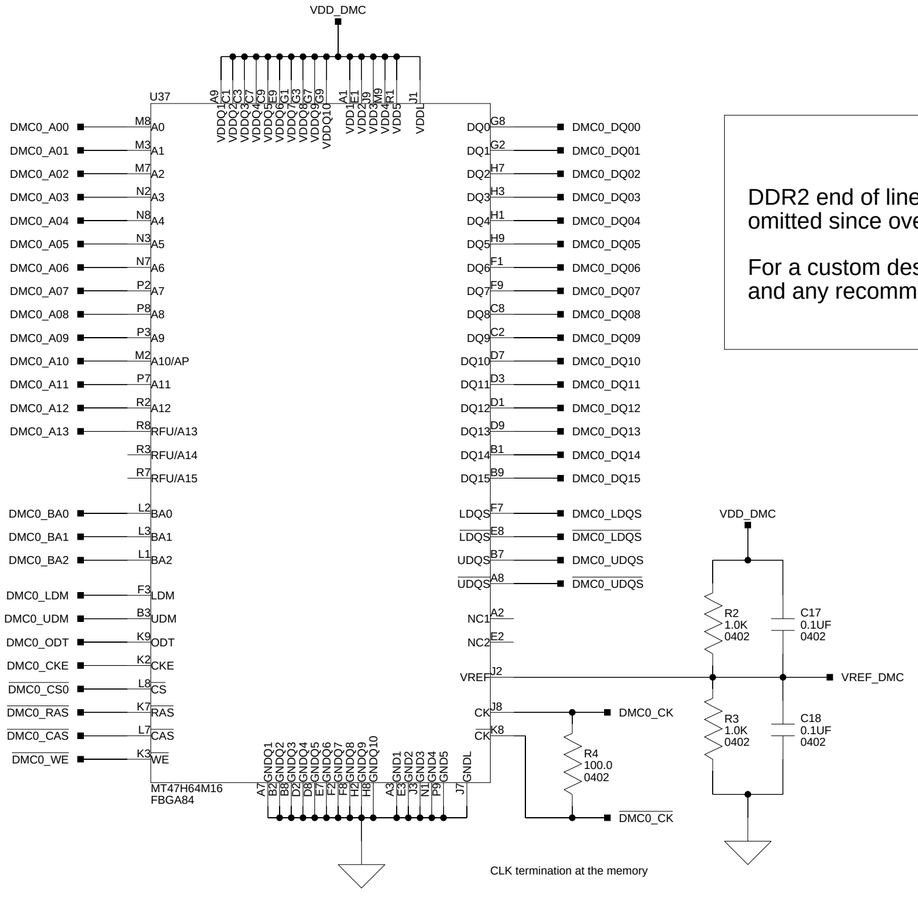
ADSP-BF609 EZ-Board

SCHEMATIC

ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

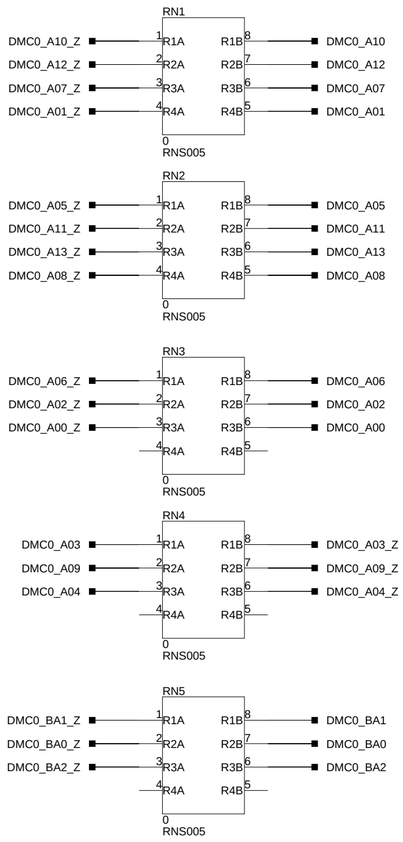
Title	ADSP-BF609 EZ-Board Title Block	
Size C	Board No. A0269-2011	Rev 1.0
Date 1/5/12	Sheet 1 of 16	

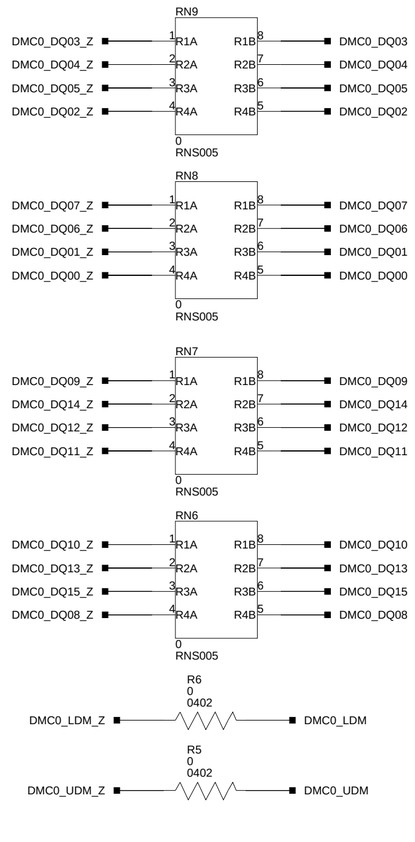


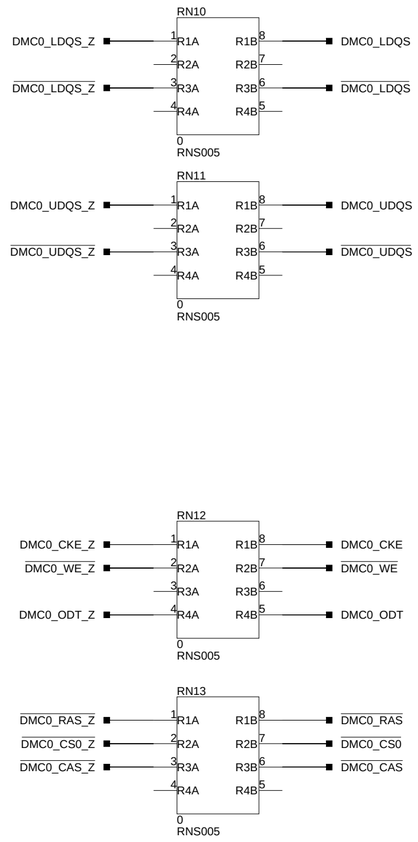


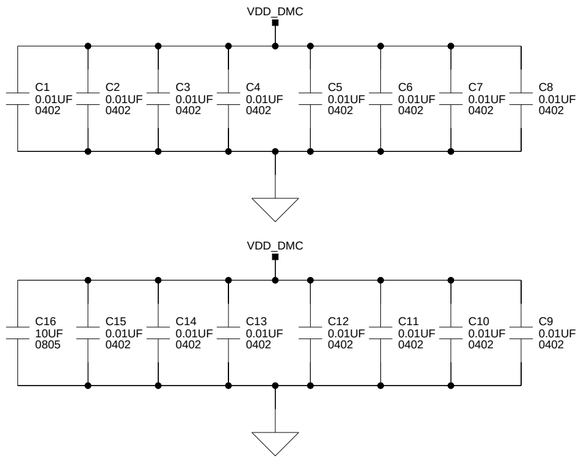
DDR2 end of line terminators and VTT tracking circuit have been omitted since overall trace length is less than 2.5" for each net.

For a custom design, please adhere to any EE-note from ADI and any recommendations by the memory manufacturer.

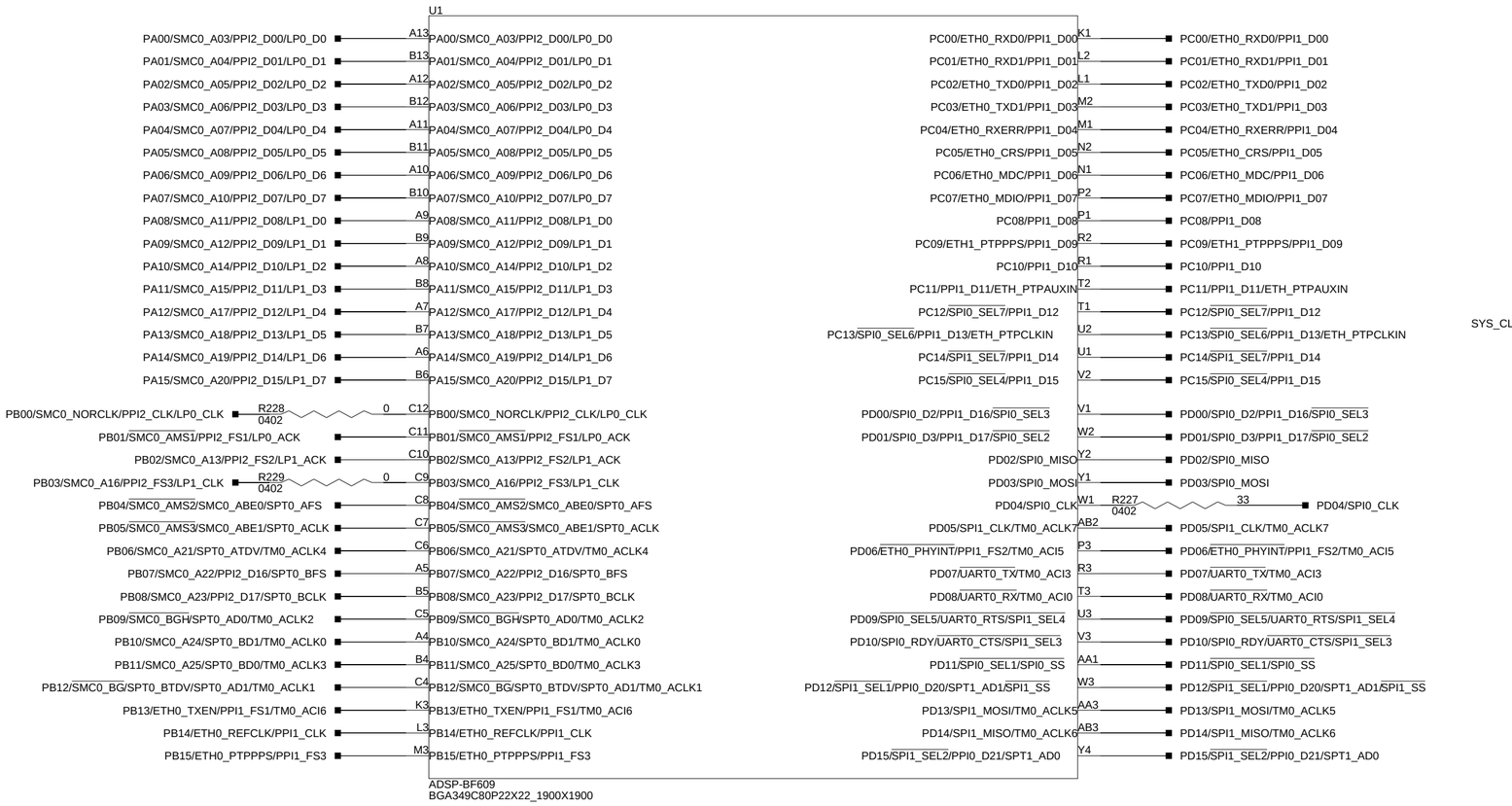


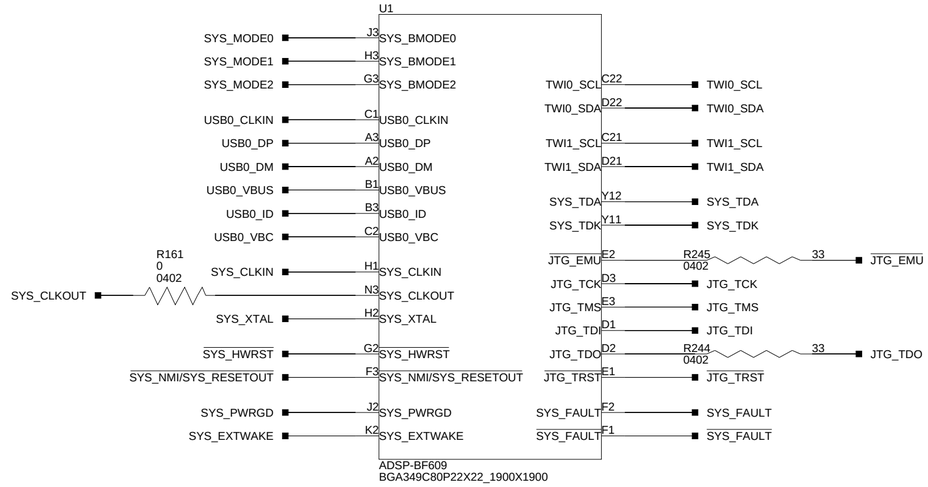


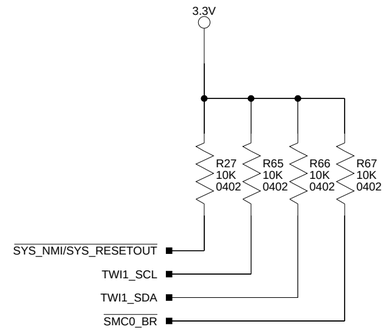


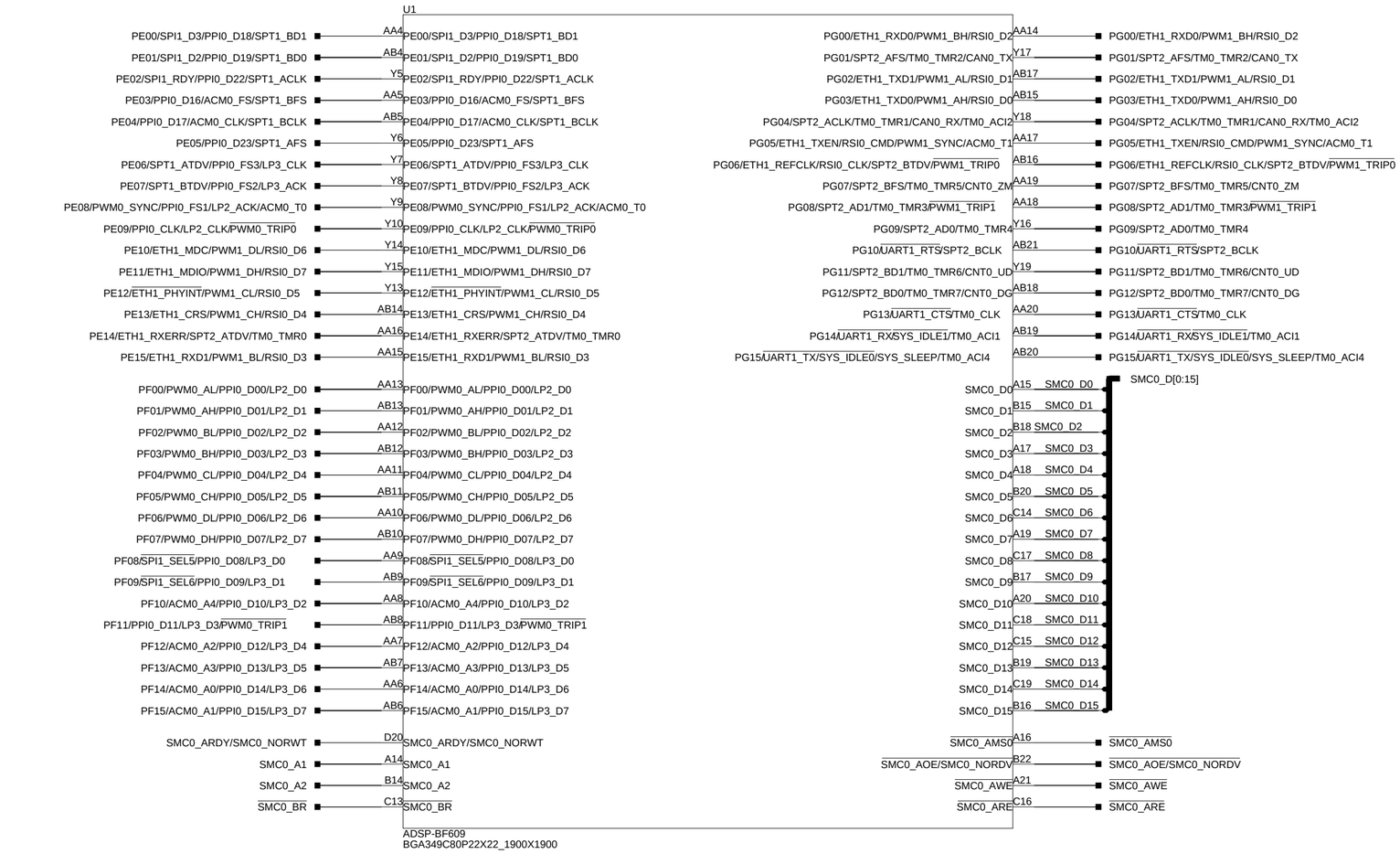


ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title	ADSP-BF609 EZ-Board DSP DDR2 Interface	
Size C	**Board No.** A0269-2011	**Rev** 1.0
Date 1/5/12	**Sheet** 2 **of** 16	

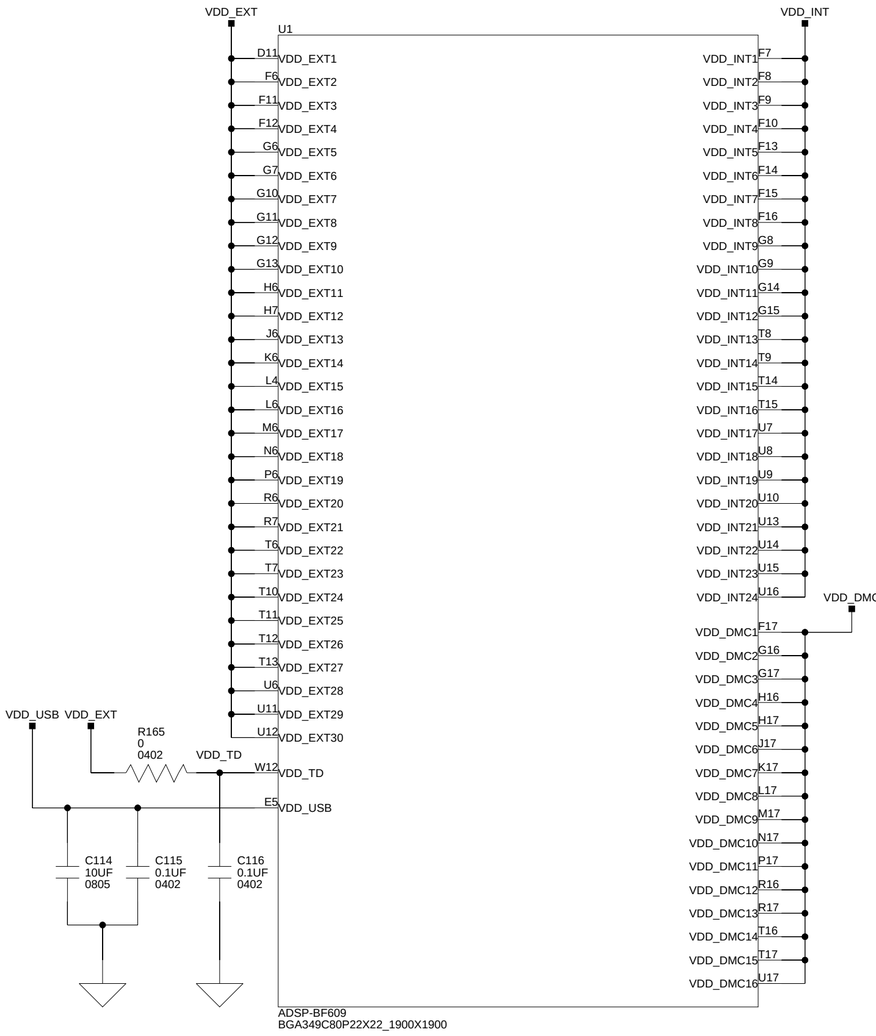


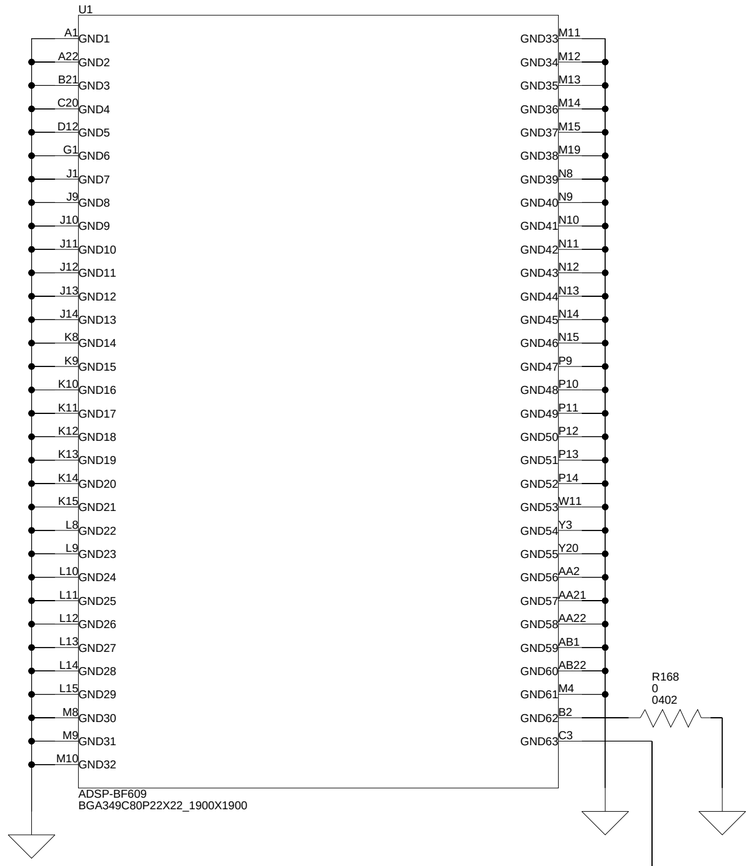


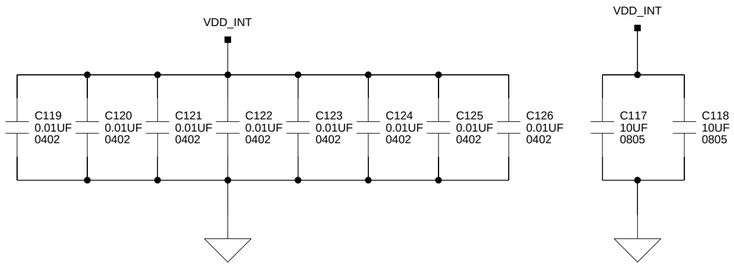


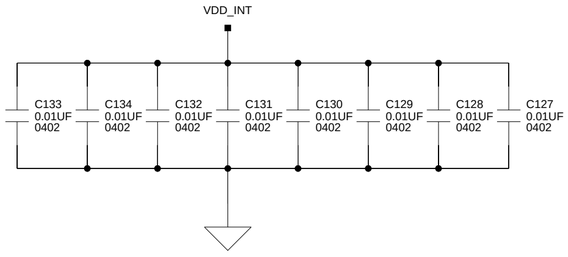


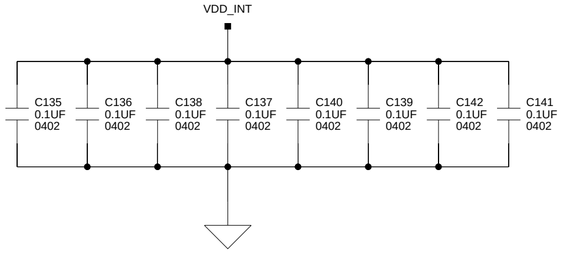
ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD		
Title	ADSP-BF609 EZ-Board DSP Signals		
Size C	**Board No.** A0269-2011		**Rev** 1.0
Date 1/5/12		**Sheet** 3 **of** 16	

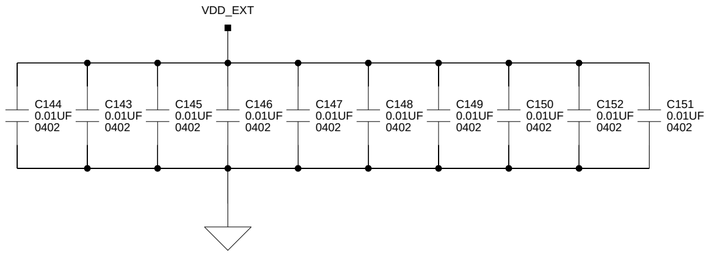


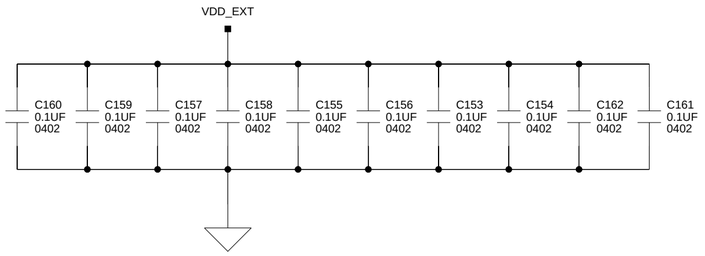


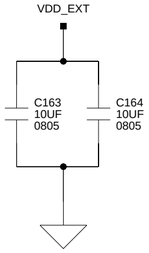


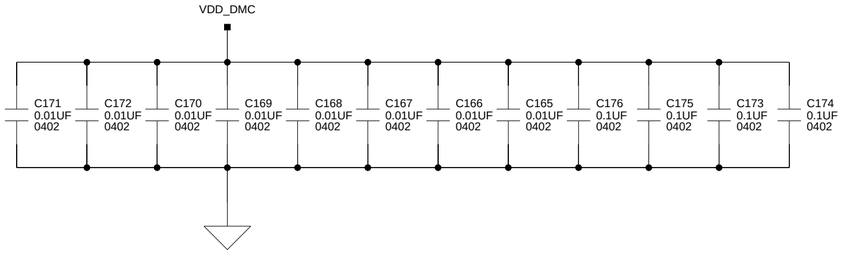


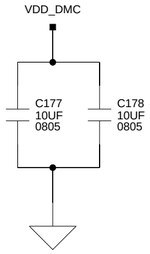






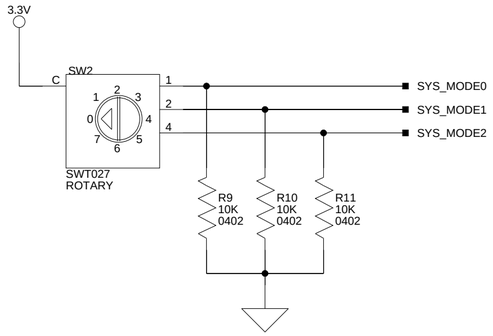






ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

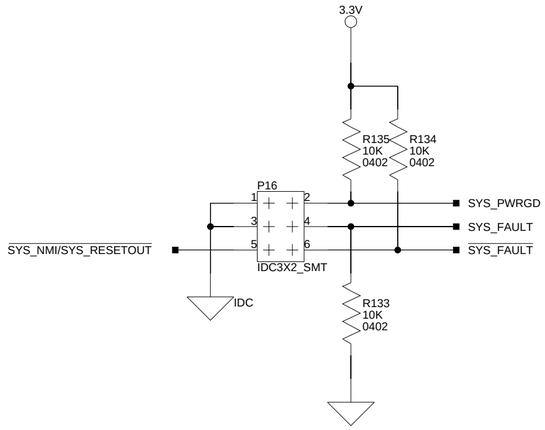
Title	ADSP-BF609 EZ-Board DSP Power and Ground	
Size C	**Board No.** A0269-2011	**Rev** 1.0
Date 1/5/12	**Sheet** 4 **of** 16	

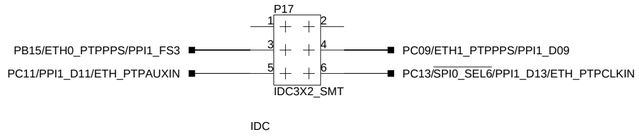


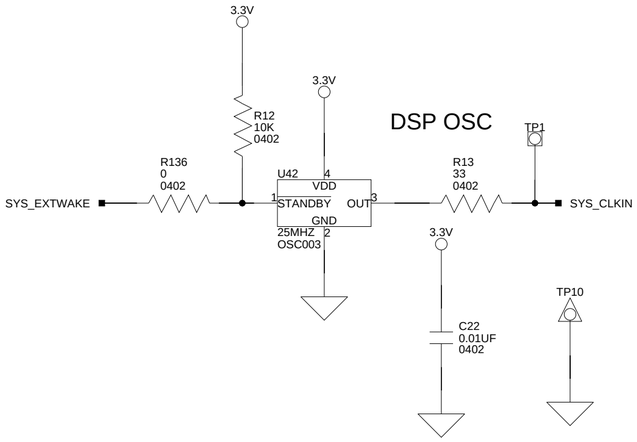
SW1: Boot mode selection switch

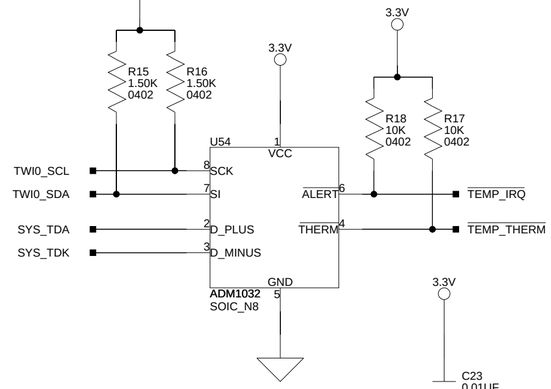
BMODE[2:0]	
000	No-boot/Idle
001	Parrallel Flash boot
010	RSI master boot
011	SPI0 master boot
100	SPI0 slave boot
101	reserved
110	LP0 slave boot
111	UART0 slave boot

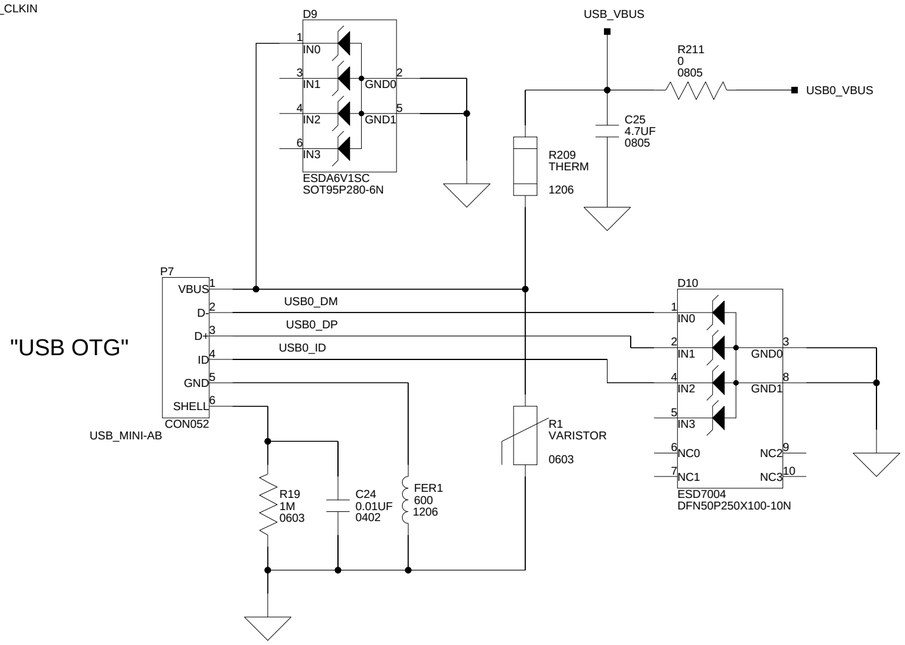
DEFAULT



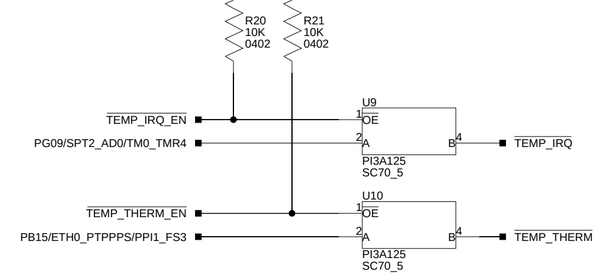




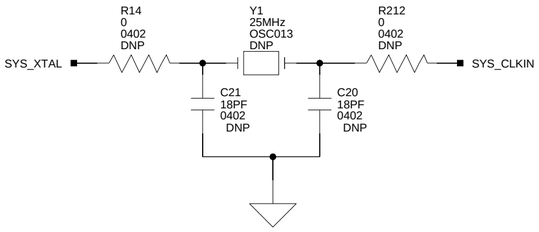


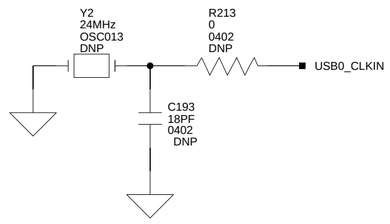


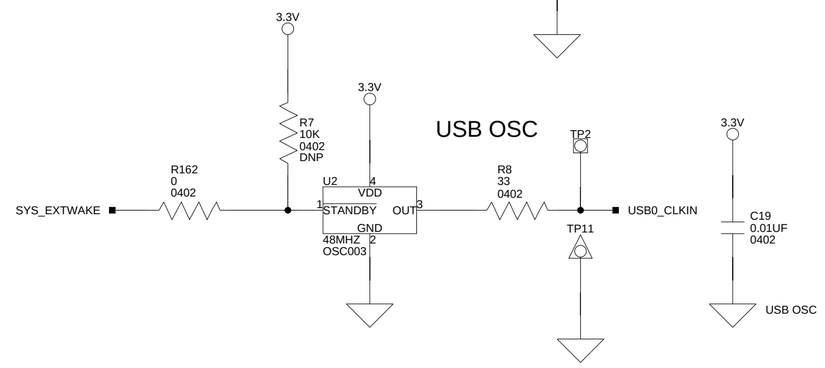
"USB OTG"

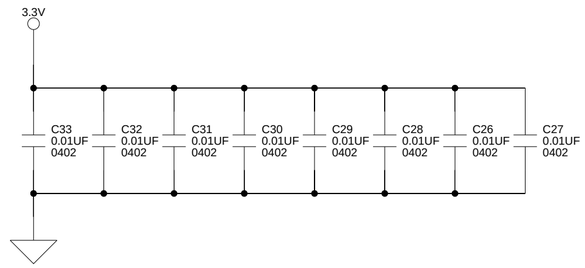


OPTIONAL DSP CRYSTAL



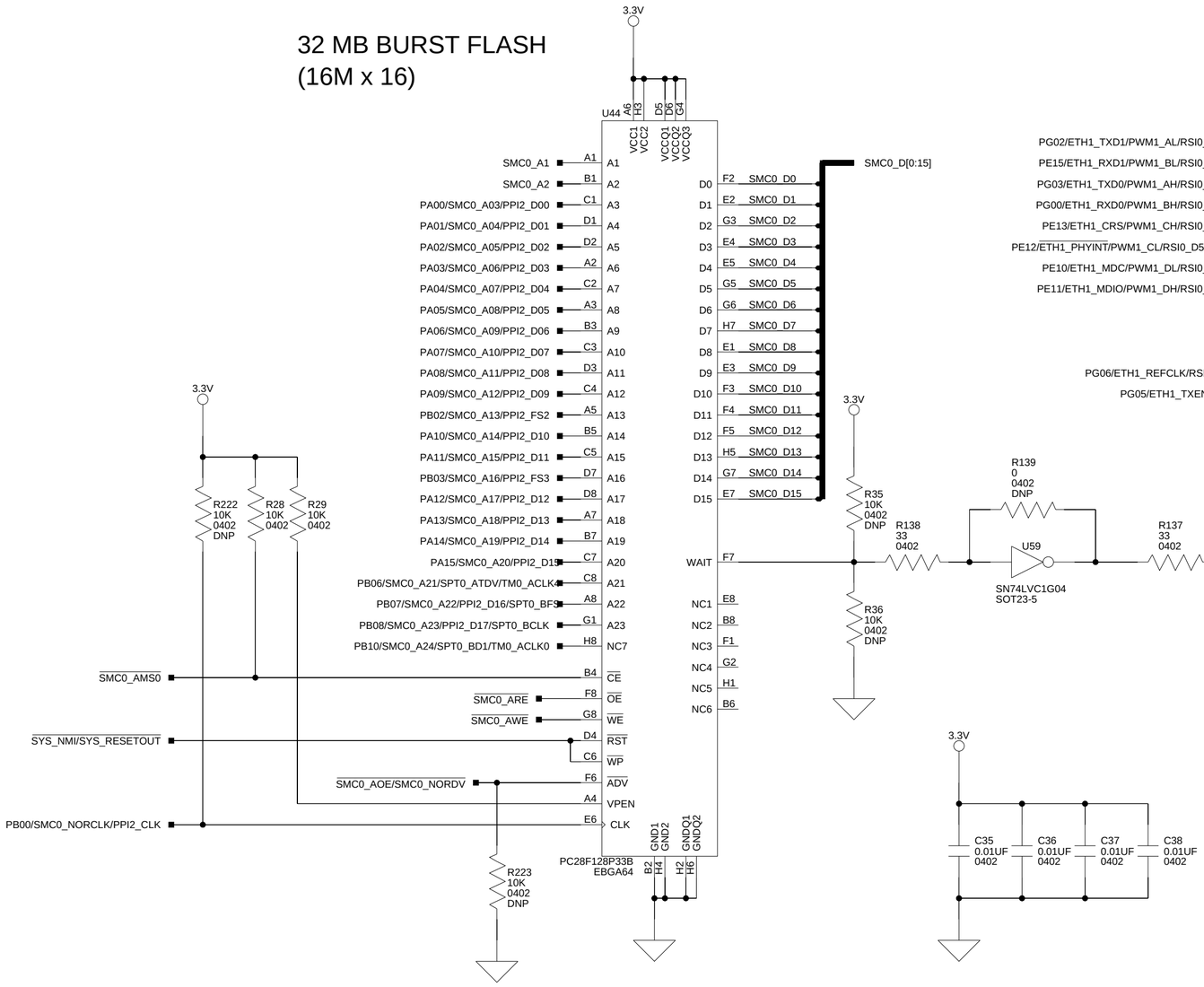




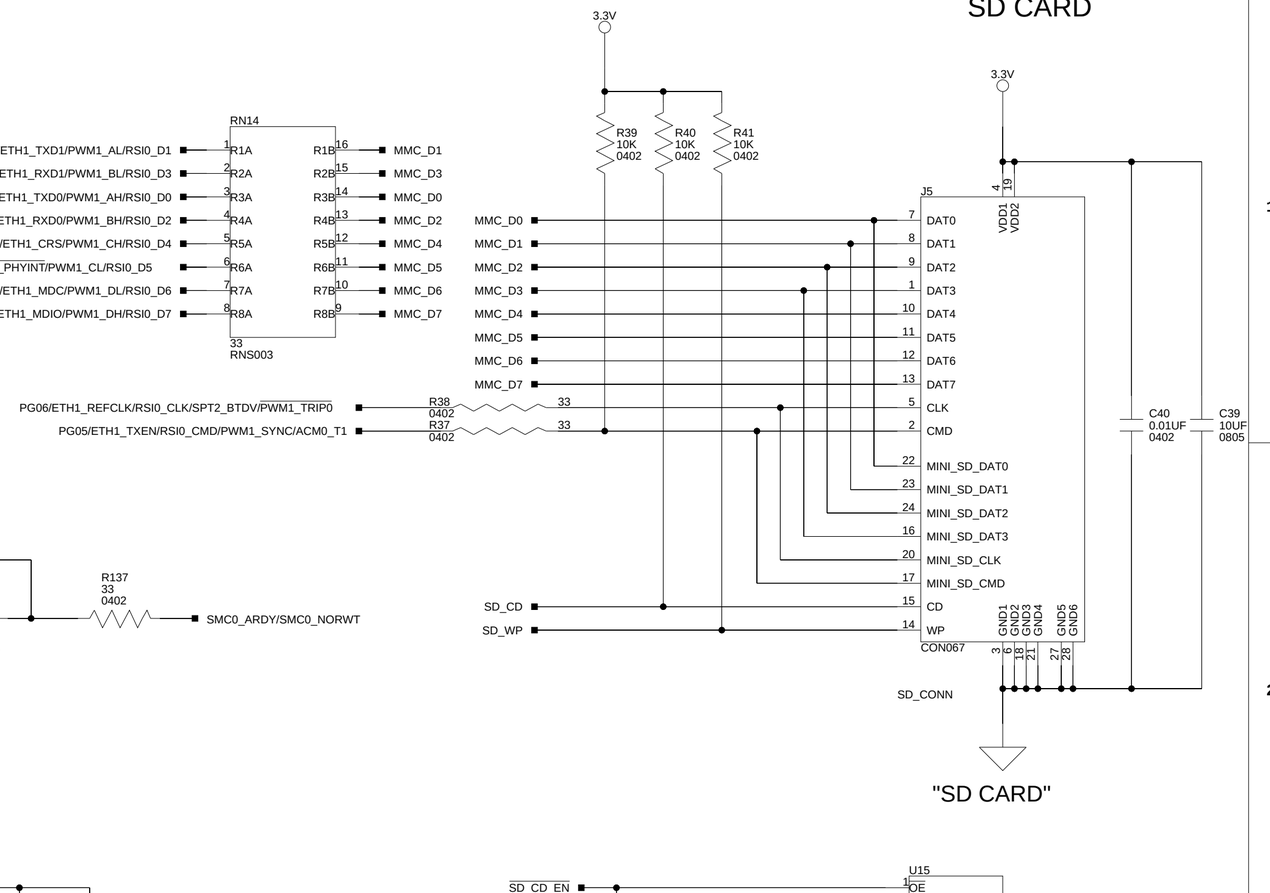


ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD		
Title	ADSP-BF609 EZ-Board Temp. Sensor, Boot Switch, DSP Clock, USB Conn		
Size C	Board No. A0269-2011		Rev 1.0
Date 1/5/12		Sheet 5 of 16	

32 MB BURST FLASH (16M x 16)

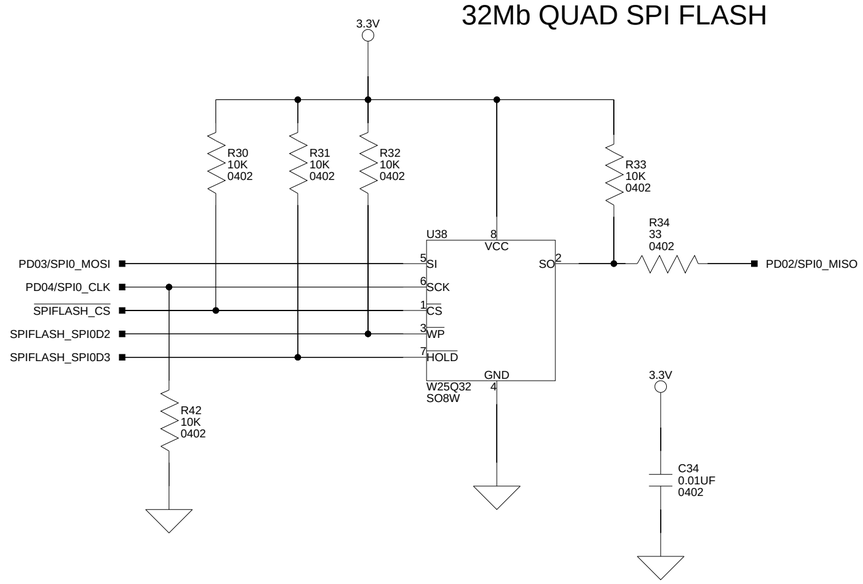


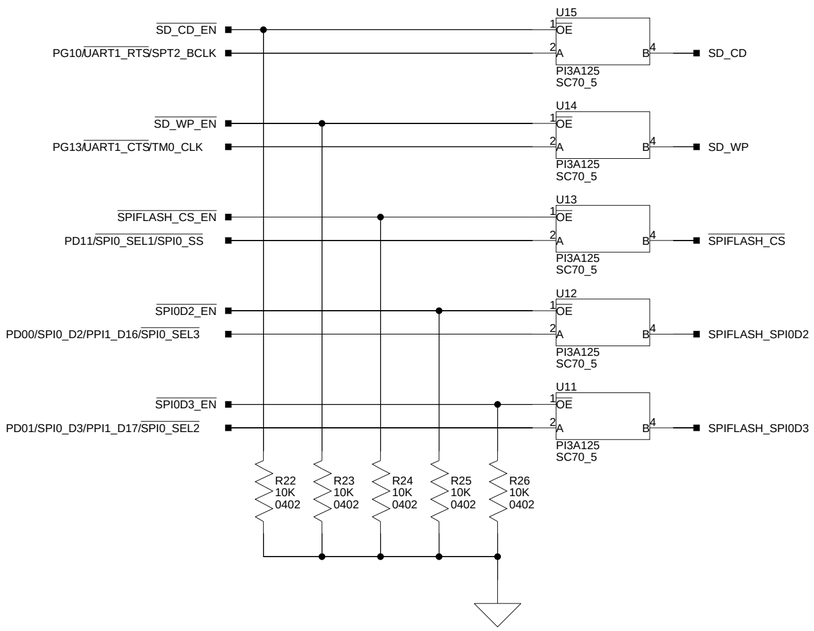
SD CARD



"SD CARD"

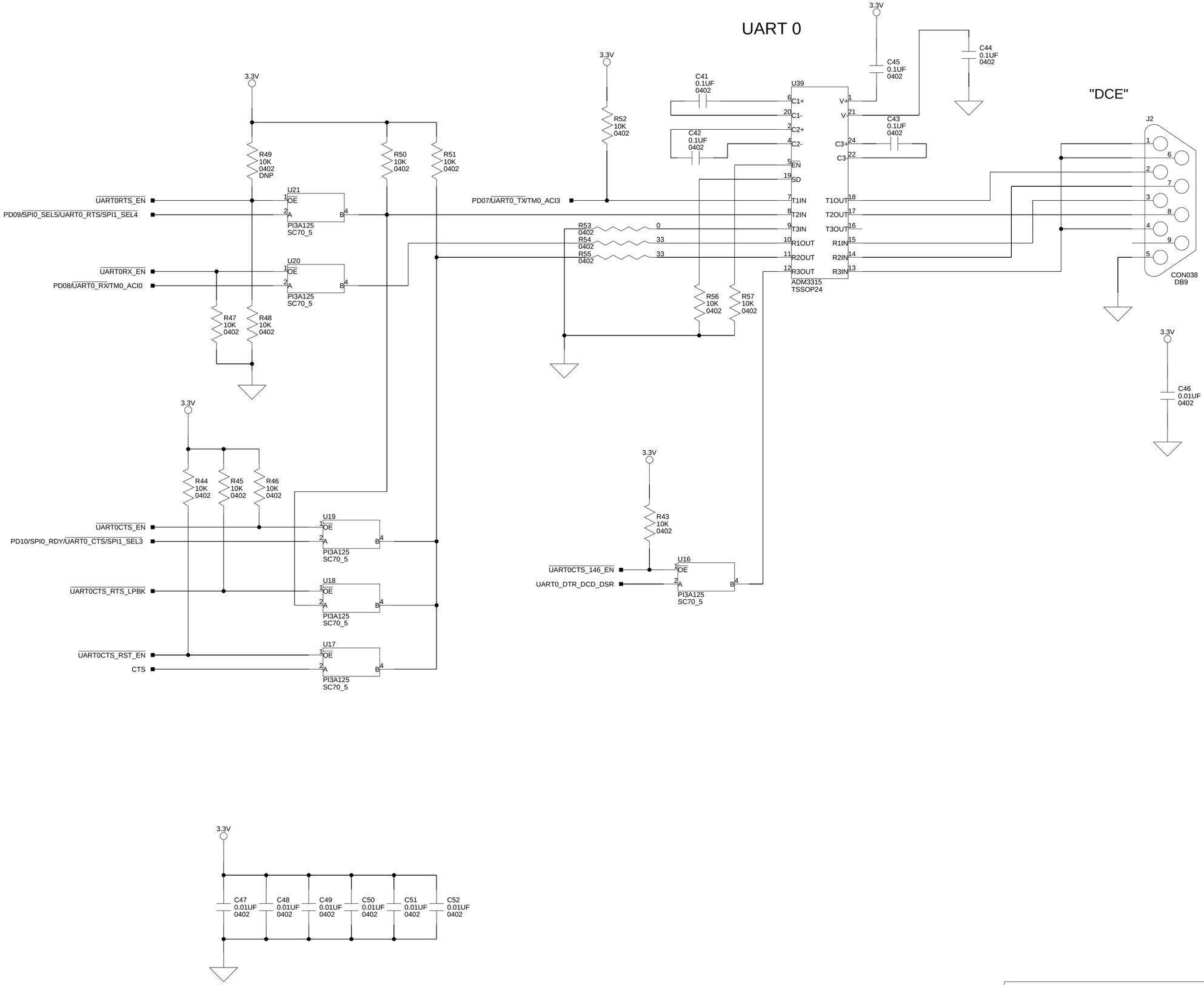
32Mb QUAD SPI FLASH



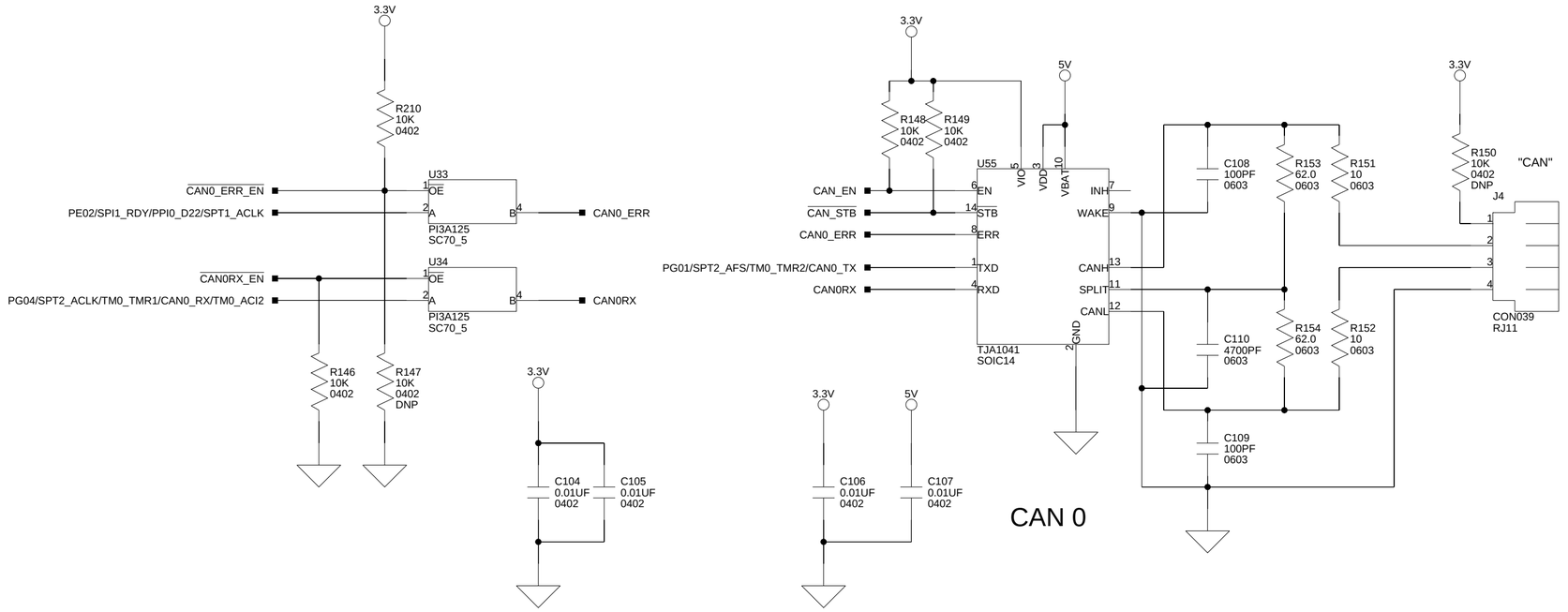


ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title	ADSP-BF609 EZ-Board Memory	
Size C	**Board No.** A0269-2011	**Rev** 1.0
Date 1/5/12	**Sheet** 6 **of** 16	

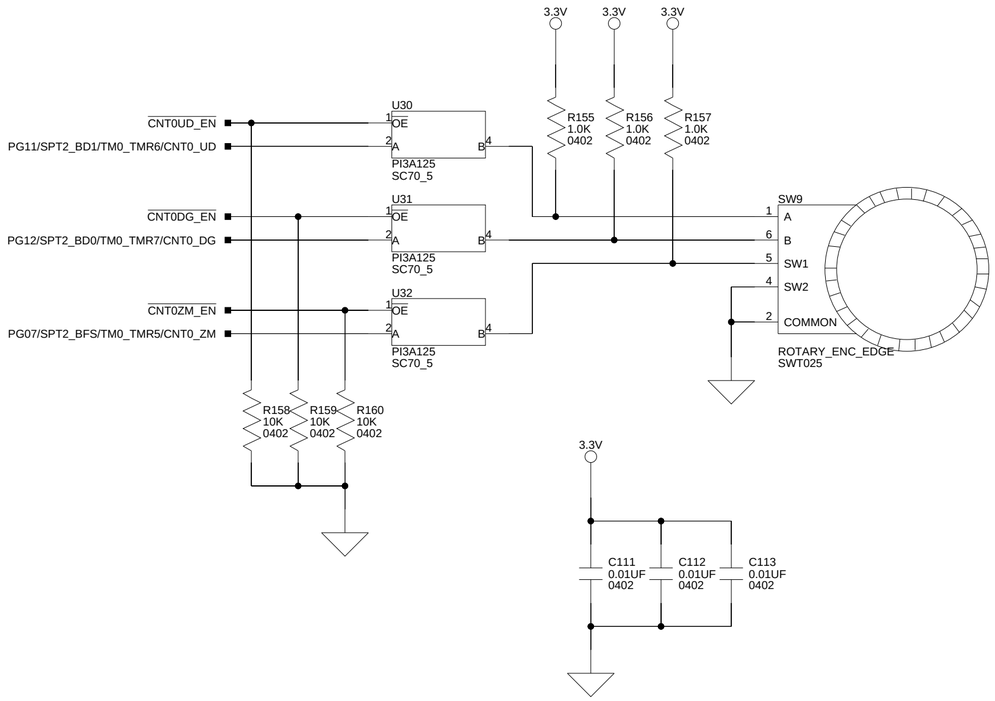
UART 0



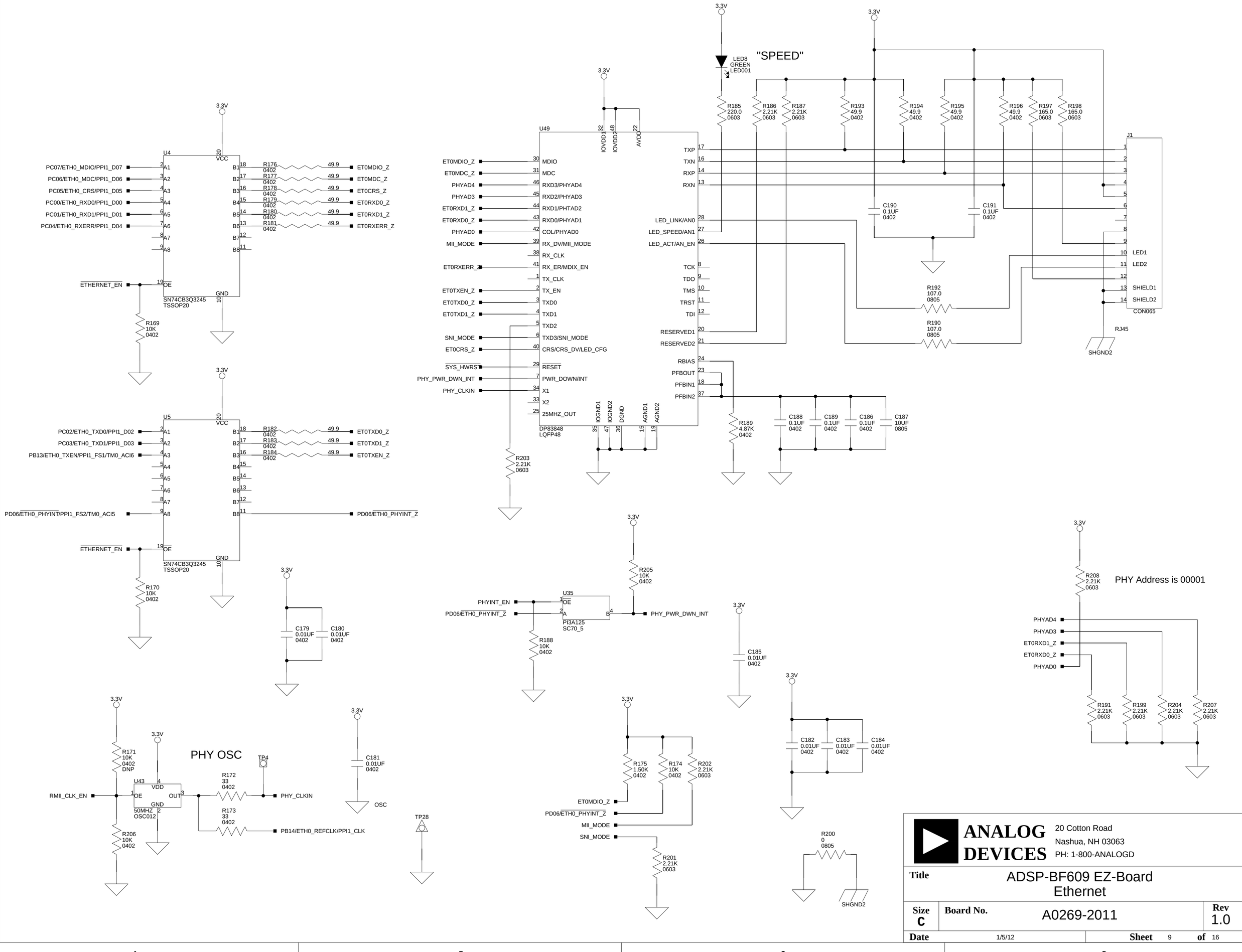
ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD		
Title	ADSP-BF609 EZ-Board UART0		
Size C	**Board No.** A0269-2011		**Rev** 1.0
Date 1/5/12		**Sheet** 7 **of** 16	



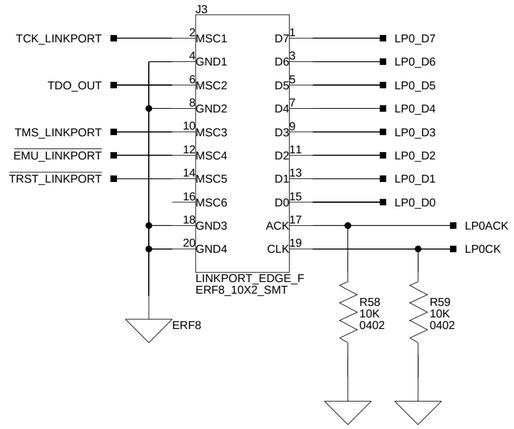
ROTARY ENCODER



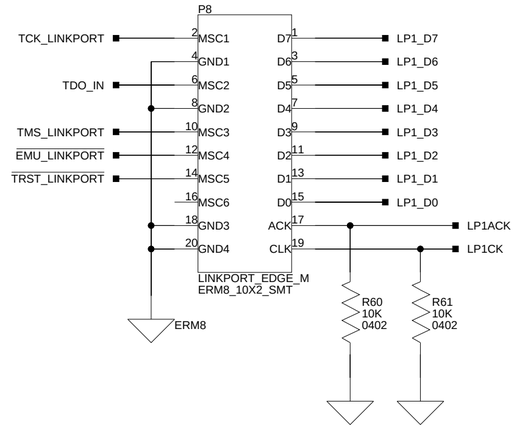
ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title	ADSP-BF609 EZ-Board CAN and Rotary Encoder	
Size C	**Board No.** A0269-2011	**Rev** 1.0
Date 1/5/12	**Sheet** 8 **of** 16	

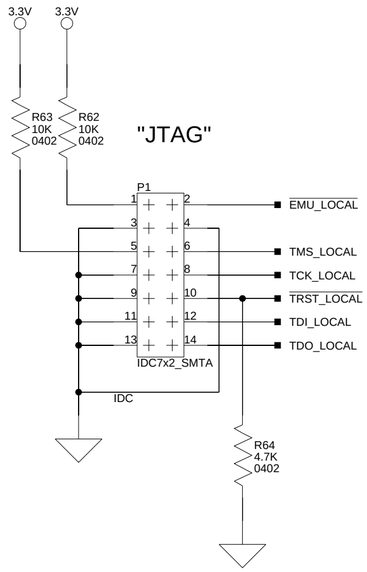

"SPEED"
LED8
GREEN
LED001
U4
U5
U49
U35
J1
SN74CB3Q3245
TSSOP20
DP83848
LQFP48
PI3A125
SC70_5
CON065
RJ45
SHGND2
PHY OSC
PHY Address is 00001
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD
Title
ADSP-BF609 EZ-Board
Ethernet
Size
C
Board No.
A0269-2011
Rev
1.0
Date
1/5/12
Sheet 9 of 16

LINK PORT 0 / JTAG OUT

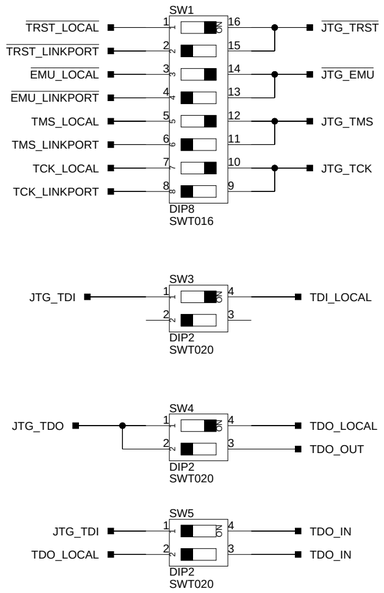


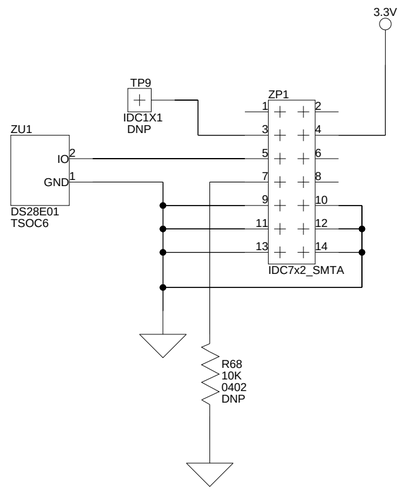
LINK PORT 1 / JTAG IN





JTAG SWITCHES





SINGLE PROCESSOR JTAG SETTINGS
EMUALTOR OR DEBUG AGENT (DEFAULT)

SWITCH	BOARD ATTACHED TO EMULATOR
SW1.1	ON
SW1.2	OFF
SW1.3	ON
SW1.4	OFF
SW1.5	ON
SW1.6	OFF
SW1.7	ON
SW1.8	OFF
SW3.1	ON
SW3.2	OFF
SW4.1	ON
SW4.2	OFF
SW5.1	OFF
SW5.2	OFF

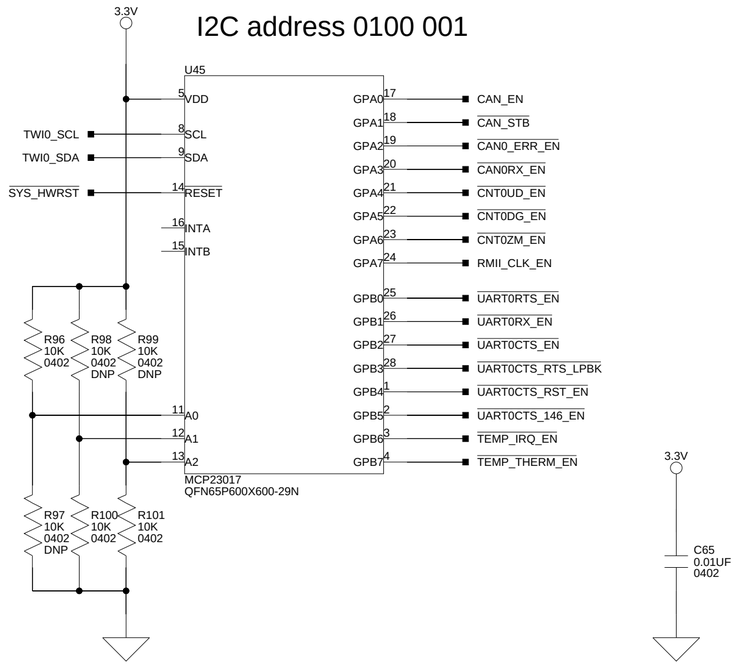
MULTI PROCESSOR JTAG SETTINGS VIA HP-USB EMUALTOR
USING TWO OR MORE EZ-BOARDS (LINK PORT CABLES
REQUIRED FOR MORE THAN TWO BOARDS)

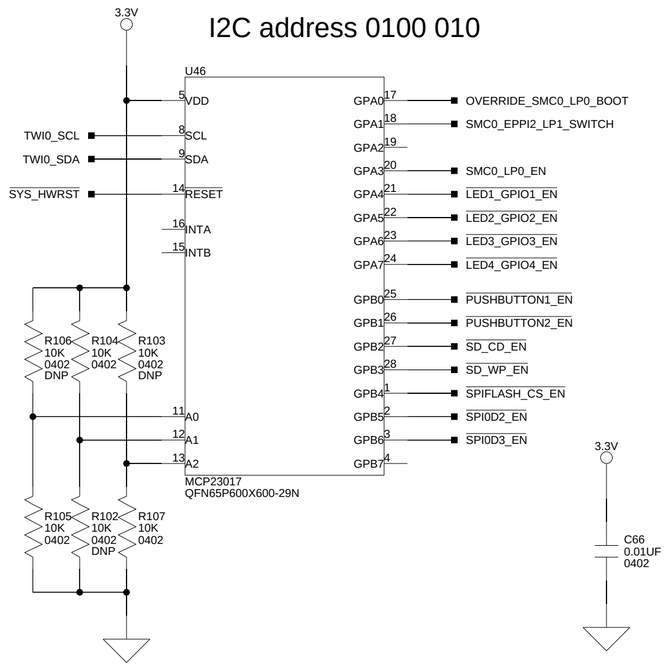
SWITCH	BOARD ATTACHED TO EMULATOR	BOARD(S) NOT ATTACHED TO EMULATOR
SW1.1	ON	OFF
SW1.2	ON	ON
SW1.3	ON	OFF
SW1.4	ON	ON
SW1.5	ON	OFF
SW1.6	ON	ON
SW1.7	ON	OFF
SW1.8	ON	ON
SW3.1	ON	OFF
SW3.2	OFF	OFF
SW4.1	OFF	OFF
SW4.2	ON	ON
SW5.1	OFF	ON
SW5.2	ON	OFF

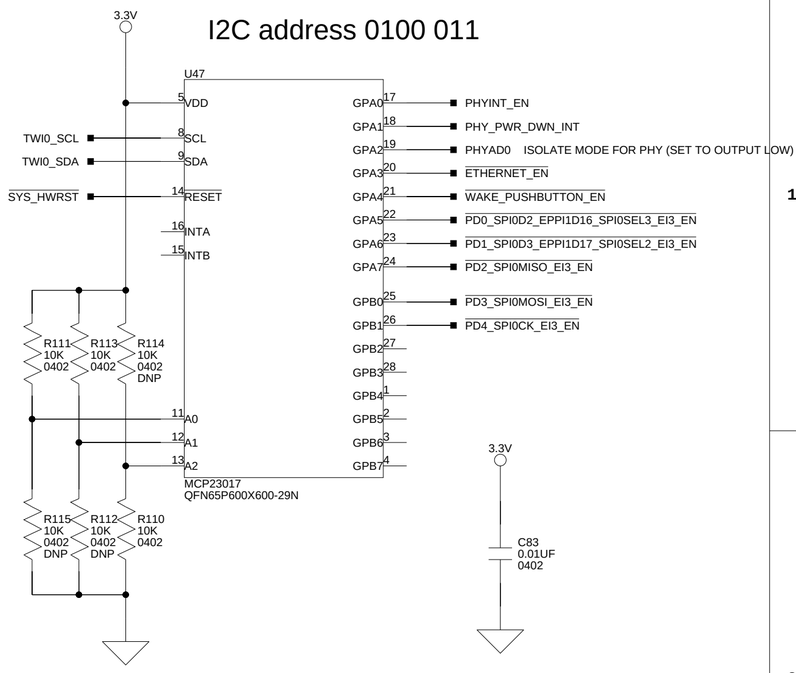
ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title	ADSP-BF609 EZ-Board JTAG, Linkport 0 and 1	
Size C	**Board No.** A0269-2011	**Rev** 1.0
Date 1/5/12	**Sheet** 10 **of** 16	

ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD		
Title	ADSP-BF609 EZ-Board Push Buttons, Reset, LEDs		
Size C	**Board No.** A0269-2011		**Rev** 1.0
Date 1/5/12	**Sheet** 11	**of** 16	

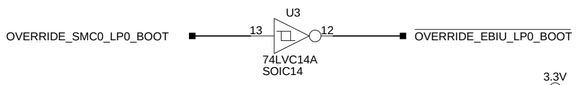


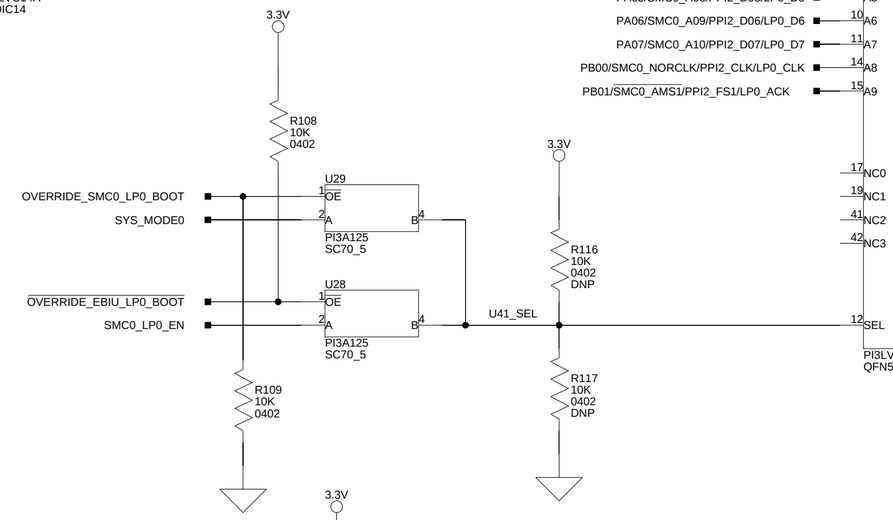


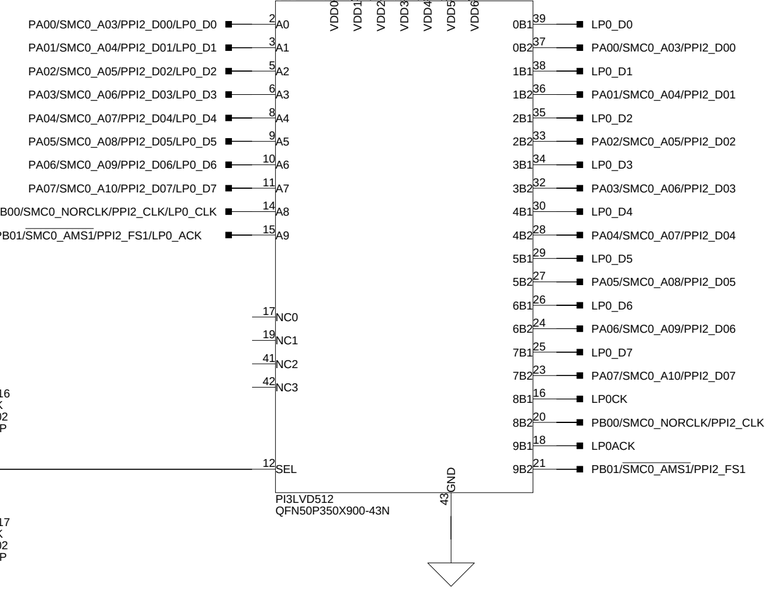


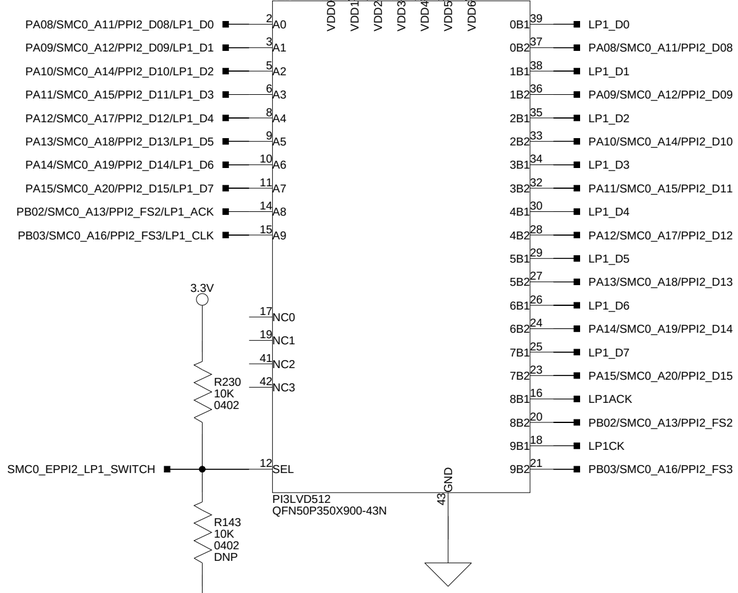
BOOT[0]	OVERRIDE_SMC0_LP0_BOOT	SMC0_LP0_EN	U41 output
0	0	X	LP0
0	1	0	LP0
1	0	X	SMC0_EPPI2
1	1	1	SMC0_EPPI2

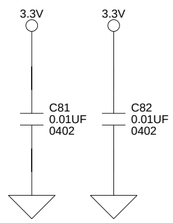
U41 output selection table

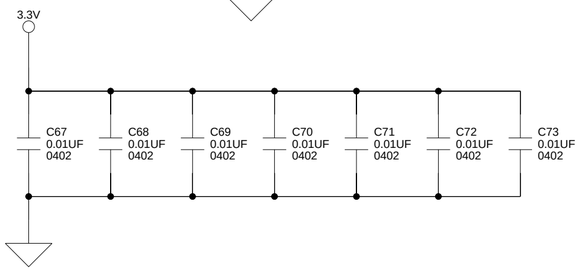


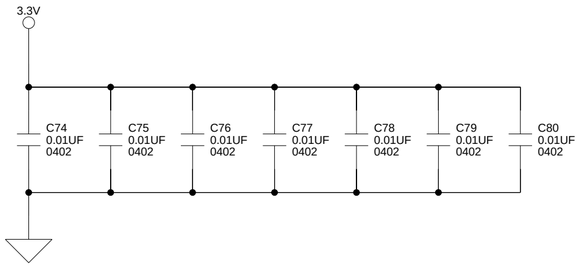












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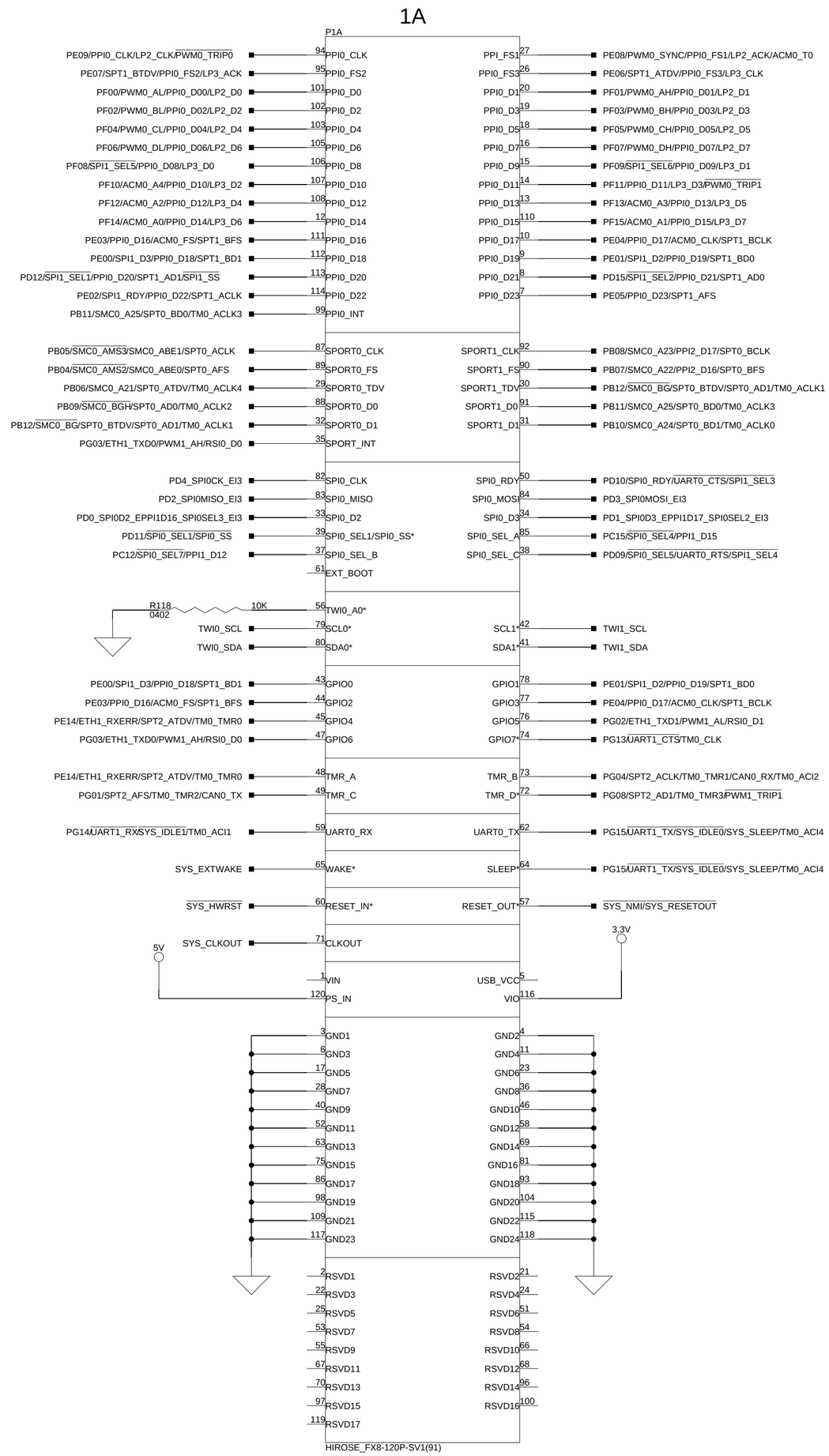

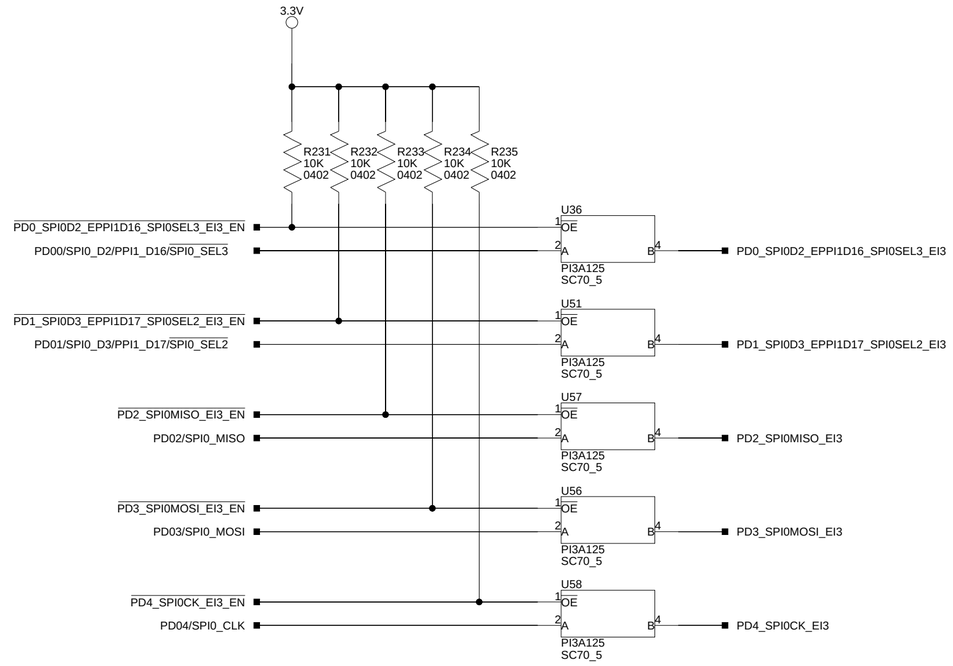

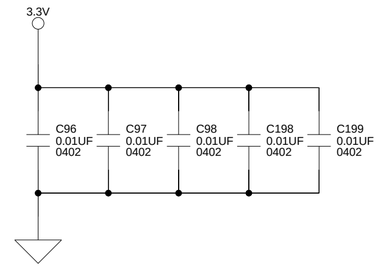

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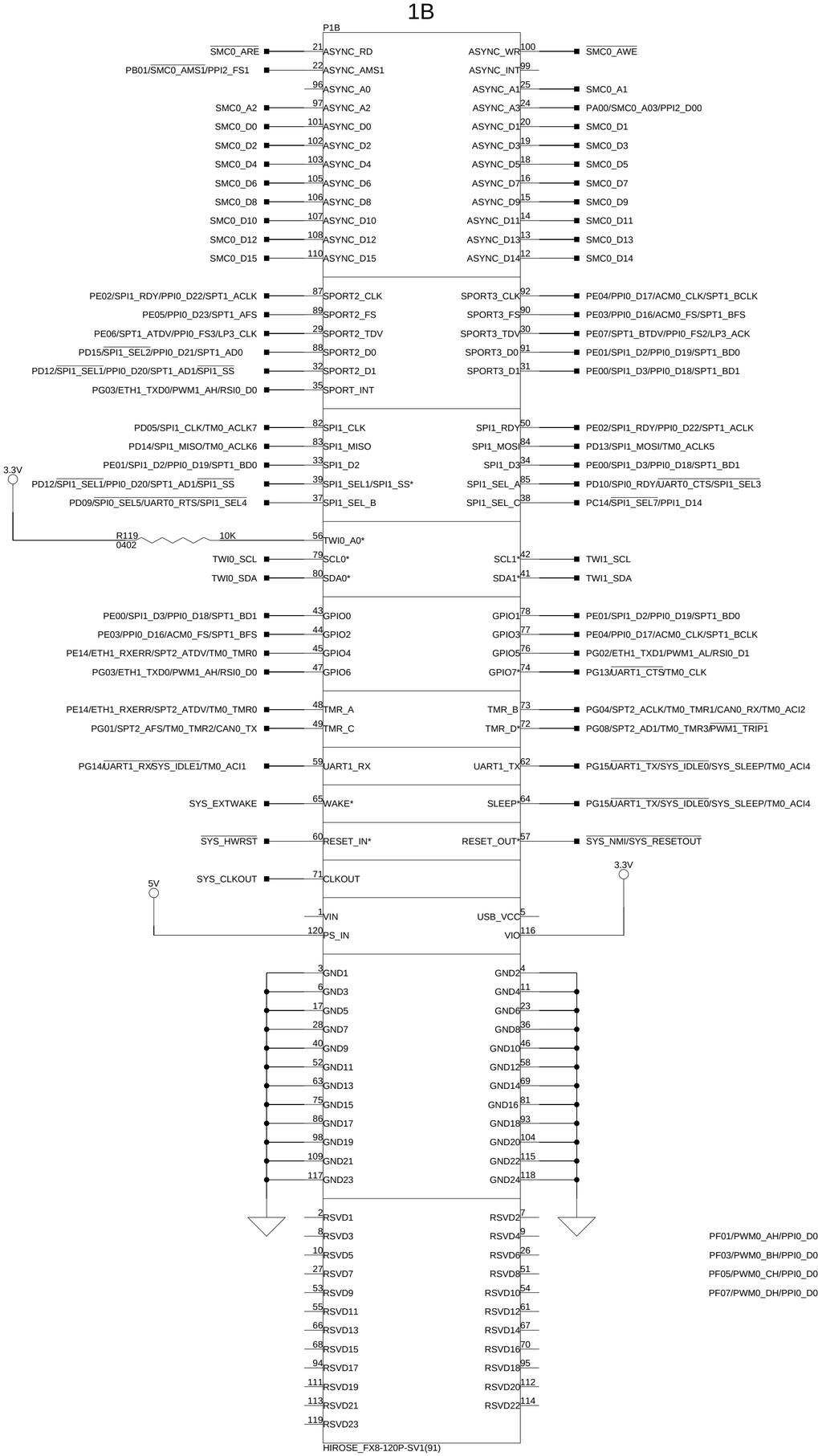

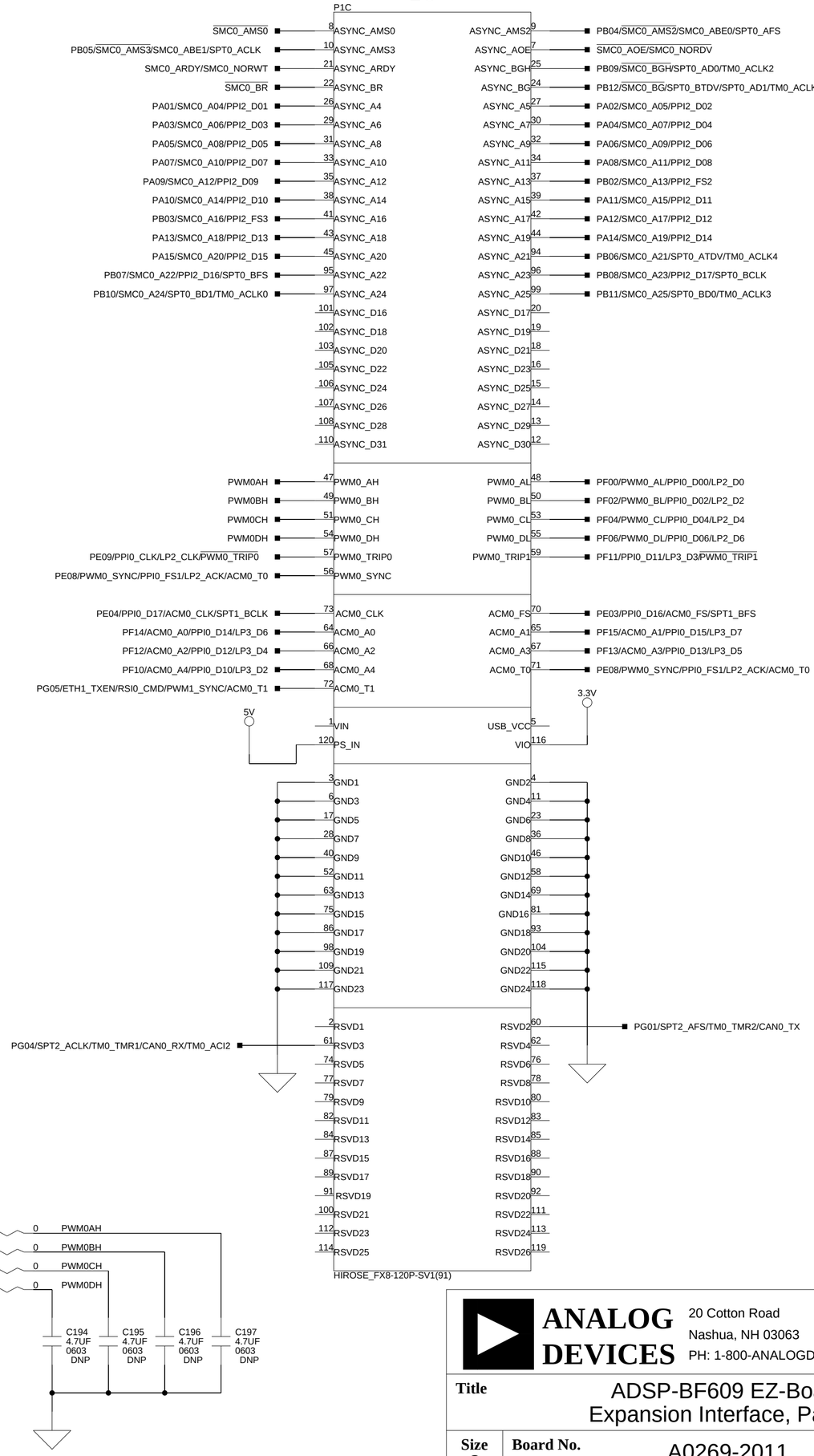

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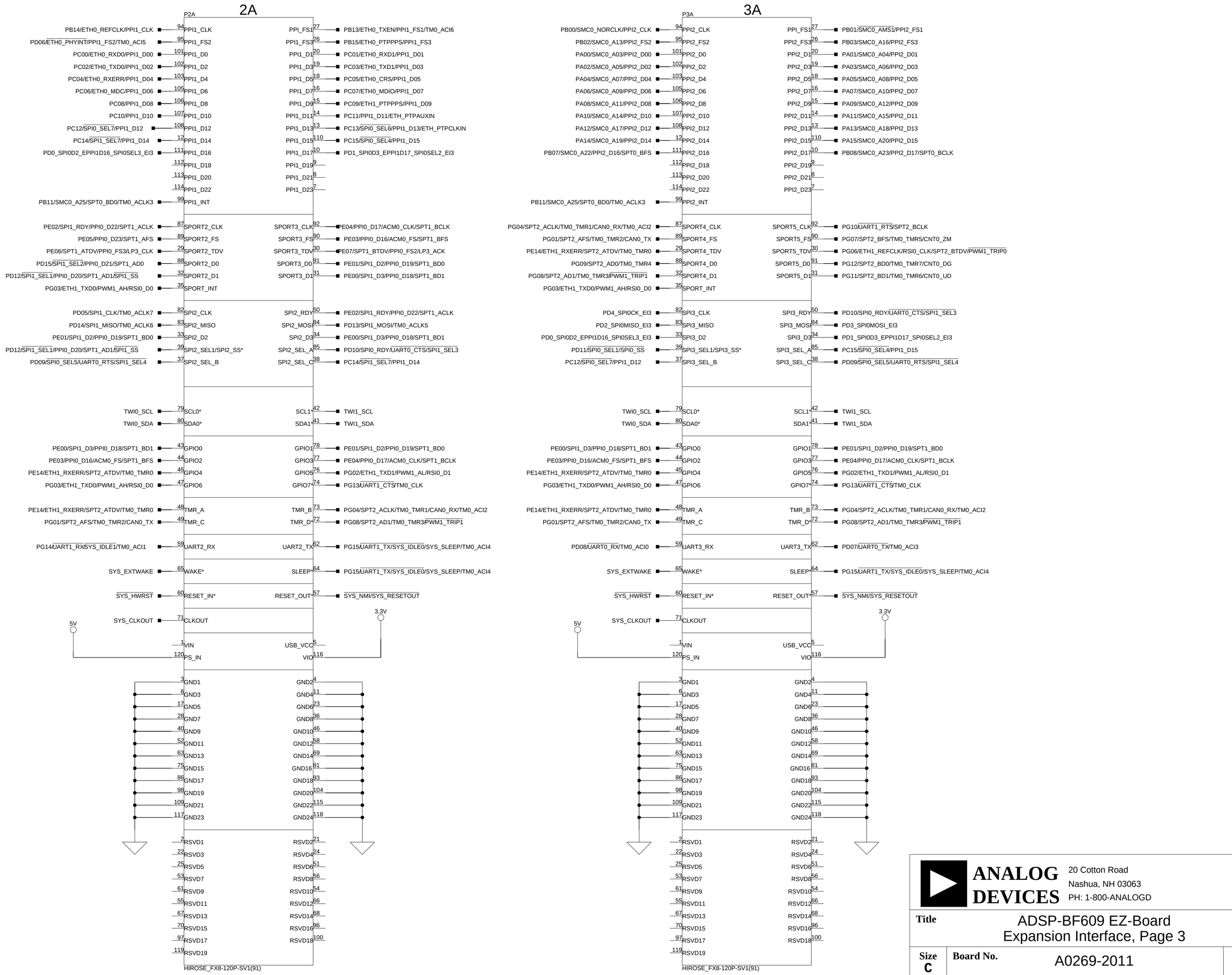

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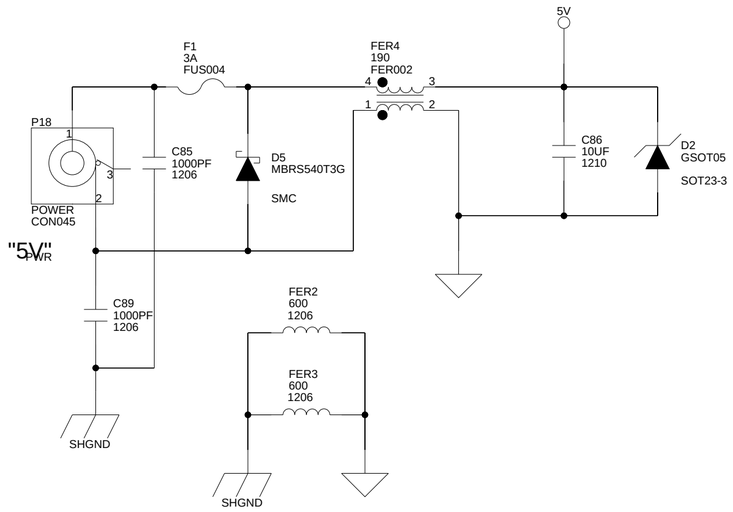

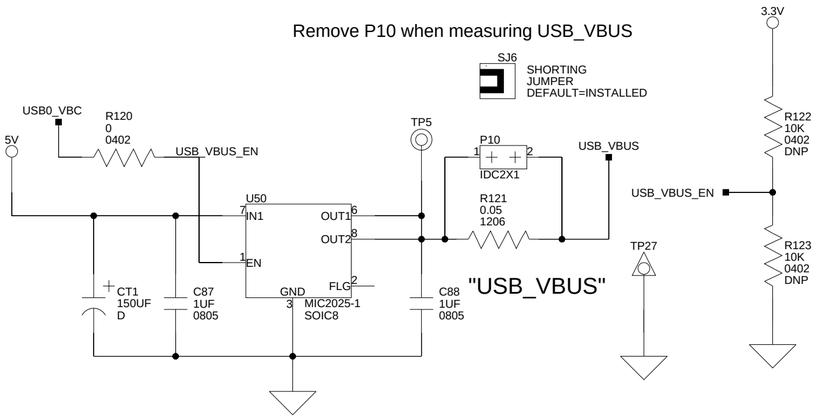

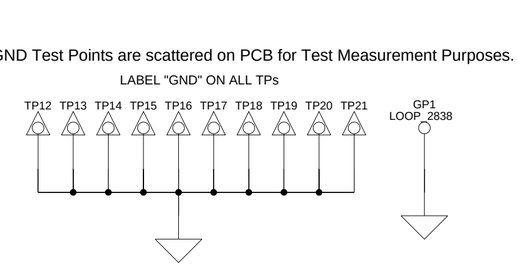

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