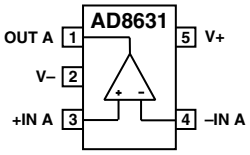
1.8 V, 5 MHz Rail-to-Rail Low Power Operational Amplifiers

AD8631/AD8632

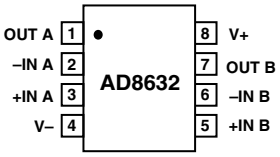
FEATURES
Single Supply Operation: 1.8 V to 6 V
Space-Saving SOT-23, μSOIC Packaging
Wide Bandwidth: 5 MHz @ 5 V, 4 MHz @ 1.8 V
Low Offset Voltage: 4 mV Max, 0.8 mV typ
Rail-to-Rail Input and Output Swing
2 V/μs Slew Rate @ 1.8 V
Only 225 μA Supply Current @ 1.8 V

APPLICATIONS
Portable Communications
Portable Phones
Sensor Interface
Active Filters
PCMCIA Cards
ASIC Input Drivers
Wearable Computers
Battery-Powered Devices
New Generation Phones
Personal Digital Assistants

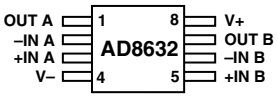
PIN CONFIGURATIONS
5-Lead SOT-23
(RT Suffix)



8-Lead SOIC
(R Suffix)



8-Lead μSOIC
(RM Suffix)



GENERAL DESCRIPTION

The AD8631 brings precision and bandwidth to the SOT-23-5 package at single supply voltages as low as 1.8 V and low supply current. The small package makes it possible to place the AD8631 next to sensors, reducing external noise pickup.

The AD8631 and AD8632 are rail-to-rail input and output bipolar amplifiers with a gain bandwidth of 4 MHz and typical voltage offset of 0.8 mV from a 1.8 V supply. The low supply current and the low supply voltage makes these parts ideal for battery-powered applications. The 3 V/μs slew rate makes the AD8631/AD8632 a good match for driving ASIC inputs, such as voice codecs.

The AD8631/AD8632 is specified over the extended industrial (–40°C to +125°C) temperature range. The AD8631 single is available in 5-lead SOT-23 surface-mount packages. The dual AD8632 is available in 8-lead SOIC and μSOIC packages.

REV. 0

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AD8631/AD8632–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = 5 V, V– = 0 V, V_{CM} = 2.5 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.8	4.0	mV
		–40°C ≤ T_A ≤ +125°C			6	mV
Input Bias Current	I_B				250	nA
		–40°C ≤ T_A ≤ +125°C			500	nA
Input Offset Current	I_{OS}				±150	nA
		–40°C ≤ T_A ≤ +125°C			550	nA
Input Voltage Range	V_{CM}		0		5	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 5 V,	63	70		dB
		–40°C ≤ T_A ≤ +125°C	56			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, 0.5 V < V_{OUT} < 4.5 V		25		V/mV
		R_L = 100 kΩ, 0.5 V < V_{OUT} < 4.5 V	100	400		V/mV
		R_L = 100 kΩ, –40°C ≤ T_A ≤ +125°C	100			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3.5		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			400		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 100 µA				
		–40°C ≤ T_A ≤ +125°C	4.965			V
		I_L = 1 mA	4.7			V
Output Voltage Swing Low	V_{OL}	I_L = 100 µA				
		–40°C ≤ T_A ≤ +125°C			35	mV
		I_L = 1 mA			200	mV
Short Circuit Current	I_{SC}	Short to Ground, Instantaneous		±10		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.2 V to 6 V,	75	90		dB
		–40°C ≤ T_A ≤ +125°C	72			dB
Supply Current/Amplifier	I_{SY}	V_{OUT} = 2.5 V		300	450	µA
		–40°C ≤ T_A ≤ +125°C			650	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	1 V < V_{OUT} < 4 V, R_L = 10 kΩ		3		V/µs
Gain Bandwidth Product	GBP			5		MHz
Settling Time	T_S	0.1%		860		ns
Phase Margin	ϕ_m			53		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.8		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		23		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		1.7		pA/√Hz

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_S = 2.2 V, V– = 0 V, V_{CM} = 1.1 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.8	4.0	mV
		–40°C ≤ T_A ≤ +125°C			6	mV
Input Bias Current	I_B				250	nA
Input Offset Current	I_{OS}				±150	nA
Input Voltage Range	V_{CM}		0		2.2	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 2.2 V,	54	70		dB
		–40°C ≤ T_A ≤ +125°C	47			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, 0.5 V < V_{OUT} < 1.7 V		25		V/mV
		R_L = 100 kΩ	50	200		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 100 µA	2.165			V
		I_L = 750 µA	1.9			V
Output Voltage Swing Low	V_{OL}	I_L = 100 µA			35	mV
		I_L = 750 µA			200	mV
POWER SUPPLY						
Supply Current/Amplifier	I_{SY}	V_{OUT} = 1.1 V		250	350	µA
		–40°C ≤ T_A ≤ +125°C			500	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		2.5		V/µs
Gain Bandwidth Product	GBP			4.3		MHz
Phase Margin	ϕ_m			50		Degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		23		nV/$\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz		1.7		pA/$\sqrt{Hz}$

Specifications subject to change without notice.

AD8631/AD8632–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = 1.8 V, V– = 0 V, V_{CM} = 0.9 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.8	4.0	mV
		0°C ≤ T_A ≤ 125°C			6	mV
Input Bias Current	I_B				250	nA
Input Offset Current	I_{OS}				±150	nA
Input Voltage Range	V_{CM}		0		1.8	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 1.8 V,				
		0°C ≤ T_A ≤ 125°C	49	65		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, 0.5 V < V_{OUT} < 1.3 V		20		V/mV
		R_L = 100 kΩ, 0.5 V < V_{OUT} < 1.3 V	40	200		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 100 μA	1.765			V
		I_L = 750 μA	1.5			V
Output Voltage Swing Low	V_{OL}	I_L = 100 μA			35	mV
		I_L = 750 μA			200	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 1.7 V to 2.2 V,	68	86		dB
		0°C ≤ T_A ≤ 125°C	65			dB
Supply Current/Amplifier	I_{SY}	V_{OUT} = 0.9 V		225	325	μA
		0°C ≤ T_A ≤ 125°C			450	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		2		V/μs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	ϕ_m			49		Degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		23		nV/$\sqrt{\text{Hz}}$
Current Noise Density	i_n	f = 1 kHz		1.7		pA/$\sqrt{\text{Hz}}$

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 6 V
Input Voltage[2] . . . . . GND to V_S
Differential Input Voltage . . . . . ±0.6 V
Internal Power Dissipation
SOT-23 (RT) . . . . . See Thermal Resistance Chart
SOIC (R) . . . . . See Thermal Resistance Chart
µSOIC (RM) . . . . . See Thermal Resistance Chart
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
R, RM, and RT Packages . . . . . –65°C to +150°C
Operating Temperature Range
AD8631, AD8632 . . . . . –40°C to +125°C
Junction Temperature Range
R, RM, and RT Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supply voltages less than 6 V the input voltage is limited to the supply voltage.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
5-Lead SOT-23 (RT)	230	146	°C/W
8-Lead SOIC (R)	158	43	°C/W
8-Lead µSOIC (RM)	210	45	°C/W

NOTE
[1]θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for SOT-23 and SOIC packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Brand
AD8631ART[1]	–40°C to +125°C	5-Lead SOT-23	RT-5	AEA
AD8632AR	–40°C to +125°C	8-Lead SOIC	SO-8	
AD8632ARM[2]	–40°C to +125°C	8-Lead µSOIC	RM-8	AGA

NOTES
[1]Available in 3,000-piece reels only.
[2]Available in 2,500-piece reels only.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8631/AD8632 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



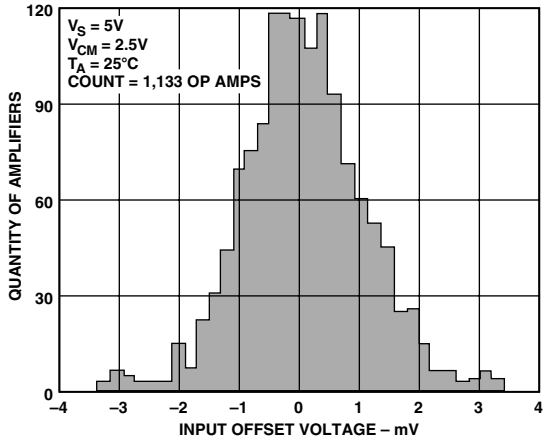


Figure 1. Input Offset Voltage Distribution

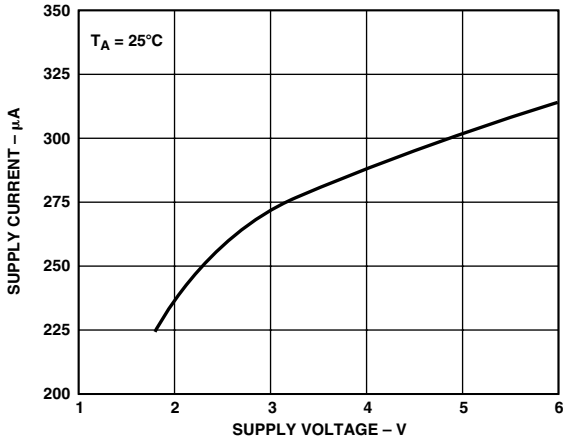


Figure 2. Supply Current per Amplifier vs. Supply Voltage

AD8631/AD8632 – Typical Characteristics

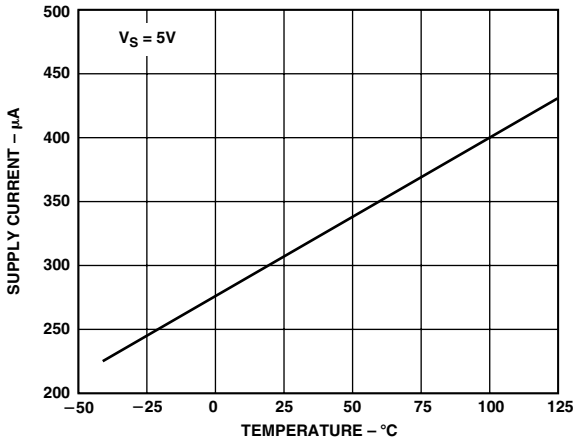


Figure 3. Supply Current per Amplifier vs. Temperature

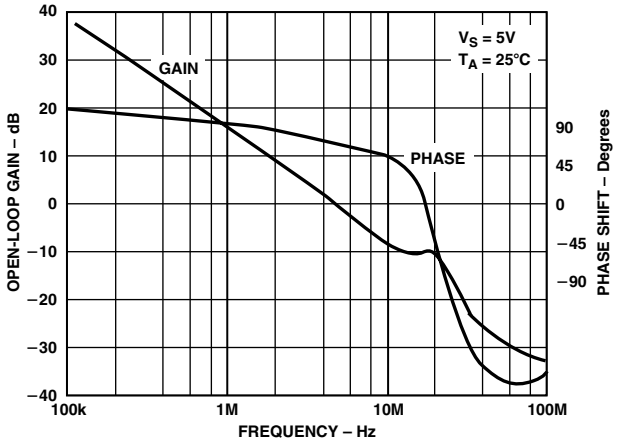


Figure 6. Open-Loop Gain vs. Frequency

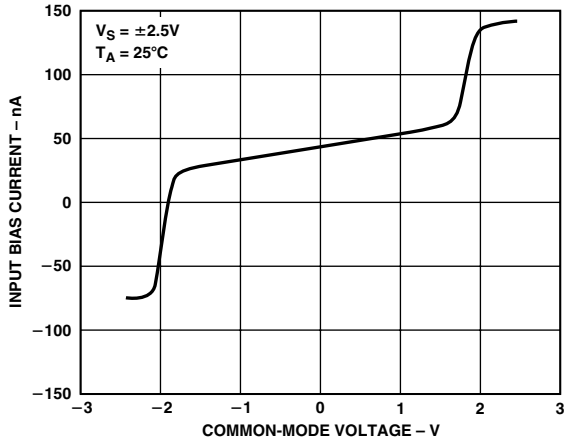


Figure 4. Input Bias Current vs. Common-Mode Voltage

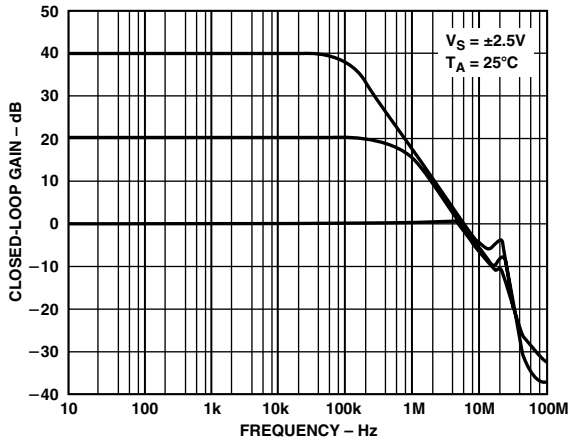


Figure 7. Closed-Loop Gain vs. Frequency

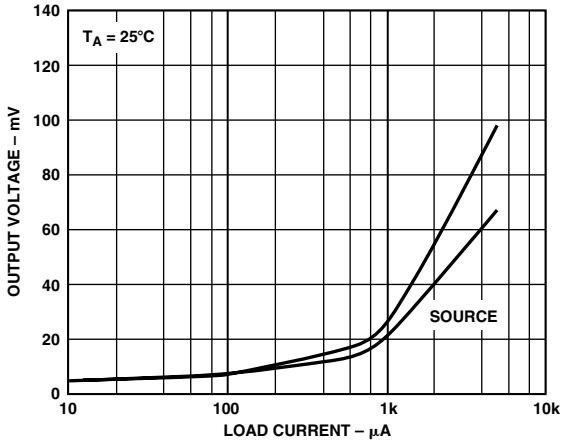


Figure 5. Output Voltage to Supply Rail vs. Load Current

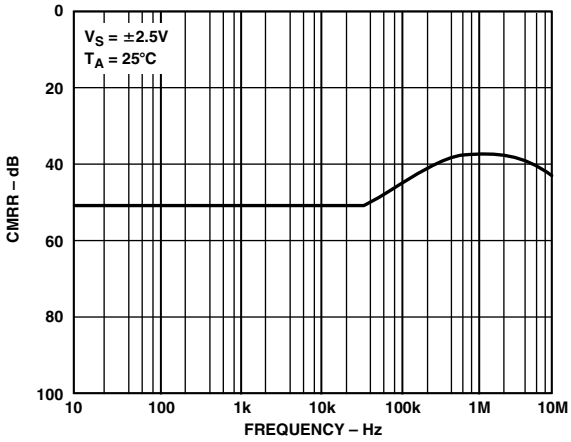


Figure 8. CMRR vs. Frequency

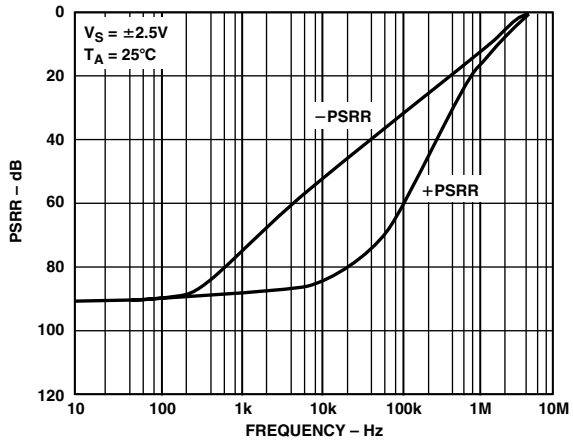


Figure 9. PSRR vs. Frequency

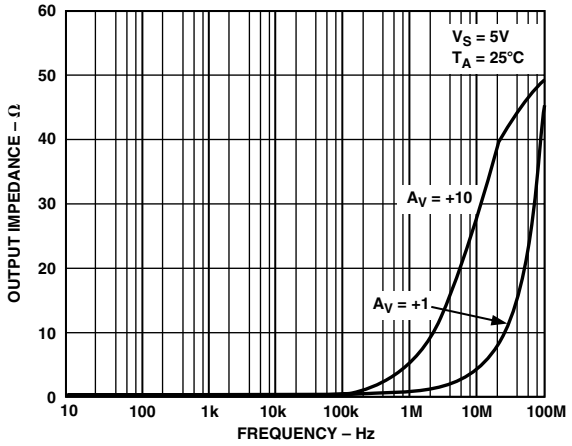


Figure 12. Output Impedance vs. Frequency

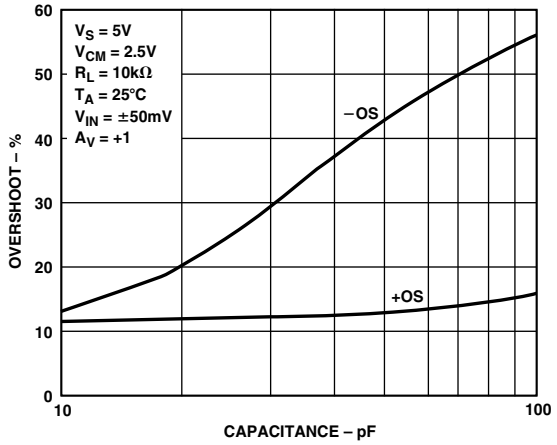


Figure 10. Overshoot vs. Capacitance Load

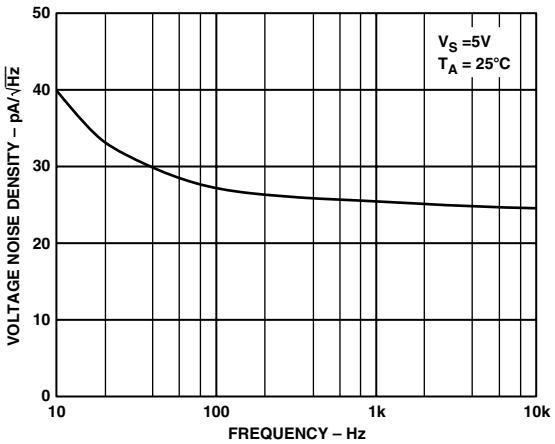


Figure 13. Voltage Noise Density vs. Frequency

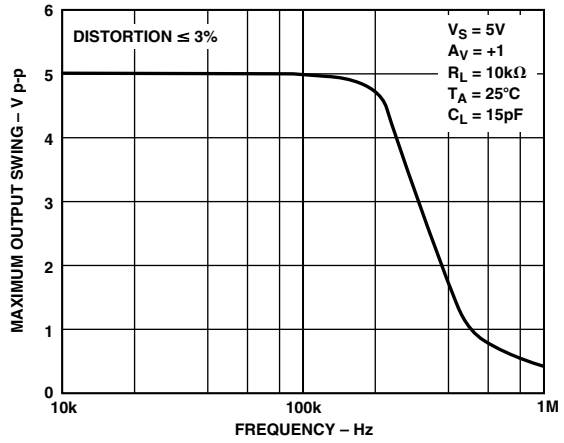


Figure 11. Output Swing vs. Frequency

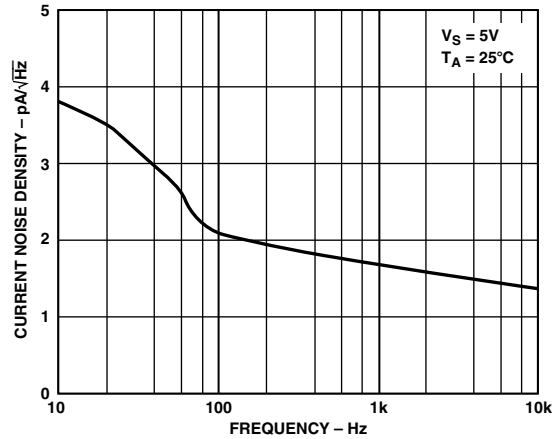


Figure 14. Current Noise Density vs. Frequency

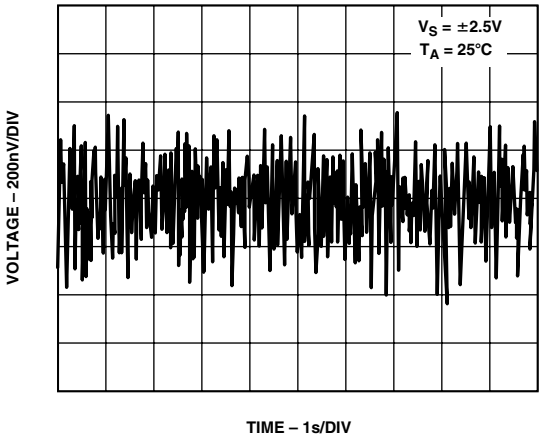


Figure 15. 0.1 Hz to 10 Hz Noise

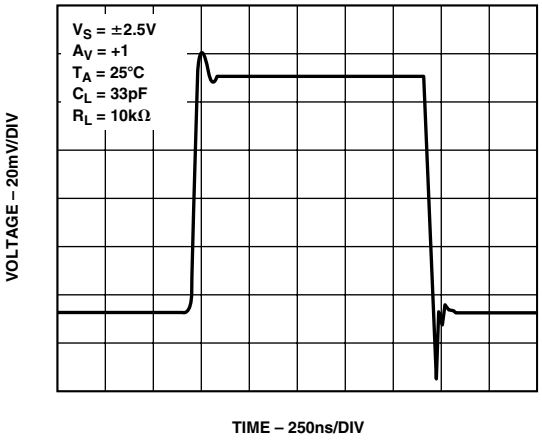


Figure 17. Small Signal Transient Response

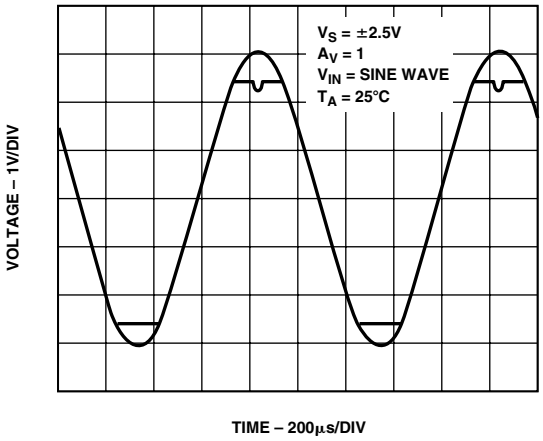


Figure 16. No Phase Reversal

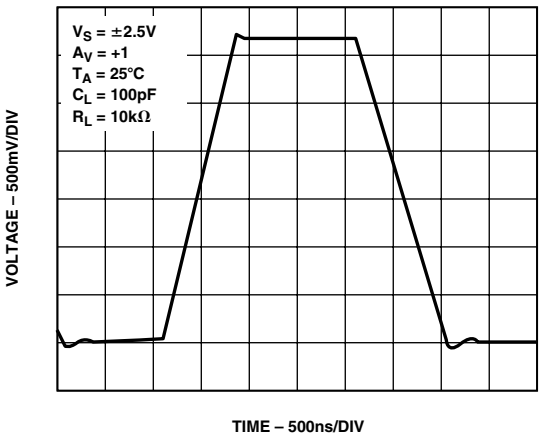


Figure 18. Large Signal Transient Response

THEORY OF OPERATION

The AD863x is a rail-to-rail operational amplifier that can operate at supply voltages as low as 1.8 V. This family is fabricated using Analog Devices' high-speed complementary bipolar process, also called XFCB. The process trench isolates each transistor to minimize parasitic capacitance, thereby allowing high-speed performance. Figure 19 shows a simplified schematic of the AD863x family.

The input stage consists of two parallel complementary differential pair: one NPN pair (Q1 and Q2) and one PNP pair (Q3 and Q4). The voltage drops across R7, R8, R9, and R10 are kept low for rail-to-rail operation. The major gain stage of the op amp is a double-folded cascode consisting of transistors Q5, Q6, Q8, and Q9. The output stage, which also operates rail-to-rail, is driven by Q14. The transistors Q13 and Q10 act as level-shifters to give more headroom during 1.8 V operation.

As the voltage at the base of Q13 increases, Q18 starts to sink current. When the voltage at the base of Q13 decreases I8 flows through D16 and Q15 increasing the VBE of Q17, then Q20 sources current.

The output stage also furnishes gain, which depends on the load resistance, since the output transistors are in common emitter configuration. The output swing when sinking or sourcing 100 μA is 35 mV maximum from each rail.

The input bias current characteristics depend on the common-mode voltage (see Figure 4). As the input voltage reaches about 1 V below V_{CC}, the PNP pair (Q3 and Q4) turns off.

The 1 kΩ input resistor R1 and R2, together with the diodes D7 and D8, protect the input pairs against avalanche damage.

The AD863x family exhibits no phase reversal as the input signal exceeds the supply by more than 0.6 V. Excessive current can flow through the input pins via the ESD diodes D1-D2 or D3-D4, in the event their ~0.6 V thresholds are exceeded. Such fault currents must be limited to 5 mA or less by the use of external series resistance(s).

LOW VOLTAGE OPERATION

Battery Voltage Discharge

The AD8631 operates at supply voltages as low as 1.8 V. This amplifier is ideal for battery-powered applications since it can operate at the end of discharge voltage of most popular batteries. Table I lists the Nominal and End-of-Discharge Voltages of several typical batteries.

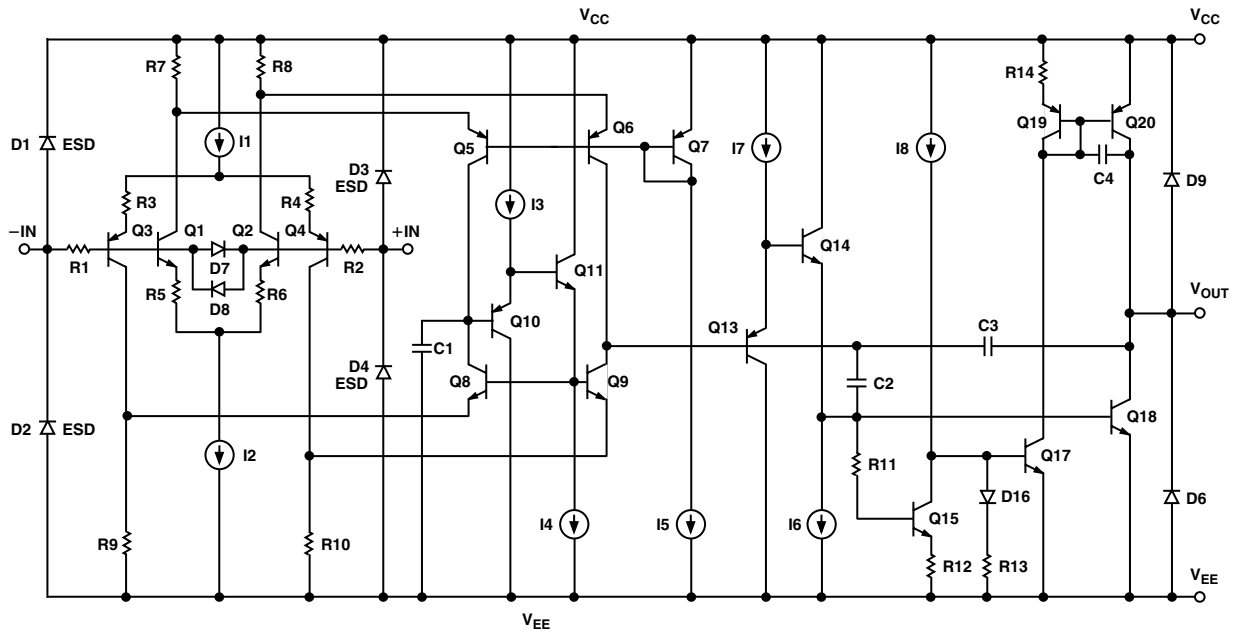


Figure 19. Simplified Schematic

Table I. Typical Battery Life Voltage Range

Battery	Nominal Voltage (V)	End-of-Voltage Discharge (V)
Lead-Acid	2	1.8
Lithium	2.6–3.6	1.7–2.4
NiMH	1.2	1
NiCd	1.2	1
Carbon-Zinc	1.5	1.1

RAIL-TO-RAIL INPUT AND OUTPUT

The AD8631 features an extraordinary rail-to-rail input and output with supply voltages as low as 1.8 V. With the amplifier's supply set to 1.8 V, the input can be set to 1.8 V p-p, allowing the output to swing to both rails without clipping. Figure 20 shows a scope picture of both input and output taken at unity gain, with a frequency of 1 kHz, at V_S = 1.8 V and V_{IN} = 1.8 V p-p.

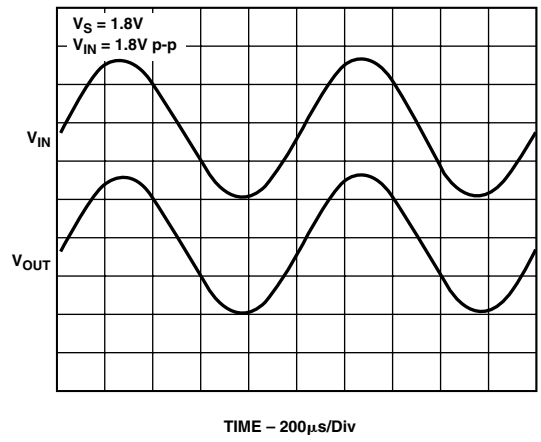


Figure 20. Rail-to-Rail Input Output

The rail-to-rail feature of the AD8631 can be observed over the supply voltage range, 1.8 V to 5 V. Traces are shown offset for clarity.

INPUT BIAS CONSIDERATION

The input bias current (I_B) is a non-ideal, real-life parameter that affects all op amps. I_B can generate a somewhat significant offset voltage. This offset voltage is created by I_B when flowing through the negative feedback resistor R_F. If I_B is 250 nA (worst case), and R_F is 100 kΩ, the corresponding generated offset voltage is 25 mV ($V_{OS} = I_B \times R_F$).

Obviously the lower the R_F the lower the generated voltage offset. Using a compensation resistor, R_B, as shown in Figure 21, can minimize this effect. With the input bias current minimized we still need to be aware of the input offset current (I_{OS}) which will generate a slight offset error. Figure 21 shows three different configurations to minimize I_B-induced offset errors.

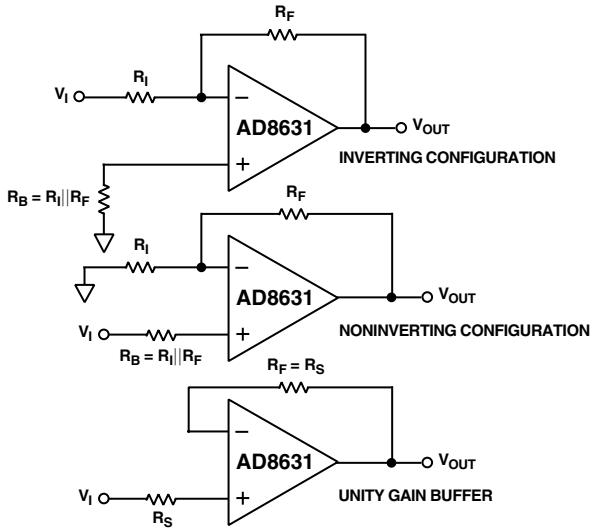


Figure 21. Input Bias Cancellation Circuits

DRIVING CAPACITIVE LOADS

Capacitive Load vs. Gain

Most amplifiers have difficulty driving capacitance due to degradation of phase margin caused by additional phase lag from the capacitive load. Higher capacitance at the output can increase the amount of overshoot and ringing in the amplifier's step response and could even affect the stability of the device. The value of capacitive load that an amplifier can drive before oscillation varies with gain, supply voltage, input signal, temperature, among others. Unity gain is the most challenging configuration for driving capacitive load. However, the AD8631 offers reasonably good capacitive driving ability. Figure 22 shows the AD8631's ability to drive capacitive loads at different gains before instability occurs. This graph is good for all V_{SY}.

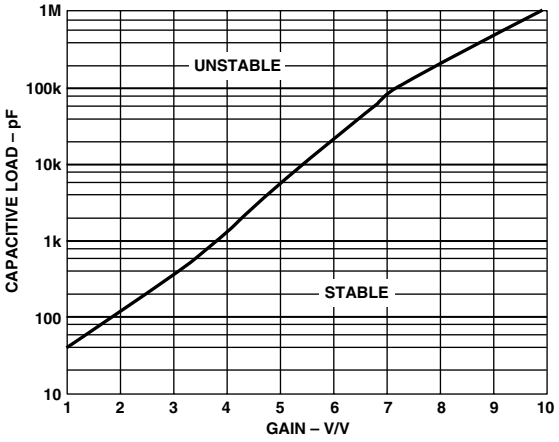
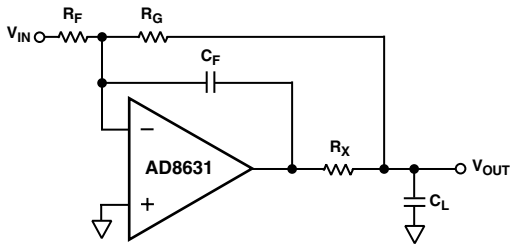


Figure 22. Capacitive Load vs. Gain

In-the-Loop Compensation Technique for Driving Capacitive Loads

When driving capacitance in low gain configuration, the in-the-loop compensation technique is recommended to avoid oscillation as is illustrated in Figure 23.



$$R_X = \frac{R_O R_G}{R_F} \quad \text{WHERE } R_O = \text{OPEN-LOOP OUTPUT RESISTANCE}$$

$$C_F = \left[1 + \left(\frac{1}{|A_{CL}|}\right)\right]\left(\frac{R_F + R_G}{R_F}\right) C_L R_O$$

Figure 23. In-the-Loop Compensation Technique for Driving Capacitive Loads

Snubber Network Compensation for Driving Capacitive Loads

As load capacitance increases, the overshoot and settling time will increase and the unity gain bandwidth of the device will decrease. Figure 24 shows an example of the AD8631 in a noninverting configuration driving a 10 kΩ resistor and a 600 pF capacitor placed in parallel, with a square wave input set to a frequency of 90 kHz and unity gain.

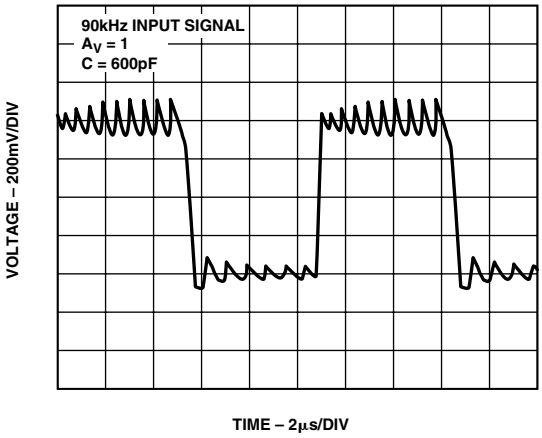


Figure 24. Driving Capacitive Loads without Compensation

By connecting a series R–C from the output of the device to ground, known as the "snubber" network, this ringing and overshoot can be significantly reduced. Figure 25 shows the network setup, and Figure 26 shows the improvement of the output response with the "snubber" network added.

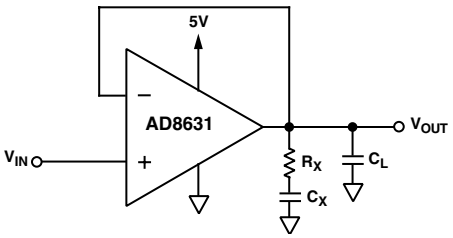


Figure 25. Snubber Network Compensation for Capacitive Loads

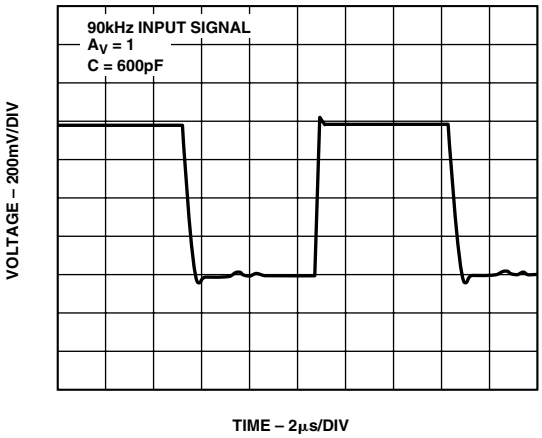


Figure 26. Photo of a Square Wave with the Snubber Network Compensation

The network operates in parallel with the load capacitor, C_L, and provides compensation for the added phase lag. The actual values of the network resistor and capacitor have to be empirically determined. Table II shows some values of snubber network for large capacitance load.

Table II. Snubber Network Values for Large Capacitive Loads

C_{LOAD}	Rx	Cx
600 pF	300 Ω	1 nF
1 nF	300 Ω	1 nF
10 nF	90 Ω	8 nF

TOTAL HARMONIC DISTORTION + NOISE

The AD863x family offers a low total harmonic distortion, which makes this amplifier ideal for audio applications. Figure 27 shows a graph of THD + N, which is ~0.02% @ 1 kHz, for a 1.8 V supply. At unity gain in an inverting configuration the value of the Total Harmonic Distortion + Noise stays consistently low over all voltages supply ranges.

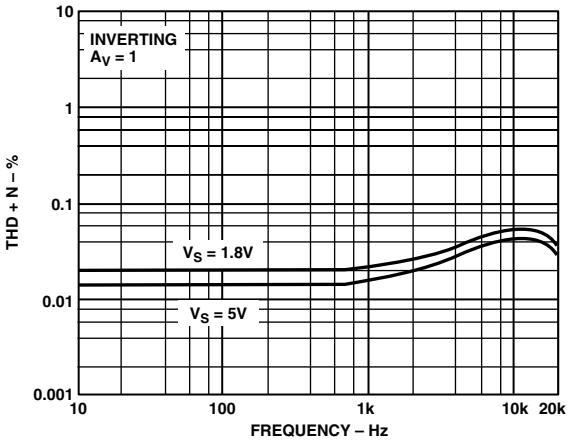


Figure 27. THD + N vs. Frequency Graph

AD8632 Turn-On Time

The low voltage, low power AD8632 features an extraordinary turn on time. This is about 500 ns for V_{SY} = 5 V, which is impressive considering the low supply current (300 μA typical per amplifier). Figure 28 shows a scope picture of the AD8632 with both channels configured as followers. Channel A has an input signal of 2.5 V and channel B has the input signal at ground. The top waveform shows the supply voltage and the bottom waveform reflects the response of the amplifier at the output of Channel A.

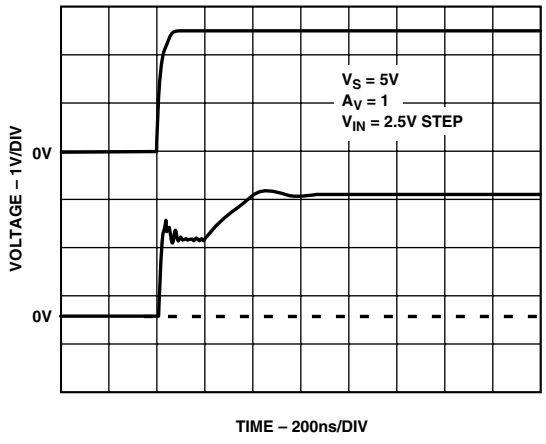


Figure 28. AD8632 Turn-On Time

A MICROPOWER REFERENCE VOLTAGE GENERATOR

Many single-supply circuits are configured with the circuit biased to one-half of the supply voltage. In these cases, a false-ground reference can be created by using a voltage divider buffered by an amplifier. Figure 28 shows the schematic for such a circuit.

The two 1 MΩ resistors generate the reference voltages while drawing only 0.9 μA of current from a 1.8 V supply. A capacitor connected from the inverting terminal to the output of the op amp provides compensation to allow a bypass capacitor to be connected at the reference output. This bypass capacitor helps establish an ac ground for the reference output.

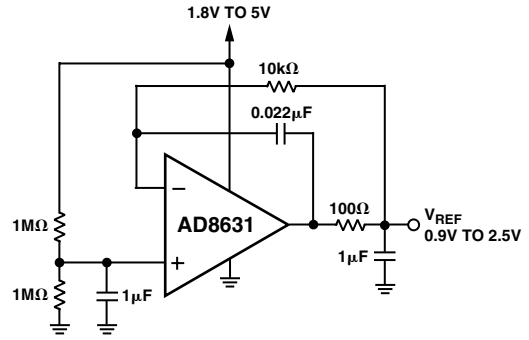


Figure 29. A Micropower Reference Voltage Generator

MICROPHONE PREAMPLIFIER

The AD8631 is ideal to use as a microphone preamplifier. Figure 30 shows this implementation.

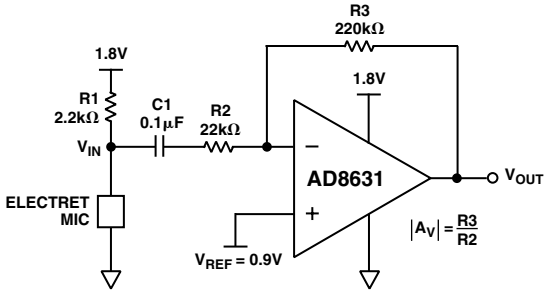


Figure 30. A Microphone Preamplifier

R1 is used to bias an electret microphone and C1 blocks dc voltage from the amplifier. The magnitude of the gain of the amplifier is approximately R3/R2 when R2 ≥ 10 × R1. V_{REF} should be equal to 1/2 × 1.8 V for maximum voltage swing.

Direct Access Arrangement for Telephone Line Interface

Figure 31 illustrates a 1.8 V transmit/receive telephone line interface for 600 Ω transmission systems. It allows full duplex transmission of signals on a transformer-coupled 600 Ω line in a differential manner. Amplifier A1 provides gain that can be adjusted to meet the modem output drive requirements. Both A1 and A2 are configured to apply the largest possible signal on a single supply to the transformer. Amplifier A3 is configured as a difference amplifier for two reasons: (1) It prevents the transmit signal from interfering with the receive signal and (2) it extracts the receive signal from the transmission line for amplification by A4. A4's gain can be adjusted in the same manner as A1's to meet the modem's input signal requirements. Standard resistor values permit the use of SIP (Single In-line Package) format resistor arrays. Couple this with the AD8631/

AD8632's 5-lead SOT-23, 8-lead μSOIC, and 8-lead SOIC footprint and this circuit offers a compact solution.

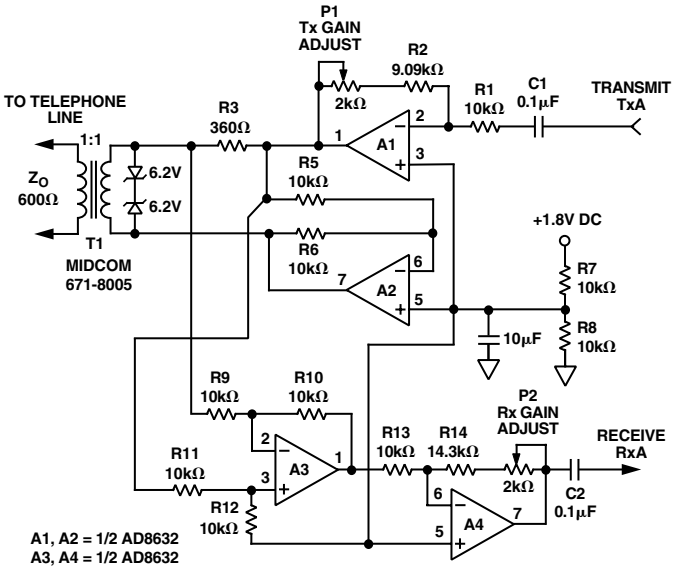


Figure 31. A Single-Supply Direct Access Arrangement for Modems

SPICE Model

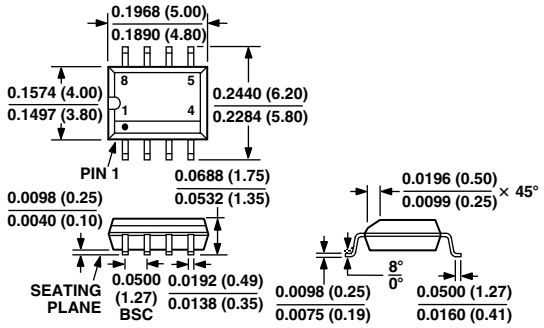
The SPICE model for the AD8631 amplifier is available and can be downloaded from the Analog Devices' web site at **http://www.analog.com**. The macro-model accurately simulates a number of AD8631 parameters, including offset voltage, input common-mode range, and rail-to-rail output swing. The output voltage versus output current characteristics of the macro-model is identical to the actual AD8631 performance, which is a critical feature with a rail-to-rail amplifier model. The model also accurately simulates many ac effects, such as gain-bandwidth product, phase margin, input voltage noise, CMRR and PSRR versus frequency, and transient response. Its high degree of model accuracy makes the AD8631 macro-model one of the most reliable and true-to-life models available for any amplifier.

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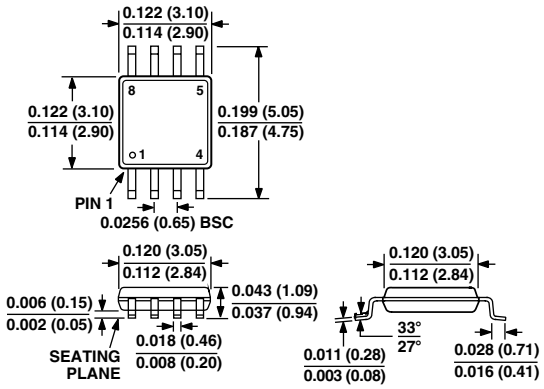
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

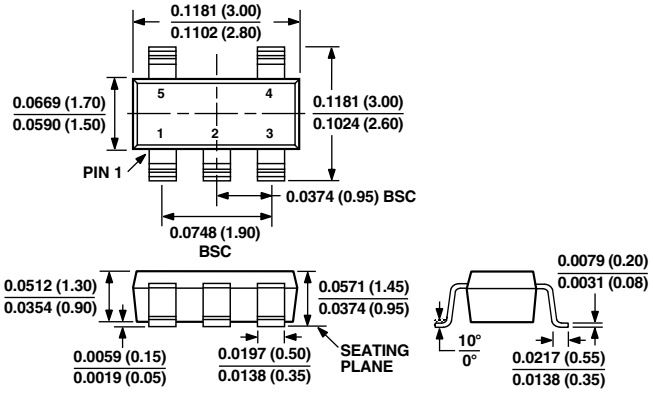
8-Lead Narrow Body SOIC (SO-8)



8-Lead μSOIC (RM-8)



5-Lead SOT-23 (RT-5)



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