AT91SAM9260-EK Evaluation Board

User Guide

Table of Contents

Section 1

Overview

1.1 Scope

The AT91SAM9260-EK evaluation kit enables the evaluation of and code development for applications running on an AT91SAM9260 device.

This guide focuses on the AT91SAM9260-EK board as an evaluation platform.

The board supports the AT91SAM9260 in an LFBGA217 package as well as in a PQFP208 package.

1.2 Deliverables

The AT91SAM9260-EK package contains the following items:

- an AT91SAM9260-EK board
- universal input AC/DC power supply with US and Europe plug adapter
- one A/B-type USB cable
- one serial RS232 cable
- one RJ45 crossed Ethernet cable
- one CD-ROM that allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.

1.3 AT91SAM9260-EK Evaluation Board

The board is equipped with an AT91SAM9260 (217-ball LFBGA package) together with the following:

- 64 Mbytes of SDRAM memory
- 256 Mbytes of NANDFlash memory
- one Atmel serial DataFlash®
- one Atmel TWI serial EEPROM
- one USB device port interface
- two USB Host port interfaces
- one DBGU serial communication port
- one complete MODEM serial communication port

- one additional serial communication port with RTS/CTS handshake control
- JTAG/ICE debug interface
- one PHY Ethernet 100-base TX with three status LEDs
- one Atmel AT73C213 Audio DAC
- one Power LED and one general-purpose LED
- two user input push buttons
- one Wakeup input push button
- one reset push button
- one DataFlash, SD/MMC card slot
- four expansion connectors (PIOA, PIOB, PIOC, IMAGE SENSOR)
- one BGA-like EBI expansion footprint connector
- one Lithium Coin Cell Battery Retainer for 12 mm cell size

Section 2

Setting Up the AT91SAM9260-EK Board

2.1 Electrostatic Warning

The AT91SAM9260-EK evaluation board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

In order to set up the AT91SAM9260-EK evaluation board, the following items are needed:

- the AT91SAM9260-EK evaluation board itself.
- AC/DC power adapter (5V at 2A), 2.1 mm by 5.5 mm

2.3 Layout

Figure 2-1. AT91SAM9260-EK Layout - Top View

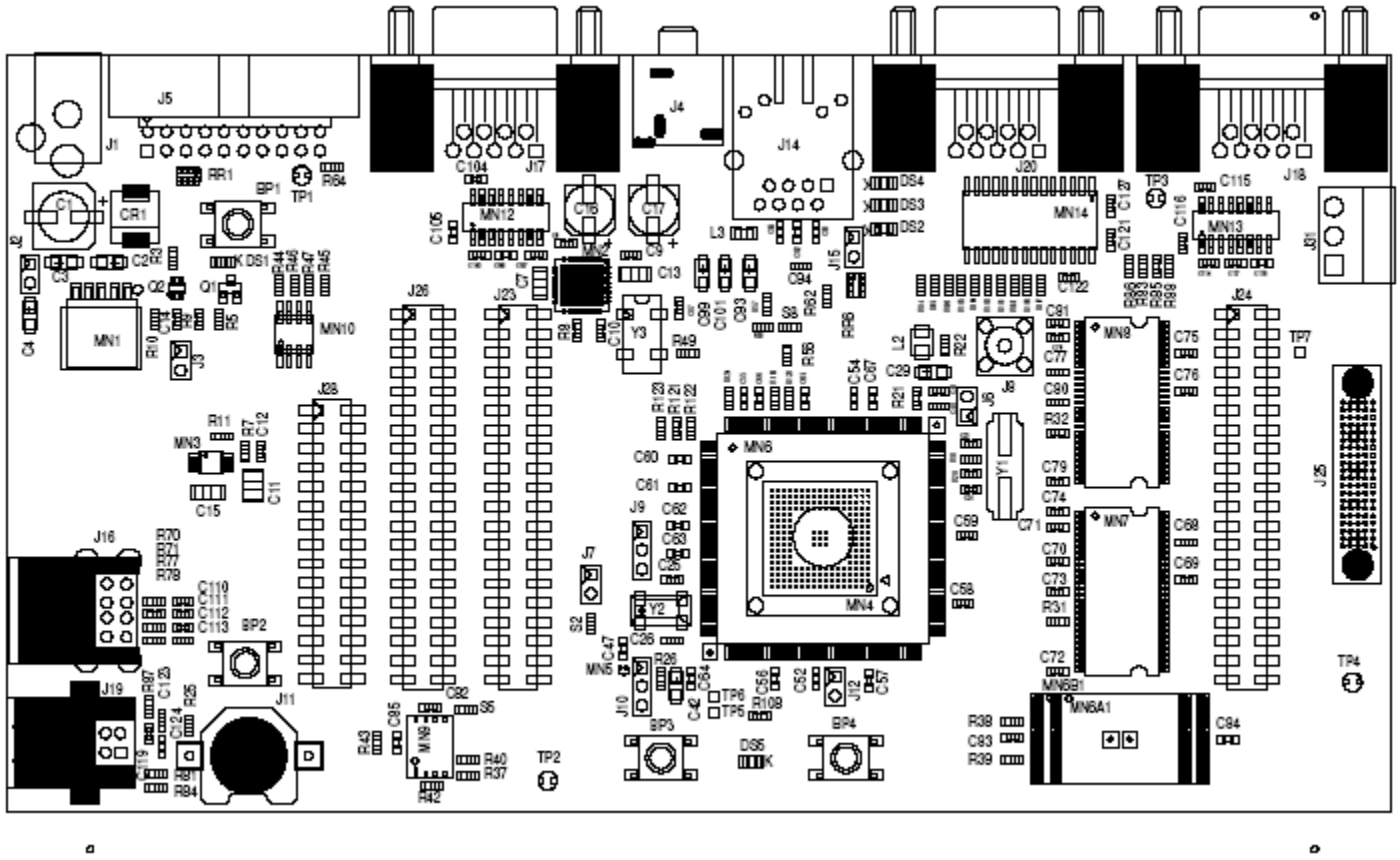
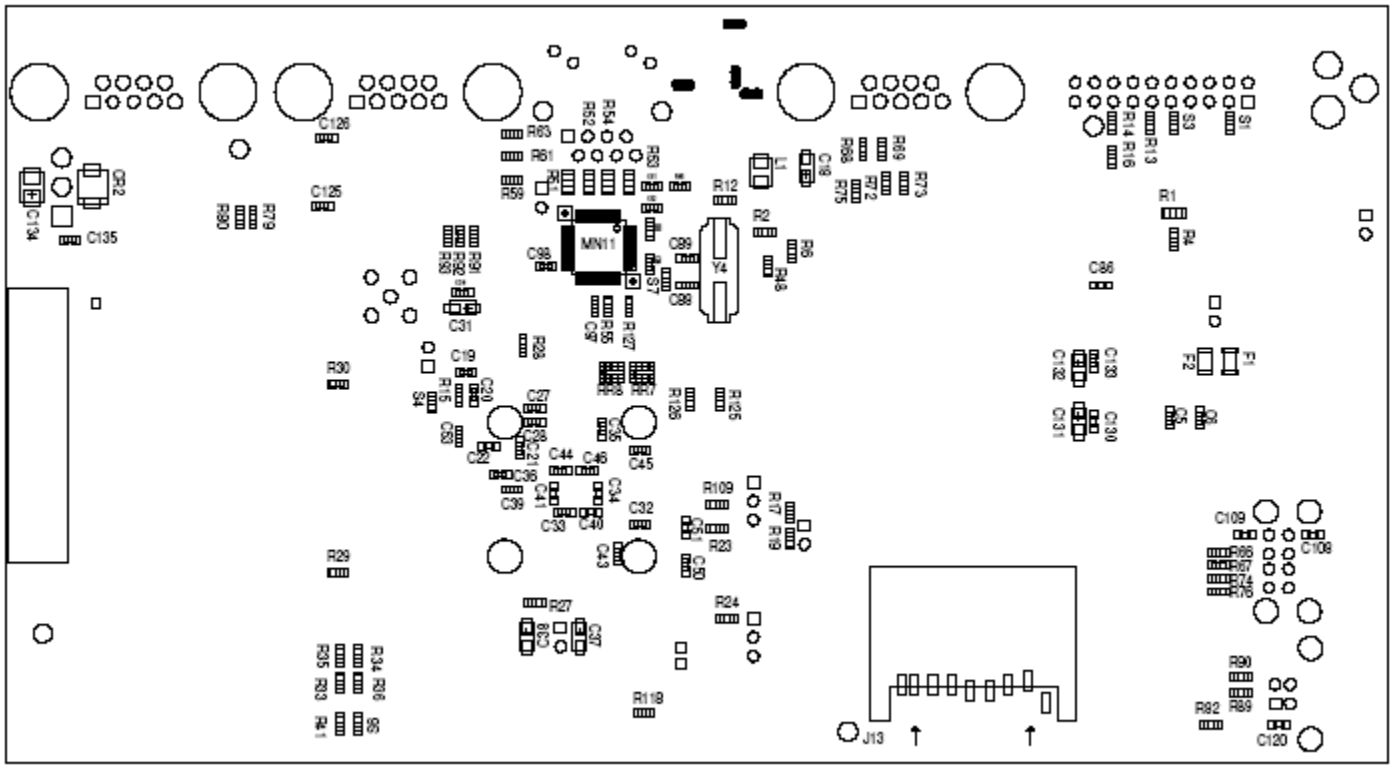


Figure 2-2. AT91SAM9260-EK Layout - Bottom View



2.4 Powering Up the Board

The AT91SAM9260-EK requires 5V DC (±5%). DC power is supplied to the board via the 2.1 mm by 5.5 mm socket J1. Coaxial plug center positive standard.

2.5 Backup Power Supply

The user has the possibility to plug a battery (3V Lithium Battery CR1225 or equivalent) in order to permanently power the backup part of the device. In this case, J10 configuration must be set in position 1, 2.

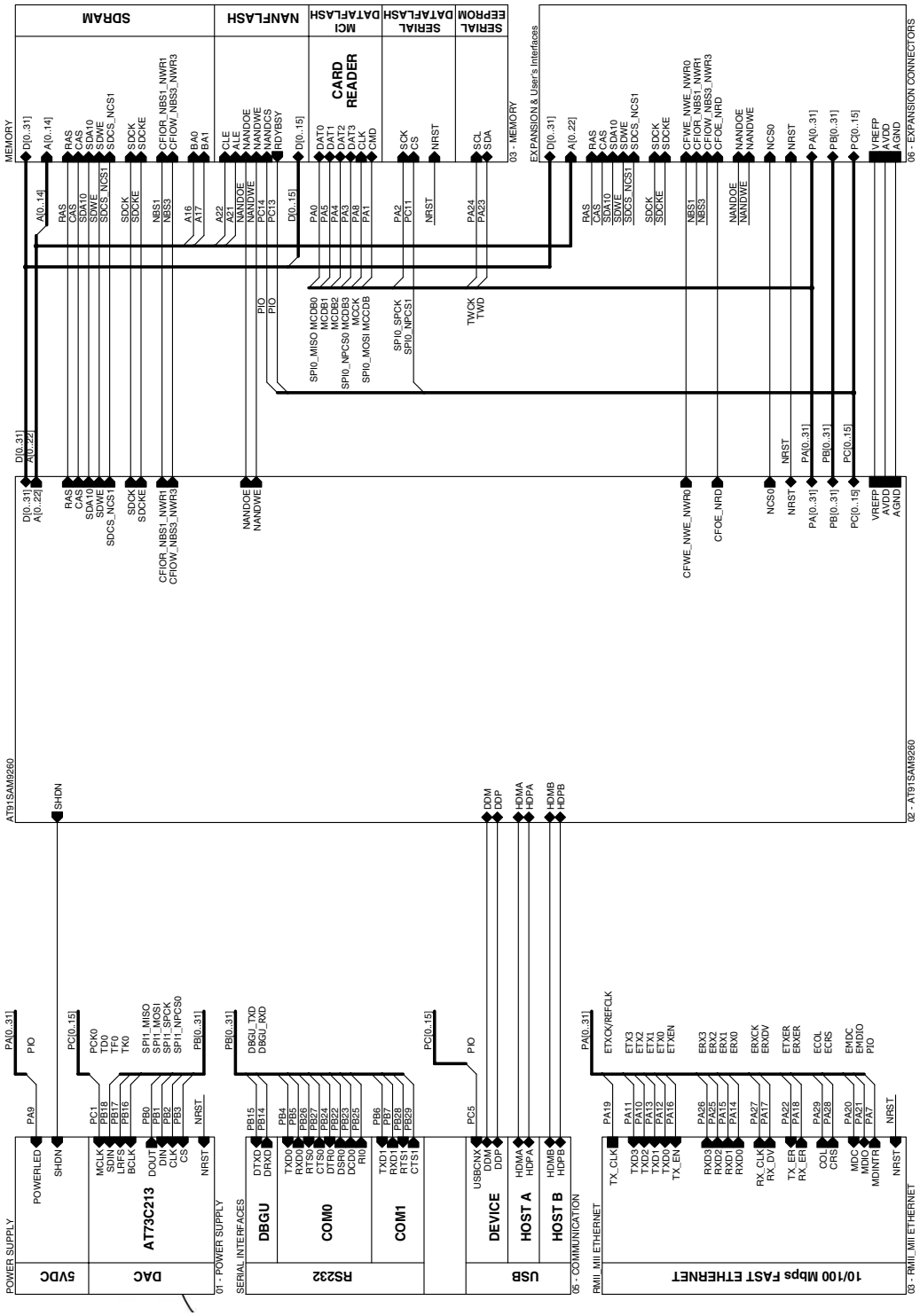
Refer to Section 4.1.

2.6 Getting Started

The AT91SAM9260-EK evaluation board is delivered with a CD-ROM containing all necessary information and step-by-step procedures for working with the most common development toolchains. Please refer to this CD-ROM, or to the AT91 web site, http://www.atmel.com/products/AT91/, for the most up-to-date information on getting started with the AT91SAM9260-EK.

2.7 AT91SAM9260-EK Block Diagram

Figure 2-3. AT91SAM9260-EK Block Diagram



Section 3

Board Description

3.1 AT91SAM9260 Microcontroller

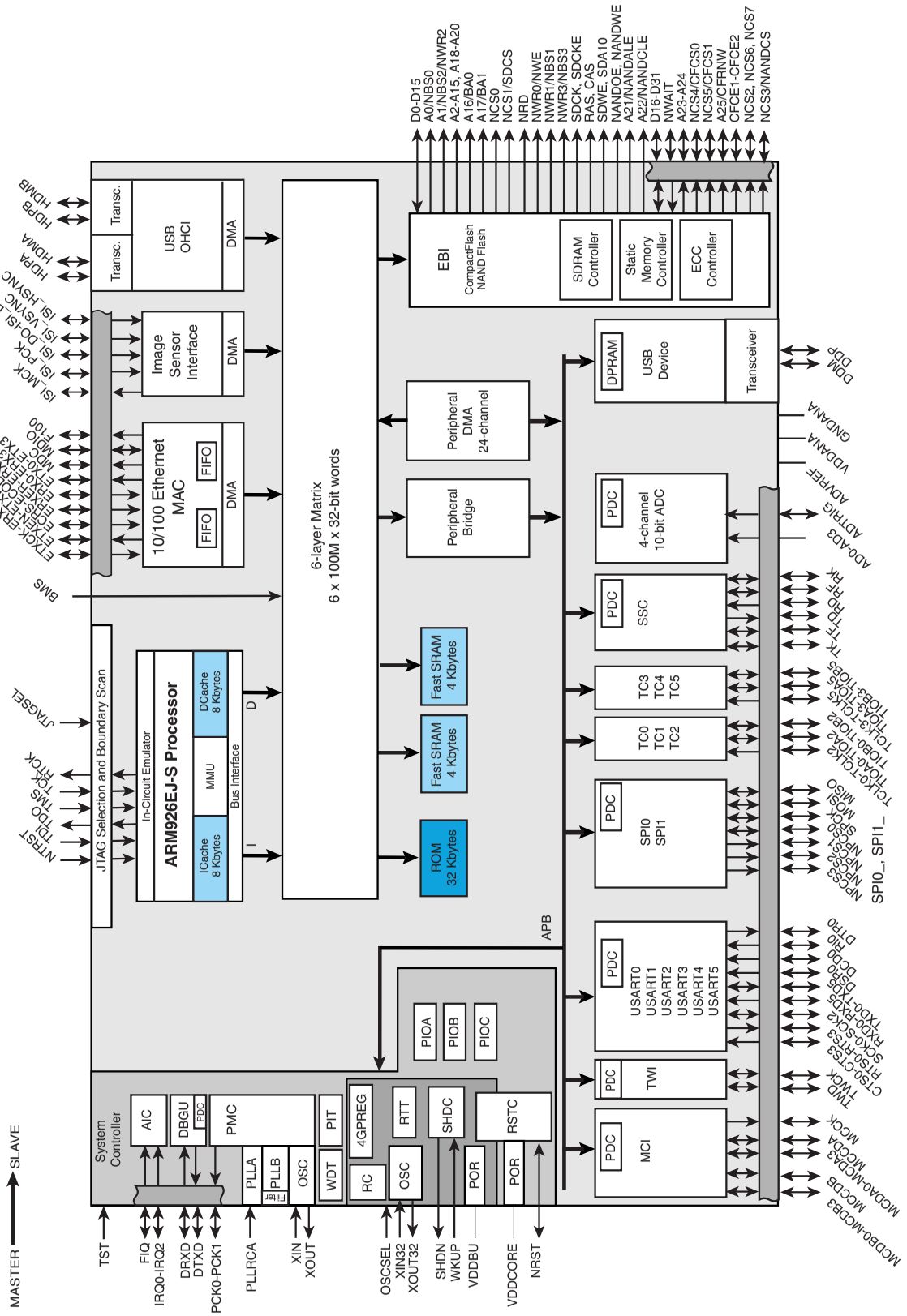
- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP Instruction Extensions, ARM Jazelle® Technology for Java® Acceleration
  - 8-KByte Data Cache, 8-KByte Instruction Cache, Write Buffer
  - 200 MIPS at 180 MHz
  - Memory Management Unit
  - EmbeddedICE™, Debug Communication Channel Support
- Additional Embedded Memories
  - One 32-KByte Internal ROM, Single-cycle Access At Maximum Matrix Speed
  - Two 4-KByte Internal SRAM, Single-cycle Access At Maximum Matrix Speed
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, ECC-enabled NANDFlash and CompactFlash®
- USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 2,432-byte Configurable Integrated DPRAM
- USB 2.0 Full Speed (12 Mbits per second) Host Single Port in the 208-lead PQFP Package and Double Port in 217-ball LFBGA Package
  - Single or Dual On-chip Transceivers
  - Integrated FIFOs and Dedicated DMA Channels
- Ethernet MAC 10/100 Base T
  - Media Independant Interface or Reduced Media Independant Interface
  - 28-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
- Image Sensor Interface
  - ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
  - 12-bit Data Interface for Support of High Sensibility Sensors
  - SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format
- Bus Matrix
  - Six 32-bit-layer Matrix
  - Boot Mode Select Option, Remap Command
- Fully-featured System Controller, including
  - Reset Controller, Shutdown Controller
  - Four 32-bit Battery Backup Registers for a Total of 16 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Real-time Timer
- Reset Controller (RSTC)
  - Based on a Power-on Reset Cell, Reset Source Identification and Reset Output

Control
- Clock Generator (CKGR)
  - Selectable 32768Hz Low-power Oscillator or Internal Low Power RC Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 3 to 20 MHz On-chip Oscillator, One up to 240 MHz PLL and One up to 130 MHz PLL
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Two Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Real-time Timer (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- One 4-channel 10-bit Analog-to-Digital Converter
- Three 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC)
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
  - High-current Drive I/O Lines, Up to 16 mA Each
- Peripheral DMA Controller Channels (PDC)
- One Two-slot MultiMedia Card Interface (MCI)
  - SDCard/SDIO and MultiMediaCard™ Compliant
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
- One Synchronous Serial Controller (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Four Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation, Manchester Encoding/Decoding
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Full Modem Signal Control on USART0
- Two 2-wire UARTs
- Two Master/Slave Serial Peripheral Interfaces (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
  - Synchronous Communications
- Two Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability

  - High-Drive Capability on Ouputs TIOA0, TIOA1, TIOA2
- One Two-wire Interface (TWI)
  - Master, Multi-master and Slave Mode Operation
  - General Call Supported in Slave Mode
  - Connection to PDC Channel To Optimize Data Transfers in Master Mode Only
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
  - 1.65V to 1.95V for VDDBU, VDDCORE, VDDOSC and VDDPLL
  - 3.0V to 3.6V for VDDIOP0, VDDIOP1 (Peripheral I/Os) and VDDANA (Analog to Digital Converter)
  - Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM (Memory I/Os)
- Available in a 208-lead PQFP and 217-ball LFBGA Package

3.2 AT91SAM9260 Block Diagram

Figure 3-1. AT91SAM9260 Block Diagram



3.3 Microcontroller

- One LFBGA 217-ball fitted on board
- One LQFP 208-lead footprint

To try the microcontroller in the LQFP package, the user has to unsolder MN4 and solder the PQFP208 microcontroller on the MN6 footprint.

3.4 Memory

- 32 Kbytes of Internal ROM
- Two 4-KByte Internal SRAM
- Atmel serial DataFlash
- 64 Mbytes of SDRAM memory (32-bit bus width)
- 256 Mbytes of NANDFlash memory (8-bit bus width)
- TWI serial EEPROM

3.5 Clock Circuitry

- 18.432 MHz standard crystal for the embedded oscillator
- Selectable 32768Hz Low-power external standard crystal Oscillator or Internal Low Power RC Oscillator

3.6 Reset Circuitry

- Internal reset controller with bi-directional reset pin
- External reset pushbutton

3.7 Shutdown Controller

- Programmable shutdown and Wake-Up
- Wake-up push button

3.8 Power Supply Circuitry

- On-board 1.8V High Efficiency step-down charge pump regulator with shutdown control
- On-board 3.3V linear regulator with shutdown control

3.9 Remote Communication

- One serial interface (DBGU COM Port) via RS-232 DB9 male socket
- One complete modem serial interface (COM Port 0) via RS-232 DB9 male socket
- One additional serial interface (COM Port 1) with RTS/CTS handshake control via RS-232 DB9 male socket
- USB V2.0 full-speed compliant, 12 Mbits per second (UDP)
- Two(1) USB Host ports V2.0 full-speed compliant, 12 Mbits per second (UHP)
- One Ethernet 100-base TX with three status LEDs

3.10 Audio Stereo Interface

- One Atmel stereo audio DAC (AT73C213)
- One 32 Ohm/20 mW Stereo Headset output (J4) with master volume and mute controls

3.11 User Interface

- Two user input pushbuttons[(2)]
- One user green LED
- One yellow power LED (can be also software controlled)

3.12 Debug Interface

- 20-pin JTAG/ICE interface connector
- DBGU COM port

3.13 Expansion Slot

- One DataFlash, SD/MMC card slot
- All I/Os of the AT91SAM9260 are routed to peripheral extension connectors
- All I/Os of the AT91SAM9260 Image Sensor Interface are routed to peripheral extension connectors
- All EBI Signals of the AT91SAM9260 are routed to extension footprint connectors (J25)

This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.

Notes: 1. Only one available with the 208-lead PQFP package.
2. Not available with the 208-lead PQFP package.

3.14 PIO Usage

Table 3-1. PIO Controller A

I/O Line	Peripheral A	Peripheral B	Comments	Function
PA0	SPI0_MISO	MCDB0		SPI DATAFLASH, SPI/MCI SD/MMC/DATAFLASH Slot
PA1	SPI0_MOSI	MCCDB		(PA0..PA5)
PA2	SPI0_SPCK			
PA3	SPI0_NPCS0	MCDB3		
PA4	RTS2	MCDB2		
PA5	CTS2	MCDB1		
PA6	MCDA0			User LED
PA7	MCCDA			ETHERNET DM9161A MII/RMII (IRQ)
PA8	MCCK			MCI SD/MMC/DATAFLASH Slot
PA9	MCDA1			Power LED
PA10	MCDA2	ETX2		ETHERNET DM9161A MII Interface (PA10..PA11)
PA11	MCDA3	ETX3		
PA12	ETX0			ETHERNET DM9161A RMII Interface (PA12..PA19)
PA13	ETX1			
PA14	ERX0			
PA15	ERX1			
PA16	ETXEN			
PA17	ERXDV			
PA18	ERXER			
PA19	ETXCK			
PA20	EMDC			ETHERNET DM9161A MII/RMII Interface (PA20..PA21)
PA21	EMDIO			
PA22	ADTRG	ETXER		ETHERNET DM9161A MII Interface
PA23	TWD	ETX2		SERIAL EEPROM (SDA)
PA24	TWCK	ETX3		SERIAL EEPROM (SCL)
PA25	TCLK0	ERX2		ETHERNET DM9161A MII Interface (PA25..PA29)
PA26	TIOA0	ERX3	High-Drive	
PA27	TIOA1	ERXCK	High-Drive	
PA28	TIOA2	ECRS	High-Drive	
PA29	SCK1	ECOL		
PA30	SCK2	RXD4		(BP3) User's interface Push Button
PA31	SCK0	TXD4		(BP4) User's interface Push Button

Table 3-2. PIO B Controller

I/O Line	Peripheral A	Peripheral B	Comments	Function
PB0	SPI1_MISO	TIOA3		Audio DAC AT73C213 (MISO)
PB1	SPI1_MOSI	TIOB3		Audio DAC AT73C213 (MOSI)
PB2	SPI1_SPCK	TIOA4		Audio DAC AT73C213 (SPCK)
PB3	SPI1_NPCS0	TIOA5		Audio DAC AT73C213 (Chip Select)
PB4	TXD0			COM PORT 0 (TXD)
PB5	RXD0			COM PORT 0 (RXD)
PB6	TXD1	TCLK1		COM PORT 1 (TXD)
PB7	RXD1	TCLK2		COM PORT 1 (RXD)
PB8	TXD2			
PB9	RXD2			
PB10	TXD3	ISI_D8		(J28) IMAGE SENSOR CONNECTOR (PB10..PB13)
PB11	RXD3	ISI_D9		
PB12	TXD5	ISI_D10		
PB13	RXD5	ISI_D11		
PB14	DRXD			SERIAL DEBUG PORT(RXD)
PB15	DTXD			SERIAL DEBUG PORT(TXD)
PB16	TK0	TCLK3		Audio DAC AT73C213 (BCLK)
PB17	TF0	TCLk4		Audio DAC AT73C213 (LRFS)
PB18	TD0	TIOB4		Audio DAC AT73C213 (SDIN)
PB19	RD0	TIOB5		(J28) IMAGE SENSOR CONNECTOR (CTRL2)
PB20	RK0	ISI_D0		(J28) IMAGE SENSOR CONNECTOR (PB20..PB31)
PB21	RF0	ISI_D1		
PB22	DSR0	ISI_D2		**Warning: Shared with COM PORT 0 (PB22..PB27)**
PB23	DCD0	ISI_D3		
PB24	DTR0	ISI_D4		
PB25	RI0	ISI_D5		
PB26	RTS0	ISI_D6		
PB27	CTS0	ISI_D7		
PB28	RTS1	ISI_PCK		**Warning: Shared with COM PORT 1 (PB28..PB29)**
PB29	CTS1	ISI_VSYNC		
PB30	PCK0	ISI_HSYNC		
PB31	PCK1	ISI_MCK		

Table 3-3. PIO C Controller

I/O Line	Peripheral A	Peripheral B	Comments	Function
PC0	AD0	SCK3		
PC1	AD1	PCK0		Audio DAC AT73C213 (MCLK)
PC2	AD2	PCK1		
PC3	AD3	SPI1_NPCS3		
PC4	A23	SPI1_NPCS2		(J28) IMAGE SENSOR CONNECTOR (CTRL1)
PC5	A24	SPI1_NPCS1		USB_CNX (VBUS DETECT)
PC6	TIOB2	CFCE1		
PC7	TIOB1	CFCE2		
PC8	NCS4/CFCS0	RTS3		
PC9	NCS5/CFCS1	TIOB0		
PC10	A25/CFRNW	CTS3		
PC11	NCS2	SPI0_NPCS1		SPI DATAFLASH memory (Chip Select)
PC12	IRQ0	NCS7		
PC13	FIQ	NCS6		NandFlash (RDYBSY)
PC14	NCS3/NANDCS	IRQ2		NandFlash (NANDCS)
PC15	NWAIT	IRQ1		
PC16	D16	SPI0_NPCS2		EBI Data Bus (PC16..PC31)
PC17	D17	SPI0_NPCS3		
PC18	D18	SPI1_NPCS1		
PC19	D19	SPI1_NPCS2		
PC20	D20	SPI1_NPCS3		
PC21	D21	EF100		
PC22	D22	TCLK5		
PC23	D23			
PC24	D24			
PC25	D25			
PC26	D26			
PC27	D27			
PC28	D28			
PC29	D29			
PC30	D30			
PC31	D31			

Section 4
Configuration

4.1 Jumpers

Table 4-1. Jumpers Configuration

Designation	Default Setting	Feature
JP2	Closed	3.3V Jumper(1)
JP3	Closed	Forces power on. To use the software shutdown control, J3 must be opened. 3V battery backup must be present and J10 jumper set in position 1-2
JP6	Closed	VDDPLL Jumper(1)
JP7	Opened	Enables boot on the internal ROM
	Closed	Enables boot on the NCS0
JP9	2 - 3	Slow Clock OSCSEL 1-2: Internal RC Oscillator 2-3: External Crystal Oscillator
JP10	2 - 3	VDDBU Jumper select (1) 1-2: Lithium 3V Battery 2-3: 1.8V from VDDCORE
JP12	Closed	VDDCORE Jumper(1)
JP15	Closed	Enables Ethernet Auto MDIX control

Note: 1. These jumpers are provided for power consumption measurement use. By default, they are closed. To use this feature, the user has to open the strap and insert an anmeter.

4.2 JTAG/ICE

Table 4-2. JTAG/ICE Configuration

Designation	Default Setting	Feature
S1	Opened	Disables the ICE NTRST input
S2	Opened	Selects ICE mode or JTAG mode (See Errata)
S3	Opened	Disables TCK <-> RTCK local loop. If S3 is closed, R13 must be unsoldered.
R13	Soldered	Enables the ICE RTCK return. S3 must be opened
R14	Soldered	Enables the ICE NRST input

4.3 Microcontroller Clock

Table 4-3. Microcontroller Clock Configuration

Designation	Default Setting	Feature
R18/R20	Soldered	Enables the use of 18.432MHz crystal. If external clock used, R18/R20 must be unsoldered and S4 closed.
S4	Opened	
J9		Slow Clock Setting. See Table 4-1.

4.4 Memory

Table 4-4. Memory Configuration

Designation	Default Setting	Feature
SDRAM		
R31 R32	Soldered Soldered	Enables MN7 Chip select access Enables MN8 Chip select access
NANDFlash (MN6x)		
R36 R34 S6	Soldered Soldered Opened	Enables the use of NANDFlash (MN6x) Enables the use of Ready Busy signalDisables write protect
SERIAL DATAFLASH (MN9)		
R40 S5	Soldered Opened	Enable the use of the Serial DataFlash (MN9) Disables the write protect.
TWI SERIAL EEPROM (MN10)		
R46 R47	Soldered Soldered	Enables SCL access Enables SDA access

4.5 Ethernet

RMII is the factory default mode.

To evaluate the MII mode, the user has to unsolder R49, R50, R127 and close S7 and S8.

When the RMII mode is used, the user can use the specific MII signals as PIO, but the following resistors must be unsoldered (R119 to R126).

4.6 Miscellaneous

Refer to the TOP level schematic for the PIO usage.

Table 4-5.

Designation	Default Setting	Feature
R82	Soldered	USB DEVICE: Enables the use of the USBCNX signal
R72 R73	Soldered Soldered	DBGU COM Port: Enables the use of DTXD output signalEnables the use of DRXD input
		RS232 COM Port 0: Enable the use of outputs signal
R94 R95 R96	Soldered	RTS0 TXD0 DTR0
		RS232 COM Port 0: Enable the use of inputs signal
R98 R101 R103 R104 R105 R106	Soldered	DCD0 DSR0 RXD0 CTS0 RI0 Enables all MAX3241E outputs buffer
		RS232 COM Port 1: Enable the use of outputs signal
R83 R85	Soldered	TXD1 RTS1
		RS232 COM Port 1: Enable the use of inputs signal
R86 R88	Soldered	RXD1 CTS1
TP1	N.A	GND Test point
TP2	N.A	GND Test point.
TP3	N.A	GND Test point.
TP4	N.A	GND Test point.
TP5	N.A	Reserved: do not use
TP6	N.A	Reserved: do not use

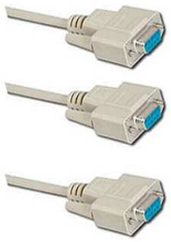
Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

- Board Layout - Top View
- Power supply and audio
- 217-ball BGA AT91SAM9260 Microcontroller
- 208-pin LQFP AT91SAM9260 Microcontroller
- Memory
- Ethernet
- Serial Interface
- Expansion and User Interface



POWER SUPPLY

5VDC
- POWERLED ← PA9 ← PA[0..31] (PIO)
- SHDN → SHDN

DAC — AT73C213
- MCLK ← PC1 ← PC[0..15] (PCK0)
- SDIN ← PB18 (TD0)
- LRFS ← PB17 (TF0)
- BCLK ← PB16 (TK0)
- DOUT → PB0 (SPI1_MISO)
- DIN ← PB1 (SPI1_MOSI)
- CLK ← PB2 (SPI1_SPCK)
- CS ← PB3 (SPI1_NPCS0)
- NRST ← NRST ← PB[0..31]

01 - POWER SUPPLY

SERIAL INTERFACES

RS232
- DBGU: DTXD ← PB15 (DBGU_TXD); DRXD → PB14 (DBGU_RXD)
- COM0: TXD0 ← PB4; RXD0 → PB5; RTS0 ← PB26; CTS0 → PB27; DTR0 ← PB24; DSR0 → PB22; DCD0 → PB23; RI0 → PB25
- COM1: TXD1 ← PB6; RXD1 → PB7; RTS1 ← PB28; CTS1 → PB29

USB
- DEVICE: USBCNX ← PC5 ← PC[0..15] (PIO); DDM ↔ DDM; DDP ↔ DDP
- HOST A: HDMA ↔ HDMA; HDPA ↔ HDPA
- HOST B: HDMB ↔ HDMB; HDPB ↔ HDPB

05 - COMMUNICATION

RMII_MII ETHERNET

10/100 Mbps FAST ETHERNET
- TX_CLK ← PA19 (ETXCK/REFCLK)
- TXD3 ← PA11 (ETX3); TXD2 ← PA10 (ETX2); TXD1 ← PA13 (ETX1); TXD0 ← PA12 (ETX0); TX_EN ← PA16 (ETXEN)
- RXD3 → PA26 (ERX3); RXD2 → PA25 (ERX2); RXD1 → PA15 (ERX1); RXD0 → PA14 (ERX0)
- RX_CLK → PA27 (ERXCK); RX_DV → PA17 (ERXDV)
- TX_ER ← PA22 (ETXER); RX_ER → PA18 (ERXER)
- COL → PA29 (ECOL); CRS → PA28 (ECRS)
- MDC ← PA20 (EMDC); MDIO ↔ PA21 (EMDIO); MDINTR → PA7 (PIO)
- NRST ← NRST

03 - RMII_MII ETHERNET

AT91SAM9260

SHDN ← SHDN

DDM ↔ DDM; DDP ↔ DDP

HDMA ↔ HDMA; HDPA ↔ HDPA

HDMB ↔ HDMB; HDPB ↔ HDPB

D[0..31]; A[0..22]

RAS; CAS; SDA10; SDWE; SDCS_NCS1

SDCK; SDCKE

CFIOR_NBS1_NWR1; CFIOW_NBS3_NWR3

NANDOE; NANDWE

PIO; PIO

CFWE_NWE_NWR0

CFOE_NRD

NCS0

NRST ← NRST

PA[0..31] ↔ PA[0..31]

PB[0..31] ↔ PB[0..31]

PC[0..31] ↔ PC[0..15]

VREFP; AVDD; AGND

02 - AT91SAM9260

MEMORY

SDRAM
- D[0..31]; A[0..14]
- RAS; CAS; SDA10; SDWE; SDCS_NCS1
- SDCK; SDCKE
- NBS1; NBS3
- A16; A17 → BA0; BA1

NANFLASH
- A22; A21 → CLE; ALE
- NANDOE; NANDWE
- PIO; PIO → PC14; PC13 → NANDCS; RDYBSY
- D[0..15]

CARD READER — MCI DATAFLASH
- SPI0_MISO MCDB0 → PA0 → DAT0
- MCDB1 → PA5 → DAT1
- MCDB2 → PA4 → DAT2
- SPI0_NPCS0 MCDB3 → PA3 → DAT3
- MCCK → PA8 → CLK
- SPI0_MOSI MCCDB → PA1 → CMD

SERIAL DATAFLASH
- SPI0_SPCK → PA2 → SCK
- SPI0_NPCS1 → PC11 → CS
- NRST

SERIAL EEPROM
- TWCK → PA24 → SCL
- TWD → PA23 → SDA

03 - MEMORY

EXPANSION & User's Interfaces
- D[0..31]; A[0..22]
- RAS; CAS; SDA10; SDWE; SDCS_NCS1
- SDCK; SDCKE
- CFWE_NWE_NWR0; CFIOR_NBS1_NWR1; CFIOW_NBS3_NWR3; CFOE_NRD
- NANDOE; NANDWE
- NCS0
- NRST
- PA[0..31]; PB[0..31]; PC[0..15]
- VREFP; AVDD; AGND

06 - EXPANSION CONNECTORS

REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	28/08/06		
A	INIT EDIT	JPG	17/10/05		

ATMEL ROUSSET

AT91SAM9260-EK

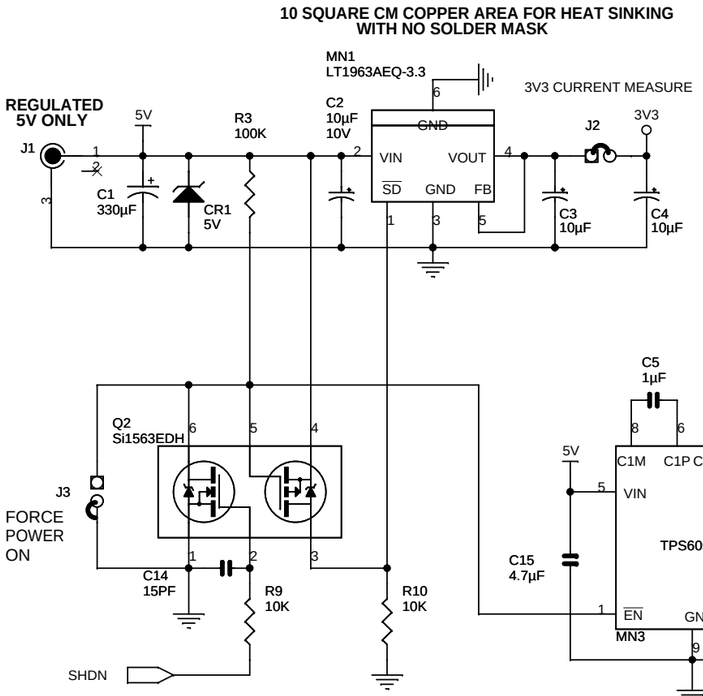
DIAGRAM

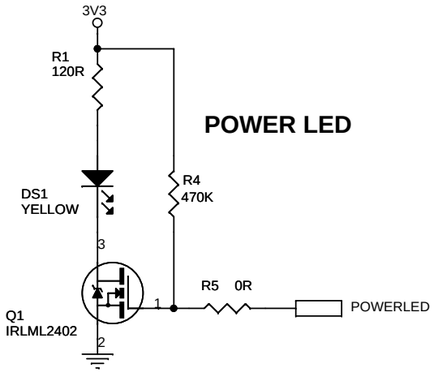
SCALE 1/1

REV. B

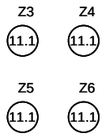
SHEET 1/8

10 SQUARE CM COPPER AREA FOR HEAT SINKING
WITH NO SOLDER MASK

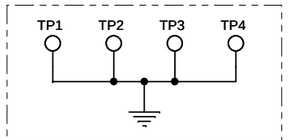




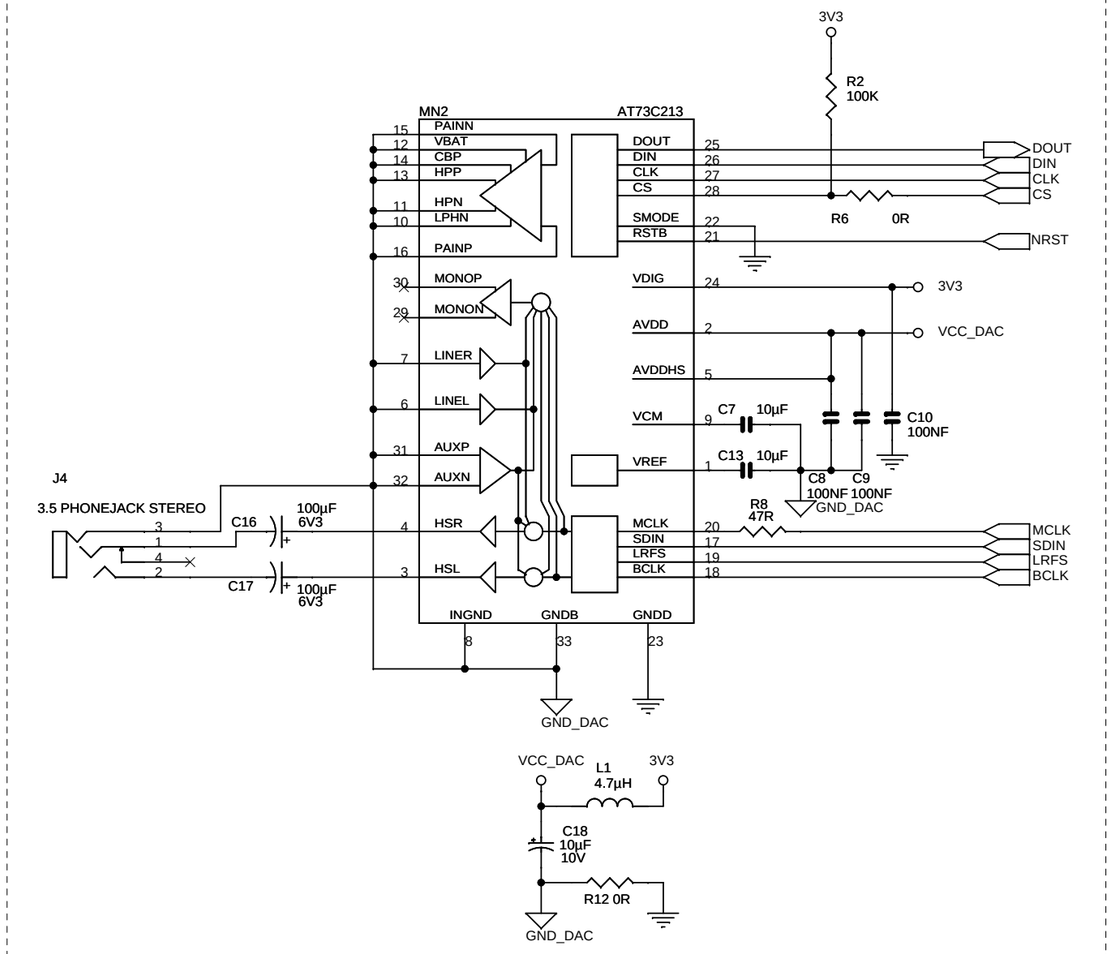
ADHESIVE FEET



GND TEST POINT



AUDIO DAC INTERFACE



REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	28/08/06		
A	INIT EDIT	JPG	17/10/05		

ATMEL ROUSSET

AT91SAM9260-EK

POWER SUPPLY & AUDIO

SCALE 1/1

REV. B

SHEET 2/8

AT91SAM9260

PC[0..15]
PB[0..31]
PA[0..31]
D[0..31]
A[0..22]

TO PQFP208 FOOTPRINT

TDI
TMS
TCK
RTCK
TDO
NTRST
JTAGSEL
PLLRCA
VDDPLL
XOUT
XIN
XOUT32
XIN32
OSCSEL
VDDBU
WKUP
TST
BMS
VREFP
AVDD
AGND
VDDCORE
VDDIOM
VDDHISI

MN4

PA0/SPI0_MISO/MCDB0
PA1/SPI0_MOSI/MCCDB
PA2/SPI0_SPCK
PA3/SPI0_NPCS0/MCDB3
PA4/RTS2/MCDB2
PA5/CTS2/MCDB1
PA6/MCDA0
PA7/MCCDA
PA8/MCCK
PA9/MCDA1
PA10/MCDA2/ETX2
PA11/MCDA3/ETX3
PA12/ETX0
PA13/ETX1
PA14/ERX0
PA15/ERX1
PA16/ETXEN
PA17/ERXDV
PA18/ERXER
PA19/ETXCK
PA20/EMDC
PA21/EMDIO
PA22/ADTRG/ETXER
PA23/TWD/ETX2
PA24/TWCK/ETX3
PA25/TCLK0/ERX2
PA26/TIOA0/ERX3
PA27/TIOA1/ERXCK
PA28/TIOA2/ECRS
PA29/SCK1/ECOL
PA30/SCK2/RXD4
PA31/SCK0/TXD4

TIOA3/SPI1_MISO/PB0
TIOB3/SPI1_MOSI/PB1
TIOA4/SPI1_SPCK/PB2
TIOA5/SPI1_NPCS0/PB3
TXD0/PB4
RXD0/PB5
TCLK1/TXD1/PB6
TCLK2/RXD1/PB7
TXD2/PB8
RXD2/PB9
ISI_D8/TXD3/PB10
ISI_D9/RXD3/PB11
ISI_D10/TXD5/PB12
ISI_D11/RXD5/PB13
DRXD/PB14
DTXD/PB15
TCLK3/TK0/PB16
TCLK4/TF0/PB17
TIOB4/TD0/PB18
TIOB5/RD0/PB19
ISI_D0/RK0/PB20
ISI_D1/RF0/PB21
ISI_D2/DSR0/PB22
ISI_D3/DCD0/PB23
ISI_D4/DTR0/PB24
ISI_D5/RI0/PB25
ISI_D6/RTS0/PB26
ISI_D7/CTS0/PB27
ISI_PCK/RTS1/PB28
ISI_VSYNC/CTS1/PB29
ISI_HSYNC/PCK0/PB30
ISI_MCK/PCK1/PB31

SCK3/AD0/PC0
PCK0/AD1/PC1
PCK1/AD2/PC2
SPI1_NPCS3/AD3/PC3
SPI1_NPCS2/A23/PC4
SPI1_NPCS1/A24/PC5
CFCE1/TIOB2/PC6
CFCE2/TIOB1/PC7
RTS3/NCS4_CFCS0/PC8
TIOB0/NCS5_CFCS1/PC9
CTS3/A25_CFRNW/PC10
SPI0_NPCS1/NCS2/PC11
NCS7/IRQ0/PC12
NCS6/FIQ/PC13
IRQ2/NCS3_NANDCS/PC14
IRQ1/NWAIT/PC15
SPI0_NPCS2/D16/PC16
SPI0_NPCS3/D17/PC17
SPI1_NPCS1/D18/PC18
SPI1_NPCS2/D19/PC19
SPI1_NPCS3/D20/PC20
EF100/D21/PC21
TCLK5/D22/PC22
D23/PC23
D24/PC24
D25/PC25
D26/PC26
D27/PC27
D28/PC28
D29/PC29
D30/PC30
D31/PC31

N.C
TP5
TP6

D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15

NBS0/A0
NWR2/NBS2/A1
A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22

RAS
CAS
SDWE
SDA10
SDCKE
SDCK
SDCS/NCS1
NCS0
CFOE/NRD
CFWE/NWE/NWR0
CFIOR/NBS1/NWR1
CFIOW/NBS3/NWR3
NANDOE
NANDWE
NRST
BMS
TST
ADVREF
VDDANA
GNDANA

3V3
RR1 100K
ICE INTERFACE
J5
ICE_NTRST
ICE_RTCK
ICE_NRST
NRST
R13 0R
R14 0R
S1
S2
S3
TDI
TMS
TCK
RTCK
TDO
JTAGSEL
NTRST
R1
N.C

C19 10NF
C20 1NF
R15 1K
PLLRCA
C21 100NF
C22 100NF
J6
1V8
VDDPLL
C23 10PF
C24 10PF
C25 10PF
C26 10PF
R18 0R
R20 0R
Y1 18.432MHz
Y2 32.768 kHz
S4
XOUT
XIN
XOUT32
XIN32
SMB MALE
J8
NOT POPULATED
OSCSEL

DDP
DDM
HDPA
HDMA
HDPB
HDMB

R16 1K
BP1
RESET

BOOT MODE SELECT
OPENED : EMBEDDED ROM
CLOSED : EBI_NCS0
R17 100K
J7
R19 1K

VREFP
AVDD
R21 0R
L2 4.7µH
C28 100NF
C29 10µF 10V
C30 100NF
C31 10µF 10V
R22 0R
C27 100NF
AGND

MN5
R1100D181C
J9
R23 10K
J10
R24
NOT POPULATED
VDDBU
Z11
J11
CR1225
R25 1K
C47 100NF
WAKE UP
BP2
WKUP
SHDN
R26 100K

WKUP SHDN VDDBU GNDBU VDDCORE VDDIOM VDDIOP0 VDDIOP1

C32 100NF
C33 100NF
C34 100NF
C35 100NF
C36 100NF
C37 10µF
J12
1V8
VDDCORE CURRENT MEASURE

R27 0R
C38 10µF
C39 100NF
C40 100NF
C41 100NF
C42 10µF 10V
C43 100NF
C44 100NF
C45 100NF
C46 100NF
R28 0R

ATMEL ROUSSET
AT91SAM9260-EK
AT91SAM9260-BGA217

REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	28/08/06		
A	INIT EDIT	JPG	17/10/05		

SCALE 1/1
REV. B
SHEET 3/8

AT91SAM9260

MN6

PC[0..15]
PB[0..31]
PA[0..31]

D[0..31]
A[0..22]

PA0	179	PA0/SPI0_MISO/MCDB0
PA1	180	PA1/SPI0_MOSI/MCCDB
PA2	181	PA2/SPI0_SPCK
PA3	182	PA3/SPI0_NPCS0/MCDB3
PA4	183	PA4/RTS2/MCDB2
PA5	184	PA5/CTS2/MCDB1
PA6	185	PA6/MCDA0
PA7	186	PA7/MCCDA
PA8	189	PA8/MCCK
PA9	190	PA9/MCDA1
PA10	191	PA10/MCDA2/ETX2
PA11	192	PA11/MCDA3/ETX3
PA12	193	PA12/ETX0
PA13	194	PA13/ETX1
PA14	195	PA14/ERX0
PA15	196	PA15/ERX1
PA16	197	PA16/ETXEN
PA17	198	PA17/ERXDV
PA18	201	PA18/ERXER
PA19	202	PA19/ETXCK
PA20	205	PA20/EMDC
PA21	206	PA21/EMDIO
PA22	207	PA22/ADTRG/ETXER
PA23	208	PA23/TWD/ETX2
PA24	1	PA24/TWCK/ETX3
PA25	2	PA25/TCLK0/ERX2
PA26	3	PA26/TIOA0/ERX3
PA27	4	PA27/TIOA1/ERXCK
PA28	7	PA28/TIOA2/ECRS
PA29	8	PA29/SCK1/ECOL

PB0	9	TIOA3/SPI1_MISO/PB0
PB1	10	TIOB3/SPI1_MOSI/PB1
PB2	11	TIOA4/SPI1_SPCK/PB2
PB3	12	TIOA5/SPI1_NPCS0/PB3
PB4	15	TXD0/PB4
PB5	16	RXD0//PB5
PB6	17	TCLK1/TXD1/PB6
PB7	18	TCLK2/RXD1/PB7
PB8	19	TXD2/PB8
PB9	20	RXD2/PB9
PB10	161	ISI_D8/TXD3/PB10
PB11	162	ISI_D9/RXD3/PB11
PB14	21	DRXD/PB14
PB15	22	DTXD/PB15
PB16	23	TCLK3/TK0/PB16
PB17	26	TCLK4/TF0/PB17
PB18	27	TIOB4/TD0/PB18
PB19	28	TIOB5/RD0/PB19
PB20	163	ISI_D0/RK0/PB20
PB21	164	ISI_D1/RF0/PB21
PB22	165	ISI_D2/DSR0/PB22
PB23	166	ISI_D3/DCD0/PB23
PB24	167	ISI_D4/DTR0/PB24
PB25	168	ISI_D5/RI0/PB25
PB26	171	ISI_D6/RTS0/PB26
PB27	172	ISI_D7/CTS0/PB27
PB28	175	ISI_PCK/RTS1/PB28
PB29	176	ISI_VSYNC/CTS1/PB29
PB30	177	ISI_HSYNC/PCK0/PB30
PB31	178	ISI_MCK/PCK1/PB31
PC0	158	SCK3/AD0/PC0
PC1	159	PCK0/AD1/PC1
PC4	62	SPI1_NPCS2/A23/PC4
PC5	67	SPI1_NPCS1/A24/PC5
PC6	63	CFCE1/TIOB2/PC6
PC7	64	CFCE2/TIOB1/PC7
PC8	61	RTS3/NCS4_CFCS0/PC8
PC9	60	TIOB0/NCS5_CFCS1/PC9
PC10	58	CTS3/A25_CFRNW/PC10
PC11	57	SPI0_NPCS1/NCS2/PC11
PC13	56	NCS6/FIQ/PC13
PC14	59	IRQ2/NCS3_NANDCS/PC14
PC15	127	IRQ1/NWAIT/PC15
D16	128	SPI0_NPCS2/D16/PC16
D17	129	SPI0_NPCS3/D17/PC17
D18	130	SPI1_NPCS1/D18/PC18
D19	131	SPI1_NPCS2/D19/PC19
D20	134	SPI1_NPCS3/D20/PC20
D21	135	EF100/D21/PC21
D22	136	TCLK5/D22/PC22
D23	137	D23/PC23
D24	138	D24/PC24
D25	139	D25/PC25
D26	140	D26/PC26
D27	141	D27/PC27
D28	142	D28/PC28
D29	143	D29/PC29
D30	144	D30/PC30
D31	145	D31/PC31

D0	106	D0
D1	107	D1
D2	108	D2
D3	109	D3
D4	110	D4
D5	111	D5
D6	112	D6
D7	118	D7
D8	119	D8
D9	120	D9
D10	121	D10
D11	122	D11
D12	123	D12
D13	124	D13
D14	125	D14
D15	126	D15

NBS0/A0	99	A0
NWR2/NBS2/A1	98	A1
A2	97	A2
A3	96	A3
A4	95	A4
A5	94	A5
A6	93	A6
A7	92	A7
A8	89	A8
A9	88	A9
A10	87	A10
A11	86	A11
A12	85	A12
A13	84	A13
A14	83	A14
A15	82	A15
BA0/A16	81	A16
BA1/A17	80	A17
A18	79	A18
A19	76	A19
A20	75	A20
A21	74	A21
A22	73	A22

DDP	55	DDP
DDM	54	DDM
HDPA	51	HDPA
HDMA	50	HDMA
TDI	30	TDI
TMS	31	TMS
TCK	34	TCK
RTCK	37	RTCK
TDO	29	TDO
JTAGSEL	43	JTAGSEL
NTRST	35	NTRST
	152	N.C
PLLRCA	154	PLLRCA
VDDPLL	148	VDDPLL
	151	GNDPLL
	155	VDDPLL
	153	GNDPLL
XOUT	150	XOUT
XIN	149	XIN
XOUT32	45	XOUT32
XIN32	46	XIN32
OSCSEL	41	OSCSEL
WKUP	48	WKUP
SHDN	49	SHDN
VDDBU	47	VDDBU
	44	GNDBU
	38, 77, 147, 174, 203	VDDCORE
	6, 14, 25, 33, 39, 53, 66, 78, 91, 113, 133, 146, 170, 173, 188, 200, 204	GND
	65, 90, 114, 132	VDDIOM
	5, 13, 24, 32, 52, 187, 199	VDDIOP0
	169	VDDIOP1

RAS	105	RAS
CAS	104	CAS
SDWE	116	SDWE
SDA10	100	SDA10
SDCKE	117	SDCKE
SDCK	115	SDCK
SDCS/NCS1	103	SDCS_NCS1
NCS0	68	NCS0
CFOE/NRD	69	CFOE_NRD
CFWE/NWE/NWR0	70	CFWE_NWE_NWR0
CFIOR/NBS1/NWR1	102	CFIOR_NBS1_NWR1
CFIOW/NBS3/NWR3	101	CFIOW_NBS3_NWR3
NANDOE	71	NANDOE
NANDWE	72	NANDWE
NRST	36	NRST
BMS	40	BMS
TST	42	TST
ADVREF	157	VREFP
VDDANA	160	AVDD
GNDANA	156	AGND

3V3

C48 100NF
C49 100NF
C50 100NF
C51 100NF
C52 100NF
C53 100NF
C54 100NF
C55 100NF
C56 100NF
C57 100NF
C58 100NF
C59 100NF
C60 100NF
C61 100NF
C62 100NF
C63 100NF
C64 100NF
C65 100NF
C66 100NF
C67 100NF

ATMEL ROUSSET

AT91SAM9260-EK
AT91SAM9260-LQFP208

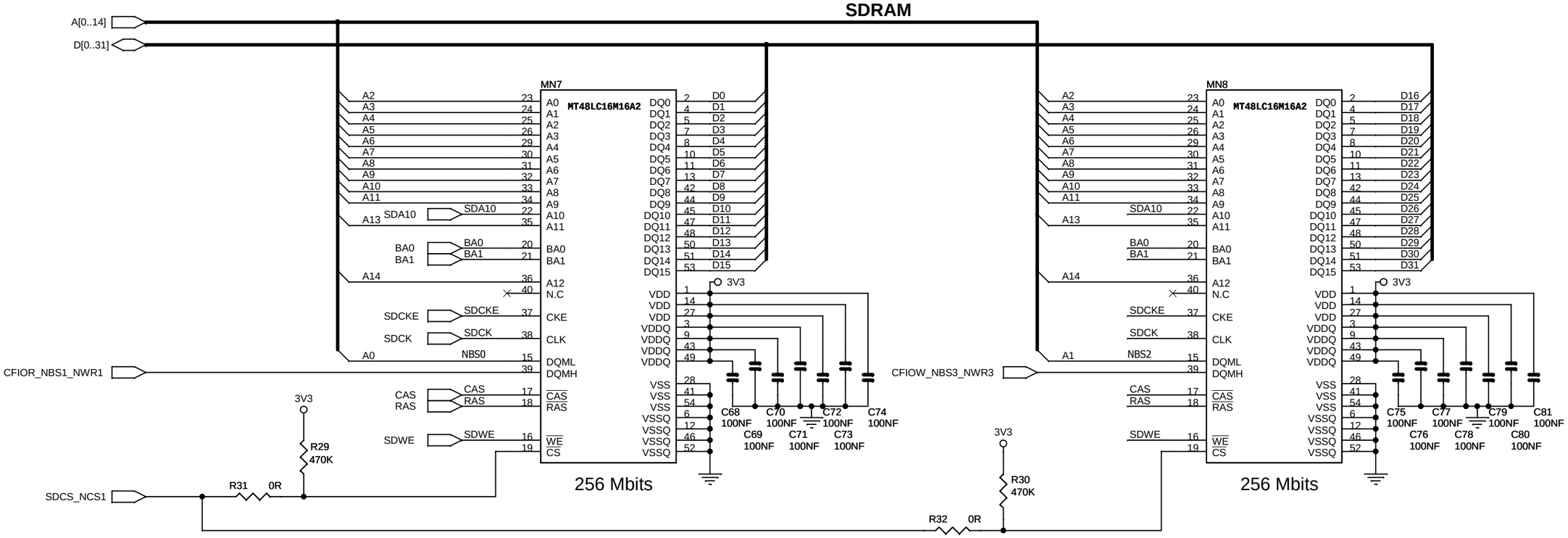
REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	28/08/06		
A	INIT EDIT	JPG	17/10/05		

SCALE 1/1

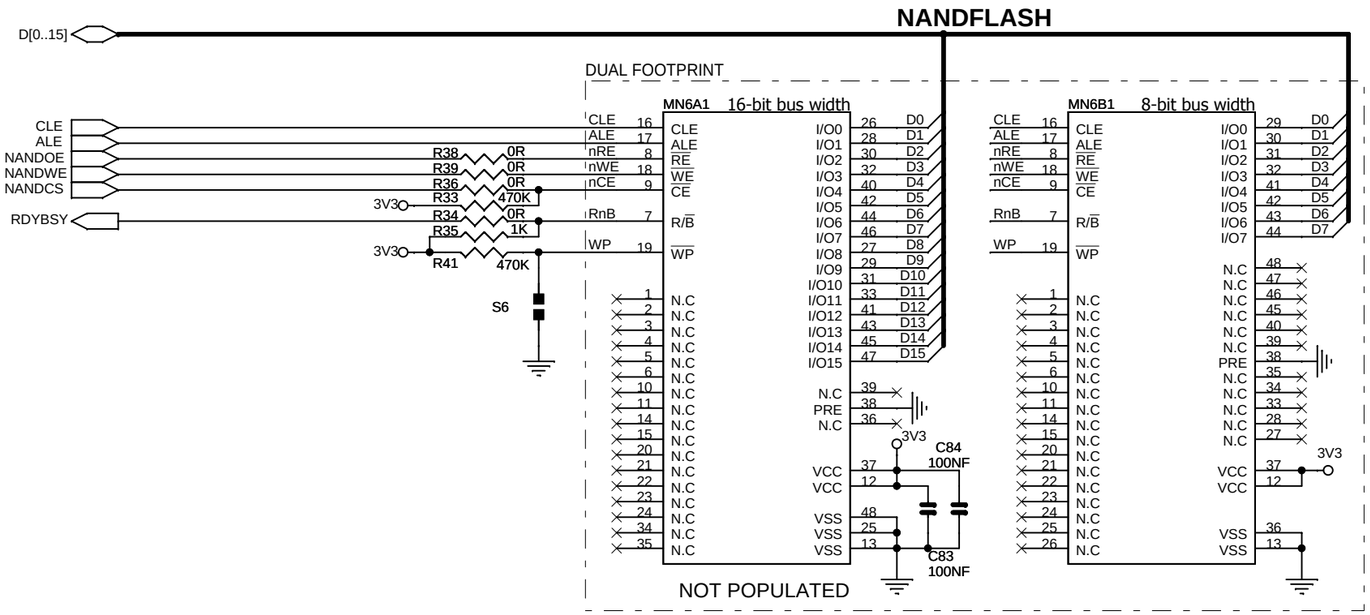
REV. B

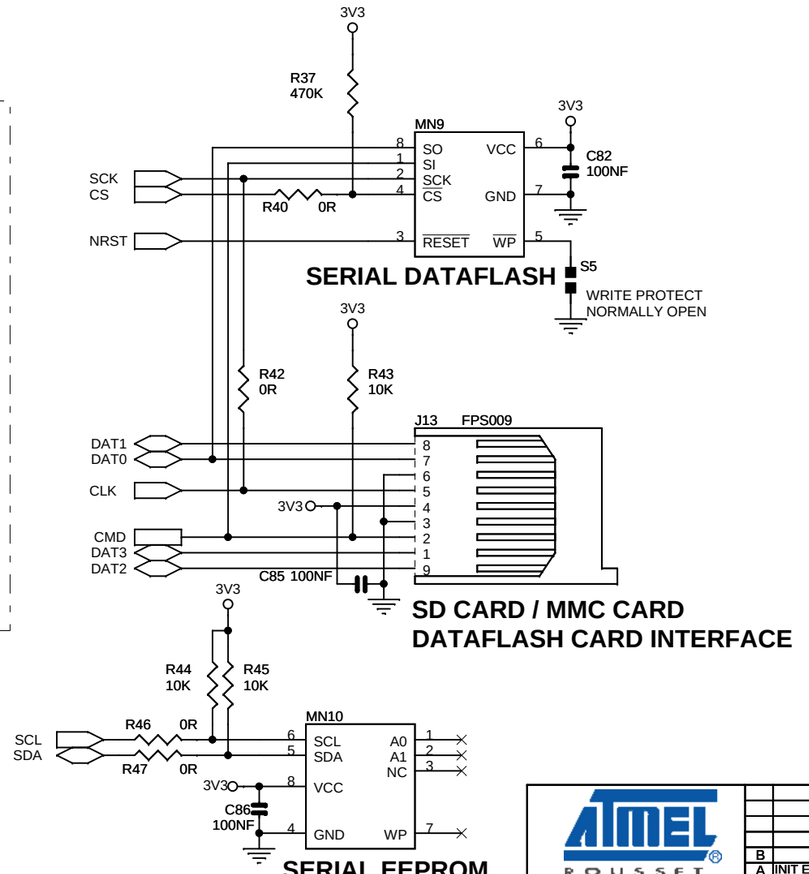
SHEET 4/8

SDRAM



NANDFLASH





B		JPG	28/08/06		
A	INIT EDIT	JPG	17/10/05		
REV	MODIF.	DES.	DATE	VER.	DATE

ATMEL ROUSSET

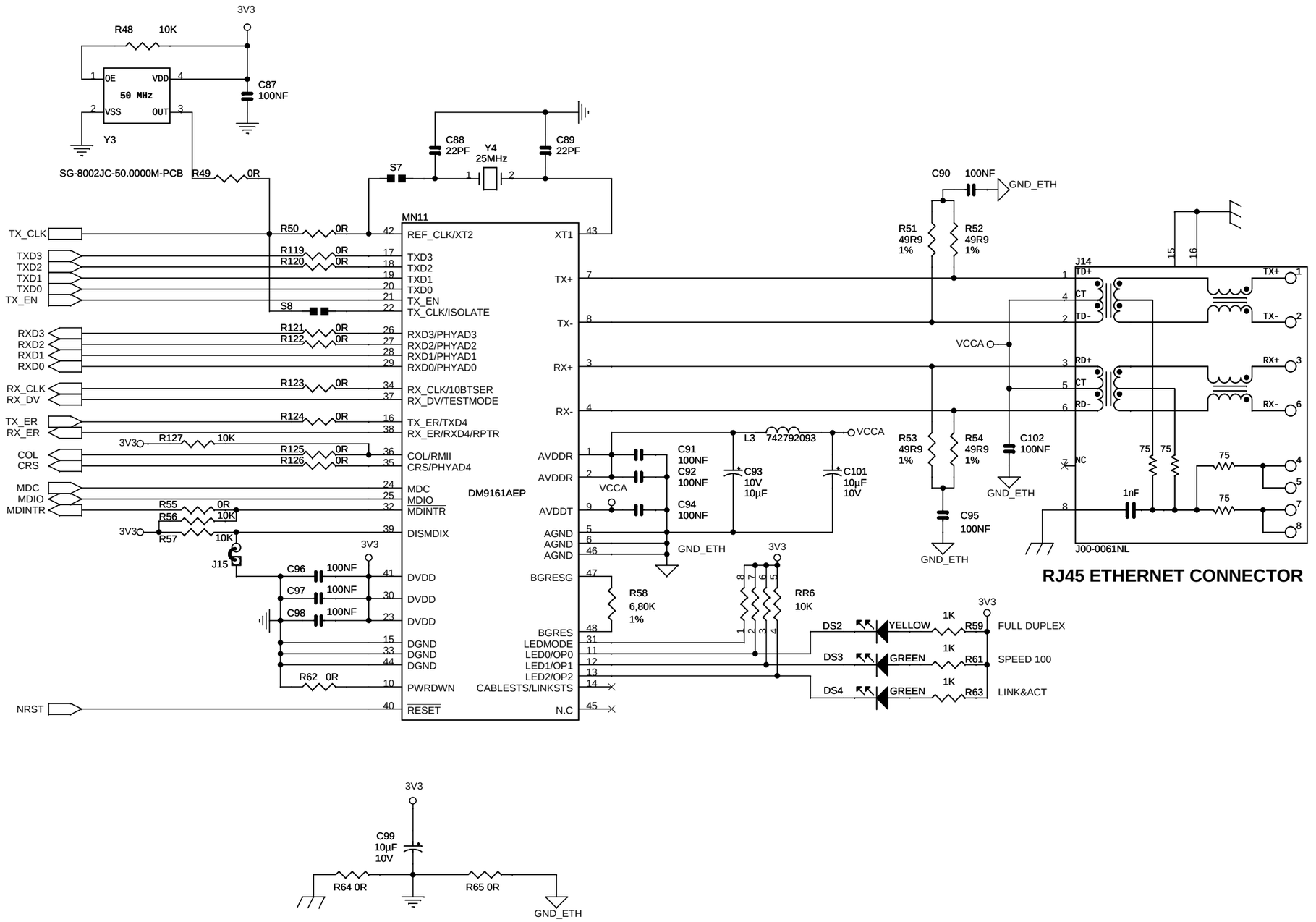
AT91SAM9260-EK

MEMORY

SCALE 1/1

REV. B

SHEET 5/8



REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	28/08/06		
A	INIT EDIT	JPG	17/10/05		

ATMEL ROUSSET

AT91SAM9260-EK

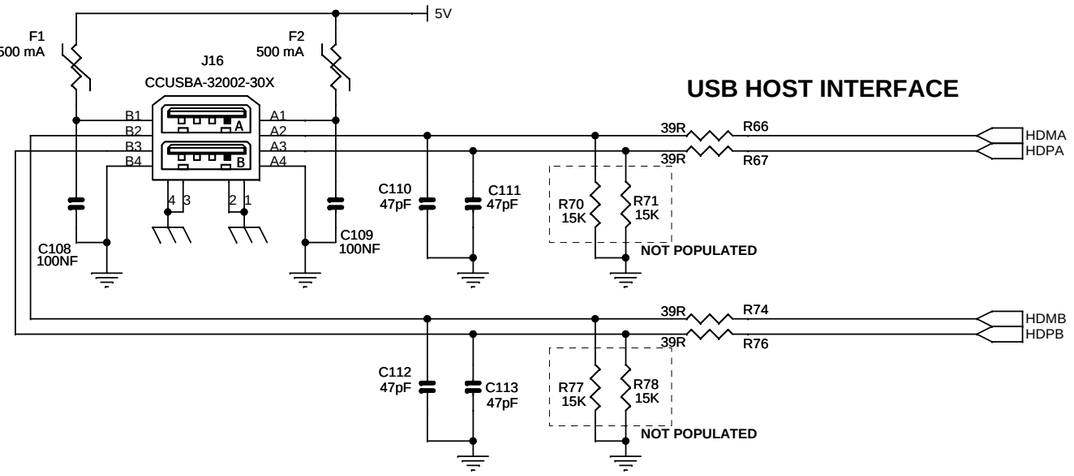
ETHERNET

SCALE 1/1

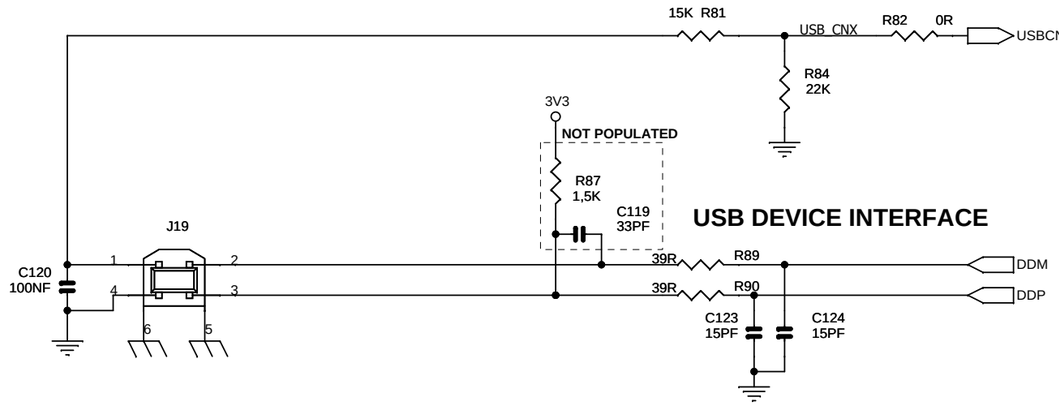
REV. B

SHEET 6/8

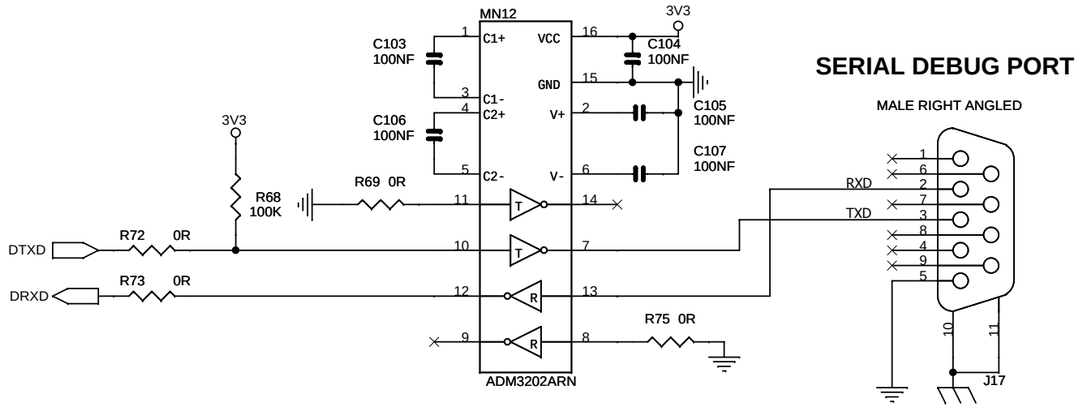
USB HOST INTERFACE



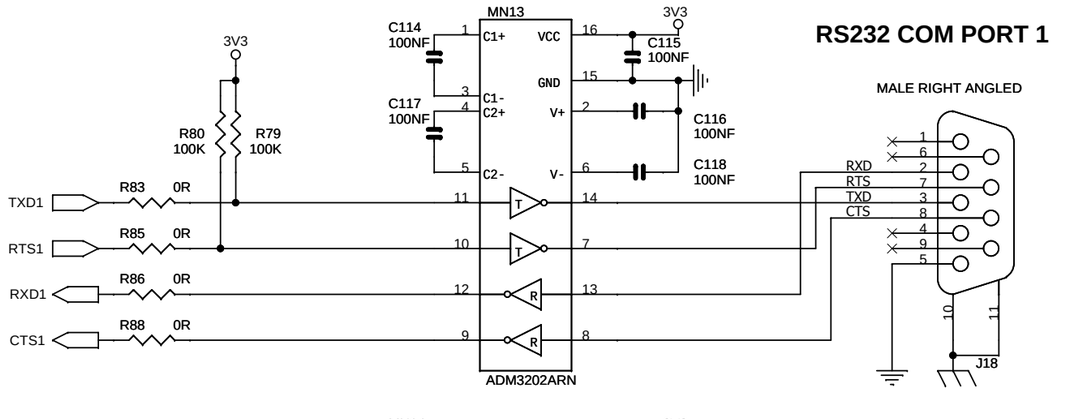
USB DEVICE INTERFACE



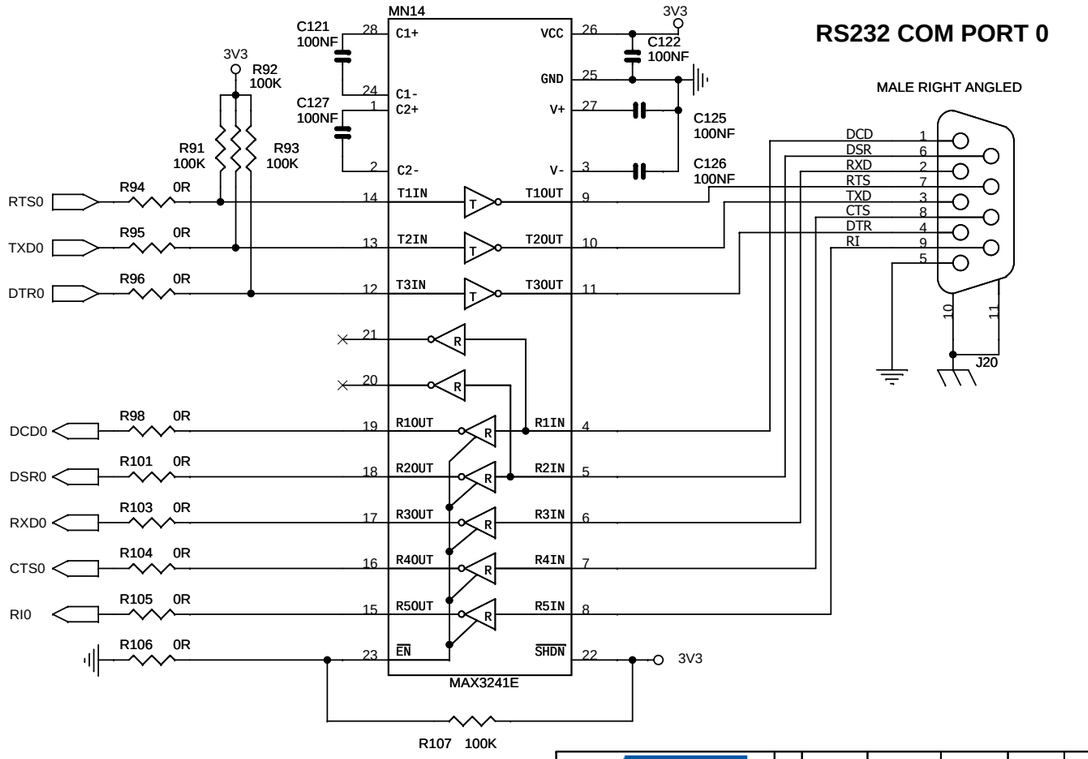
SERIAL DEBUG PORT



RS232 COM PORT 1



RS232 COM PORT 0



REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	28/08/06		
A	INIT EDIT	JPG	17/10/05		

ATMEL ROUSSET

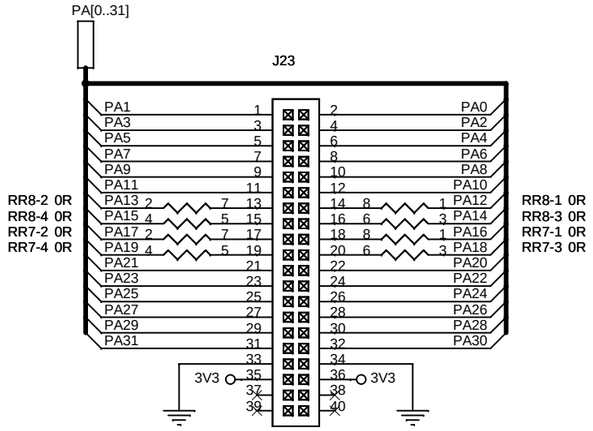
AT91SAM9260-EK

SERIAL INTERFACES

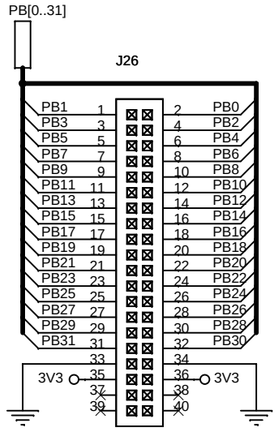
SCALE 1/1

REV. B

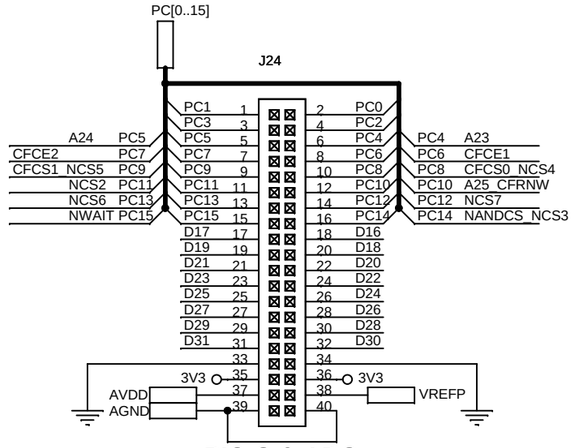
SHEET 7/8



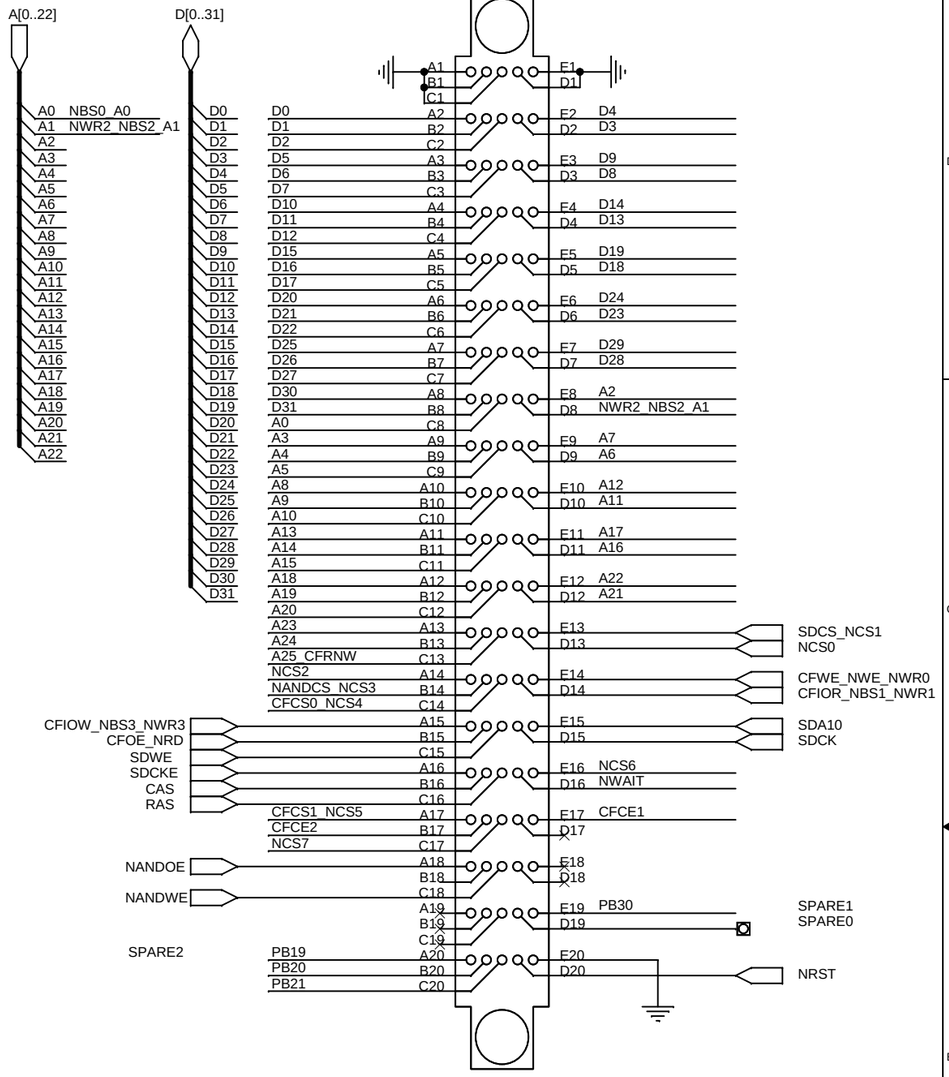
PIO A



PIO B



PIO C & ADC



EBI CONNECTORS
NOT POPULATED

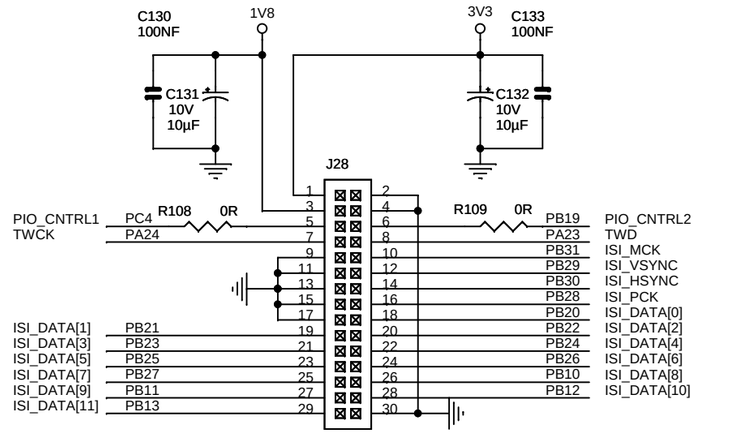
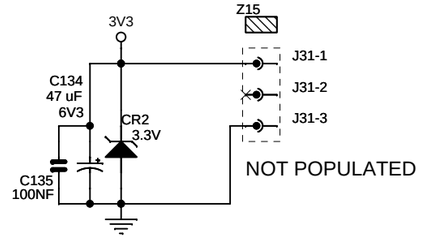
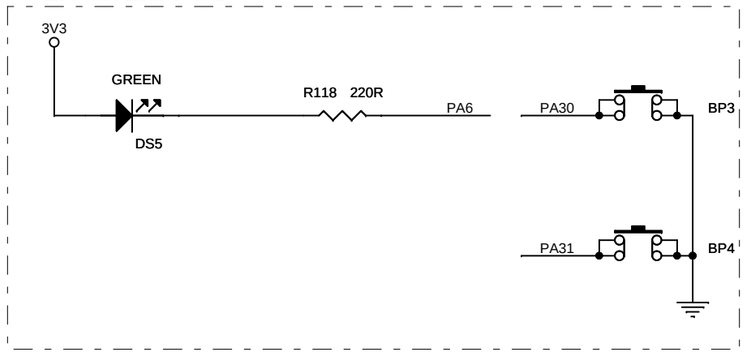


IMAGE SENSOR CONNECTOR



NOT POPULATED

USER INTERFACE



REV	MODIF.	DES.	DATE	VER.	DATE
B		JPG	28/08/06		
A	INIT EDIT	JPG	17/10/05		

ATMEL ROUSSET

AT91SAM9260-EK

EXPANSION & UI

SCALE 1/1

REV. B

SHEET 8/8

Section 6

Errata

6.1 VDD Backup Jumper Selector (J10)

The silkscreen is wrong. The markings for BB and 1V8 are inverted.

The marking should be:

- On J10 pin 1 (square pin): BB.
- On J10 pin 3: 1V8.

6.2 JTAGSEL S2 Footprint Selector

The S2 footprint must never be shorted to select a JTAG mode, otherwise the chip can be damaged.

By default, the JTAGSEL input pin integrates a pull-down resistor (ICE mode). To select the JTAG mode, connect the JTAGSEL input pin at VDDBU power.

6.3 TWI line pullups for Fast Mode operation

In order to use the TWI in Fast Mode (up to 400 Kbits/s), the default 10 KΩ resistors R44 and R45 should be replaced by smaller values (e.g., 2.2 KΩ).

Note that there is no need to change the pull-up resistors if the TWI is used in Standard Mode (up to 100 Kbits/s).

6.4 AT73C213 clocking

In the present schematics (block diagram p.10 and sheet 1/8, p.26), the MCLK and BCLK sources implementation does not guarantee a correct phase relation as specified in the AT73C213 datasheet.

Problem Fix/Workaround:

In his own design, the user must make sure the BCLK and MCLK clocks generation implements the timing specified in the AT73C213 datasheet.

Section 7

Revision History

7.1 Revision History

Table 7-1.

Document	Comments	Change Request Ref.
6234A	First issue.	
6234B	New Figure 2-3, " AT91SAM9260-EK Block Diagram". Inserted Section 3.14, " PIO Usage". Added new schematics in Section 5. Added new Section 6, Errata.	3315
6234C	Added errata Section 6.3, "TWI line pullups for Fast Mode operation". Added errata Section 6.4, "AT73C213 clocking"	4086 4227

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Atmel Europe
Le Krebs
8, rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-Yvelines
Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature

6234C–ATARM–22-Mar-07