LPV531 Programmable Micropower CMOS Input, Rail-to-Rail Output Operational Amplifier

Check for Samples: LPV531

FEATURES

- **(Typical 5V Supply, unless otherwise Noted.)**
- **Supply Voltage 2.7V to 5.5V**
- **Dynamic Power Mode Setting**
- **Continuously Programmable Supply Current**
  - **Range 5 µA to 425 µA**
- **Continuously Programmable Bandwidth**
  - **Range 73 kHz to 4.6 MHz**
- **Input Common Mode Voltage Range −0.3V to 3.8V**
- **CMRR 95 dB**
- **Rail-to-Rail Output Voltage Swing**
- **Input Offset Voltage 1 mV**

APPLICATIONS

- **AC Coupled Circuits**
- **Portable Instrumentation**
- **Active Filters**

Typical Application

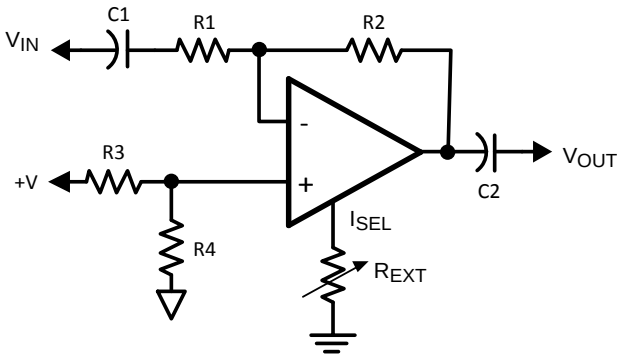


Figure 1. AC Coupled Application

DESCRIPTION

The LPV531 is an extremely versatile operational amplifier. A single external resistor gives the system designer the ability to define the quiescent current, gain bandwidth product and output short circuit current. This innovative feature gives the system designer a method to dynamically switch the power level to optimize the performance of the op amp and meet the system design requirements.

The LPV531 can be tailored to a wide variety of applications. It offers the system designer the ability to dynamically trade off supply current for bandwidth by adjusting the current drawn from the I_{SEL} pin using a DAC or switching in different value resistors in series with the I_{SEL} pin. The LPV531 is capable of operating from 73 kHz, consuming only 5 µA, to as fast as 4.6 MHz, consuming only 425 µA. The input offset voltage is relatively independent and therefore is not significantly affected by the chosen power level.

Utilizing a CMOS input stage, the LPV531 achieves an input bias current of 50 fA and a common mode input voltage which extends from the negative rail to within 1.2V of the positive supply. The LPV531's rail-to-rail class AB output stage enables this op amp to offer maximum dynamic range at low supply voltage.

Offered in the space saving 6-pin SOT package, the LPV531 is ideal for use in handheld electronics and portable applications. The LPV531 is manufactured using TI's advanced VIP50 process.

A fixed supply current/gain bandwidth is available upon request.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	
Human Body Model	2000V
Machine Model	200V
V_{IN} Differential	±2V
Supply Voltage (V^+ - V^-)	6V
Storage Temperature Range	−65°C to +150°C
Junction Temperature (4)	+150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp. (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0Ω in series with 200 pF.
(4) Typical values represent the most likely parametric norm.

Operating Ratings (1)

Operating Temperature Range	−40°C to +85°C
Supply Voltage (V^+ – V^-)	2.7V to 5.5V
Package Thermal Resistance (θ_{JA}) (2)	
6-Pin SOT	171°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

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5V Full Power Mode Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, I_{SEL} pin connected to V^-, R_L = 100 kΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			±1	±4.5 **±5**	mV
ΔV_{OS}	Input Offset Voltage Difference	(V_{OS} in Full Power Mode) − (V_{OS} in Low Power Mode)		±0.1	±2	mV
TC V_{OS}	Input Offset Average Drift	(3)		±2		µV/°C
I_B	Input Bias Current	(4)		.05	±10 **±100**	pA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.5V	72 **68**	95		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5.5V V_{CM} = 1V	74 **70**	90		dB
CMVR	Input Common Mode Voltage Range	CMRR ≥ 50 dB	−0.3		3.8	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V R_L = 1 kΩ to $V^+/2$	87 **84**	96		dB
		V_O = 0.5V to 4.5V R_L = 10 kΩ to $V^+/2$	104 **100**	114		
		V_O = 0.5V to 4.5V R_L = 100 kΩ, to $V^+/2$	108 **104**	128		
V_O	Output Swing High	R_L = 1 kΩ to $V^+/2$		120	180 **195**	mV from V^+
		R_L = 10 kΩ to $V^+/2$		55	80 **85**	
		R_L = 100 kΩ to $V^+/2$		30	50 **60**	
	Output Swing Low	R_L = 1 kΩ to $V^+/2$		160	210 **230**	mV
		R_L = 10 kΩ to $V^+/2$		105	120 **135**	
		R_L = 100 kΩ to $V^+/2$		95	120 **135**	
I_{SC}	Output Short Circuit Current (5)	Sourcing, V_O = 2.5V V_{ID} = 100 mV		−15	−8 **−3**	mA
		Sinking, V_O = 2.5V V_{ID} = −100 mV	13 **10**	24		
I_S	Supply Current			425	530 **650**	µA
SR	Slew Rate (6)	A_V = +1, V_{IN} = 0.5V to 3.5V C_L = 15 pF	1.55 **1**	2.5		V/µs
GBW	Gain Bandwidth Product	C_L = 20 pF		4.6		MHz
e_n	Input-Referred Voltage Noise	f = 100 kHz		20		nV/√Hz
		f = 1 kHz		28		
i_n	Input-Referred Current Noise	f = 1 kHz		6		fA/√Hz

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(4) Specified by design.
(5) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(6) Slew rate is the slower of the rising or falling slew rates.

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5V Mid-Power Mode Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, I_{SEL} pin connected to V^- through 100 kΩ resistor, R_L = 100 kΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			±1	±4.5 **±5**	mV
ΔV_{OS}	Input Offset Voltage Difference	(V_{OS} in Full Power Mode) − (V_{OS} in Low Power Mode)		±0.1	±2	mV
TC V_{OS}	Input Offset Average Drift	(3)		±2		µV/°C
I_B	Input Bias Current	(4)		.05	±10 **±100**	pA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.5V	72 **68**	92		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5.5V	72 **68**	88		dB
CMVR	Input Common Mode Voltage Range	CMRR ≥ 50 dB	−0.3		3.8	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V R_L = 10 kΩ to $V^+/2$	86 **82**	96		dB
		V_O = 0.5V to 4.5V R_L = 100 kΩ to $V^+/2$	100 **98**	114		
V_O	Output Swing High	R_L = 10 kΩ to $V^+/2$		115	160 **175**	mV from V^+
		R_L = 100 kΩ to $V^+/2$		65	110 **120**	
	Output Swing Low	R_L = 10 kΩ to $V^+/2$		150	165 **180**	mV
		R_L = 100 kΩ to $V^+/2$		105	120 **135**	
I_{SC}	Output Short Circuit Current (5)	Sourcing, V_O = 2.5V V_{ID} = 100 mV		−4	−1.5 **−1**	mA
		Sinking, V_O = 2.5V V_{ID} = −100 mV	1.5 **1**	4		
I_S	Supply Current			42	55 **62**	µA
SR	Slew Rate (6)	A_V = +1, V_{IN} = 0.5V to 3.5V	180 **100**	250		V/ms
GBW	Gain Bandwidth Product	C_L = 20 pF		625		kHz
e_n	Input-Referred Voltage Noise	f = 100 kHz		55		nV/√Hz
		f = 1 kHz		60		
i_n	Input-Referred Current Noise	f = 1 kHz		6		fA/√Hz

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(4) Specified by design.
(5) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(6) Slew rate is the slower of the rising or falling slew rates.

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5V Low Power Mode Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, I_{SEL} connected to V^- through 1 MΩ resistor, R_L = 100 kΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			±1	±4.5 **±5**	mV
ΔV_{OS}	Input Offset Voltage Difference	(V_{OS} in Full Power Mode) − (V_{OS} in Low Power Mode)		±0.1	±2	mV
TC V_{OS}	Input Offset Average Drift	(3)		±2		µV/°C
I_B	Input Bias Current	(4)		.05	±10 **±100**	pA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.5V	72 **68**	90		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5.5V	72 **68**	85		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	−0.3		3.8	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V R_L = 10 kΩ to $V^+/2$		90		dB
		V_O = 0.5V to 4.5V R_L = 100 kΩ to $V^+/2$	80 **78**	100		
V_O	Output Swing High	R_L = 10 kΩ to $V^+/2$		175	400 **1600**	mV from V^+
		R_L = 100 kΩ to $V^+/2$		115	200 **230**	
	Output Swing Low	R_L = 10 kΩ to $V^+/2$		250	1200 **1800**	mV
		R_L = 100 kΩ to $V^+/2$		150	165 **180**	
I_{SC}	Output Short Circuit Current (5)	Sourcing, V_O = 2.5V V_{ID} = 100 mV		−400	−100 **−35**	µA
		Sinking, V_O = 2.5V V_{ID} = −100 mV	80 **35**	300		
I_S	Supply Current			5	7 **8**	µA
SR	Slew Rate (6)	A_V = +1, V_{IN} = 0.5V to 3.5V	10 **8**	28		V/ms
GBW	Gain Bandwidth Product	C_L = 20 pF		73		kHz
e_n	Input-Referred Voltage Noise	f = 1 kHz		200		nV/√Hz
i_n	Input-Referred Current Noise	f = 1 kHz		60		fA/√Hz

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(4) Specified by design.
(5) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(6) Slew rate is the slower of the rising or falling slew rates.

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Power Select Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$, R_L = 100 kΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
t_{LF}	Time from Low Power Mode to Full Power Mode			210		ns
t_{FL}	Time from Full Power Mode to Low Power Mode			500		ns
V_{REXT}	Voltage @ I_{SEL} Pin	I_{SEL} Pin Left Open	100	110	125	mV
R_{INT}			9	11	14.5	kΩ

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.

Connection Diagram

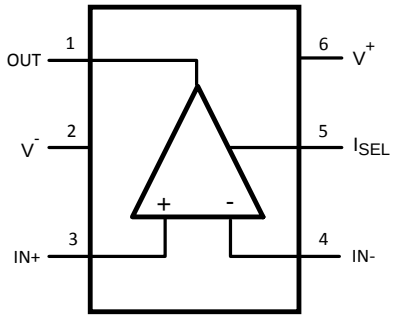


Figure 2. 6-Pin SOT – Top View
See Package Number DDC

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Typical Performance Characteristics

Unless otherwise specified, V^+ = 5V, T_J = 25°C. For Full Power Mode the I_{SEL} pin is connected to V^-; for Mid-Power Mode the I_{SEL} pin is connected to V^- through a 100 kΩ resistor; for Low Power Mode the I_{SEL} pin is connected to V^- through a 1 MΩ resistor.

Supply Current vs. I_{SEL}

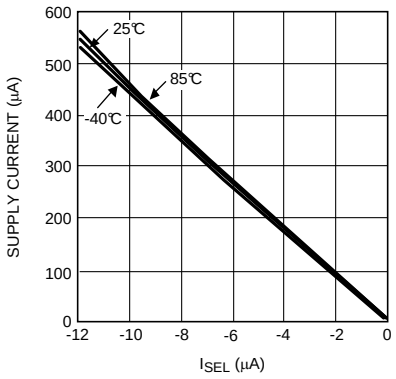


Figure 3.

Supply Current vs. I_{SEL}

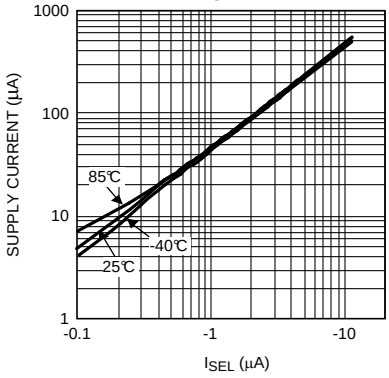


Figure 4.

Supply Current vs. Supply Voltage (Full Power Mode)

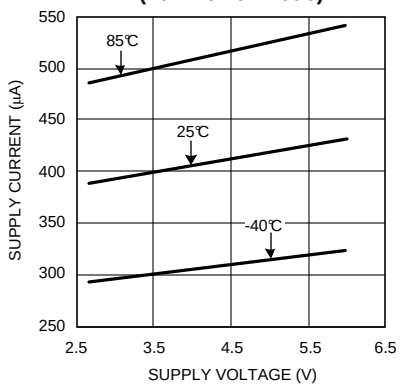


Figure 5.

Supply Current vs. Supply Voltage (Mid Power Mode)

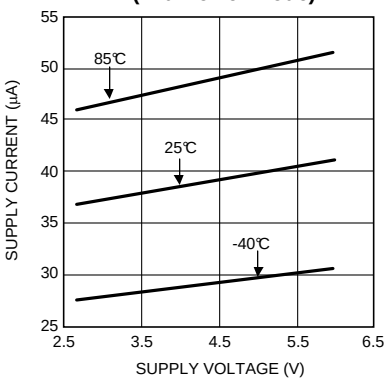


Figure 6.

Supply Current vs. Supply Voltage (Low Power Mode)

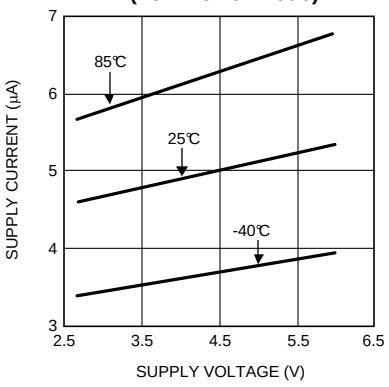


Figure 7.

Gain and Phase vs. Frequency (Full Power Mode)

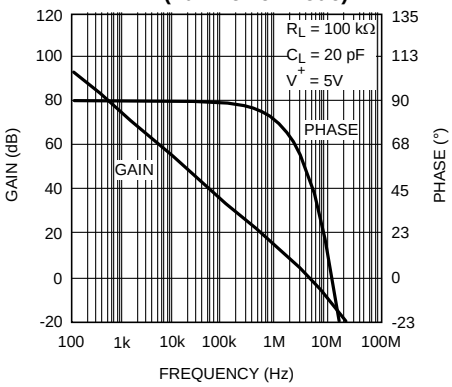


Figure 8.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V^+ = 5V, T_J = 25°C. For Full Power Mode the I_{SEL} pin is connected to V^-; for Mid-Power Mode the I_{SEL} pin is connected to V^- through a 100 kΩ resistor; for Low Power Mode the I_{SEL} pin is connected to V^- through a 1 MΩ resistor.

Gain and Phase vs. Frequency (Mid Power Mode)

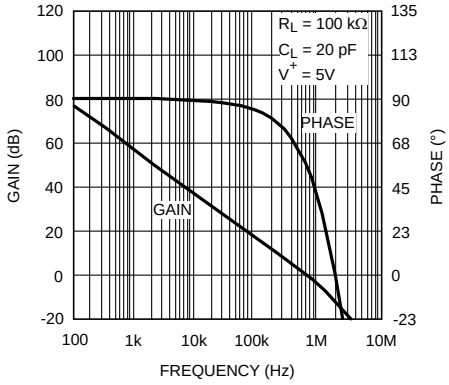


Figure 9.

Gain and Phase vs. Frequency (Low Power Mode)

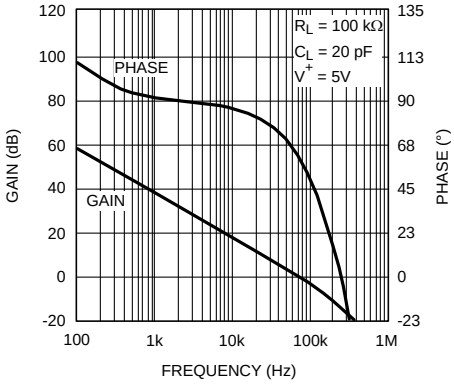


Figure 10.

Input Offset Voltage vs. Common Mode Voltage (Full Power Mode)

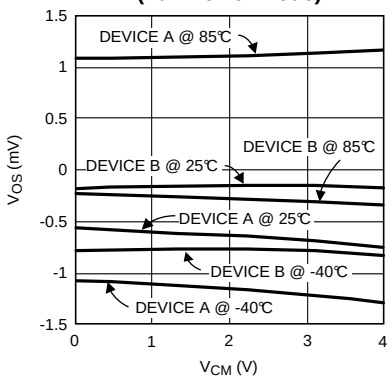


Figure 11.

Input Offset Voltage vs. Common Mode Voltage (Mid Power Mode)

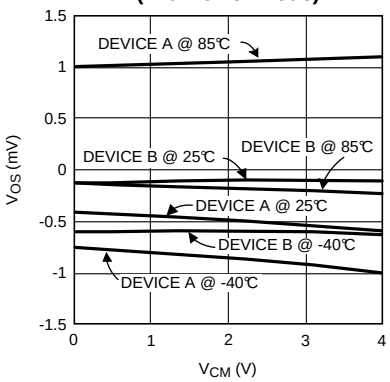


Figure 12.

Input Offset Voltage vs. Common Mode Voltage (Low Power Mode)

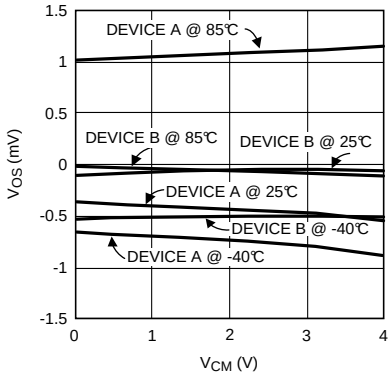


Figure 13.

CMRR vs. Frequency

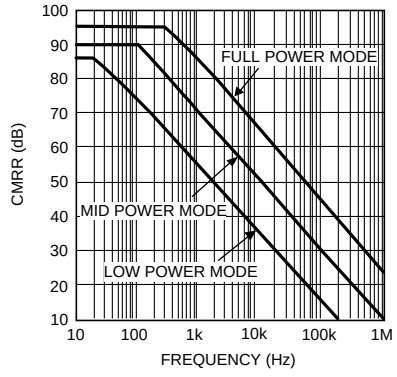


Figure 14.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V^+ = 5V, T_J = 25°C. For Full Power Mode the I_{SEL} pin is connected to V^-; for Mid-Power Mode the I_{SEL} pin is connected to V^- through a 100 kΩ resistor; for Low Power Mode the I_{SEL} pin is connected to V^- through a 1 MΩ resistor.

PSRR vs. Frequency (Full Power Mode)

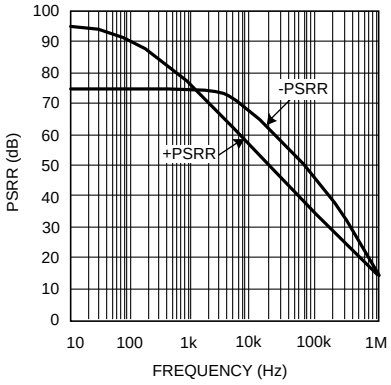


Figure 15.

PSRR vs. Frequency (Mid Power Mode)

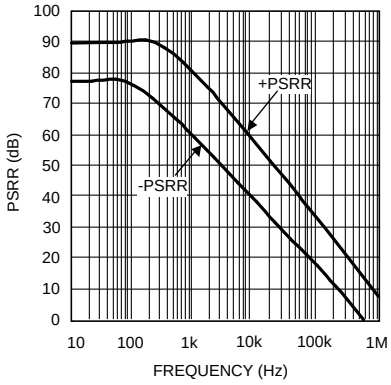


Figure 16.

PSRR vs. Frequency (Low Power Mode)

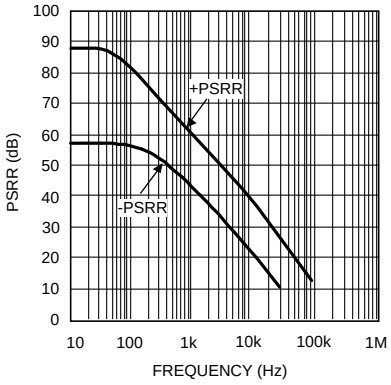


Figure 17.

Small Signal Non-Inverting Response (Full Power Mode)

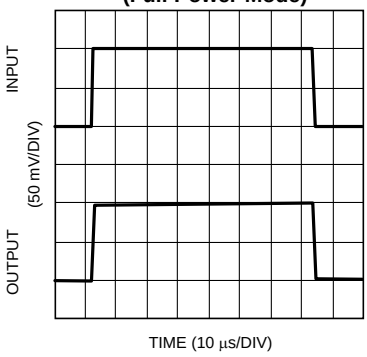


Figure 18.

Small Signal Non-Inverting Response (Mid Power Mode)

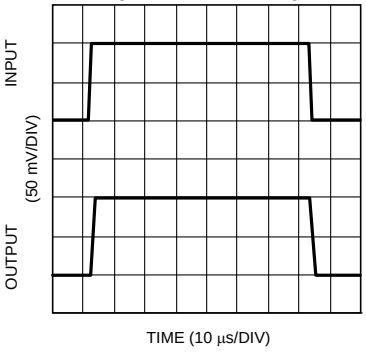


Figure 19.

Small Signal Non-Inverting Response (Low Power Mode)

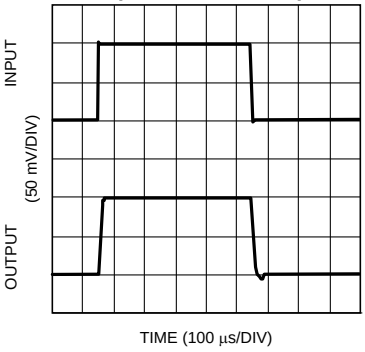


Figure 20.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V^+ = 5V, T_J = 25°C. For Full Power Mode the I_{SEL} pin is connected to V^-; for Mid-Power Mode the I_{SEL} pin is connected to V^- through a 100 kΩ resistor; for Low Power Mode the I_{SEL} pin is connected to V^- through a 1 MΩ resistor.

Large Signal Non-Inverting Response (Full Power Mode)

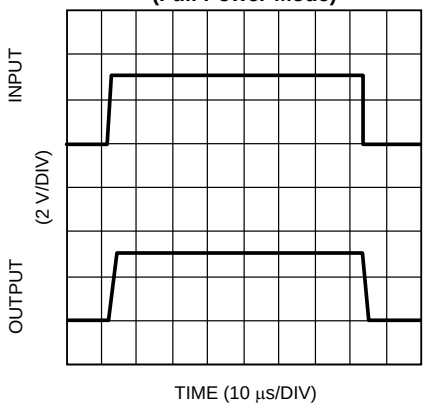


Figure 21.

Large Signal Non-Inverting Response (Mid Power Mode)

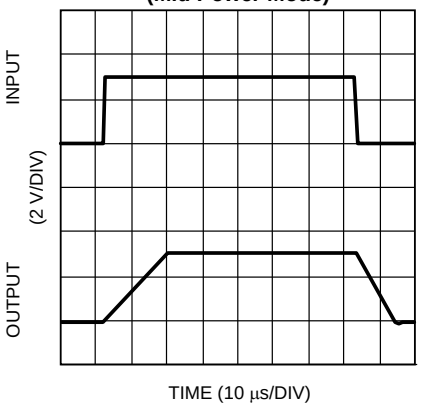


Figure 22.

Large Signal Non-Inverting Response (Low Power Mode)

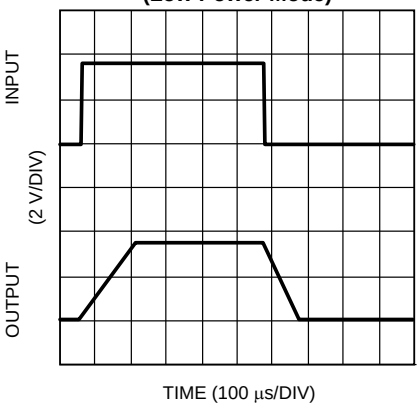


Figure 23.

Small Signal Inverting Pulse Response (Full Power Mode)

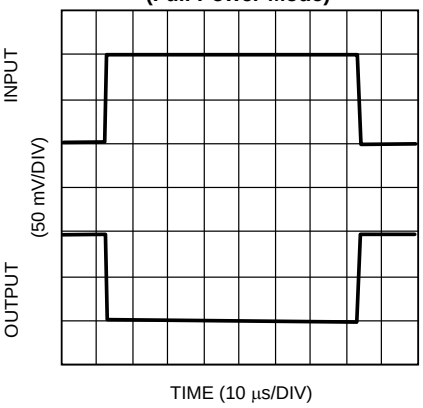


Figure 24.

Small Signal Inverting Pulse Response (Mid Power Mode)

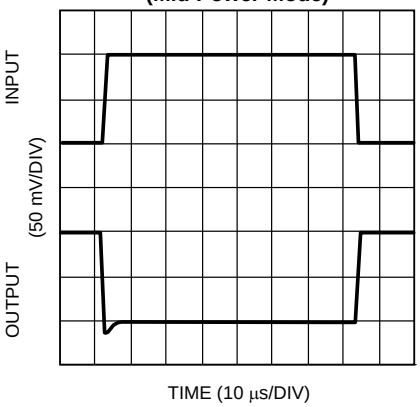


Figure 25.

Small Signal Inverting Pulse Response (Low Power Mode)

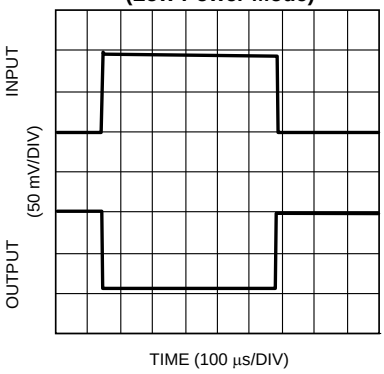


Figure 26.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V^+ = 5V, T_J = 25°C. For Full Power Mode the I_{SEL} pin is connected to V^-; for Mid-Power Mode the I_{SEL} pin is connected to V^- through a 100 kΩ resistor; for Low Power Mode the I_{SEL} pin is connected to V^- through a 1 MΩ resistor.

Large Signal Inverting Response (Full Power Mode)

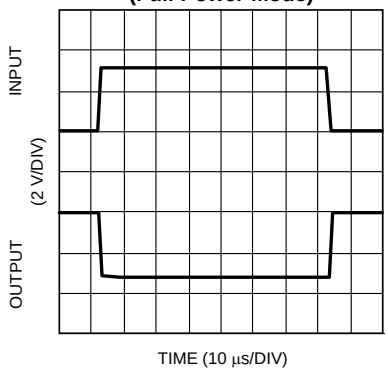


Figure 27.

Large Signal Inverting Response (Mid Power Mode)

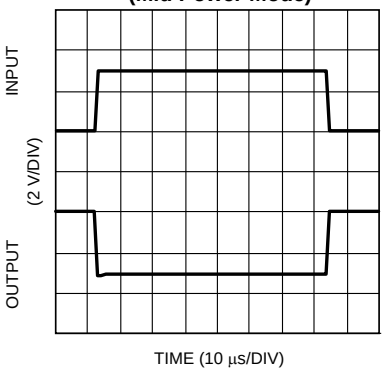


Figure 28.

Large Signal Inverting Response (Low Power Mode)

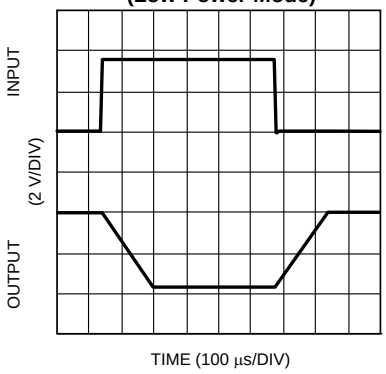


Figure 29.

I_{SINK} vs. Supply Current

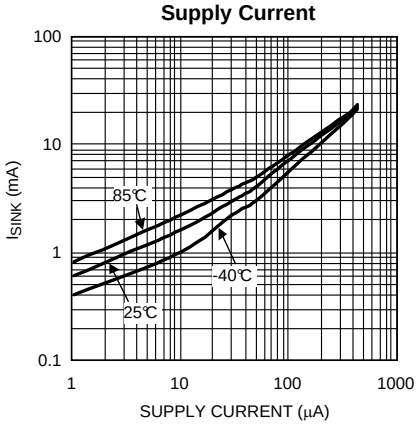


Figure 30.

I_{SOURCE} vs. Supply Current

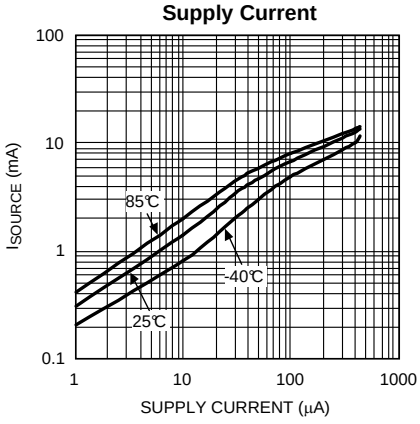


Figure 31.

Gain Bandwidth Product vs. I_{SEL}

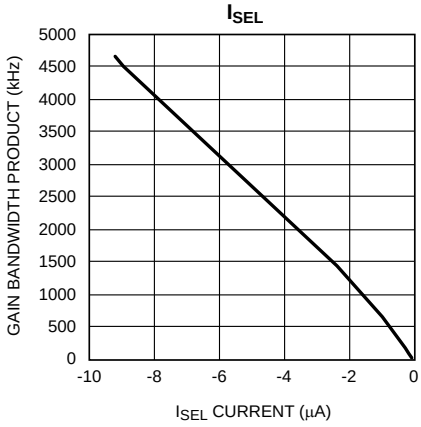


Figure 32.

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Typical Performance Characteristics (continued)

Unless otherwise specified, V^+ = 5V, T_J = 25°C. For Full Power Mode the I_{SEL} pin is connected to V^-; for Mid-Power Mode the I_{SEL} pin is connected to V^- through a 100 kΩ resistor; for Low Power Mode the I_{SEL} pin is connected to V^- through a 1 MΩ resistor.

Input Referred Voltage Noise vs. Frequency

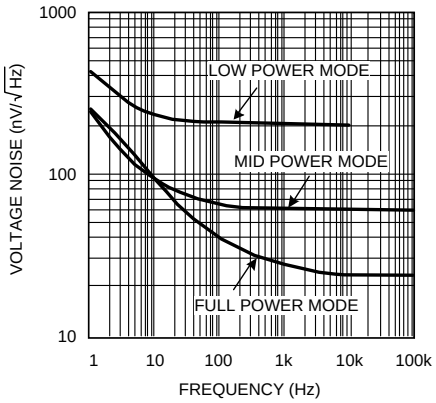


Figure 33.

Phase Margin vs. Capacitive Load

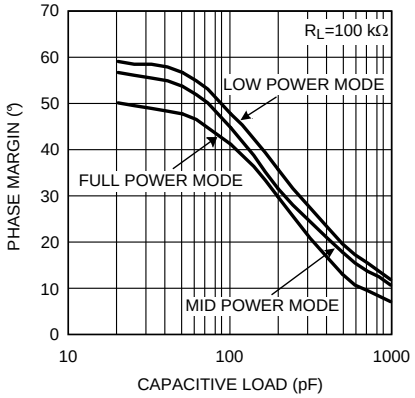


Figure 34.

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APPLICATION INFORMATION

The LPV531 is an extremely versatile operational amplifier because performance and power consumption can be adjusted during operation. This provides a method to dynamically optimize the supply current, the bandwidth and the output short circuit current in the application. The power level can be set by the current drawn from the I_{SEL} pin according to the application performance requirements.

CIRCUIT TOPOLOGY

As shown in Figure 35, the LPV531 contains two internal bias reference generators that deliver a reference current (I_{REF}) to the amplifier core. The programmable bias generator generates a 110 mV reference voltage (V_{INT}). This reference voltage is converted into a programmable reference current (I_{PROG}) through the internal resistor (R_{INT}) and the external resistor (R_{EXT}) connected to the I_{SEL} pin. Internally, I_{PROG} is added to the output current from the low power bias generator (I_{STDB}). When the I_{SEL} pin is left floating, I_{PROG} equals zero and the I_{REF} equals I_{STDB}. The value of I_{STDB} is such that in this mode the power supply current is below 1 µA. In this 1 µA power mode, the LPV531 is functional but performance over the full temperature range is not ensured. The 1 µA power mode operation is only recommended for applications with a temperature range between 0 and 70°C.

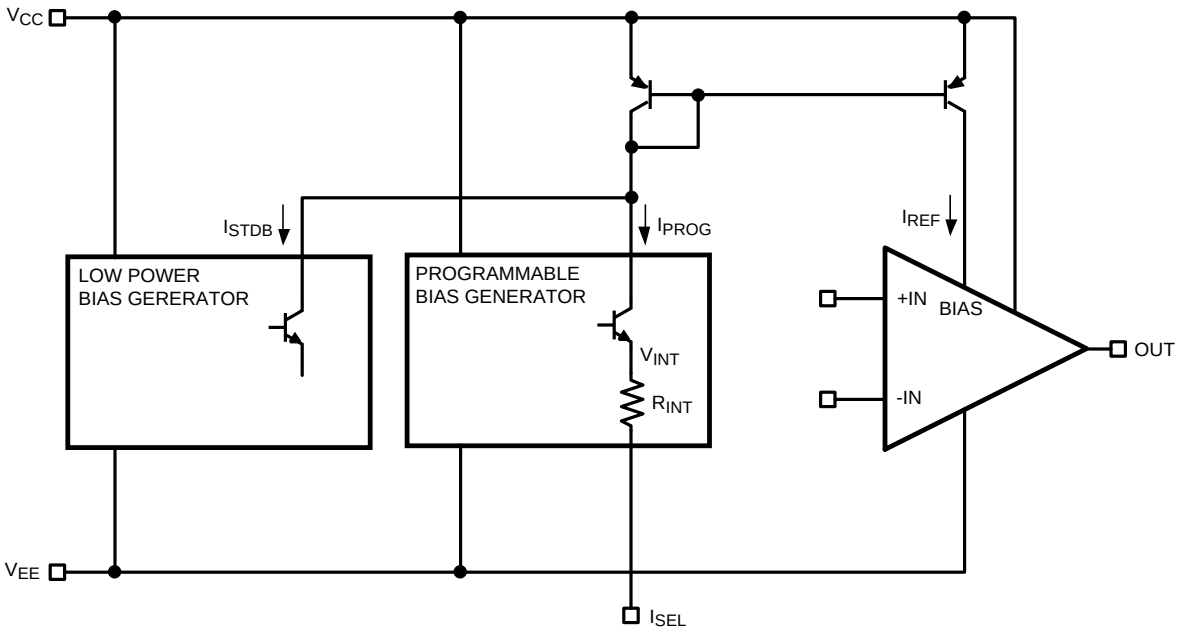


Figure 35. Simplified Schematic

POWER MODE CONTROL

To illustrate typical configurations three possible solutions to control the power mode(s) of the LPV531 will be described.

Single Power Mode

If the application requires one single power mode for the LPV531, then the easiest way to achieve this is to connect a resistor (R_{EXT}) from the I_{SEL} pin to V^-. Together with the internal circuitry, R_{EXT} will determine the current drawn from the I_{SEL} pin. Internally the I_{SEL} pin is connected to an 11 kΩ internal series resistor (R_{INT}) which is biased at V_{INT} = 110 mV. This set up is illustrated in Figure 36.

For a desired supply current, bandwidth, short circuit current, or load resistance, the required value of R_{EXT} can be calculated using the equations in the section “DETERMINING THE I_{SEL} LEVELS”.

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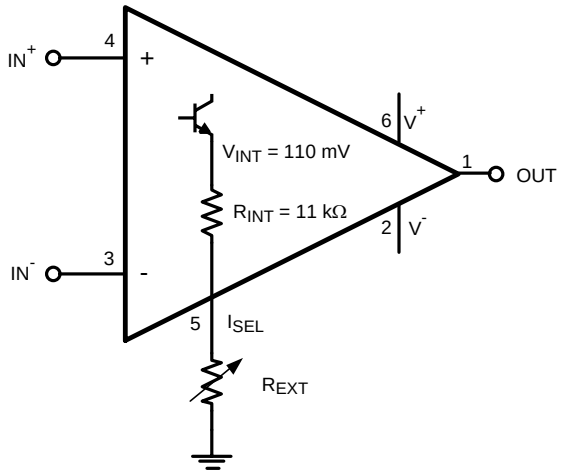


Figure 36. Single Power Mode

Switched Discrete Power Modes

In this typical application, the LPV531 can operate at two (or more) power modes in order to fulfill the demands of the design. One of the modes is used to save power. It is a low power mode which is set by using a large resistor. The others are the higher power modes which are set by one or more smaller resistors. The larger resistor that sets the low power mode can be permanently connected while the smaller resistor(s) can be switched in parallel to set the high power mode(s). This configuration allows the designer to get the required performance from the LPV531 when needed.

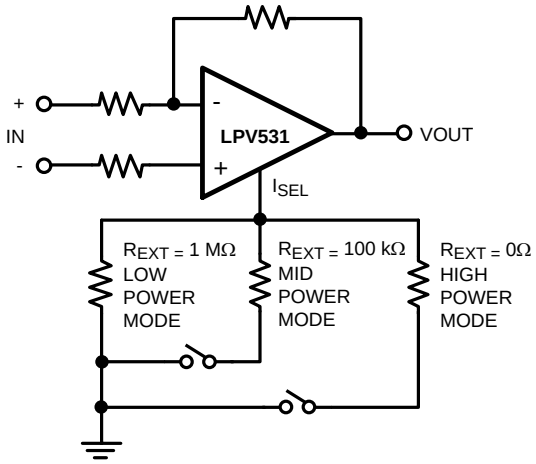


Figure 37. Power Modes Set by Resistors and Switches

The switches shown in Figure 37 can be easily implemented with an open drain I/O port of an ASIC or any other simple pull down switch.

DAC Controlled Power Modes

For voltage controlled filter applications, where control of the gain bandwidth is essential, a DAC and a resistive voltage divider can be used. In this application the current drawn from the I_{SEL} pin is controlled by the DAC. The DAC's total output range is divided to match the V^- to V_{INT} voltage which has the range of 0-110 mV.

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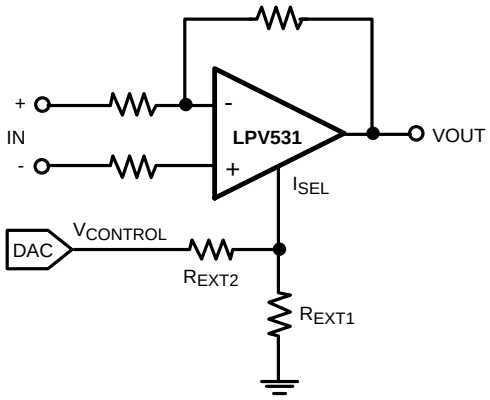


Figure 38. DAC Controlled Power Mode Configurations

The output of the resistive voltage divider should have an impedance that is small compared to the value of R_{INT} to allow a linear control of the power level. Therefore, R_{EXT2} needs to have a value in the order of $R_{INT}/10$ and R_{EXT1} = 125 mV * R_{EXT2} /$V_{CONTROL,MAX}$. For 1 µA power mode operation, these resistor values will divide the maximum voltage of $V_{CONTROL}$ to 125 mV.

DETERMINING THE R_{EXT} VALUES AND I_{SEL} LEVELS

To determine the value of R_{EXT} that is needed for a certain supply current or bandwidth, the following equations can be used:

$$PSI = 1\ \mu A + 40\ x\ \frac{110\ mV}{R_{EXT} + 11k} \tag{1}$$

or

$$R_{EXT} = 40\ x\ \frac{110\ mV}{PSI - 1\ \mu A}\ -11\ k\Omega \tag{2}$$

$$GBW = 11\ kHz + \frac{50[GHz \cdot \Omega]}{R_{EXT} + 11\ k\Omega} \quad or \quad R_{EXT} = \frac{50[GHz \cdot \Omega]}{GBW - 11\ kHz}\ -11\ k\Omega \tag{3}$$

For the power modes characterized in this datasheet, these formulas lead to the values in Table 1. These values deviate slightly from the typical values presented in the Electrical Characteristics tables. The values in Table 1 are calculated using approximated linear equations while the values in the Electrical Characteristics tables are the result of characterization measurement procedures.

Table 1. Values for Characterized Power Modes

R_{EXT}	I_{SEL}	Supply Current	Gain Bandwidth Product
1Ω	9 µA	400 µA	4.6 MHz
100 kΩ	0.9 µA	40 µA	460 kHz
1 MΩ	99 nA	5.3 µA	60 kHz

To calculate the R_{EXT} which will allow the LPV531 to deliver a minimum output current at all times and over all temperatures, use the following equations:

$$ISC = \frac{35V}{R_{EXT} + 11\ k\Omega} \quad or \quad R_{EXT} = \frac{35V}{ISC}\ -11\ k\Omega \tag{4}$$

If the output has to be kept at $V^+/2$ for a known load resistance, the required R_{EXT} can be calculated with the following equations:

$$R_{LOAD,MIN} = \frac{0.07}{R_{EXT} + 11\ k\Omega} \quad \text{or} \quad R_{EXT} = \frac{0.07}{R_{LOAD,MIN}} - 11\ k\Omega \tag{5}$$

For the characterized power modes these equations lead to the minimum values in Table 2 below.

Table 2. Minimum Values for Characterized Power Modes

R_{EXT}	I_{SEL}	I_{SC}	R_{LOAD}
1Ω	9 µA	3 mA	770Ω
100 kΩ	0.9 µA	300 µA	7.8 kΩ
1 MΩ	99 nA	55 µA	70.8 kΩ

The smallest load resistor that the LPV531 can drive when in low power mode is 70.8 kΩ, as shown in Table 2. When driving smaller loads, such as the 10 kΩ load resistor used in the Electrical Characteristics tables specification, the output swing in the low power mode is limited. If the application requires a 10 kΩ load then it is not recommended to use the LPV531 in low power mode.

I_{SEL} SENSITIVITY

The I_{SEL} pin is a current reference that directly affects the entire internal bias condition. Therefore, the I_{SEL} pin is very sensitive to parasitic signal coupling. In order to protect the I_{SEL} pin from unwanted distortion, it is important to route the PCB layout such that there is as little coupling between the I_{SEL} pin and the output or other signal traces as possible.

Typical Application

AC COUPLED CIRCUITS

The programmable power mode makes the LPV531 ideal for AC coupled circuits where the circuit needs to be kept active to maintain a quiescent charge on the coupling capacitors with minimal power consumption. Figure 39 shows the schematic of an inverting AC coupled amplifier using the LPV531 with the I_{SEL} pin controlled by I/O ports of a microcontroller. The advantage of the low power active mode for AC coupled amplifiers is the elimination of the time needed to re-establish a quiescent operating point when the amplifier is switched to full power mode.

When an amplifier without a low power active mode is used in low power applications, there are two ways to minimize power consumption. The first method turns off the amplifier by switching off power to the op amp using a transistor switch. The second method uses an amplifier with a shutdown pin. Both of these methods have the problem of allowing the coupling capacitors, C_1 and C_2 to discharge the quiescent DC voltage stored on them when in the shutdown state. When the amplifier is turned on again, the quiescent DC voltages must reestablish themselves. During this time, the amplifier's output is not usable because the output signal is a mixture of the amplified input signal and the charging voltage on the coupling capacitors. The settling time can range from a several milliseconds to several seconds depending on the resistor and capacitor values.

When the LPV531 is placed into the low power mode, the power consumption is minimal but the amplifier is active to maintain the quiescent DC voltage on the coupling capacitors. The transition back to the operational high power mode is fast, within a few hundred nanoseconds. The active low power mode of the LPV531 separates two critical aspects of a low power AC amplifier design. The values of the gain resistors, bias resistors, and coupling capacitors can be chosen independently of the turn-on and stabilization time.

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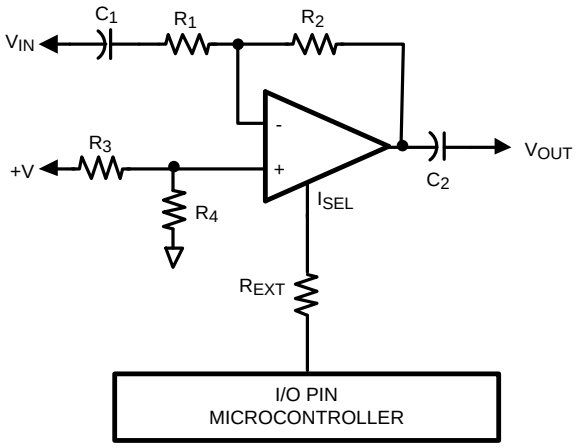


Figure 39. Inverting AC Coupled Application

PROGRAMMABLE POWER LEVELS AND THE EFFECTS OF STABILITY COMPENSATION METHODS USING EXTERNAL COMPONENTS

In some op amp application circuits, external capacitors are used to improve the stability of the feedback loop around the amplifier. When using the programmable power level feature of the LPV531 such stability improvement methods may not work. This is related to the internal frequency compensation method applied inside the LPV531.

Figure 40 shows the bode plot of the frequency response of the LPV531. The gain-bandwidth product is determined by the transconductance of the input stage ($g_{m,in}$) and the internal Miller compensation capacitor (C_m). The non-dominant pole is formed by the transconductance of the output stage ($g_{m,out}$) and the load capacitance connected to the output of the LPV531 (C_l). The frequency response crosses the frequency axis with a single-pole slope (20 dB/decade). This ensures the stability of feedback loops formed around the LPV531.

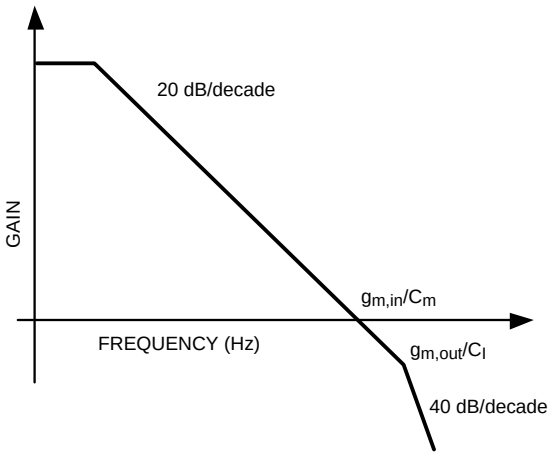


Figure 40. Bode Plot of the Frequency Response

When the load capacitance is increased, the pole at the output will shift to lower frequencies. Eventually, the output pole will shift below the unity gain frequency. This will cause the frequency characteristic to move through the 0 dB axis with a slope of 40 dB/decade and a feedback loop formed around the LPV531 may oscillate. The LPV531 is internally compensated in such a manner that it will be stable for load capacitances up to 100 pF.

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When the power setting of the LPV531 is reduced, both the transconductance of the input stage and the transconductance of the output stage will scale lineary with the power level to lower levels. This means that both the unity gain frequency and the pole to the transconductance of the output stage and the load capacitance will move down. Because both the unity gain frequency and the output pole move down in similar amounts, the stability of the LPV531 is still the same. This is shown in Figure 41 which gives the phase margin as a function of the load capacitance in the low power mode (5 µA), mid-power mode (40 µA) and high power mode (400 µA). Though the power level and unity gain frequency move with about two decades, the phase margin as a function of the capacitive load is hardly affected. This means that when the LPV531 is stable in an application circuit with a given load capacitance in the high power mode, the circuit will remain stable with the same capacitive load connected when the power level is reduced.

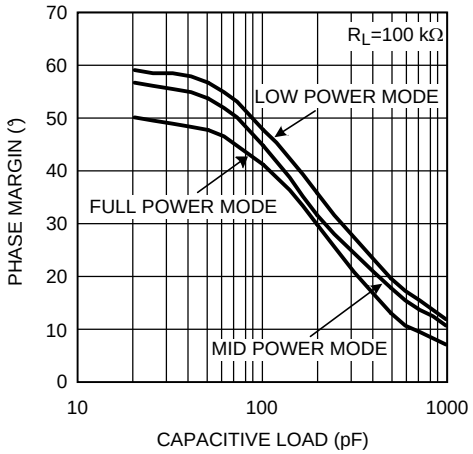


Figure 41. Phase Margin vs. Capacitive Load

Figure 42 shows a method that is sometimes used to allow an op amp to drive larger capacitors than it was originally designed to do. The capacitive load is isolated from the output of the op amp with an isolation resistor (R_{ISO}). This moves the output pole, that was originally located at $g_{m,out}/C_l$, to a higher frequency. This method requires that the value of R_{ISO} is in the same order of magnitude as $1/g_{m,out}$. For the LPV531, this method will not be effective when used across a broad range of power levels. This is because the high power mode will require a relatively small value for R_{ISO}, while such a small R_{ISO} will be ineffective at low power levels. In most applications this should not be a problem as the LPV531 can drive sufficient capacitive loads without the need for an external isolation resistor.

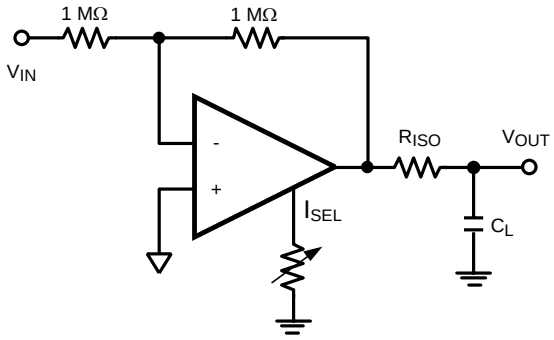
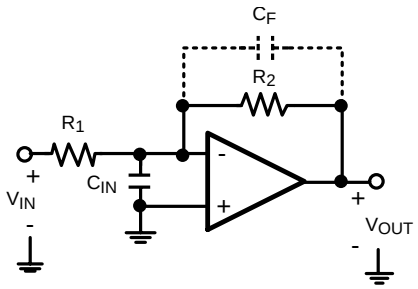


Figure 42. Compensation by Isolation Resistor

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INPUT CAPACITANCE AND FEEDBACK CIRCUIT ELEMENTS

The LPV531 has a very low input bias current (50 fA). To obtain this performance a large CMOS input stage is used, which adds to the input capacitance of the op amp, C_{IN}. Though this does not affect the DC and low frequency performance, at higher frequencies the input capacitance interacts with the input and the feedback impedances to create a pole, which results in lower phase margin and gain peaking. The gain peaking can be reduced by carefully choosing the appropriate feedback resistor, as well as, by using a feedback capacitance, C_F. For example, in the inverting amplifier shown in Figure 43, if C_{IN} and C_F are ignored and the open loop gain of the op amp is considered infinite then the gain of the circuit is $-R_2/R_1$. An op amp, however, usually has a dominant pole, which causes its gain to drop with frequency. Hence, this gain is only valid for DC and low frequency. To understand the effect of the input capacitance coupled with the non-ideal gain of the op amp, the circuit needs to be analyzed in the frequency domain using a Laplace transform.



$$A_V = - \frac{V_{OUT}}{V_{IN}} = - \frac{R_2}{R_1}$$

Figure 43. Inverting Amplifier

For simplicity, the op amp is modeled as an ideal integrator with a unity gain frequency of A_0 . Hence, its transfer function (or gain) in the frequency domain is A_0/s. Solving the circuit equations in the frequency domain, ignoring C_F for the moment, results in the following equation for the gain:

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{\left[1 + \frac{s}{\left(\frac{A_0 R_1}{R_1 + R_2}\right)} + \frac{s^2}{\left(\frac{A_0}{C_{IN} R_2}\right)}\right]} \tag{6}$$

It can be inferred from the denominator of the transfer function that it has two poles, whose expressions can be obtained by solving for the roots of the denominator:

$$P_{1,2} = \frac{-1}{2C_{IN}} \left[\frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)^2 - \frac{4\,A_0 C_{IN}}{R_2}} \right] \tag{7}$$

Equation 7 shows that as the values of R_1 and R_2 are increased, the magnitude of the poles is reduced, and hence the bandwidth of the amplifier is decreased. Furthermore, R_1 and R_2 are related by the gain of the amplifier.

$A_V = -R_2/R_1$, or alternatively

$R_2 = -A_V R_1$

It is the presence of pairs of poles in Equation 7 that causes gain peaking. In order to eliminate this effect, the poles should be placed in Butterworth position, since poles in Butterworth position do not cause gain peaking. To achieve a Butterworth pair, the quantity under the square root in Equation 7 should be set to equal −1. Using this fact and the relation between R_1 and R_2, the optimum value for R_1 can be found. This is shown in Equation 8. If R_1 is chosen to be larger than this optimum value, gain peaking will occur.

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$$R_1 < \frac{(1 - A_V)^2}{2A_0A_VC_{IN}} \quad (8)$$

In Figure 43, C_F is added to compensate for input capacitance and to increase stability. In addition, C_F reduce or eliminates the gain peaking that can be caused by having a larger feedback resistor.

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REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	20

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LPV531MK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	AV2A	Samples
LPV531MKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	AV2A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

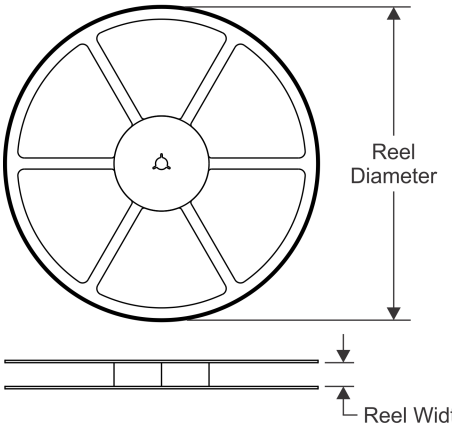
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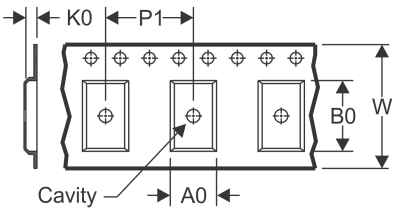
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

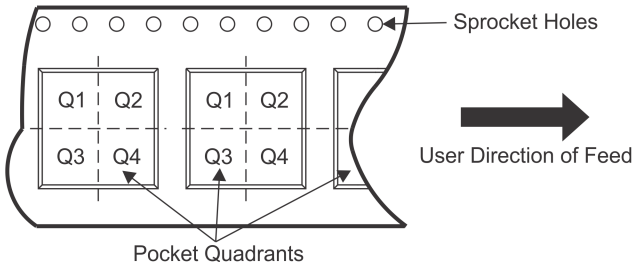


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

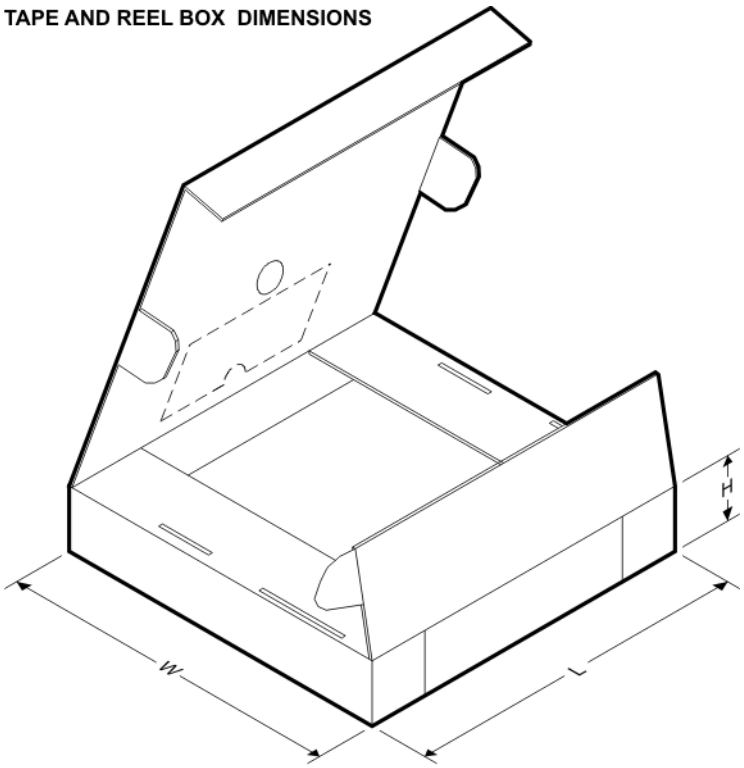
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV531MK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV531MKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

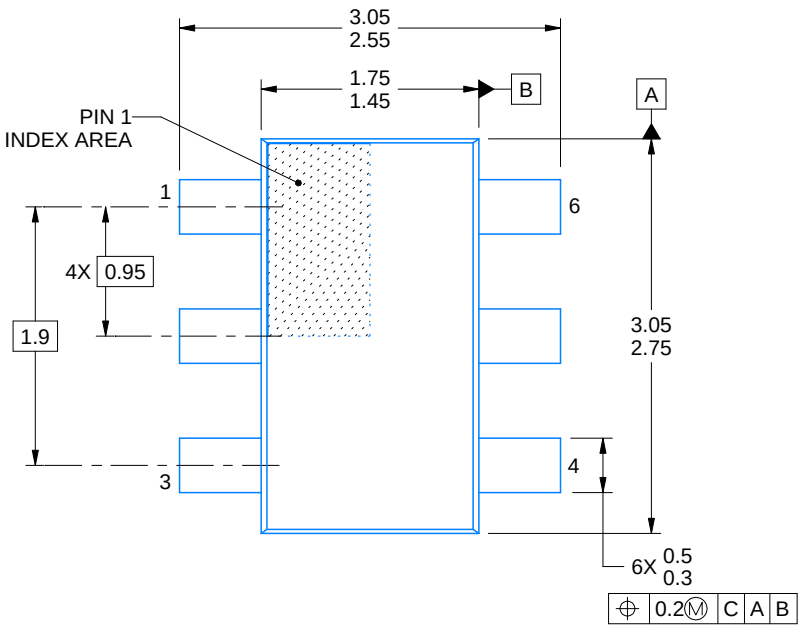
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV531MK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LPV531MKX/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0

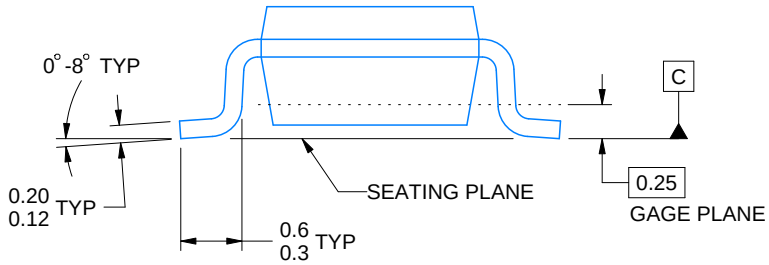
PACKAGE OUTLINE

DDC0006A

SOT - 1.1 max height

SOT

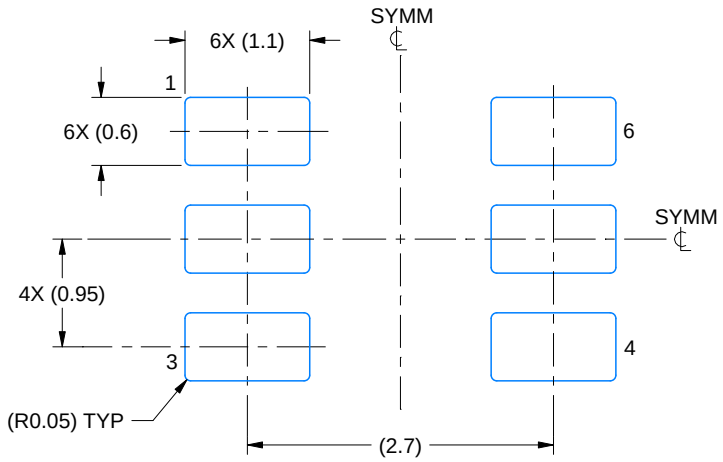




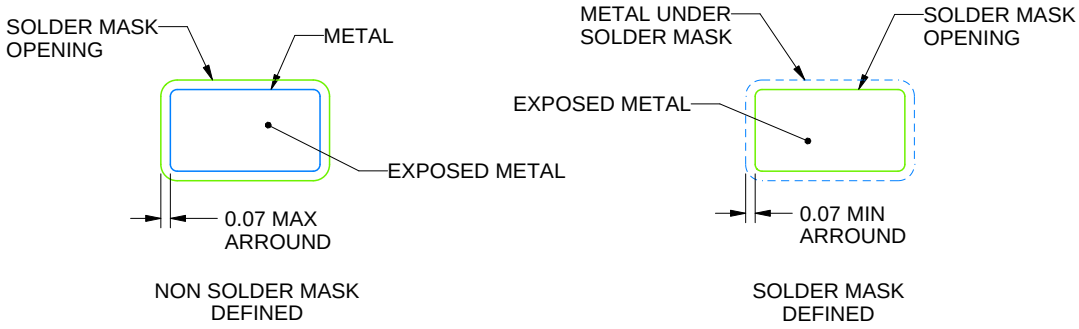
4214841/A 08/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

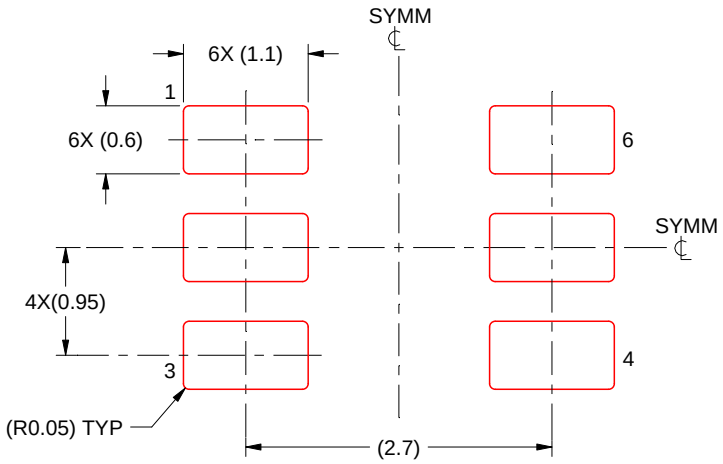


SOLDERMASK DETAILS

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NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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