Keywords: Sub-1V voltage reference, low dropout, low impedance

APPLICATION NOTE 5710

AN ACCURATE, LOW-IMPEDANCE, LOW-DROPOUT, SUB-1V BANDGAP REFERENCE IS COMPACT AND PROLONGS BATTERY LIFE

Abstract: A compact, accurate, sub-1V, low-impedance, low-dropout bandgap reference is presented in this paper. The circuit concept presented here is a sub-1V (0.9V in the design example) bandgap reference that can be set from a bit above V_{BE}, depending on the operating temperature range, and up to the normal bandgap voltage. The circuit idea is realized in 90nm BiCMOS technology. Simulation results show that over a 200°C temperature range, the proposed circuit can achieve 15ppm over line and load regulation. The core can be realized in a CMOS process using parasitic pnp devices.

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Introduction

A voltage reference is a critical building block in most analog circuits. In battery-operated, portable applications the minimum system voltage is continuously being lowered to prolong battery life. The theoretical minimum supply needed for analog circuitry is a threshold plus the saturation voltage of a current source, usually V_{DSSAT}. For BiCMOS processes, or CMOS processes with parasitic pnp transistors, the minimum operating voltage will be $V_{BE} + V_{DSSAT}$, assuming that the CMOS VT threshold is lower than V_{BE}.

In this article a new bandgap reference core is presented that can be set anywhere between slightly above V_{BE} to V_{BG}. The lowest output voltage (V_0) depends on the lowest temperature that needs to be covered. The design examples below will show that these configurations approach the theoretical minimum operating voltage by 50mV to 100mV from -50°C to +150°C.

Sub-1V voltage references have been realized in different ways before. Engineers have documented[1–5] various architectures in current mode, where CTAT and PTAT currents are generated and added together to a resistor to generate a reference voltage. However, it was shown[6] that those configurations have high noise due to the current mirrors. Because of the mirror mismatches, it is difficult to get the same accuracy using current mirrors compared to the normal bandgap configuration. Without trimming, a well-designed bandgap circuit can normally achieve 3% to 5% 6δ accuracy from -40°C to +125°C. Even with a reasonably high overdrive, it is difficult for the current mirrors to achieve this level of accuracy. If overdrive is increased for better matching, it also increases the necessary headroom as V_{DSSAT} is increased.

There is another way[6, 7] to generate a sub-1V reference. The reference voltage is expressed in Equation 1:

$$V_{REF} = kV_{BE} + \Delta V_{BE} = kV_{BE} + V_T \ln(N) \quad \text{(Eq. 1)}$$

where N is the ratio of the area of the two emitters.

As shown in Equation 1, the voltage is set in the 100mV to 200mV range. A presentation in 2006[7] gave the design example as N = 10, V_{REF}= 130mV.

A reference voltage close to ground is not desirable because the noise and the offset in the next stage will be proportionally larger than the reference voltage. Consequently, the overall accuracy deteriorates. This article presents a novel approach that resolves the aforementioned issues and provides superior performance. For example, a 0.9V reference can be generated with a 1.0V supply or lower, depending on the load.

The New Proposed Core for a Sub-1V Reference

A BiCMOS Process with npns

Figure 1 shows the proposed core.

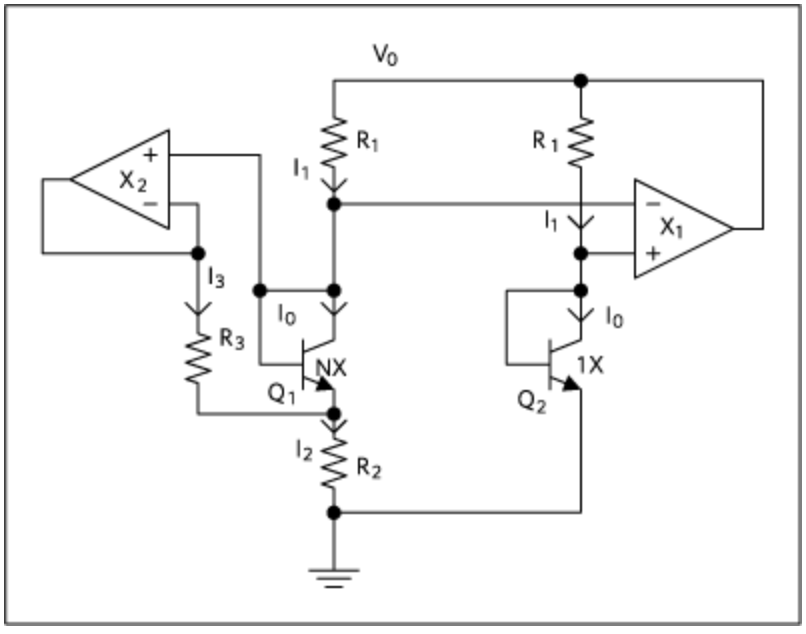

Figure 1. New bandgap core.

Mathematically, it can be shown that V_0 becomes a scaled version of the bandgap voltage, V_{BG}:

$$I_2 \times R_2 = \Delta V_{BE} = V_T \ln(N) \quad \text{(Eq. 2)}$$

$$V_0 = (1 - R_1/R_3) \times V_{BG} \quad \text{(Eq. 3)}$$

where:

$$V_{BG} = (V_{BG1} + V_T \times \ln N \times R_3/R_2 \times ((R_1 + R_2)/(R_3 - R_1)) \quad \text{(Eq. 3)}$$

The supply headroom requirement is $V_0 + V_{DSSAT}$, and the output is low impedance.

A CMOS Process with Parasitic pnps

A possible pnp version is shown in **Figure 2**.

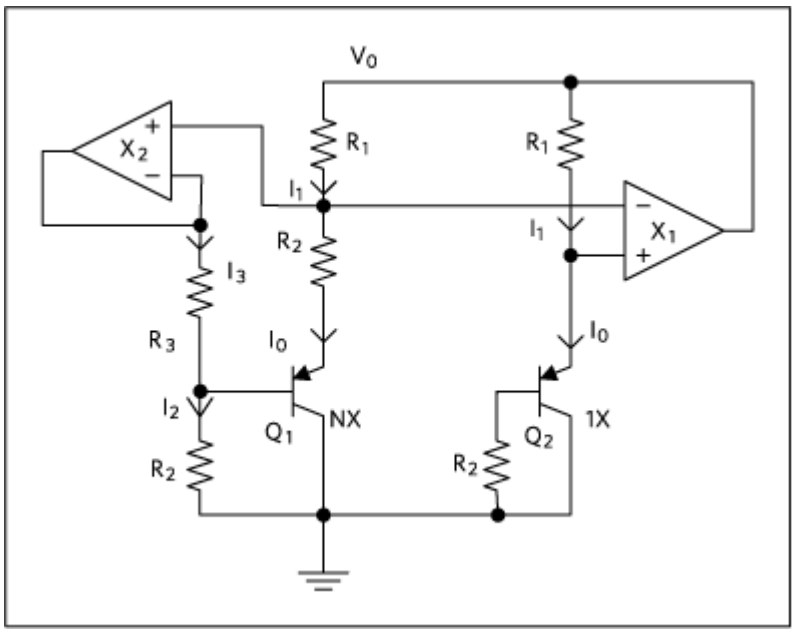

Figure 2. A pnp version for a CMOS process.

Design Example with Simulation Results

A simplified version of Figure 1 is shown in **Figure 3**; it saves an op amp (X2). The I_3 current can be generated by adding two resistors along with Q_3. In this case, I_4 can be set to I_0 at room temperature by choosing an appropriate R4, approximately equal to $R_1/2$. At other temperatures, I_4 will not be equal to I0, and this will introduce an error term. But since V_{BE} is a very weak function of I_0, therefore, the error is negligible. See **Figure 4**.

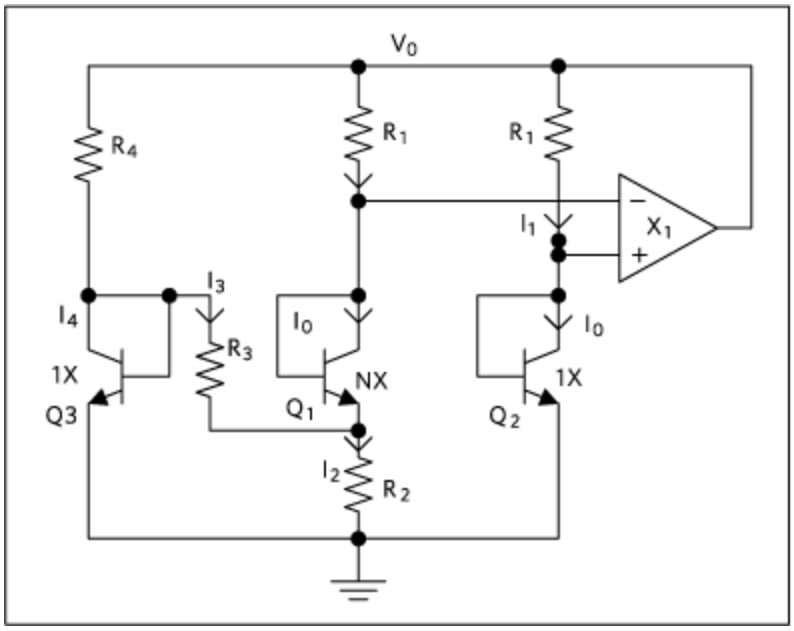

Figure 3. Simplified version of the proposed npn core.

As a design example for this core, V_0 = 0.9V is chosen.

For low-power applications, the quiescent current (I_Q) is targeted in the µA range. Based on the configuration in Figure 3, we have three variables, R_1, R_2, and R_3, and two equations, (Equation 3 and Equation 4), defined by V_0 and V_{BG}. Therefore, I2 is chosen to get one more equation to derive all three resistor values.

From Equation 3:

$$R_2 = (V_T \times \ln N)/I_2 \quad \text{(Eq. 5)}$$

From Equations 4 and 5:

$$R_1 = \frac{V_{BG} \times \left(1 - V_T \times \ln N / V_0\right) - V_{BE1}}{I_2 \times V_{BG}/V_0} \quad \text{(Eq. 6)}$$

$$R_3 = \frac{R_1}{1 - V_0/V_{BG}} \quad \text{(Eq. 7)}$$

There is no individual knob to control the output voltage and its TC separately. Here is the procedure to fine-

tune the circuit to the zero TC point and to obtain the desired output voltage.

1. Find the exact V_{BE1} voltage in simulation.
2. Find V_{BG} by adjusting R_2 until V_0 is zero TC. Now follow this procedure: increase R_2 if V_0 has a positive TC; decrease R_2 if V_0 has a negative TC. Note the value of zero TC V_0, then:
   $V_{BG} = V_0/(1 - R_1/R_3)$ (Eq. 8)
3. Recalculate R1, R2, and R3 using the new V_{BG} and V_{BE} values.
   V_{BG} = 1.203V
   V_{BE1} = 0.58V
   I_2 = 1.0µA
   N = 8
   $R_4 = ½R_1$ = 206kΩ.

The final calculated design parameters are shown in **Table 1**:

Table 1. Calculated Values for Design Example

°C	-55	25	150
V_{BE1}	0.74	0.58	0.33
V_{BG}	1.203	1.203	1.203
V_T	0.019	0.026	0.036906
I_2	7.32E-07	1.00E-06	1.42E-06
I_3	4.52E-07	3.55E-07	2.02E-07
I_0	2.79E-07	6.45E-07	1.22E-06
I_1	2.79E-07	6.45E-07	1.22E-06
R_1	4.120E+05	4.120E+05	4.120E+05
R_2	5.407E+04	5.407E+04	5.407E+04
R_3	1.636E+06	1.636E+06	1.636E+06
R_4	2.060E+05	2.060E+05	2.060E+05

Realizing Figure 3 in a 90nm BiCMOS process with transistor circuitry, the simulation results are plotted in **Figure 4**. The typical case is: supply voltage = 1.5V; output load = 10µA; all process corners (bipolar, CMOS, resistor, capacitor) having line and load combinations with supply voltage = (V_0 + 0.1V) and 1.65V; output load = 0µA and 20µA. The circuit has temperature compensation and 0.1% LSB trim. The results show that V_0 stays within 2.6mV, less than ±0.15% from -50°C to +150°C, or 15ppm over line and load. With processes variation and 0.1% LSB trimming, this bandgap voltage reference can achieve ±0.45% accuracy over 200°C temperature range.

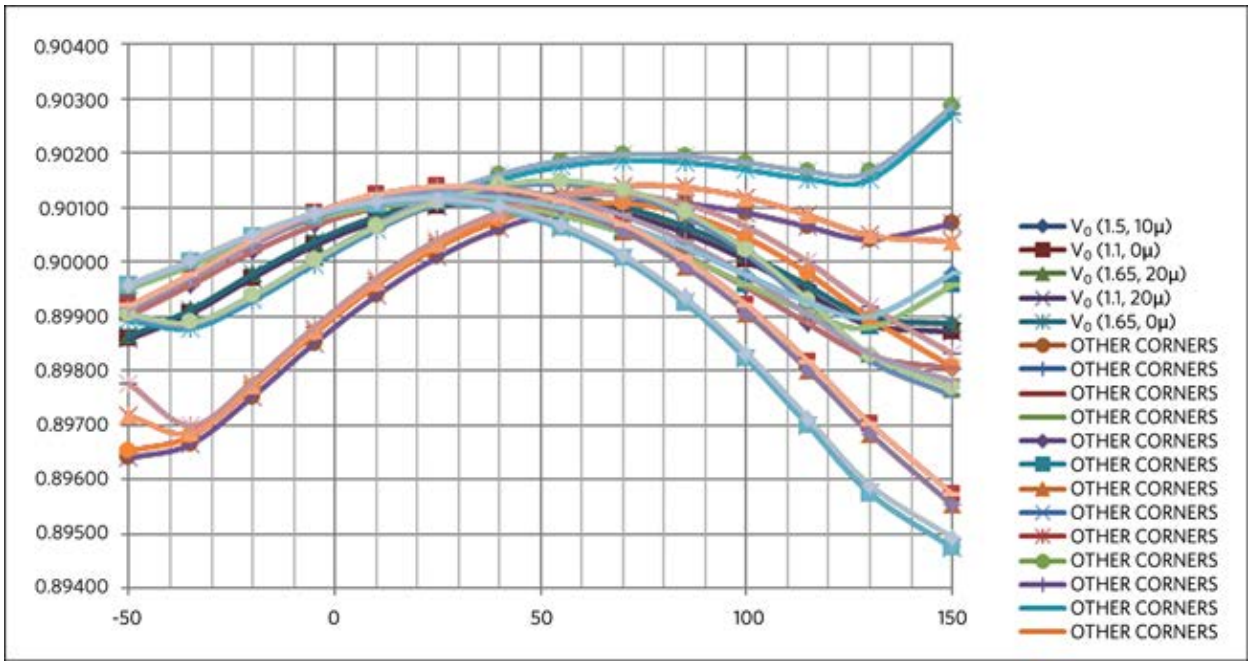

Figure 4. Simulation results of npn core.

Performance Comparison

Table 2 compares the performance of proposed cores with existing designs:

Table 2. Performance Comparison Table for Different Sub-1V Bandgap Circuits

	Proposed Core	Reference 5	Reference 3	Reference 6
Tech/m	90n BiCMOS	500n CMOS	600n CMOS	500n BiCMOS
V_{DD}/V	1-1.65*	0.93-5	0.98-1.5	1 up
V_{REF}/mV	900	228	603	190.9
TC/ppm	15	34	34.7	11
I_Q/µA	6	28	18	20
PSRR/dB @100Hz @10kHz @1MHz	-84 -62.2 -28.6	-58 – -12	– -44 –	–
Noise/(nV/√ Hz) @100Hz	1573	200	–	40
Area/mm ^{2}	0.023**	0.0464	0.24	0.4

*It uses 1.65V devices, so the maximum voltage is 1.65V. If a 4.5V device is used, it can go up to 4.5V.
**Die size is based on placement of all components in corresponding wells with DRC cleaned.

Conclusion

This article shows an elegant way of creating a compact, sub-1V bandgap reference in a low-dropout and low-impedance configuration. This proposed solution has a superior accuracy of about 20ppm with load, line regulation, and temperature variation. The headroom requirement approaches the theoretical minimum. The die size is comparable with a traditional bandgap reference with three more components (2 resistors and 1 npn). This design is small and can enhance the circuitry working with a lower battery voltage that is beneficial, even critical to portable designs.

References

1. H. Banba et al, “A CMOS bandgap reference circuit with sub-1-V operation,” **IEEE J. Solid State Circuits**, vol. 34, no. 5, pp. 670-674, May 1999.
2. P. Malcovati et al., “Curvature compensated BiCMOS bandgap with 1-V supply voltage,” **IEEE J. Solid-State Circuits**, vol. 36, no. 7, pp. 1076-1081, Jul 2001.
3. K.N. Leung and Philip K. T. Mok, “A sub-1-V 15ppm/C CMOS bandgap voltage reference without requiring low threshold voltage device,” **IEEE J. Solid-State Circuits**, vol. 37, no. 4 pp. 526-530, Apr, 2002.
4. Zhidong Liu and Yuhua Cheng, “A Sub-1V CMOS Bandgap Reference with High-order Curvature Compensation,” **IEEE International Conference of Electron Devices and Solid-State Circuits**, 2009 EDSSC.
5. David C. W. Ng, David K. K. Kwong, and Ngai Wong, “A sub-1V, 26uW, low-output-impedance CMOS Bandgap Reference with a low Dropout or Source Follower Mode,” **IEEE Transactions on VLSI Systems**, Vol. 19, No. 7 July 2011.
6. Keith Sanborn, Dongsheng Ma, and Vadim Ivanov, “A sub-1-V Low-Noise Bandgap Voltage Reference,” **IEEE Journal of Solid-State Circuits**, vol. 42, no. 11, November 2007.
7. I.M. Filanovsky, V. Ivanov, K.E. Sanborn, University of Alberta, Edmonton, Canada, Texas Instruments, “Sub-1V Supply Bandgap voltage references based on Asymmetric Differential Pair,” **49th IEEE International Midwest Symposium on Circuits and Systems** (MWSCAS), Vol. 2, 2006.

General References

G. Giustolisi, G. Palumbo, M. Criscione, and F. Cutri, “A low-voltage low-power voltage reference based on subthreshold MOSFETs,” **IEEE Journal of Solid-State Circuits**, Vol. 38, No. 1, pp. 151-154 January 2003.

Giuseppe De Vita and Giuseppe Iannaccone, “A sub1V, 10ppm/C, Nanopower Voltage Reference Generator,” **IEEE Journal of Solid-State Circuits**, Vol. 42. No 7, pp. 1536-1542, July 2007.

Related Parts		
MAX6023	Precision, Low-Power, Low-Dropout, UCSP Voltage Reference	Free Samples
MAX6034	Precision, Micropower, Low-Dropout, SC70 Series Voltage Reference	Free Samples
MAX6035	High-Supply-Voltage, Precision Voltage Reference in SOT23	Free Samples
MAX6100	Low-Cost, Micropower, Low-Dropout, High-Output-Current, SOT23 Voltage References	Free Samples
MAX6101	Low-Cost, Micropower, Low-Dropout, High-Output-Current, SOT23 Voltage References	Free Samples
MAX6102	Low-Cost, Micropower, Low-Dropout, High-Output-Current, SOT23 Voltage References	Free Samples
MAX6103	Low-Cost, Micropower, Low-Dropout, High-Output-Current, SOT23 Voltage References	Free Samples
MAX6104	Low-Cost, Micropower, Low-Dropout, High-Output-Current, SOT23 Voltage References	Free Samples
MAX6105	Low-Cost, Micropower, Low-Dropout, High-Output-Current, SOT23 Voltage References	Free Samples
MAX6106	Low-Cost, Micropower, Low-Dropout, High-Output-Current, SOT23 Voltage References	Free Samples
MAX6107	Low-Cost, Micropower, Low-Dropout, High-Output-Current, SOT23 Voltage References	Free Samples

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