

AN-1717 LM2833X MSOP-PowerPAD Demo Board

1 Introduction

The LM2833X MSOP-PowerPAD demo board is designed to demonstrate the capabilities of the LM2833X 1.5 MHz switching regulator in an MSOP-PowerPAD-10 package.

The demo board is configured to provide an output of 1.2 V at up to 3A from an input voltage range of 3 V to 5.5 V. The board is thermally optimized with the small solution size of 1.2" X 1.1", shown in the demo board schematic in [Figure 1](#). The output voltage can be configured to a different value by changing the ratio between R1 and R2 according to [Equation 1](#):

$$R1 = R2 \times (V_{OUT} / V_{FB} - 1) \tag{1}$$

The feedback voltage VFB is regulated at 0.60 V typically.

C5 on the board is reserved for two purposes given different application scenarios. First, at high V_{OUT} applications, the control loop bandwidth is not as large as at low V_{OUT} . Adding C5 at high V_{OUT} can significantly improve the load step response by boosting the loop bandwidth without significantly compromising phase margin. Secondly, it also helps to minimize output voltage overshoot during sluggish startup, short circuit release, and recovery from thermal shutdown, since it creates a feed-forward path between V_{OUT} and VFB, thus speeding up Gm-amplifier recovery. In practice, for a few k Ω of voltage divider bottom resistor R2, a 47nF ceramic capacitor is usually a good choice for C5. Note for applications where V_{OUT} is close to VFB, since R1 is small, the effectiveness of adding C5 becomes decreasingly appreciable. Therefore, other measures need to be taken to achieve the desired performance. For example, to minimize output overshoot during slow startup at high V_{OUT} , an alternative approach is to apply a separate signal at the EN terminal after V_{IN} is fully established.

Another component that is not populated on the board is C4, which is reserved for applications where a large output capacitor is desired.

[Table 1](#) lists the bill of materials (BOM) on this demo board. The measured performance characteristics and layout of this board are also included below.

2 Powering up the Board

Powering up the LM2833X MSOP-PowerPAD demo board is a single-step procedure, simply by applying a DC voltage of 3 V to 5.5 V to V_{IN} and GND terminals. By default, V_{INC} is connected to V_{IN} through a low pass filter to remove any high frequency noise present at the input. EN is connected to V_{INC} through a 100 k Ω resistor. A separate logic signal at the EN terminal can be used, if startup and shutdown need to be controlled. A load can be connected between V_{OUT} and GND terminals before or after the board is powered up. At V_{OUT} of 1.2 V, the internal soft-start circuit can bring up V_{OUT} smoothly regardless of load or input voltage.

The LM2833X is designed to skip some pulses at very light loads to maintain output voltage regulation. Depending on load levels, the circuit may operate in either discontinuous or continuous conduction mode.

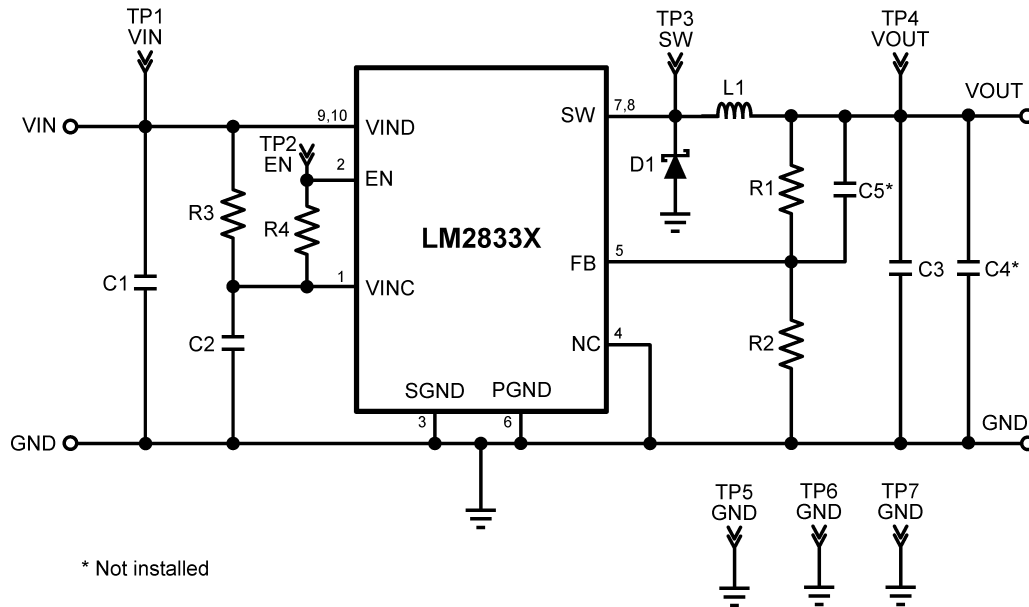
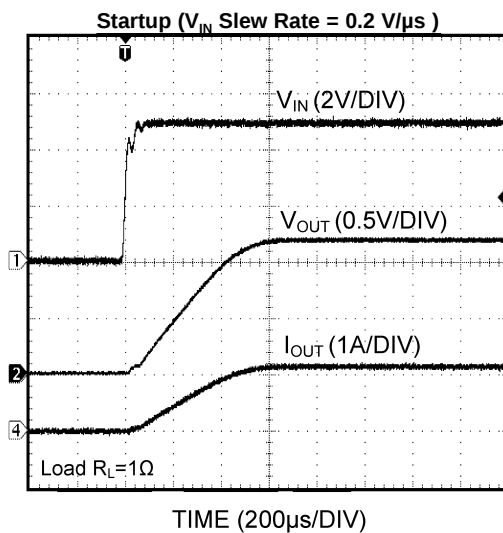
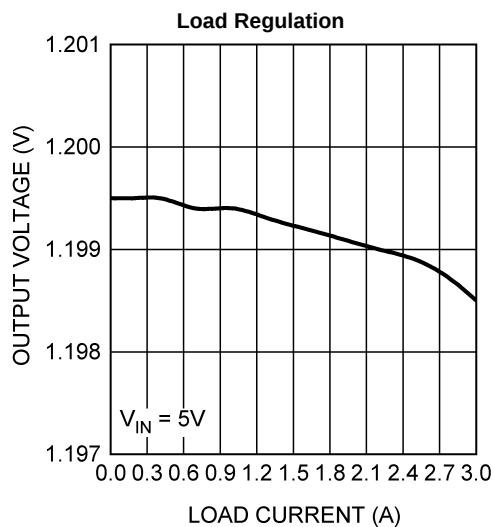
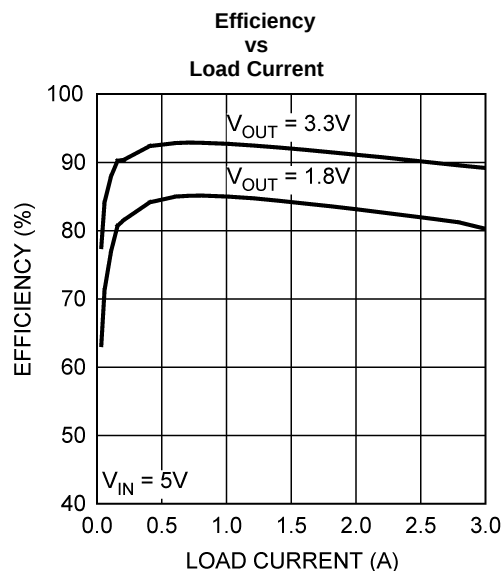
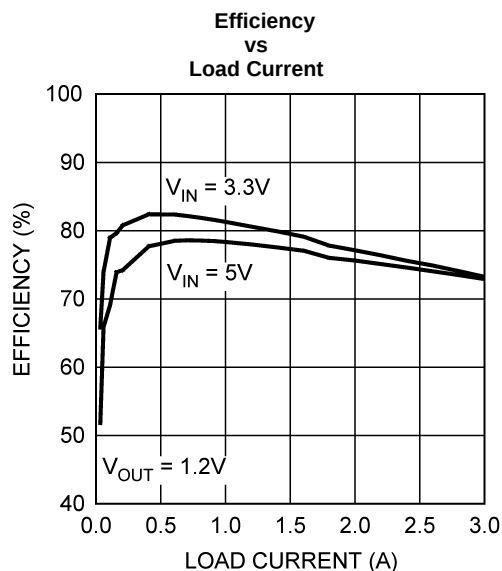
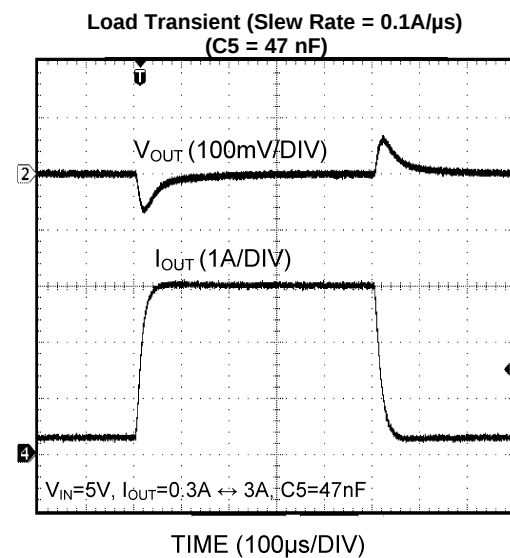
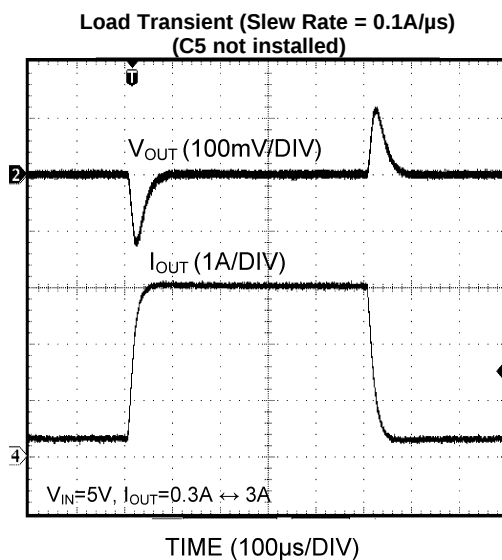
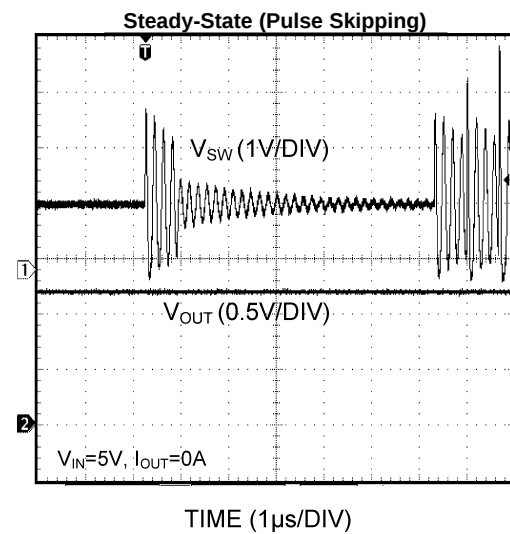
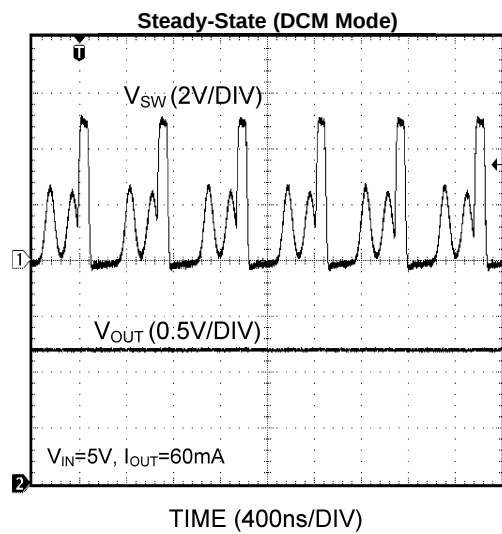
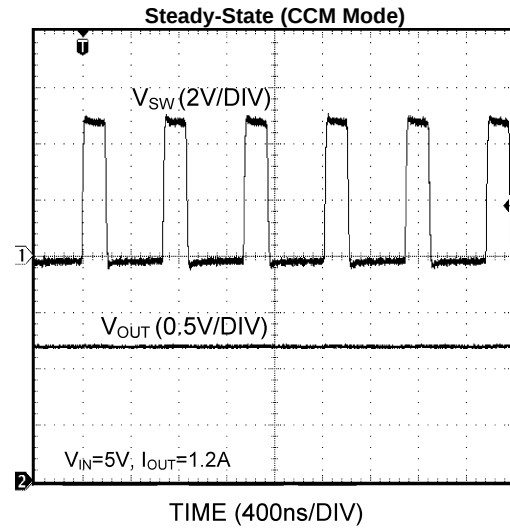
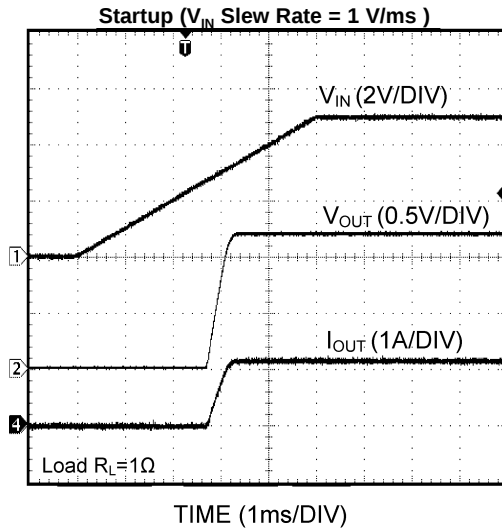
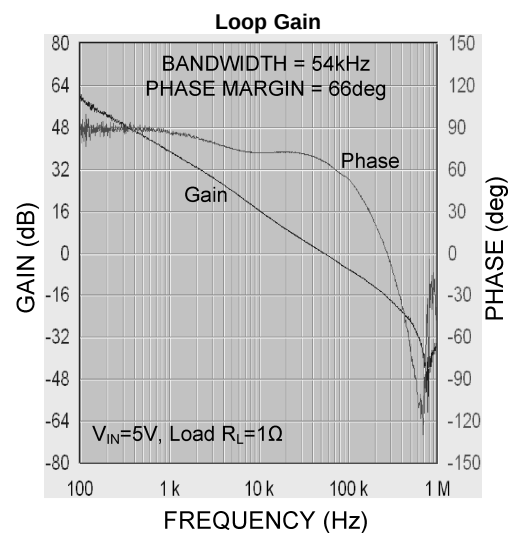
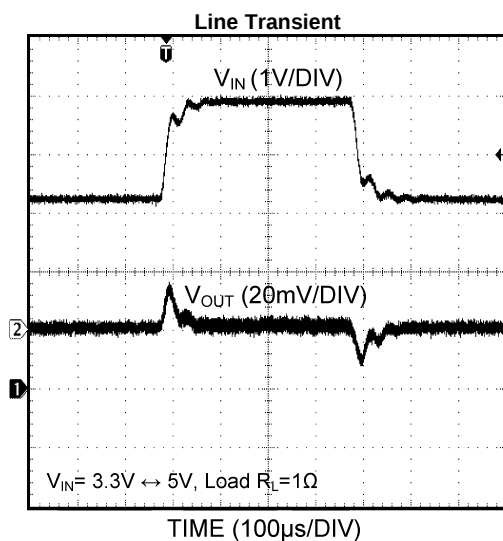


Figure 1. LM2833X MSOP-PowerPAD Demo Board Schematic

3 Typical Performance Characteristics







4 Bill of Materials (BOM)

Table 1. Bill of Materials (BOM)

Part ID	Part Value	Part Number	Manufacturer
U1	1.5 MHz 3.0A buck regulator, MSOP-PowerPAD-10	LM2833	Texas Instruments
L1	1.8 μH, 3.6A, 5x5.2x2.2mm ³	LTF5022T-1R8N3R6	TDK
C1	22 μF, 6.3 V, X5R, 1206	C3216X5R0J226MT	TDK
C2	0.22 μF, 10 V, X7R, 0805	GRM216R71A224KC01D	Murata
C3	47 μF, 6.3 V, X5R, 1206	JMK316BJ476ML-T	Taiyo Yuden
C4	Open		
C5	Open		
D1	Schottky, 30 V, 3A, 3-4E1A	CMS01	Toshiba
R1	2.00 kΩ, 1%, 1/8W, 0805	CRCW08052K00FKEA	Vishay
R2	2.00 kΩ, 1%, 1/8W, 0805	CRCW08052K00FKEA	Vishay
R3	10.0 Ω, 1%, 1/8W, 0805	CRCW080510R0FKEA	Vishay
R4	100 kΩ, 1%, 1/8W, 0805	CRCW0805100KFKEA	Vishay

5 Layout

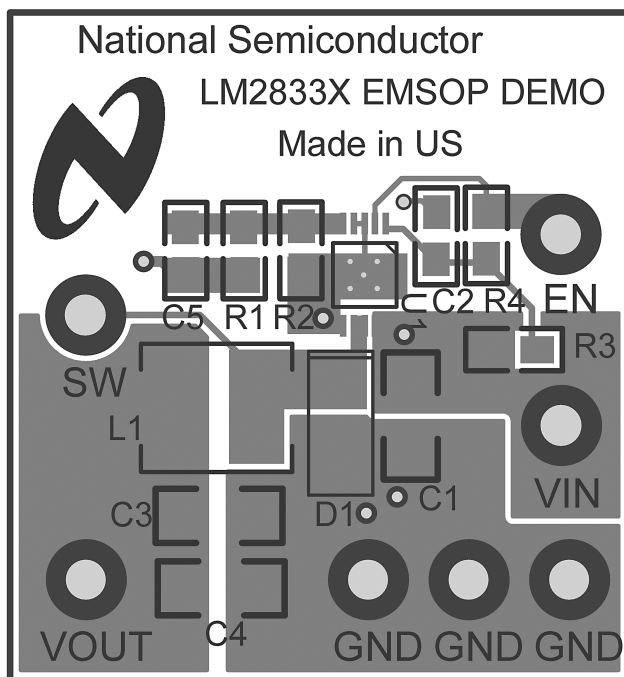


Figure 2. Top Layer and Top Overlay

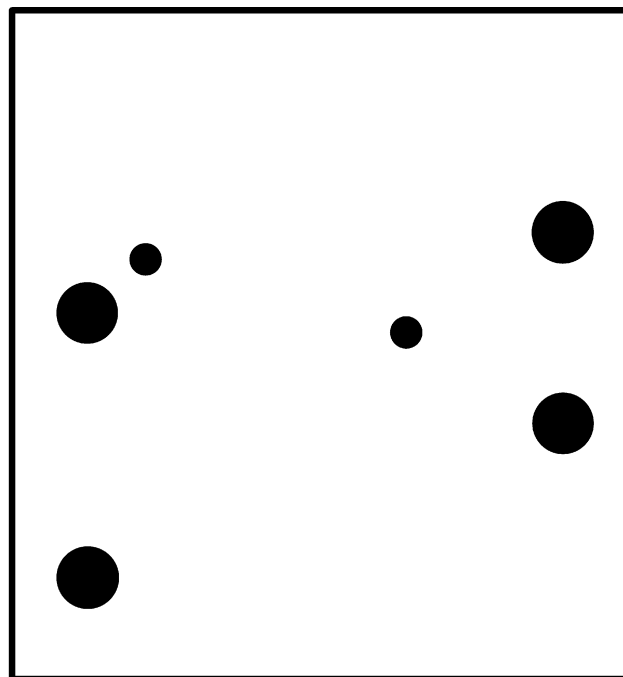


Figure 3. Internal Plane 1 (GND)

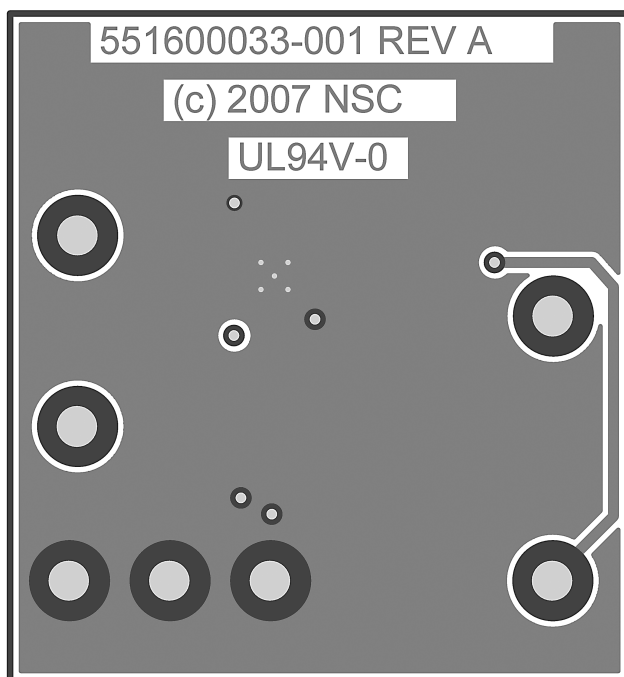


Figure 4. Bottom Layer

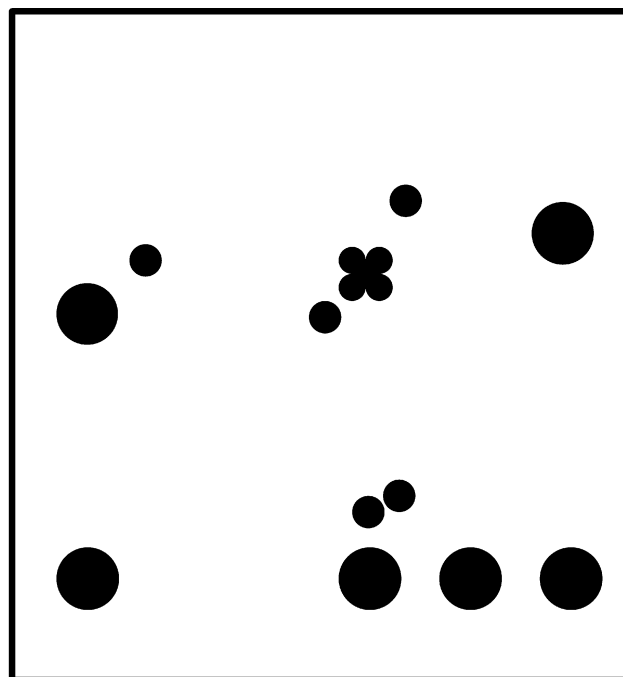


Figure 5. Internal Plane 2 (V_{IN})

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