3.3-V/5-V HIGH-SPEED DIGITAL ISOLATORS

FEATURES

- Controlled Baseline
  - One Assembly Site
  - One Test Site
  - One Fabrication Site
- Extended Temperature Performance of –55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- 4000-$V_{(peak)}$ Isolation
  - UL 1577, IEC 60747-5-2 (VDE 0884, Rev. 2) IEC 61010-1
  - 50-kV/μs Transient Immunity Typical
- Signaling Rate 0 Mbps to 150 Mbps
  - Low Propagation Delay
  - Low Pulse Skew (Pulse-Width Distortion)
- Low-Power Sleep Mode
- High Electromagnetic Immunity
- Low Input Current Requirement
- Failsafe Output
- Drop-In Replacement for Most Opto and Magnetic Isolators

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

APPLICATIONS

- Industrial Fieldbus
  - Modbus
  - Profibus
  - DeviceNet™ Data Buses
  - Smart Distributed Systems (SDS™)
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

DESCRIPTION/ORDER INFORMATION

The ISO721, ISO721M, ISO722, and ISO722M are digital isolators with a logic input and output buffer separated by a silicon oxide (SiO_2) insulation barrier. This barrier provides galvanic isolation of up to 4000 V. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground, and interfering with or damaging sensitive circuitry.

A binary input signal is conditioned, translated to a balanced signal, then differentiated by the capacitive isolation barrier. Across the isolation barrier, a differential comparator receives the logic transition information, then sets or resets a flip-flop and the output circuit accordingly. A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received for more than 4 μs, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

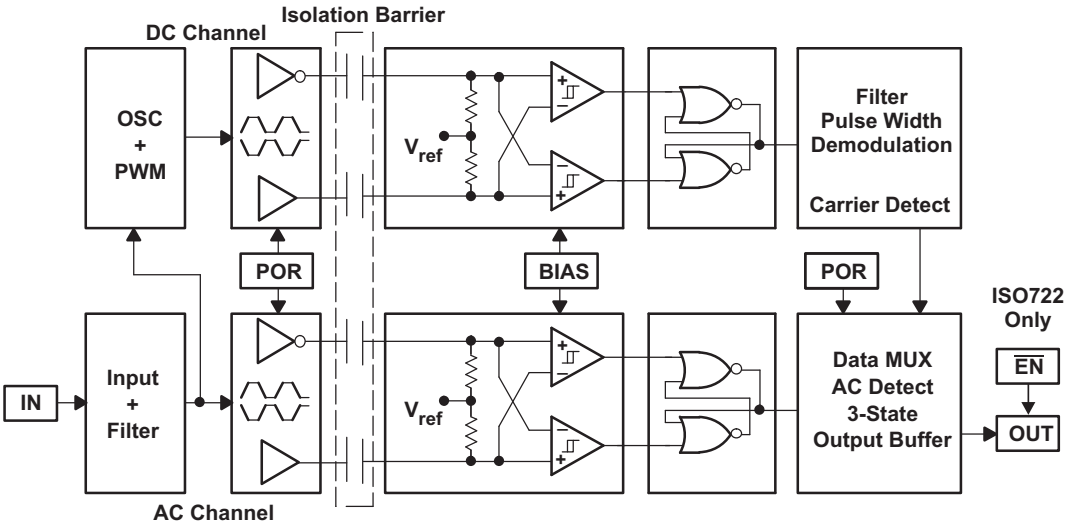
SDS is a trademark of Honeywell.
DeviceNet is a trademark of Open Devicenet Vendors Association, Inc.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2008, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTION DIAGRAM



The symmetry of the dielectric and capacitor within the integrated circuitry provides for close capacitive matching, and allows fast transient voltage changes between the input and output grounds without corrupting the output. The small capacitance and resulting time constant provide for fast operation with signaling rates(2) from 0 Mbps (dc) to 100 Mbps for the ISO721/ISO722, and 0 Mbps to 150 Mbps with the ISO721M/ISO722M.

These devices require two supply voltages of 3.3 V, 5 V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply and all outputs are 4-mA CMOS.

The ISO721 has TTL input thresholds and a noise-filter at the input that prevents transient pulses of up to 2 ns in duration from being passed to the output of the device.

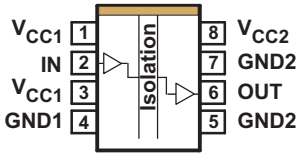
The ISO721M has CMOS $V_{CC}/2$ input thresholds, but do not have the noise filter and the additional propagation delay. These features of the ISO721M also provide for reduced jitter operation.

The ISO721M is characterized for operation over the ambient temperature range of –55°C to 125°C.

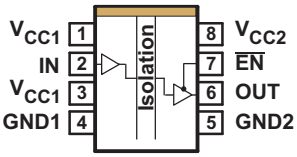
(2) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

Copyright © 2008, Texas Instruments Incorporated

D PACKAGE
ISO721, ISO721M
(TOP VIEW)



D PACKAGE
ISO722, ISO722M
(TOP VIEW)



AVAILABLE OPTIONS(1)

PRODUCT(2)	OUTPUT ENABLED	INPUT THRESHOLDS	NOISE FILTER	PACKAGE	TOP-SIDE MARKING	ORDERING NUMBER	GREEN
ISO721(3)	NO	TTL	YES	SOIC-8	-	-	Pb Free Sb/Br Free
ISO721M	NO	CMOS	NO	SOIC-8	721MEP	ISO721MMDREP (reel)	
ISO722(3)	YES	TTL	YES	SOIC-8	-	-	
ISO722M(3)	YES	CMOS	NO	SOIC-8	-	-	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Product Preview

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice: CA-5A	Recognized under 1577 Component Recognition Program(1)
File Number: 40014131	File Number: 1698195	File Number: E181974

(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

Copyright © 2008, Texas Instruments Incorporated

ABSOLUTE MAXIMUM RATINGS(1)

					UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}				–0.5 V to 6 V
V_I	Voltage at IN, OUT, or $\overline{EN}$ terminal				–0.5 V to 6 V
I_O	Output Current				±15 mA
ESD	Electrostatic discharge	Human-Body Model	JEDEC Standard 22, Test Method A114-C.01	All pins	±2 kV
		Charged-Device Model	JEDEC Standard 22, Test Method C101		±1 kV
T_J	Maximum junction temperature				170°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values. Vrms values are not listed in this publication.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage, V_{CC1}, V_{CC2}		4.5		5.5	V
			3		3.6	
I_{OH}	High-level output current				4	mA
I_{OL}	Low-level output current		-4			
t_{ui}	Input pulse width	ISO72x	10			ns
		ISO72xM	6.67			
V_{IH}	High-level input voltage (IN, $\overline{EN}$)	ISO72x	2		V_{CC}	V
V_{IL}	Low-level input voltage (IN, $\overline{EN}$)		0		0.8	
V_{IH}	High-level input voltage (IN, $\overline{EN}$)	IOS72xM	0.7 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage (IN, $\overline{EN}$)		0		0.3 V_{CC}	
T_J	Junction temperature	See the Thermal Characteristics table			150	°C
H	External magnetic field intensity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

IEC 60747-5-2 INSULATION CHARACTERISTICS(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATIONS	UNIT
V_{IORM}	Maximum working insulation voltage		560	V
V_{PR}	Input to output test voltage	After Input/Output Safety Test Subgroup 2/3 V_{PR} = V_{IORM} × 1.2, t = 10 s, Partial discharge < 5 pC	672	V
		Method a, V_{PR} = V_{IORM} × 1.6, Type and sample test with t = 10 s, Partial discharge < 5 pC	896	V
		Method b1, V_{PR} = V_{IORM} × 1.875, 100 % Production test with t = 1 s, Partial discharge < 5 pC	1050	V
V_{IOTM}	Transient overvoltage	t = 60 s	4000	V
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

Copyright © 2008, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} 5 V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, No load		0.5	1	mA
		25 Mbps			2	4	
I_{CC2}	V_{CC2} supply current	Quiescent	V_I = V_{CC} or 0 V, No load		8	12	mA
		25 Mbps	V_I = V_{CC} or 0 V, No load		10	14	
V_{OH}	High-level output voltage		I_{OH} = -4 mA, See Figure 1	V_{CC} – 0.8	4.6		V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1		0.2	0.4	V
			I_{OL} = 20 µA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN at 2 V			10	µA
I_{IL}	Low-level input current		IN at 0.8 V	–10			
I_{OZ}	High-impedance output current	ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}		1		µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 5	25	50		kV/µs

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} 5 V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 1		17		ns
t_{PHL}	Propagation delay , high-to-low-level output				17		
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$				0.5		
t_{PLH}	Propagation delay, low-to-high-level output	ISO721M		2	10	16	
t_{PHL}	Propagation delay, high-to-low-level output			2	10	16	
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$				0.5	1	
$t_{sk(pp)}$ (1)	Part-to-part skew					3	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See Figure 1		1		ns
t_f	Output signal fall time				1		
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-mpedance output	ISO722 ISO722M	See Figure 2		8		ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output				4		µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See Figure 3		8		ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output				5		µs
t_{fs}	Failsafe output delay time from input power loss		See Figure 4		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100 Mbps NRZ data input, See Figure 6		2		ns
			100 Mbps unrestricted bit run length data input, See Figure 6		3		
		ISO72xM	150 Mbps NRZ data input, See Figure 6		1		
			150 Mbps unrestricted bit run length data input, See Figure 6		2		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

Copyright © 2008, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, No load		0.5	1	mA
		25 Mbps			2	4	
I_{CC2}	V_{CC2} supply current	Quiescent	V_I = V_{CC} or 0 V, No load		4	6.5	mA
		25 Mbps	V_I = V_{CC} or 0 V, No load		5	7.5	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4	3		V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1		0.2	0.4	V
			I_{OL} = 20 µA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN at 2 V			10	µA
I_{IL}	Low-level input current		IN at 0.8 V	–10			
I_{OZ}	High-impedance output current	ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}		1		µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 5	25	40		kV/µs

SWITCHING CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 1		19		ns
t_{PHL}	Propagation delay , high-to-low-level output				19		
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$				0.5		
t_{PLH}	Propagation delay, low-to-high-level output	ISO721M		3	12	20	
t_{PHL}	Propagation delay, high-to-low-level output			3	12	20	
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$				0.5	1	
$t_{sk(pp)}$ (1)	Part-to-part skew					5	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See Figure 1		2		ns
t_f	Output signal fall time				2		
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-mpedance output	ISO722 ISO722M	See Figure 2		11		ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output				6		µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See Figure 3		13		ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output				6		µs
t_{fs}	Failsafe output delay time from input power loss		See Figure 4		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100 Mbps NRZ data input, See Figure 6		2		ns
			100 Mbps unrestricted bit run length data input, See Figure 6		3		
		ISO72xM	150 Mbps NRZ data input, See Figure 6		1		
			150 Mbps unrestricted bit run length data input, See Figure 6		2		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

Copyright © 2008, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, No load		0.3	0.5	mA
		25 Mbps			1	2	
I_{CC2}	V_{CC2} supply current	Quiescent	V_I = V_{CC} or 0 V, No load		8	12	mA
		25 Mbps	V_I = V_{CC} or 0 V, No load		10	14	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.8	4.6		V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1		0.2	0.4	V
			I_{OL} = 20 µA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN at 2 V			10	µA
I_{IL}	Low-level input current		IN at 0.8 V	–10			
I_{OZ}	High-impedance output current	ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}		1		µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 5	25	40		kV/µs

SWITCHING CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 1		17		ns
t_{PHL}	Propagation delay , high-to-low-level output				17		
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$				0.5		
t_{PLH}	Propagation delay, low-to-high-level output	ISO721M		3	12	21	
t_{PHL}	Propagation delay, high-to-low-level output			3	12	21	
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$				0.5	1	
$t_{sk(pp)}$ (1)	Part-to-part skew				0	5	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See Figure 1		1		ns
t_f	Output signal fall time				1		
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-mpedance output	ISO722 ISO722M	See Figure 2		9		ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output				5		µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See Figure 3		9		ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output				5		µs
t_{fs}	Failsafe output delay time from input power loss		See Figure 4		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100 Mbps NRZ data input, See Figure 6		2		ns
			100 Mbps unrestricted bit run length data input, See Figure 6		3		
		ISO72xM	150 Mbps NRZ data input, See Figure 6		1		
			150 Mbps unrestricted bit run length data input, See Figure 6		2		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

Copyright © 2008, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, No load		0.3	0.5	mA
		25 Mbps			1	2	
I_{CC2}	V_{CC2} supply current	Quiescent	V_I = V_{CC} or 0 V, No load		4	6.5	mA
		25 Mbps	V_I = V_{CC} or 0 V, No load		5	7.5	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4	3		V
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1		0.2	0.4	V
			I_{OL} = 20 µA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN at 2 V			10	µA
I_{IL}	Low-level input current		IN at 0.8 V	–10			
I_{OZ}	High-impedance output current	ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}		1		µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 5	25	40		kV/µs

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 1		20		ns
t_{PHL}	Propagation delay , high-to-low-level output				20		
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$				0.5		
t_{PLH}	Propagation delay, low-to-high-level output	ISO721M		3	12	25	
t_{PHL}	Propagation delay, high-to-low-level output			3	12	25	
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$				0.5	1	
$t_{sk(pp)}$ (1)	Part-to-part skew					5	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See Figure 1		2		ns
t_f	Output signal fall time				2		
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-mpedance output	ISO722 ISO722M	See Figure 2		13		ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output				6		µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output		See Figure 3		13		ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output				6		µs
t_{fs}	Failsafe output delay time from input power loss		See Figure 4		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100 Mbps NRZ data input, See Figure 6		2		ns
			100 Mbps unrestricted bit run length data input, See Figure 6		3		
		ISO72xM	150 Mbps NRZ data input, See Figure 6		1		
			150 Mbps unrestricted bit run length data input, See Figure 6		2		

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

Copyright © 2008, Texas Instruments Incorporated

PARAMETER MEASUREMENT INFORMATION

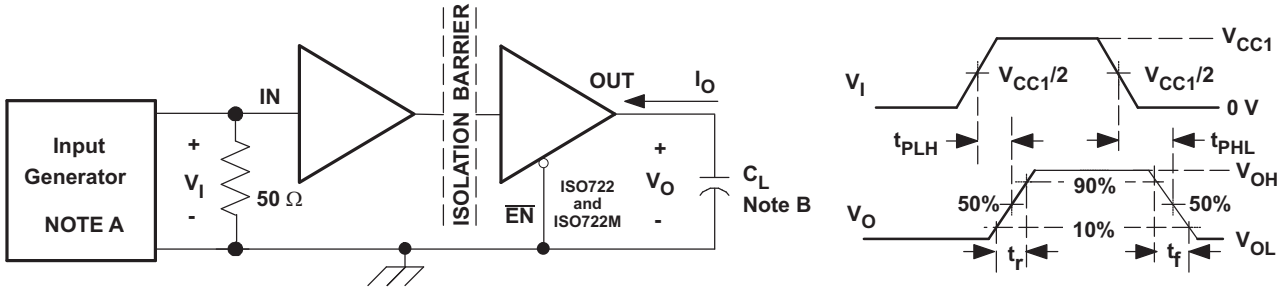


Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms

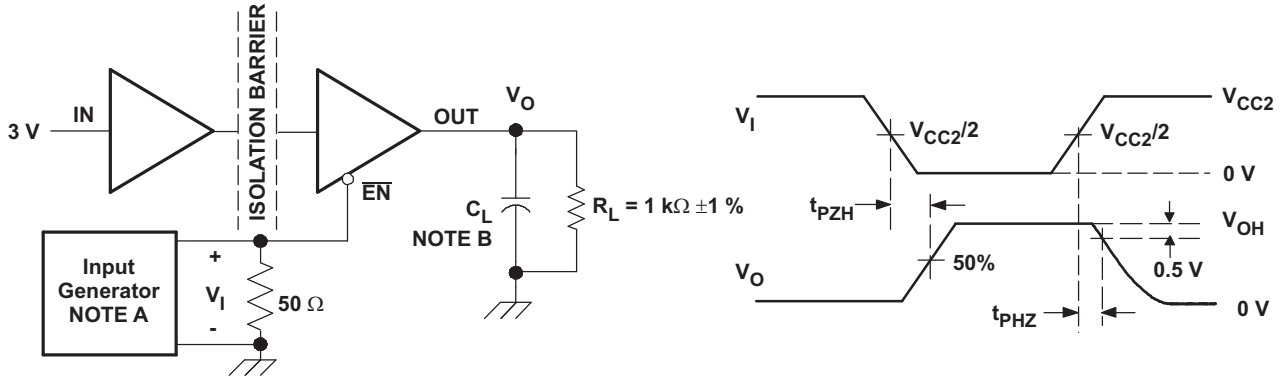
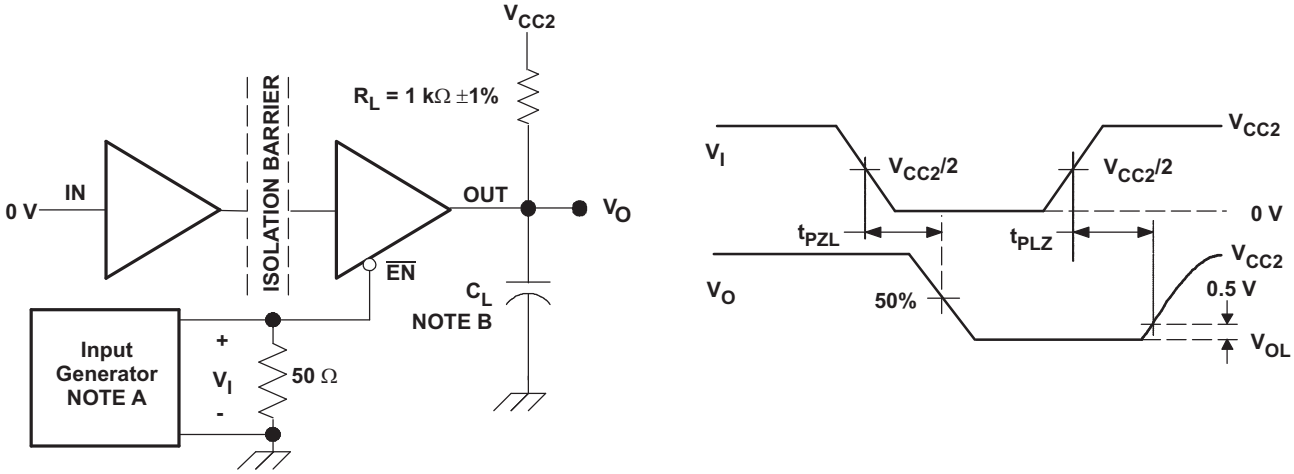


Figure 2. ISO722 Sleep-Mode High-Level Output Test Circuit and Voltage Waveforms

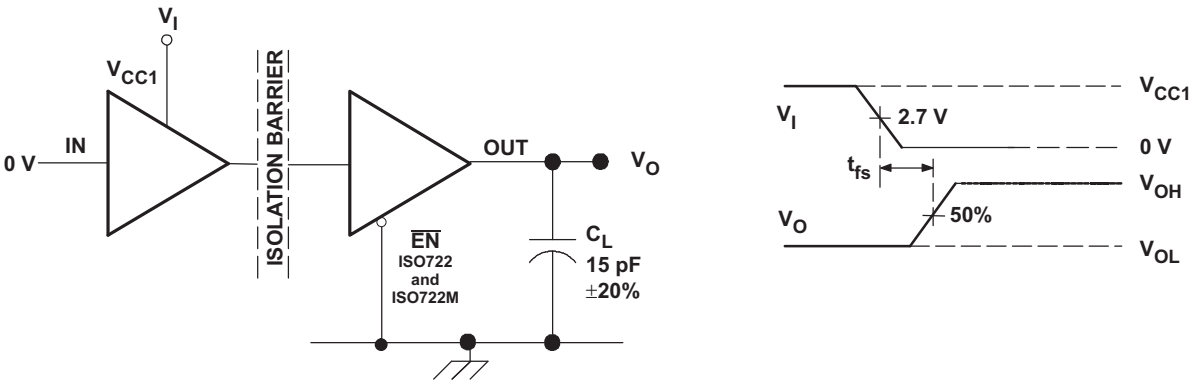


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

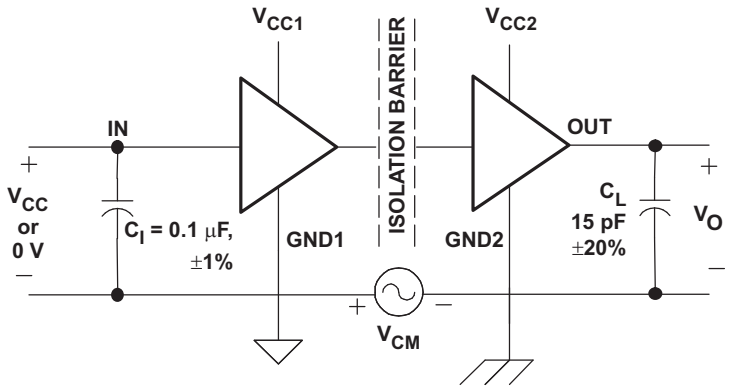
Figure 3. ISO722 Sleep-Mode Low-Level Output Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: V_I transition time is 100 ns

Figure 4. Failsafe Delay Time Test Circuit and Voltage Waveforms

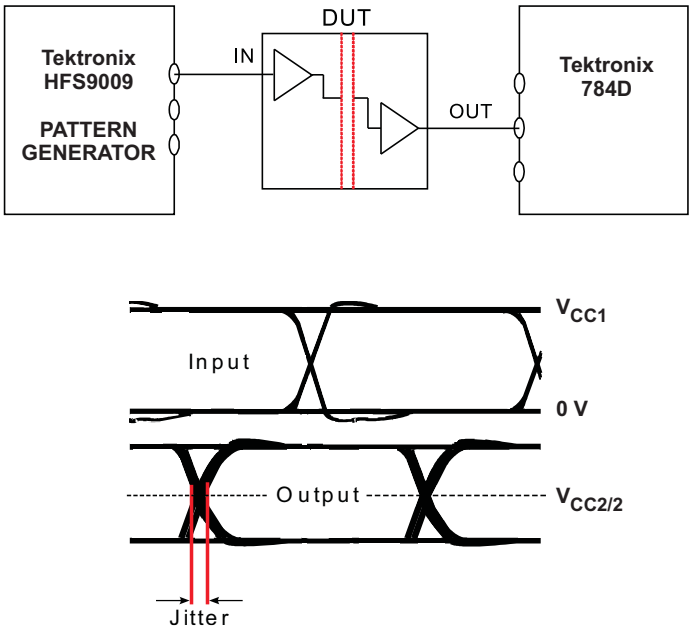


NOTE: Pass/Fail criteria is no change in V_O.

Figure 5. Common-Mode Transient Immunity Test Circuit and Voltage Waveform

Copyright © 2008, Texas Instruments Incorporated

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: Bit pattern run length is 2^{16} – 1. Transition Time is 800 ps. NRZ data input has no more than five consecutive ones or zeros.

Figure 6. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

DEVICE INFORMATION

PACKAGE CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(101)	Minimum air gap (Clearance) (1)	Shortest terminal to terminal distance through air	4.8			mm
L(102)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	4.3			mm
C_{TI}	Tracking resistance (comparative tracking index)	DIN IEC 60112/VDE 0303 Part 1	≥ 175			V
	Minimum internal gap (internal clearance)	Distance through insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T_A < 100 °C		$>10^{12}$		Ω
		Input to output, V_{IO} = 500 V, 100°C ≤ T_A< T_A max.		$>10^{11}$		Ω
C_{IO}	Barrier capacitance Input-to-output	V_I = 0.4 sin (4E6πt)		1		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)		1		pF

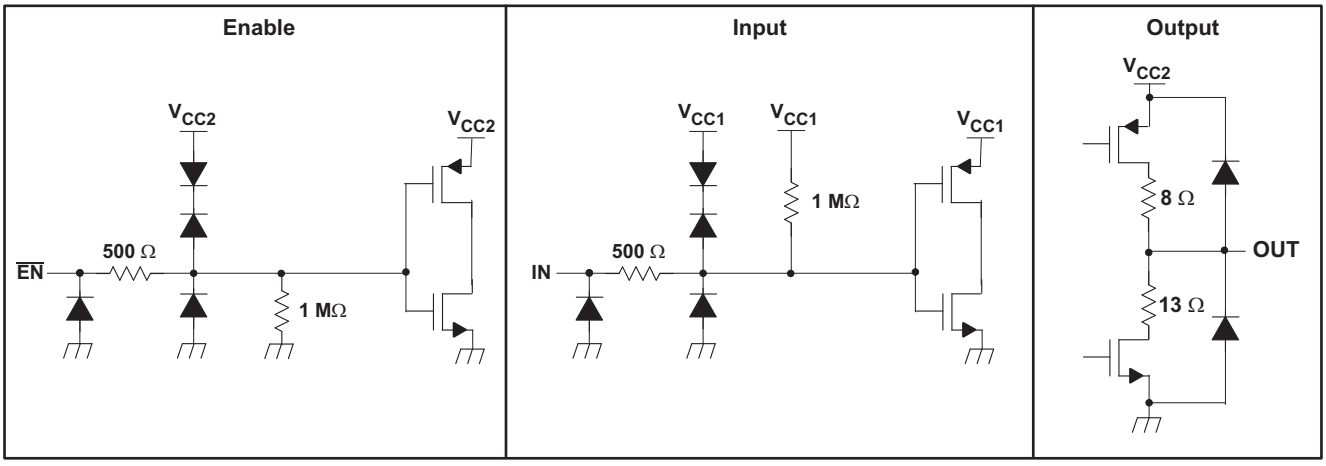
(1) Creepage and clearance requirements are applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.
Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	IIIa
Installation classification	Rated mains voltage ≤150 VRMS	I-IV
	Rated mains voltage ≤300 VRMS	I-III

DEVICE I/O SCHEMATIC

Equivalent Input and Output Schematic Diagrams



Copyright © 2008, Texas Instruments Incorporated

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply, and without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 263°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			100	mA
		θ_{JA} = 263°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C			153	
T_S	Maximum case temperature				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

THERMAL CHARACTERISTICS
(over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-Air		Low-K Thermal Resistance(1)		263		°C/W
			High-K Thermal Resistance(1)		125		°C/W
θ_{JB}	Junction-to-Board Thermal Resistance				44		°C/W
θ_{JC}	Junction-to-Case Thermal Resistance				75		°C/W
P_D	Device Power Dissipation	ISO72x	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 100 Mbps 50% duty cycle square wave			159	mW
		ISO72xM	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 150 Mbps 50% duty cycle square wave			195	

(1) Tested in accordance with the Low-K or High-K thermal metric definition of EIA/JESD51-3 for leaded surface mount packages.

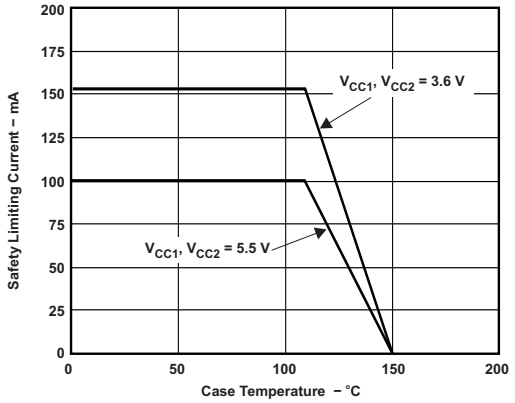


Figure 7. θ_{JC} THERMAL DERATING CURVE per IEC 60747-5-2

FUNCTION TABLE

ISO721 (1)

V_{CC1}	V_{CC2}	INPUT (IN)	OUTPUT (OUT)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = powered up (V_{CC} ≥ 3 V); PD = powered down (V_{CC} ≤ 2.5 V), X = irrelevant, H = high Level; L = low level

ISO722 (1)

V_{CC1}	V_{CC2}	INPUT (IN)	ISO722/ISO722M__ OUTPUT ENABLE ($\overline{EN}$)	OUTPUT (OUT)
PU	PU	H	L or Open	H
		L	L or Open	L
		X	H	Z
		Open	L or Open	H
PD	PU	X	L or Open	H
PD	PU	X	H	Z

(1) PU = powered up (V_{CC} ≥ 3 V); PD = powered down (V_{CC} ≤ 2.5 V), X = irrelevant, H = high Level; L = low level

Copyright © 2008, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS

RMS SUPPLY CURRENT vs SIGNALING RATE

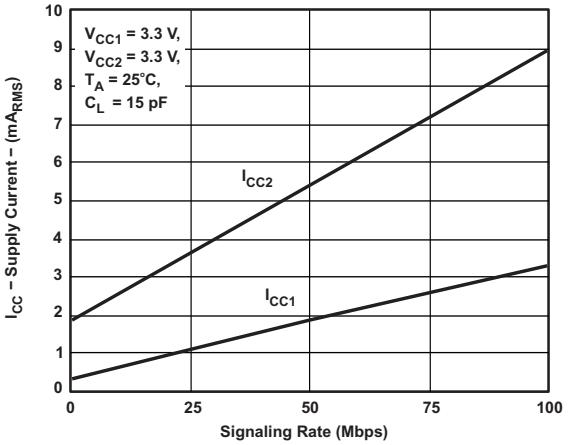


Figure 8.

RMS SUPPLY CURRENT vs SIGNALING RATE

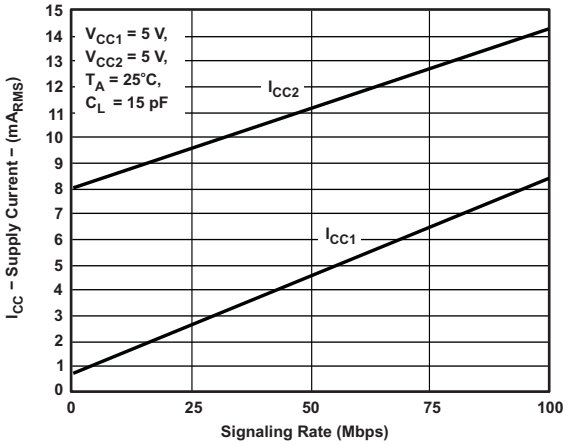


Figure 9.

PROPAGATION DELAY vs FREE-AIR TEMPERATURE

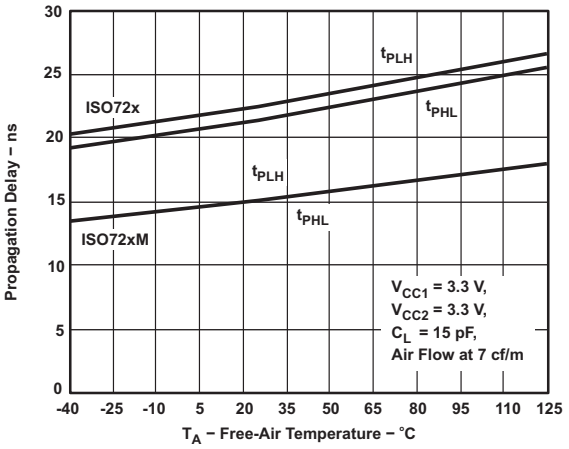


Figure 10.

PROPAGATION DELAY vs FREE-AIR TEMPERATURE

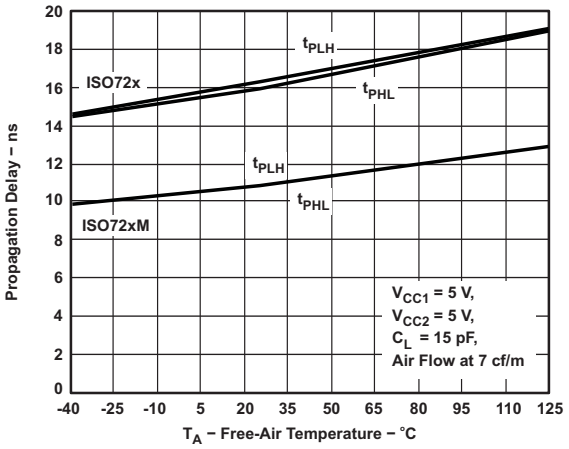


Figure 11.

ISO72x INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

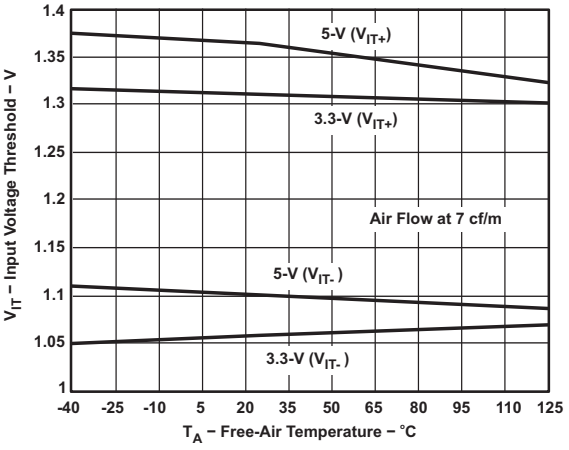


Figure 12.

ISO72xM INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

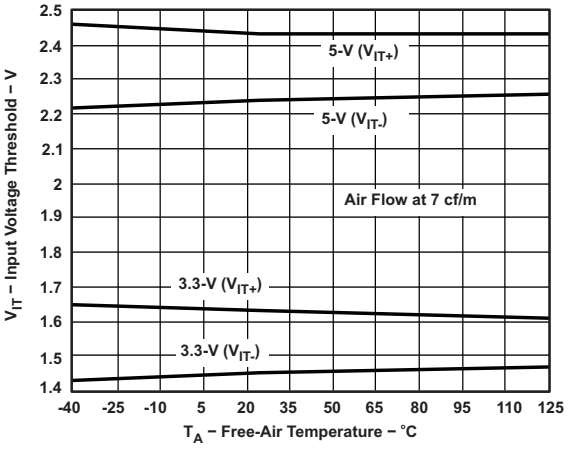


Figure 13.

Copyright © 2008, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

V_{CC1} FAILSAFE THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

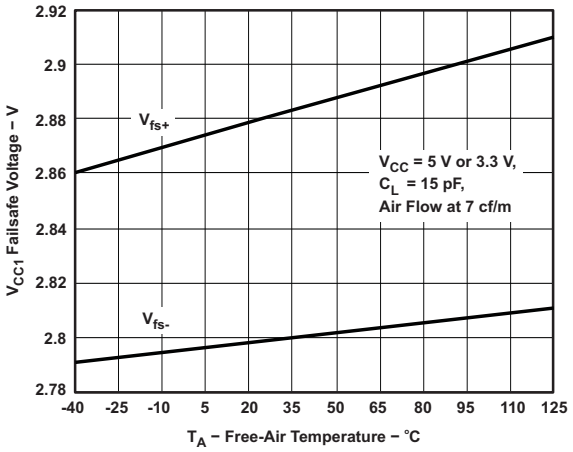


Figure 14.

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

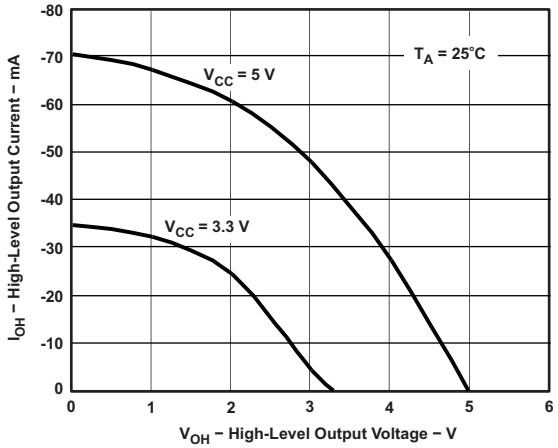


Figure 15.

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

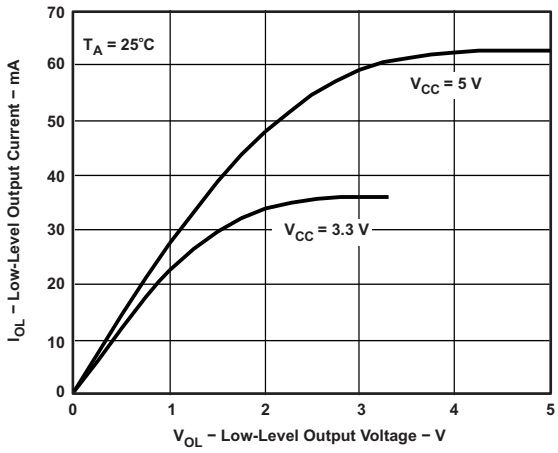


Figure 16.

Copyright © 2008, Texas Instruments Incorporated

APPLICATION INFORMATION

MANUFACTURER CROSS-REFERENCE DATA

The ISO72xx isolators have the same functional pinout as most other vendors, and they are often pin-for-pin drop-in replacements. The notable differences in the products are propagation delay, signaling rate, power consumption, and transient protection rating. Table 1 is used as a guide for replacing other isolators with the ISO72x family of single channel isolators.

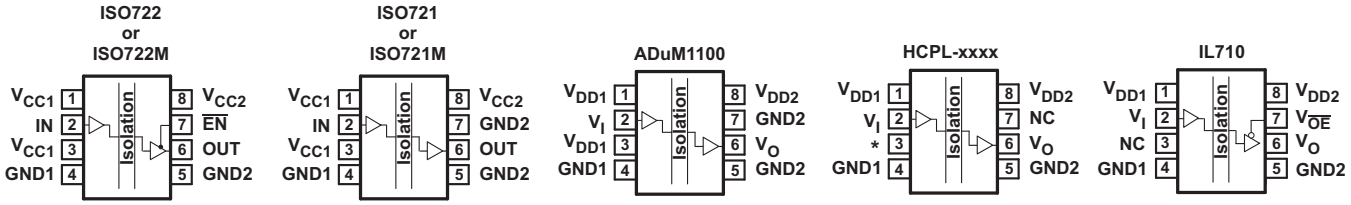


Figure 17. Pin Cross Reference

Table 1. CROSS REFERENCE

ISOLATOR	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7		PIN 8
							ISO721 OR ISO721M	ISO722 OR ISO722M	
ISO721(1)(2)	V_{CC1}	IN	V_{CC1}	GND1	GND2	OUT	GND2	$\overline{EN}$	V_{CC2}
ADuM1100(1)(2)	V_{DD1}	V_I	V_{DD1}	GND1	GND2	V_O	GND2		V_{DD2}
HCPL-xxxx	V_{DD1}	V_I	*Leave Open(3)	GND1	GND2	V_O	NC(4)		V_{DD2}
IL710	V_{DD1}	V_I	NC(5)	GND1	GND2	V_O	$V_{\overline{OE}}$		V_{DD2}

(1) The ISO72xx pin 1 and pin 3 are internally connected together. Either or both may be used as V_{CC1}.
(2) The ISO721 and ISO721M pin 5 and pin 7 are internally connected together. Either or both may be used as GND2.
(3) Pin 3 of the HCPL devices must be left open. This is not a problem when substituting an ISO72xx device since the extra V_{CC1} on pin 3 may be left an open circuit as well.
(4) An HCPL device PIN 7 must be left floating (open) or grounded when an ISO722 or ISO722M device is to be used as a drop-in replacement. If pin 7 of the ISO722 or ISO722M device is placed in a high logic state, the output of the device is disabled
(5) Pin 3 of the IL710 must not be tied to ground on the circuit board since this shorts the ISO72xx's V_{CC1} to ground. The IL710 pin 3 may only be tied to V_{CC} or left open to drop in an ISO72xx.

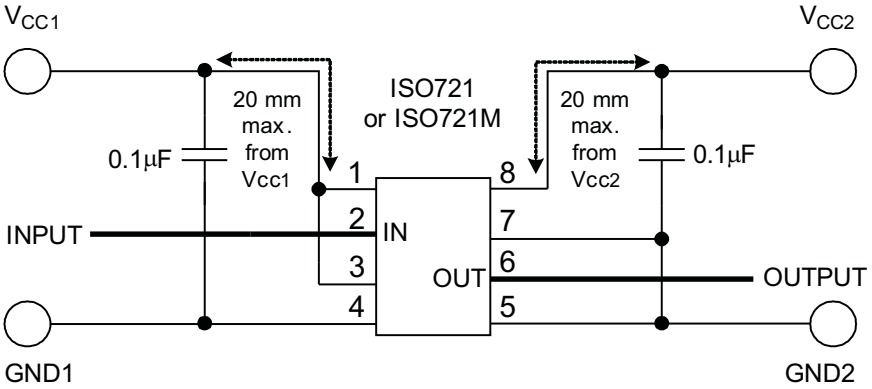
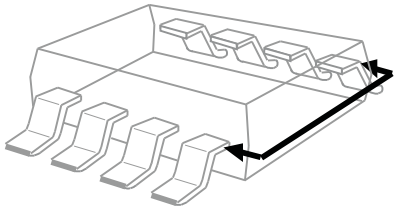


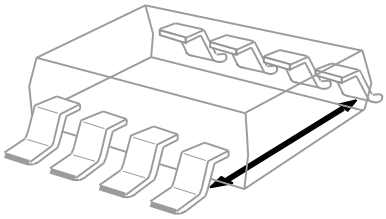
Figure 18. Basic Application Circuit

ISOLATION GLOSSARY

Creepage Distance — The shortest path between two conductive input-to-output leads measured along the surface of the insulation. The shortest distance path is found around the end of the package body.



Clearance — The shortest distance between two conductive input-to-output leads measured through air (line of sight).



Input-to-Output Barrier Capacitance -- The total capacitance between all input terminals connected together, and all output terminals connected together.

Input-to-Output Barrier Resistance -- The total resistance between all input terminals connected together, and all output terminals connected together.

Primary Circuit -- An internal circuit directly connected to an external supply mains or other equivalent source that supplies the primary circuit electric power.

Secondary Circuit -- A circuit with no direct connection to primary power, and derives its power from a separate isolated source.

Comparative Tracking Index (CTI) -- CTI is an index used for electrical insulating materials. It is defined as the numerical value of the voltage that causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface -- the higher CTI value of the insulating material, the smaller the minimum creepage distance.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as *tracking*.

Copyright © 2008, Texas Instruments Incorporated

Insulation:

Operational insulation -- Insulation needed for the correct operation of the equipment.

Basic insulation -- Insulation to provide basic protection against electric shock.

Supplementary insulation -- Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

Double insulation -- Insulation comprising both basic and supplementary insulation.

Reinforced insulation -- A single insulation system which provides a degree of protection against electric shock equivalent to double insulation.

Pollution Degree:

Pollution Degree 1 -- No pollution, or only dry, nonconductive pollution occurs. The pollution has no influence.

Pollution Degree 2 -- Normally, only nonconductive pollution occurs. However, a temporary conductivity caused by condensation must be expected.

Pollution Degree 3 -- Conductive pollution occurs or dry nonconductive pollution occurs, which becomes conductive due to condensation that is to be expected.

Pollution Degree 4 – Continuous conductivity occurs due to conductive dust, rain, or other wet conditions.

Installation Category:

Overvoltage Category -- This section is directed at insulation co-ordination by identifying the transient overvoltages that may occur, and by assigning four different levels as indicated in IEC 60664.

1. Signal Level -- Special equipment or parts of equipment.
2. Local Level -- Portable equipment etc.
3. Distribution Level -- Fixed installation
4. Primary Supply Level -- Overhead lines, cable systems

Each category should be subject to smaller transients than the category above.

Copyright © 2008, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO721MMDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	721MEP	Samples
ISO721MMDREPG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	721MEP	Samples
V62/08627-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	721MEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ISO721M-EP :

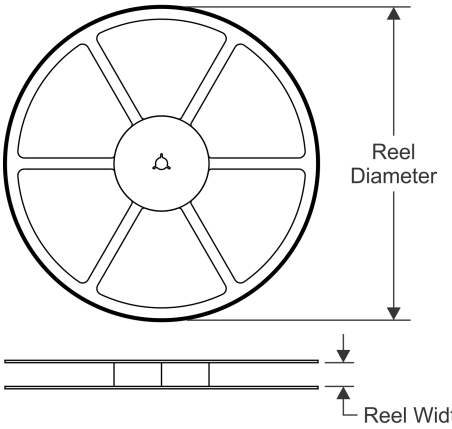
- Catalog: ISO721M

NOTE: Qualified Version Definitions:

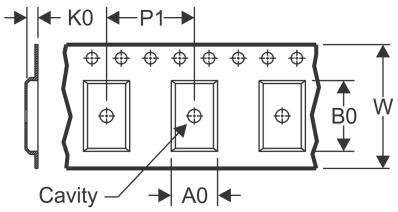
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

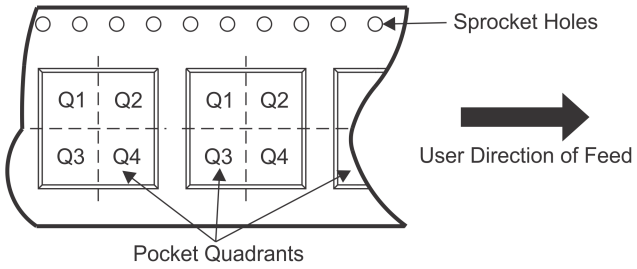


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

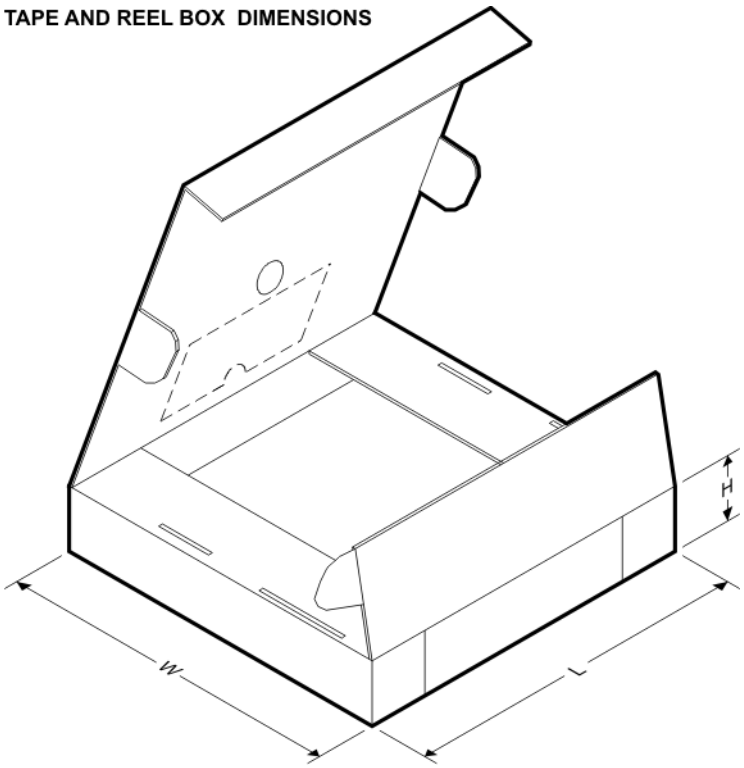
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

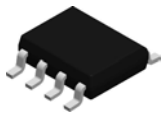
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO721MMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO721MMDREP	SOIC	D	8	2500	350.0	350.0	43.0

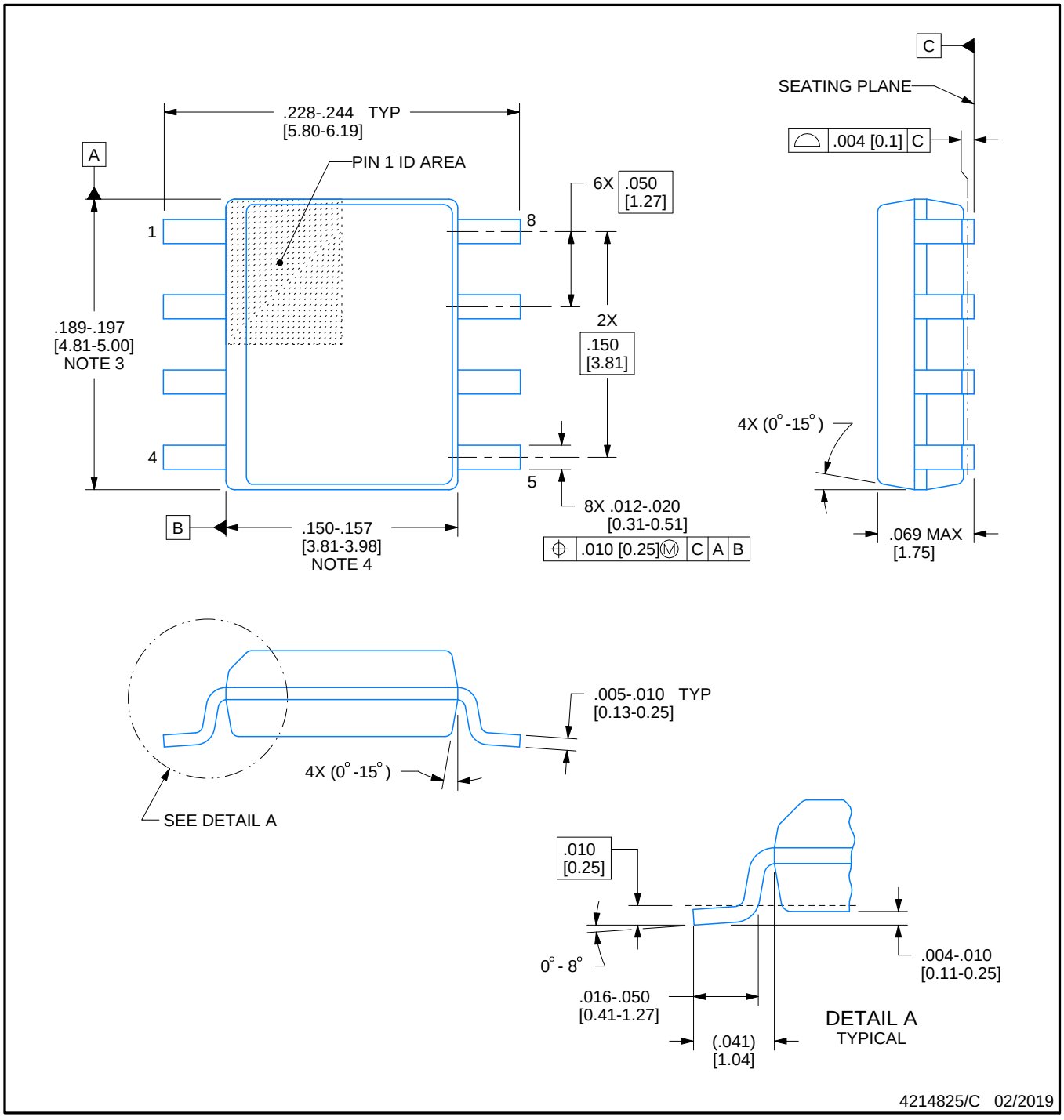


PACKAGE OUTLINE

D0008A

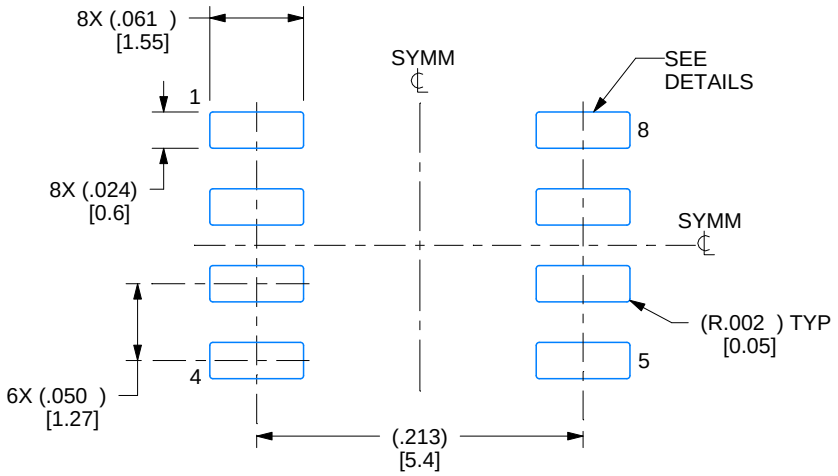
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

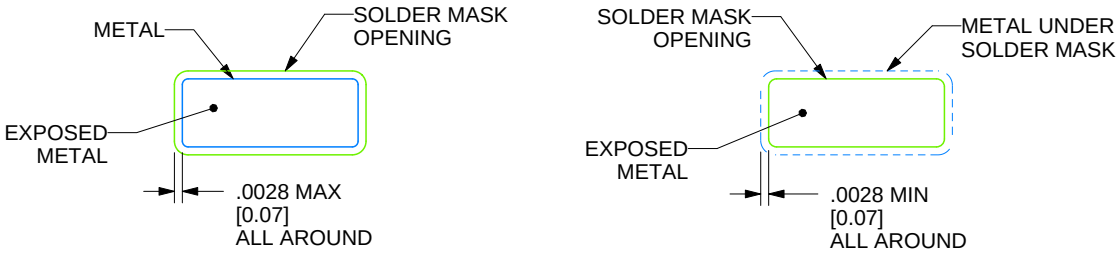


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

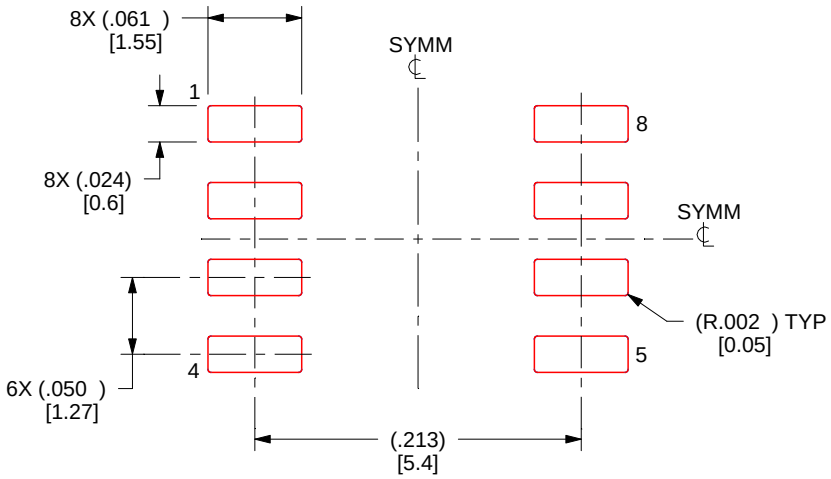
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated