5 kV, 6-Channel, SPIsolator Digital Isolator for SPI with Delay Clock

Data Sheet

ADuM4150

FEATURES

- Supports up to 40 MHz SPI clock speed in delay clock mode
- Supports up to 17 MHz SPI clock speed in 4-wire mode
- 4 high speed, low propagation delay, SPI signal isolation channels
- 2 data channels at 250 kbps
- Delayed compensation clock line
- 20-lead SOIC_IC with 8.3 mm creepage
- High temperature operation: 125°C
- High common-mode transient immunity: >25 kV/µs
- Safety and regulatory approvals
  - UL recognition per UL 1577
    - 5000 V rms for 1 minute SOIC long package
  - CSA Component Acceptance Notice 5A
  - VDE certificate of conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 849 V peak

APPLICATIONS

- Industrial programmable logic controllers (PLC)
- Sensor isolation

GENERAL DESCRIPTION

The ADuM4150[1] is a 6-channel, SPIsolator™ digital isolator optimized for isolated serial peripheral interfaces (SPIs). Based on the Analog Devices, Inc., *i*Coupler® chip scale transformer technology, the low propagation delay in the CLK, MO/SI, MI/SO, and $\overline{SS}$ SPI bus signals supports SPI clock rates of up to 17 MHz. These channels operate with 13 ns propagation delay and 1 ns jitter to optimize timing for SPI.

The ADuM4150 isolator also provides two additional independent low data rate isolation channels, one channel in each direction. Data in the slow channels is sampled and serialized for a 250 kbps data rate with 2.5 µs of jitter.

The ADuM4150 supports a delay clock output on the master side of the device. This output can be used with an additional clocked port on the master to support 40 MHz clock performance. See the Delay Clock section for more information.

FUNCTIONAL BLOCK DIAGRAM

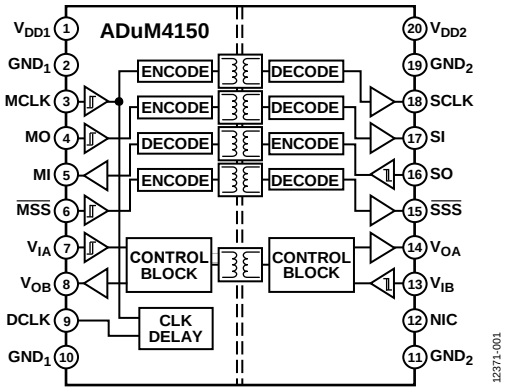


Figure 1.

Table 1. Related Products

Product	Description
ADuM3150	3.75 kV, high speed, clock delayed SPIsolator
ADuM3151/ADuM3152/ ADuM3153	3.75 kV, multichannel SPIsolator
ADuM3154	3.75 kV, multiple slave SPIsolator
ADuM4151/ADuM4152/ ADuM4153	5 kV, multichannel SPIsolator
ADuM4154	5 kV, multiple slave SPIsolator

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,262,600; and 7,075,329. Other patents are pending.

Rev. C
Document Feedback

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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7/2017—Rev. B to Rev. C

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9/2016—Rev. A to Rev. B

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10/2014—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V. Minimum and maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 2. Switching Specifications

		A Grade			B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
MCLK, MO, SO									
SPI Clock Rate	SPI_{MCLK}			10			17	MHz	
Data Rate Fast (MO, SO)	DR_{FAST}			40			40	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			24		12	13	ns	50% input to 50% output
Pulse Width	PW	12.5			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			2			2	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Codirectional Channel Matching[1]	t_{PSKCD}			2			2	ns	
Jitter, High Speed	J_{HS}		1			1		ns	
$\overline{MSS}$									
Data Rate Fast	DR_{FAST}			40			40	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		21	24		21	24	ns	50% input to 50% output
Pulse Width	PW	12.5			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			2			2	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Setup Time[2]	$\overline{MSS}_{SETUP}$	1.5			10			ns	
Jitter, High Speed	J_{HS}		1			1		ns	
DCLK[3]									
Data Rate				40			40	MHz	
Propagation Delay	t_{PHL}, t_{PLH}			50			35	ns	$t_{PMCLK} + t_{PSO}$ + 3 ns
Pulse Width Distortion	PWD			3			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Pulse Width	PW	12			12			ns	Within PWD limit
Clock Delay Error	$DCLK_{ERR}$	0	4.5	12	1	5.5	12	ns	$t_{PDCLK} - (t_{PMCLK} + t_{PSO})$
Jitter	J_{DCLK}		1			1		ns	
V_{IA}, V_{IB}									
Data Rate Slow	DR_{SLOW}			250			250	kbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	0.1		2.6	0.1		2.6	µs	50% input to 50% output
Pulse Width	PW	4			4			µs	Within PWD limit
Jitter, Low Speed	J_{LS}			2.5			2.5	µs	
V_{Ix}[4] Minimum Input Skew[5]	$t_{VIx\ SKEW}$	10			10			ns	

[1] Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.
[2] The $\overline{MSS}$ signal is glitch filtered in both speed grades, whereas the other fast signals are not glitch filtered in the B grade. To guarantee that $\overline{MSS}$ reaches the output ahead of another fast signal, set up $\overline{MSS}$ prior to the competing signal by different times depending on speed grade.
[3] t_{PMCLK} is the propagation delay of the MCLK signal from Side 1 to Side 2. t_{PSO} is the propagation delay of the SO signal from Side 2 to Side 1. t_{PDCLK} is the difference between the DCLK signal and the round trip propagation delay.
[4] $V_{Ix} = V_{IA}$ or V_{IB}.
[5] An internal asynchronous clock, not available to users, samples the low speed signals. If edge sequence in codirectional channels is critical to the end application, the leading pulse must be at least 1 $t_{VIx\ SKEW}$ time ahead of a later pulse to guarantee the correct order or simultaneous arrival at the output.

Table 3. For All Grades[1, 2, 3]

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
1 MHz, A Grade and B Grade	I_{DD1}		5	8.5	mA	C_L = 0 pF, DR_{FAST} = 1 MHz, DR_{SLOW} = 0 MHz
	I_{DD2}		6.5	11	mA	C_L = 0 pF, DR_{FAST} = 1 MHz, DR_{SLOW} = 0 MHz
17 MHz, B Grade	I_{DD1}		15	23	mA	C_L = 0 pF, DR_{FAST} = 17 MHz, DR_{SLOW} = 0 MHz
	I_{DD2}		13.5	21	mA	C_L = 0 pF, DR_{FAST} = 17 MHz, DR_{SLOW} = 0 MHz
DC SPECIFICATIONS						
MCLK, $\overline{MSS}$, MO, SO, V_{IA}, V_{IB}						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Input Hysteresis	V_{IHYST}		500		mV	
Input Current per Channel	I_I	−1	+0.01	+1	µA	0 V ≤ V_{INPUT} ≤ V_{DDx}
SCLK, $\overline{SSS}$, MI, SI, V_{OA}, V_{OB}, DCLK						
Output Voltages						
Logic High	V_{OH}	V_{DDx} − 0.1	5.0		V	I_{OUTPUT} = −20 µA, V_{INPUT} = V_{IH}
		V_{DDx} − 0.4	4.8		V	I_{OUTPUT} = −4 mA, V_{INPUT} = V_{IH}
Logic Low	V_{OL}		0.0	0.1	V	I_{OUTPUT} = 20 µA, V_{INPUT} = V_{IL}
			0.2	0.4	V	I_{OUTPUT} = 4 mA, V_{INPUT} = V_{IL}
V_{DD1}, V_{DD2} Undervoltage Lockout	UVLO		2.6		V	
Supply Current per High Speed Channel						
Dynamic Input	$I_{DDI(D)}$		0.080		mA/Mbps	
Dynamic Output	$I_{DDO(D)}$		0.046		mA/Mbps	
Supply Current for All Low Speed Channels						
Quiescent Side 1 Current	$I_{DD1(Q)}$		4.4		mA	
Quiescent Side 2 Current	$I_{DD2(Q)}$		6.1		mA	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	|CM|	25	35		kV/µs	V_{INPUT} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V

[1] V_{DDx} = V_{DD1} or V_{DD2}.
[2] V_{INPUT} is the input voltage of any of the MCLK, $\overline{MSS}$, MO, SO, V_{IA}, or V_{IB} pins.
[3] I_{OUTPUT} is the output current of any of the SCLK, DCLK, $\overline{SSS}$, MI, SI, V_{OA}, or V_{OB} pins.
[4] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining output voltages within the V_{OH} and V_{OL} limits. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at T_A = 25°C and V_{DD1} = V_{DD2} = 3.3 V. Minimum and maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 4. Switching Specifications

		A Grade			B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
MCLK, MO, SO									
SPI Clock Rate	SPI_{MCLK}			8.3			12.5	MHz	
Data Rate Fast (MO, SO)	DR_{FAST}			40			40	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			30			20	ns	50% input to 50% output
Pulse Width	PW	12.5			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			3			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Codirectional Channel Matching[1]	t_{PSKCD}			3			3	ns	
Jitter, High Speed	J_{HS}		1			1		ns	
$\overline{MSS}$									
Data Rate Fast	DR_{FAST}			40			40	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			30			30	ns	50% input to 50% output
Pulse Width	PW	12.5			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			3			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Setup Time[2]	$\overline{MSS}_{SETUP}$	1.5			10			ns	
Jitter, High Speed	J_{HS}		1			1		ns	
DCLK[3]									
Data Rate				40			40	MHz	
Propagation Delay	t_{PHL}, t_{PLH}			60			40	ns	$t_{PMCLK} + t_{PSO}$ + 3 ns
Pulse Width Distortion	PWD			3			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Pulse Width	PW	12			12			ns	Within PWD limit
Clock Delay Error	$DCLK_{ERR}$	−4	+2.4	+9	−3	+2.5	+8	ns	$t_{PDCLK} - (t_{PMCLK} + t_{PSO})$
Jitter	J_{DCLK}		1			1		ns	
V_{IA}, V_{IB}									
Data Rate Slow	DR_{SLOW}			250			250	kbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	0.1		2.6	0.1		2.6	µs	50% input to 50% output
Pulse Width	PW	4			4			µs	Within PWD limit
Jitter, Low Speed	J_{LS}			2.5			2.5	µs	
V_{Ix}[4] Minimum Input Skew[5]	$t_{VIx\ SKEW}$	10			10			ns	

[1] Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.
[2] The $\overline{MSS}$ signal is glitch filtered in both speed grades, whereas the other fast signals are not glitch filtered in the B grade. To guarantee that $\overline{MSS}$ reaches the output ahead of another fast signal, set up $\overline{MSS}$ prior to the competing signal by different times depending on speed grade.
[3] t_{PMCLK} is the propagation delay of the MCLK signal from Side 1 to Side 2. t_{PSO} is the propagation delay of the SO signal from Side 2 to Side 1. t_{PDCLK} is the difference between the DCLK signal and the round trip propagation delay.
[4] $V_{Ix} = V_{IA}$ or V_{IB}.
[5] An internal asynchronous clock, not available to users, samples the low speed signals. If edge sequence in codirectional channels is critical to the end application, the leading pulse must be at least 1 $t_{VIx\ SKEW}$ time ahead of a later pulse to guarantee the correct order or simultaneous arrival at the output.

Table 5. For All Grades[1, 2, 3]

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
1 MHz, A Grade and B Grade	I_{DD1}		3.5	6	mA	C_L = 0 pF, DR_{FAST} = 1 MHz, DR_{SLOW} = 0 MHz
	I_{DD2}		4.9	8	mA	C_L = 0 pF, DR_{FAST} = 1 MHz, DR_{SLOW} = 0 MHz
17 MHz, B Grade	I_{DD1}		9.5	20	mA	C_L = 0 pF, DR_{FAST} = 17 MHz, DR_{SLOW} = 0 MHz
	I_{DD2}		8	16	mA	C_L = 0 pF, DR_{FAST} = 17 MHz, DR_{SLOW} = 0 MHz
DC SPECIFICATIONS						
MCLK, $\overline{MSS}$, MO, SO, V_{IA}, V_{IB}						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Input Hysteresis	V_{IHYST}		500		mV	
Input Current per Channel	I_I	−1	+0.01	+1	µA	0 V ≤ V_{INPUT} ≤ V_{DDx}
SCLK, $\overline{SSS}$, MI, SI, V_{OA}, V_{OB}, DCLK						
Output Voltages						
Logic High	V_{OH}	V_{DDx} − 0.1	3.3		V	I_{OUTPUT} = −20 µA, V_{INPUT} = V_{IH}
		V_{DDx} − 0.4	3.1		V	I_{OUTPUT} = −4 mA, V_{INPUT} = V_{IH}
Logic Low	V_{OL}		0.0	0.1	V	I_{OUTPUT} = 20 µA, V_{INPUT} = V_{IL}
			0.2	0.4	V	I_{OUTPUT} = 4 mA, V_{INPUT} = V_{IL}
V_{DD1}, V_{DD2} Undervoltage Lockout	UVLO		2.6		V	
Supply Current per High Speed Channel						
Dynamic Input	$I_{DDI(D)}$		0.086		mA/Mbps	
Dynamic Output	$I_{DDO(D)}$		0.019		mA/Mbps	
Supply Current for All Low Speed Channels						
Quiescent Side 1 Current	$I_{DD1(Q)}$		2.9		mA	
Quiescent Side 2 Current	$I_{DD2(Q)}$		4.6		mA	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	|CM|	25	35		kV/µs	V_{INPUT} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V

[1] V_{DDx} = V_{DD1} or V_{DD2}.
[2] V_{INPUT} is the input voltage of any of the MCLK, $\overline{MSS}$, MO, SO, V_{IA}, or V_{IB} pins.
[3] I_{OUTPUT} is the output current of any of the SCLK, DCLK, $\overline{SSS}$, MI, SI, V_{OA}, or V_{OB} pins.
[4] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining output voltages within the V_{OH} and V_{OL} limits. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, and V_{DD2} = 3.3 V. Minimum and maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 6. Switching Specifications

		A Grade			B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
MCLK, MO, SO									
SPI Clock Rate	SPI_{MCLK}			9.2			15.6	MHz	
Data Rate Fast (MO, SO)	DR_{FAST}			40			40	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			27			16	ns	50% input to 50% output
Pulse Width	PW	12.5			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			3			2	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Codirectional Channel Matching[1]	t_{PSKCD}			2			2	ns	
Jitter, High Speed	J_{HS}		1			1		ns	
$\overline{MSS}$									
Data Rate Fast	DR_{FAST}			40			40	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			26			26	ns	50% input to 50% output
Pulse Width	PW	12.5			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			2			2	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Setup Time[2]	$\overline{MSS}_{SETUP}$	1.5			10			ns	
Jitter, High Speed	J_{HS}		1			1		ns	
DCLK[3]									
Data Rate				40			40	MHz	
Propagation Delay	t_{PHL}, t_{PLH}			50			35	ns	$t_{PMCLK} + t_{PSO}$ + 3 ns
Pulse Width Distortion	PWD			3			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Pulse Width	PW	12			12			ns	Within PWD limit
Clock Delay Error	$DCLK_{ERR}$	−5	0	+7	−5	+1.2	+9	ns	$t_{PDCLK} - (t_{PMCLK} + t_{PSO})$
Jitter	J_{DCLK}		1			1		ns	
V_{IA}, V_{IB}									
Data Rate Slow	DR_{SLOW}			250			250	kbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	0.1		2.6	0.1		2.6	µs	50% input to 50% output
Pulse Width	PW	4			4			µs	Within PWD limit
Jitter, Low Speed	J_{LS}			2.5			2.5	µs	
V_{Ix}[4] Minimum Input Skew[5]	$t_{VIx\ SKEW}$	10			10			ns	

[1] Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.
[2] The $\overline{MSS}$ signal is glitch filtered in both speed grades, whereas the other fast signals are not glitch filtered in the B grade. To guarantee that $\overline{MSS}$ reaches the output ahead of another fast signal, set up $\overline{MSS}$ prior to the competing signal by different times depending on speed grade.
[3] t_{PMCLK} is the propagation delay of the MCLK signal from Side 1 to Side 2. t_{PSO} is the propagation delay of the SO signal from Side 2 to Side 1. t_{PDCLK} is the difference between the DCLK signal and the round trip propagation delay.
[4] $V_{Ix} = V_{IA}$ or V_{IB}.
[5] An internal asynchronous clock, not available to users, samples the low speed signals. If edge sequence in codirectional channels is critical to the end application, the leading pulse must be at least 1 $t_{VIx\ SKEW}$ time ahead of a later pulse to guarantee the correct order or simultaneous arrival at the output.

Table 7. For All Grades[1, 2, 3]

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
1 MHz, A Grade and B Grade	I_{DD1}		5.3	8.5	mA	C_L = 0 pF, DR_{FAST} = 1 MHz, DR_{SLOW} = 0 MHz
	I_{DD2}		4.9	8	mA	C_L = 0 pF, DR_{FAST} = 1 MHz, DR_{SLOW} = 0 MHz
17 MHz, B Grade	I_{DD1}		16	23	mA	C_L = 0 pF, DR_{FAST} = 17 MHz, DR_{SLOW} = 0 MHz
	I_{DD2}		10	16	mA	C_L = 0 pF, DR_{FAST} = 17 MHz, DR_{SLOW} = 0 MHz
DC SPECIFICATIONS						
MCLK, $\overline{MSS}$, MO, SO, V_{IA}, V_{IB}						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Input Hysteresis	V_{IHYST}		500		mV	
Input Current per Channel	I_I	−1	+0.01	+1	µA	0 V ≤ V_{INPUT} ≤ V_{DDx}
SCLK, $\overline{SSS}$, MI, SI, V_{OA}, V_{OB}, DCLK						
Output Voltages						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{OUTPUT} = −20 µA, V_{INPUT} = V_{IH}
		V_{DDx} − 0.4	V_{DDx} − 2.0		V	I_{OUTPUT} = −4 mA, V_{INPUT} = V_{IH}
Logic Low	V_{OL}		0.0	0.1	V	I_{OUTPUT} = 20 µA, V_{INPUT} = V_{IL}
			0.2	0.4	V	I_{OUTPUT} = 4 mA, V_{INPUT} = V_{IL}
V_{DD1}, V_{DD2} Undervoltage Lockout	UVLO		2.6		V	
Supply Current for All Low Speed Channels						
Quiescent Side 1 Current	$I_{DD1(Q)}$		4.4		mA	
Quiescent Side 2 Current	$I_{DD2(Q)}$		4.6		mA	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	|CM|	25	35		kV/µs	V_{INPUT} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V

[1] V_{DDx} = V_{DD1} or V_{DD2}.
[2] V_{INPUT} is the input voltage of any of the MCLK, $\overline{MSS}$, MO, SO, V_{IA}, or V_{IB} pins.
[3] I_{OUTPUT} is the output current of any of the SCLK, DCLK, $\overline{SSS}$, MI, SI, V_{OA}, or V_{OB} pins.
[4] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining output voltages within the V_{OH} and V_{OL} limits. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V and V_{DD2} = 5 V. Minimum and maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 8. Switching Specifications

		A Grade			B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
MCLK, MO, SO									
SPI Clock Rate	SPI_{MCLK}			9.2			15.6	MHz	
Data Rate Fast (MO, SO)	DR_{FAST}			40			40	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			27			16	ns	50% input to 50% output
Pulse Width	PW	12.5			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			2			2	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Codirectional Channel Matching[1]	t_{PSKCD}			3			3	ns	
Jitter, High Speed	J_{HS}		1			1		ns	
$\overline{MSS}$									
Data Rate Fast	DR_{FAST}			40			40	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			26			26	ns	50% input to 50% output
Pulse Width	PW	12.5			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			3			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Setup Time[2]	$\overline{MSS}_{SETUP}$	1.5			10			ns	
Jitter, High Speed	J_{HS}		1			1		ns	
DCLK[3]									
Data Rate				40			40	MHz	
Propagation Delay	t_{PHL}, t_{PLH}			60			40	ns	$t_{PMCLK} + t_{PSO}$ + 3 ns
Pulse Width Distortion	PWD			3			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Pulse Width	PW	12			12			ns	Within PWD limit
Clock Delay Error	$DCLK_{ERR}$	2	7	13	2	6.8	11	ns	$t_{PDCLK} - (t_{PMCLK} + t_{PSO})$
Jitter	J_{DCLK}		1			1		ns	
V_{IA}, V_{IB}									
Data Rate Slow	DR_{SLOW}			250			250	kbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	0.1		2.6	0.1		2.6	µs	50% input to 50% output
Pulse Width	PW	4			4			µs	Within PWD limit
Jitter, Low Speed	J_{LS}			2.5			2.5	µs	
V_{Ix}[4] Minimum Input Skew[5]	$t_{VIx\ SKEW}$	10			10			ns	

[1] Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.
[2] The $\overline{MSS}$ signal is glitch filtered in both speed grades, whereas the other fast signals are not glitch filtered in the B grade. To guarantee that $\overline{MSS}$ reaches the output ahead of another fast signal, set up $\overline{MSS}$ prior to the competing signal by different times depending on speed grade.
[3] t_{PMCLK} is the propagation delay of the MCLK signal from Side 1 to Side 2. t_{PSO} is the propagation delay of the SO signal from Side 2 to Side 1. t_{PDCLK} is the difference between the DCLK signal and the round trip propagation delay.
[4] $V_{Ix} = V_{IA}$ or V_{IB}.
[5] An internal asynchronous clock, not available to users, samples the low speed signals. If edge sequence in codirectional channels is critical to the end application, the leading pulse must be at least 1 $t_{VIx\ SKEW}$ time ahead of a later pulse to guarantee the correct order or simultaneous arrival at the output.

Table 9. For All Grades[1, 2, 3]

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
1 MHz, A Grade and B Grade	I_{DD1}		3.5	6	mA	C_L = 0 pF, DR_{FAST} = 1 MHz, DR_{SLOW} = 0 MHz
	I_{DD2}		6.8	11	mA	C_L = 0 pF, DR_{FAST} = 1 MHz, DR_{SLOW} = 0 MHz
17 MHz, B Grade	I_{DD1}		12.5	20	mA	C_L = 0 pF, DR_{FAST} = 17 MHz, DR_{SLOW} = 0 MHz
	I_{DD2}		14	21	mA	C_L = 0 pF, DR_{FAST} = 17 MHz, DR_{SLOW} = 0 MHz
DC SPECIFICATIONS						
MCLK, $\overline{MSS}$, MO, SO, V_{IA}, V_{IB}						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Input Hysteresis	V_{IHYST}		500		mV	
Input Current per Channel	I_I	−1	+0.01	+1	µA	0 V ≤ V_{INPUT} ≤ V_{DDx}
SCLK, $\overline{SSS}$, MI, SI, V_{OA}, V_{OB}, DCLK						
Output Voltages						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{OUTPUT} = −20 µA, V_{INPUT} = V_{IH}
		V_{DDx} − 0.4	V_{DDx} − 2.0		V	I_{OUTPUT} = −4 mA, V_{INPUT} = V_{IH}
Logic Low	V_{OL}		0.0	0.1	V	I_{OUTPUT} = 20 µA, V_{INPUT} = V_{IL}
			0.2	0.4	V	I_{OUTPUT} = 4 mA, V_{INPUT} = V_{IL}
V_{DD1}, V_{DD2} Undervoltage Lockout	UVLO		2.6		V	
Supply Current for All Low Speed Channels						
Quiescent Side 1 Current	$I_{DD1(Q)}$		2.9		mA	
Quiescent Side 2 Current	$I_{DD2(Q)}$		6.1		mA	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	|CM|	25	35		kV/µs	V_{INPUT} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V

[1] V_{DDx} = V_{DD1} or V_{DD2}.
[2] V_{INPUT} is the input voltage of any of the MCLK, $\overline{MSS}$, MO, SO, V_{IA}, or V_{IB} pins.
[3] I_{OUTPUT} is the output current of any of the SCLK, DCLK, $\overline{SSS}$, MI, SI, V_{OA}, or V_{OB} pins.
[4] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining output voltages within the V_{OH} and V_{OL} limits. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 10.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		1.0		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		46		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device: Pin 1 through Pin 10 are shorted together, and Pin 11 through Pin 20 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM4150 is approved by the organizations listed in Table 11. See Table 16 and the Insulation Lifetime section for recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 11.

UL	CSA	VDE
Recognized Under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
5000 V rms Single Protection	Basic insulation per CSA 60950-1-07+A1+A2 and IEC 60950-12nd Ed+A1+A2., 800 V rms (1131 V peak) maximum working voltage[3] Reinforced Insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.+A1+A2, 400 V rms (565 V peak) maximum working voltage Reinforced insulation (2MOPP) per IEC 60601-1 Ed.3.1, 250 V rms (353 V peak) maximum working	Reinforced insulation, 849 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each model is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10, each model is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marked on the component designates DIN V VDE V 0884-10 approval.
[3] Use at working voltages above 400 $V_{AC\ RMS}$ shortens lifetime of the isolator significantly. See Table 16 for recommended maximum working voltages under ac and dc conditions.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 12.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.3	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017	mm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marked on packages denotes DIN V VDE V 0884-10 approval.

Table 13.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V peak
Input-to-Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V peak
Input-to-Output Test Voltage, Method a				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1274	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1019	V peak
Highest Allowable Overvoltage		V_{IOTM}	6000	V peak
Surge Isolation Voltage	$V_{IOSM(TEST)}$ = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6250	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	2.4	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

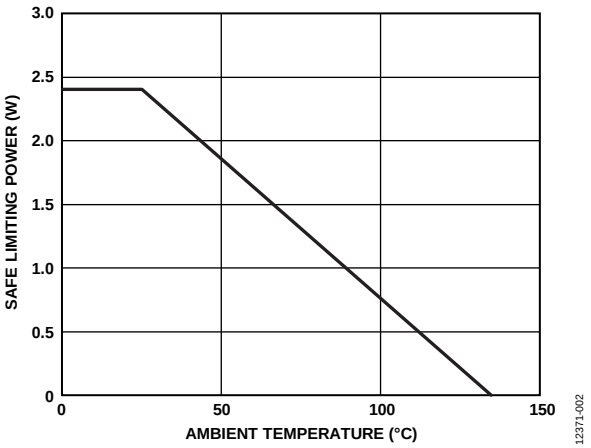


Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 14.

Parameter	Symbol	Value
Operating Temperature Range	T_A	−40°C to +125°C
Supply Voltage Range[1]	V_{DD1}, V_{DD2}	3.0 V to 5.5 V
Input Signal Rise/Fall Times		1.0 ms

[1] See the DC Correctness and Magnetic Field Immunity section for information on the immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 15.

Parameter	Rating[1]
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB}, MCLK, MO, SO, $\overline{MSS}$)	−0.5 V to V_{DDx} + 0.5 V
Output Voltages (SCLK, DCLK, $\overline{SSS}$, MI, SI, V_{OA}, V_{OB})	−0.5 V to V_{DDx} + 0.5 V
Average Output Current per Pin[2]	−10 mA to +10 mA
Common-Mode Transients[3]	−100 kV/µs to +100 kV/µs

[1] V_{DDx} = V_{DD1} or V_{DD2}.
[2] See Figure 2 for maximum safety rated current values across temperature.
[3] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 16. Maximum Continuous Working Voltage[1]

Parameter	Value	Constraint
60 Hz AC Voltage	400 V rms	20 year lifetime at 0.1% failure rate, zero average voltage
DC Voltage	1173 V peak	Limited by the creepage of the package, Pollution Degree 2, Material Group II[2, 3]

[1] See the Insulation Lifetime section for details.
[2] Other pollution degree and material group requirements yield a different limit.
[3] Some system level standards allow components to use the printed wiring board (PWB) creepage values. The supported dc voltage may be higher for those standards.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

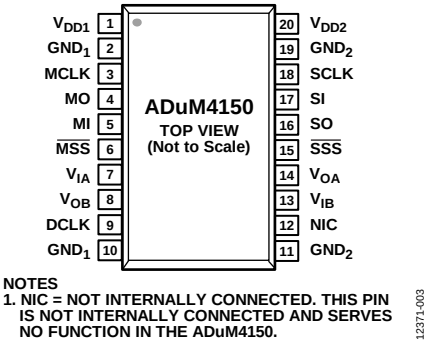


Figure 3. Pin Configuration

Table 17. Pin Function Descriptions

Pin No.	Mnemonic	Direction	Description
1	V_{DD1}	Power	Input Power Supply for Isolator Side 1. A bypass capacitor from V_{DD1} to GND_1 to local ground is required.
2,10	GND_1	Return	Ground 1. Ground reference for Isolator Side 1.
3	MCLK	Input	SPI Clock from the Master Controller.
4	MO	Input	SPI Data from the Master to the Slave MO/SI Line.
5	MI	Output	SPI Data from Slave to the Master MI/SO Line.
6	$\overline{MSS}$	Input	Slave Select from the Master. This signal uses an active low logic. The slave select pin may require as much as 10 ns setup time from the next clock or data edge, depending on speed grade.
7	V_{IA}	Input	Low Speed Data Input A.
8	V_{OB}	Output	Low Speed Data Output B.
9	DCLK	Output	Delayed Clock Output. This pin provides a delayed copy of the MCLK.
11,19	GND_2	Return	Ground 2. Ground reference for Isolator Side 2.
12	NIC	None	No Internal Connection. This pin is not internally connected and serves no function in the ADuM4150.
13	V_{IB}	Input	Low Speed Data Input B.
14	V_{OA}	Output	Low Speed Data Output A.
15	$\overline{SSS}$	Output	Slave Select to the Slave. This signal uses an active low logic.
16	SO	Input	SPI Data from the Slave to the Master MI/SO Line.
17	SI	Output	SPI Data from the Master to the Slave MO/SI Line.
18	SCLK	Output	SPI Clock from the Master Controller.
20	V_{DD2}	Power	Input Power Supply for Isolator Side 2. A bypass capacitor from V_{DD2} to GND_2 to local ground is required.

Table 18. Power-Off Default State Truth Table (Positive Logic)[1]

V_{DD1} State	V_{DD2} State	Side 1 Outputs	Side 2 Outputs	$\overline{SSS}$	Notes
Unpowered	Powered	Z	Z	Z	Outputs on an unpowered side are high impedance within one diode drop of ground
Powered	Unpowered	Z	Z	Z	Outputs on an unpowered side are high impedance within one diode drop of ground

[1] Z is high impedance.

TYPICAL PERFORMANCE CHARACTERISTICS

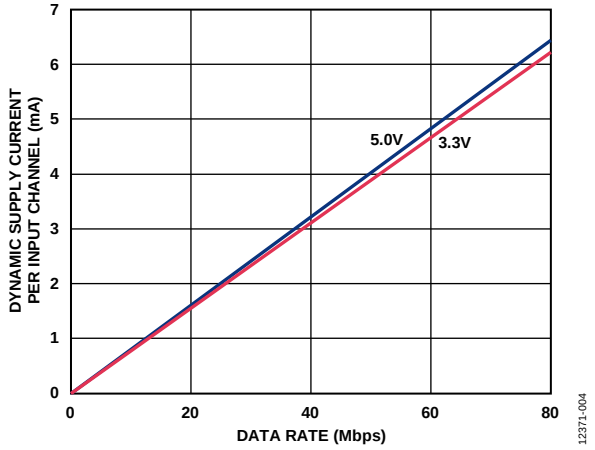


Figure 4. Typical Dynamic Supply Current per Input Channel vs. Data Rate for 5.0 V and 3.3 V Operation

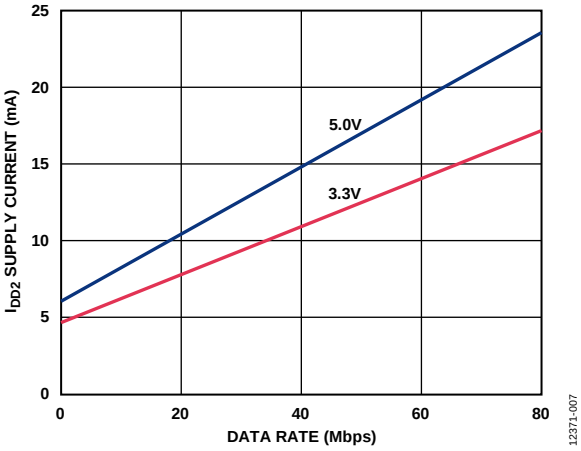


Figure 7. Typical I_{DD2} Supply Current vs. Data Rate for 5.0 V and 3.3 V Operation

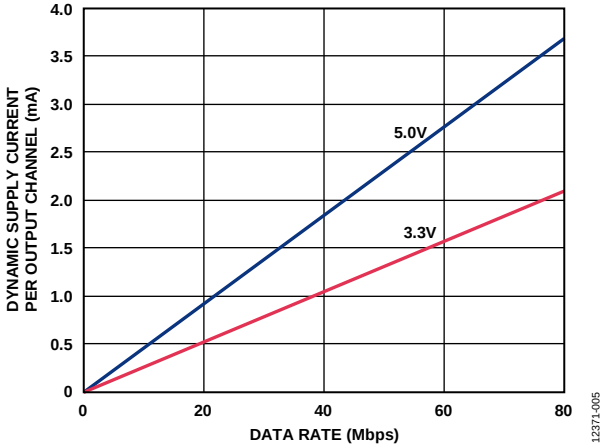


Figure 5. Typical Dynamic Supply Current per Output Channel vs. Data Rate for 5.0 V and 3.3 V Operation

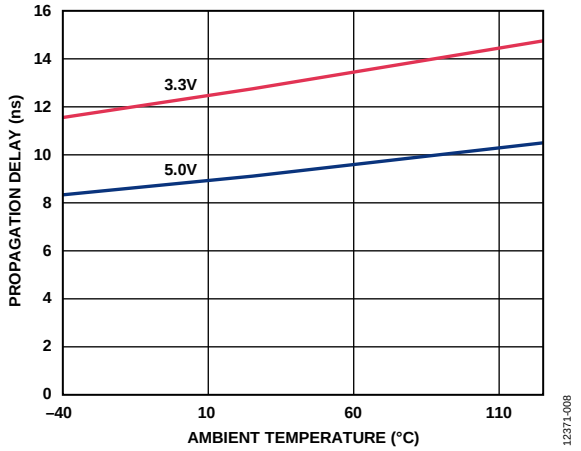


Figure 8. Typical Propagation Delay vs. Ambient Temperature for High Speed Channels Without Glitch Filter (See the High Speed Channels Section for Additional Information)

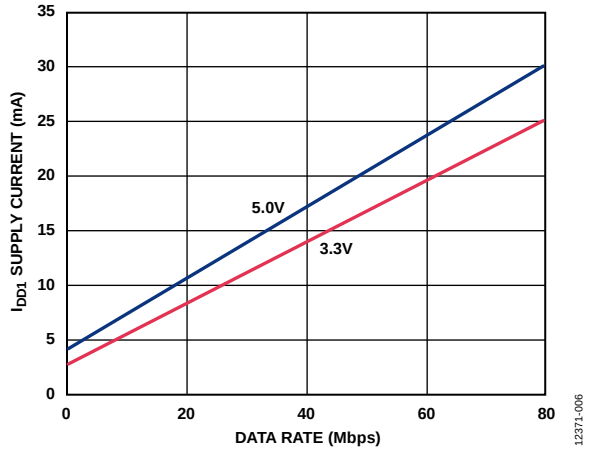


Figure 6. Typical I_{DD1} Supply Current vs. Data Rate for 5.0 V and 3.3 V Operation

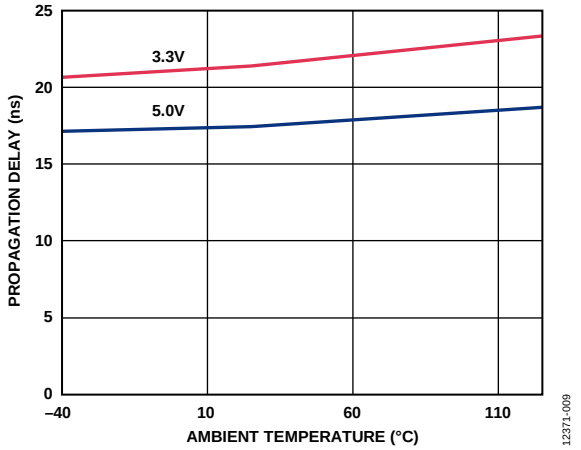


Figure 9. Typical Propagation Delay vs. Ambient Temperature for High Speed Channels with Glitch Filter (See the High Speed Channels Section for Additional Information)

APPLICATIONS INFORMATION

INTRODUCTION

The ADuM4150 is part of a family of devices created to optimize isolation of SPI for speed and to provide additional low speed channels for control and status monitoring functions. The isolators are based on differential signaling *i*Coupler technology for enhanced speed and noise immunity.

High Speed Channels

The ADuM4150 has four high speed channels. The first three, CLK, MI/SO, and MO/SI (the slash indicates the connection of the particular input and output, forming a datapath across the isolator that corresponds to an SPI bus signal), are optimized for either low propagation delay in the B grade, or high noise immunity in the A grade. The difference between the grades is the addition of a glitch filter to these three channels in the A grade version, which increases propagation delay. The B grade version, with a maximum propagation delay of 13 ns, supports a maximum clock rate of 17 MHz in a standard 4-wire SPI. However, because the glitch filter is not present in the B grade version, ensure that spurious glitches of less than 10 ns are not present.

Glitches of less than 10 ns in the B grade devices can cause the second edge of the glitch to be missed. This pulse condition is seen as a spurious data transition on the output that is corrected by a refresh or the next valid data edge. It is recommended to use A grade devices in noisy environments.

The relationship between the SPI signal paths and the pin mnemonics of the ADuM4150 and data directions is summarized in Table 19.

Table 19. Pin Mnemonic Correspondence to SPI Signal Path Names

SPI Signal Path	Master Side 1	Data Direction	Slave Side 2
CLK	MCLK	→	SCLK
MO/SI	MO	→	SI
MI/SO	MI	←	SO
$\overline{SS}$	$\overline{MSS}$	→	$\overline{SSS}$

The datapaths are SPI mode agnostic. The CLK and MO/SI SPI datapaths are optimized for propagation delay and channel-to-channel matching. The MI/SO SPI datapath is optimized for propagation delay. The device does not synchronize to the clock channel, so there are no constraints on the clock polarity or the timing with respect to the data lines. To allow compatibility with nonstandard SPI interfaces, the MI pin is always active, and does not tristate when the slave select is not asserted. This precludes tying several MI lines together without adding a tristate buffer or multiplexor.

The $\overline{SS}$ (slave select bar) is typically an active low signal. It can have many different functions in SPI and SPI like busses. Many of these functions are edge triggered; therefore, the $\overline{SS}$ path contains a glitch filter in both the A grade and the B grade. The glitch filter prevents short pulses from propagating to the output or causing other errors in operation. The $\overline{MSS}$ signal requires a 10 ns setup time in the B grade prior to the first active clock edge to allow the added propagation time of the glitch filter.

Low Speed Data Channels

The low speed data channels are provided as economical isolated datapaths where timing is not critical. The dc value of all high and low speed inputs on a given side of the device is sampled simultaneously, packetized, and shifted across an isolation coil. The high speed channels are compared for dc accuracy, and the low speed data is transferred to the appropriate low speed outputs. The process is then reversed by reading the inputs on the opposite side of the device, packetizing them, and sending them back for similar processing. The dc correctness data for the high speed channels is handled internally, and the low speed data is clocked to the outputs simultaneously.

This bidirectional data shuttling is regulated by a free running internal clock. Because data is sampled at discrete times based on this clock, the propagation delay for a low speed channel is between 0.1 µs and 2.6 µs depending on where the input data edge changes with respect to the internal sample clock.

Figure 10 illustrates the behavior of the low speed channels.

- Point A: The data may change as much as 2.6 µs before it is sampled, then it takes about 0.1 µs to propagate to the output. This difference appears as 2.5 µs of uncertainty in the propagation delay time.
- Point B: Data pulses that are less than the minimum low speed pulse width may not be transmitted at all because they may not be sampled.

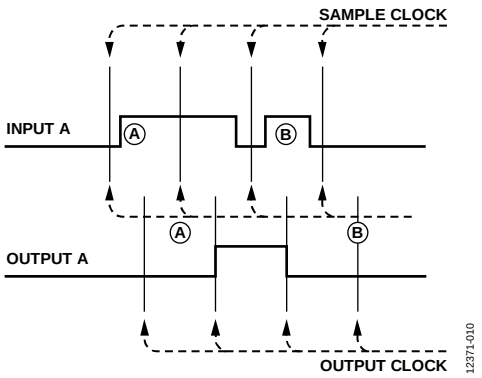


Figure 10. Low Speed Channel Timing

Delay Clock

The delay clock (DCLK) function allows SPI data transfers at speeds beyond the limitations usually set by propagation delay. The maximum speed of the clock in a 4-wire SPI application is set by the requirement that data shifts out on one clock edge and returning data shifts in on the complementary clock edge. In isolated systems, the delay through the isolator is significant. The first clock edge, telling the slave to present its data, must propagate through the isolator. The slave acts upon the clock edge, and data propagates back through the isolator to the master. The data must arrive back at the master before the complementary clock edge for the data to shift properly into the master.

For the example shown in Figure 11, if an isolator has a 50 ns propagation delay, it requires more than 100 ns for the response from the slave to arrive back at the master. This means that the fastest clock period for the SPI bus is 200 ns or 5 MHz, and assumes ideal conditions, such as no trace propagation delay or delay in the slave for simplicity.

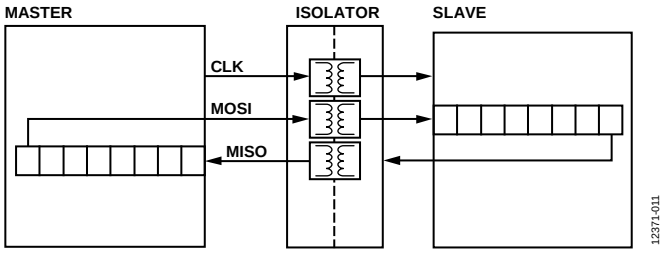


Figure 11. Standard SPI Configuration

To avoid this limitation on the SPI clock, a second receive buffer can be used as shown in Figure 12, together with a clock signal that is delayed to match the data coming back from the slave. The proper delay of the clock was accomplished in the past by sending a copy of the clock back through a matching isolator channel and using the delayed clock to shift the slave data into a secondary buffer. Using an extra channel is costly because it consumes an additional high speed isolator channel.

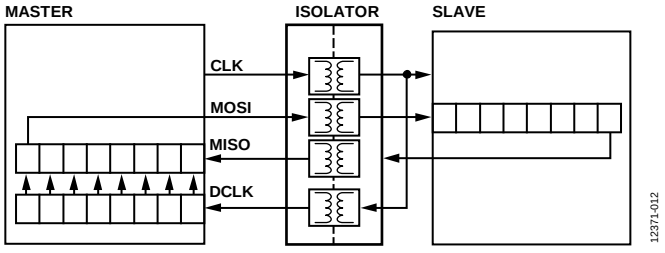


Figure 12. High Speed SPI Using Isolation Channel Delay

The ADuM4150 eliminates the need for the extra high speed channel by implementing a delay circuit on the master side, as shown in Figure 13. DCLK is trimmed at the production test to match the round trip propagation delay of each isolator. The DCLK signal can be used as if the clock signal had propagated alongside the data from the slave in the scheme outlined previously.

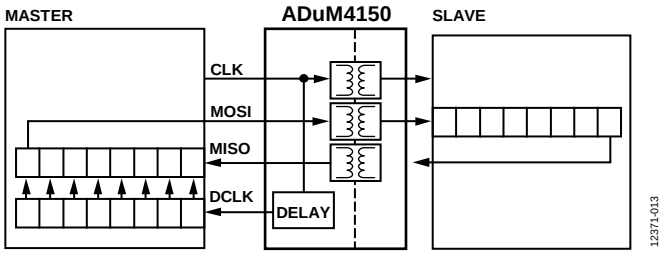


Figure 13. High Speed SPI Using Precision Clock Delay

This configuration can operate at clock rates of up to 40 MHz. The MI/SO data is shifted into the secondary receive buffer by DCLK and then transferred internally by the master to its final destination. The ADuM4150 does not need to use an extra expensive isolator channel to achieve these data transfer speeds. Note that the $\overline{SS}$ channel is not shown here for clarity.

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM4150 digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at both the V_{DD1} and V_{DD2} supply pins (see Figure 14). The capacitor value must be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 20 mm.

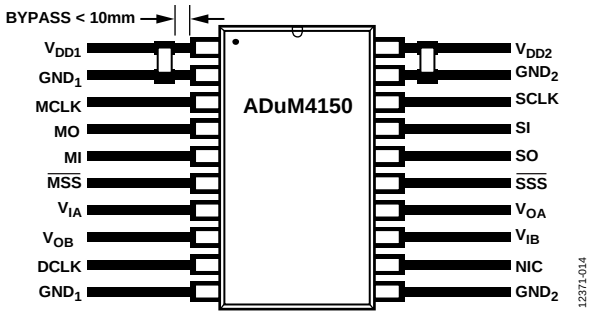


Figure 14. Recommended PCB Layout

In applications involving high common-mode transients, it is important to minimize board coupling across the isolation barrier. Furthermore, design the PCB layout so that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this may cause voltage differentials between pins that exceed the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The input-to-output propagation delay time for a high-to-low transition can differ from the propagation delay time of a low-to-high transition.

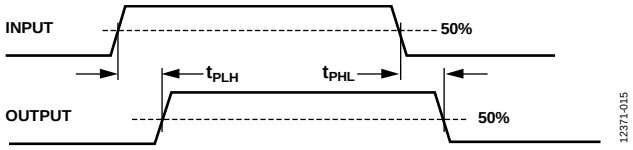


Figure 15. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values, and an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM4150 component.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and is, therefore, either set or reset by the pulses indicating input logic transitions. In the absence of logic transitions at the input for more than ~1.2 µs, a periodic set of refresh pulses indicative of the correct input state are sent via the low speed channel to ensure dc correctness at the output.

If the low speed decoder receives no pulses for more than approximately 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a high-Z state by the watchdog timer circuit.

The limitation on the magnetic field immunity of the device is set by the condition in which the induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines such conditions. The ADuM4150 is examined in a 3 V operating condition because it represents the most susceptible mode of operation for this product.

The pulses at the transformer output have amplitudes greater than 1.5 V. The decoder has a sensing threshold of about 1.0 V, therefore establishing a 0.5 V margin in which induced voltages are tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum\pi r_n^2; n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density.
r_n is the radius of the n^{th} turn in the receiving coil.
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM4150 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 16.

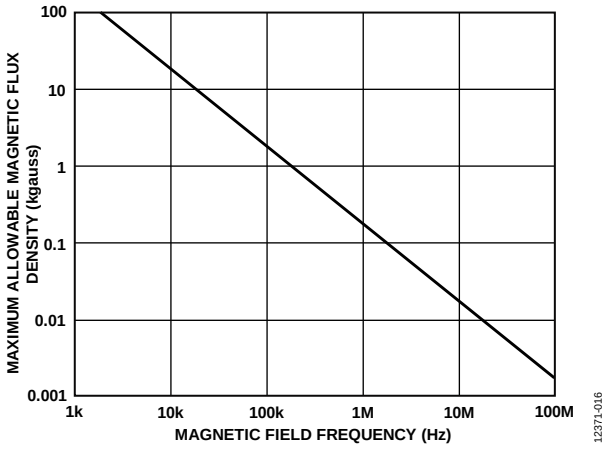


Figure 16. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.5 kgauss induces a voltage of 0.25 V at the receiving coil. This voltage is about 50% of the sensing threshold and does not cause a faulty output transition. If such an event occurs, with the worst-case polarity, during a transmitted pulse, the interference reduces the received pulse from >1.0 V to 0.75 V. This voltage is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM4150 transformers. Figure 17 expresses these allowable current magnitudes as a function of frequency for selected distances. The ADuM4150 is very insensitive to external fields. Only extremely large, high frequency currents very close to the component may potentially be concerns. For the 1 MHz example noted, placing a 1.2 kA current 5 mm away from the ADuM4150 affects component operation.

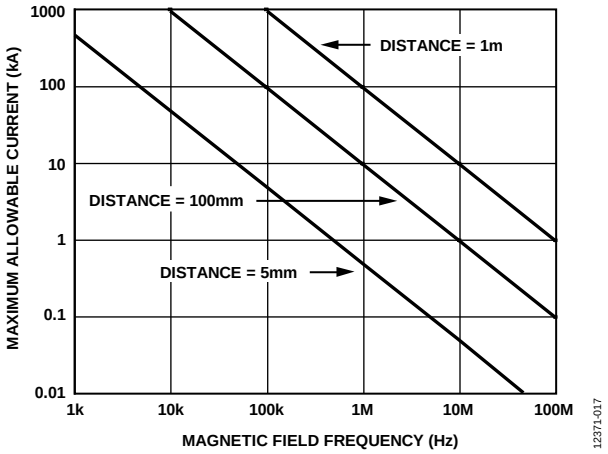


Figure 17. Maximum Allowable Current for Various Current to ADuM4150 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by PCB traces may induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Take care to avoid PCB structures that form loops.

POWER CONSUMPTION

The supply current at a given channel of the ADuM4150 isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel and whether it is a high or low speed channel.

The low speed channels draw a constant quiescent current caused by the internal ping-pong datapath. The operating frequency is low enough that the capacitive losses caused by the recommended capacitive load are negligible compared to the quiescent current. The explicit calculation for the data rate is eliminated for simplicity, and the quiescent current for each side of the isolator attributable to the low speed channels can be found in Table 3, Table 5, Table 7, and Table 9 for the particular operating voltages. These quiescent currents add to the high speed current, as shown in the following equations, for the total current for each side of the isolator. Dynamic currents are from Table 3 and Table 5 for the respective voltages.

For Side 1, the supply current is given by

$$I_{DD1} = I_{DDI(D)} \times (f_{MCLK} + f_{MO} + f_{\overline{MSS}}) + f_{MI} \times (I_{DDO(D)} + ((0.5 \times 10^{-3}) \times C_{L(MI)} \times V_{DD1})) + f_{MCLK} \times (I_{DDO(D)} + ((0.5 \times 10^{-3}) \times C_{L(DCLK)} \times V_{DD1})) + I_{DD1(Q)}$$

For Side 2, the supply current is given by

$$I_{DD2} = I_{DDI(D)} \times f_{SO} + f_{SCLK} \times (I_{DDO(D)} + ((0.5 \times 10^{-3}) \times C_{L(SCLK)} \times V_{DD2})) + f_{SI} \times (I_{DDO(D)} + ((0.5 \times 10^{-3}) \times C_{L(SI)} \times V_{DD2})) + f_{SSx} \times (I_{DDO(D)} + ((0.5 \times 10^{-3}) \times C_{L(SSx)} \times V_{DD2})) + I_{DD2(Q)}$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

f_x is the logic signal data rate for the specified channel, expressed in units of Mbps.
$C_{L(x)}$ is the load capacitance of the specified output (pF).
V_{DDx} is the supply voltage of the side being evaluated (V).
$I_{DD1(Q)}$, $I_{DD2(Q)}$ are the specified Side 1 and Side 2 quiescent supply currents (mA).

Figure 4 and Figure 5 show the typical dynamic supply current per channel as a function of data rate for an input and unloaded output. Figure 6 and Figure 7 show the total I_{DD1} and I_{DD2} supply currents as a function of data rate for ADuM4150 channel configurations with all high speed channels running at the same speed and the low speed channels at idle.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

Two types of insulation degradation are of primary interest: breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and therefore can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the ADuM4150 isolator is presented in Table 12.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. It is the working voltage applicable to tracking that is specified in most standards.

Testing and modeling have shown that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as: dc stress, which causes very little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this stress reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as is shown in Equation 2. For insulation wear out with the polyimide materials used in this product, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ RMS}{}^2 + V_{DC}{}^2} \quad (1)$$

or

$$V_{AC\ RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2} \quad (2)$$

where:
V_{RMS} is the total rms working voltage.
$V_{AC\ RMS}$ is the time varying portion of the working voltage.
V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following is an example that frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V ac rms and a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage clearance and lifetime of a device, see Figure 18 and the following equations.

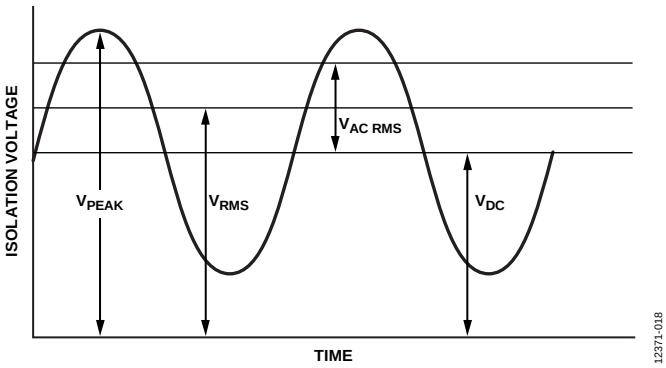


Figure 18. Critical Voltage Example

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\ RMS}{}^2 + V_{DC}{}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

V_{RMS} = 466 V rms

This working voltage of 466 V rms is used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. The ac rms voltage can be obtained from Equation 2.

$$V_{AC\ RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2}$$

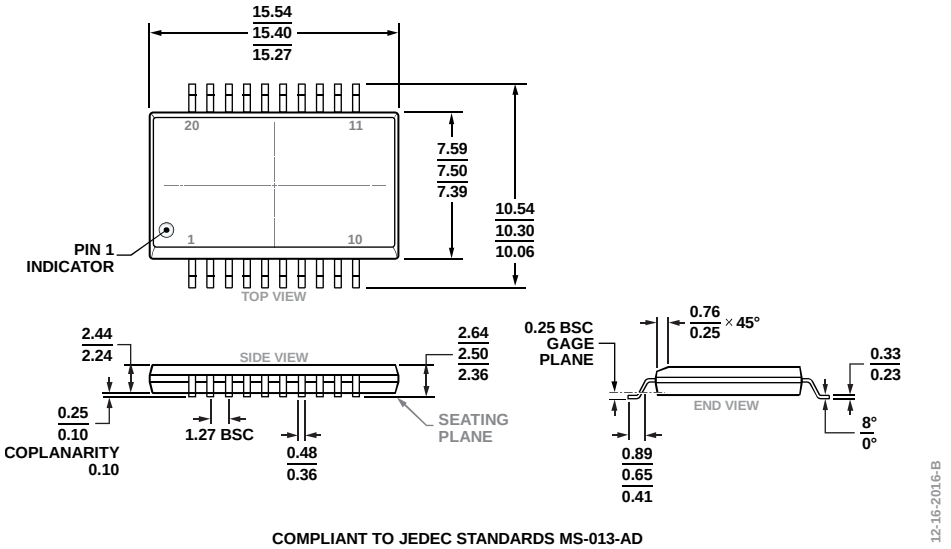
$$V_{AC\ RMS} = \sqrt{466^2 - 400^2}$$

$V_{AC\ RMS}$ = 240 V rms

In this case, ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage in Table 16 for expected lifetime, less than a 60 Hz sine wave, and it is well within the limit for a 50 year service life.

Note that the dc working voltage limit in Table 16 is set by the creepage of the package as specified in IEC 60664-1. This value may differ for specific system level standards.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AD

Figure 19. 20-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC] Wide Body (RI-20-1) Dimension shown in millimeters

ORDERING GUIDE

Model[1, 2]	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Maximum Data Rate (MHz)	Maximum Propagation Delay, 5 V (ns)	Isolation Rating (V ac)	Temperature Range	Package Description	Package Option
ADuM4150ARIZ	4	2	10	24	5000	−40°C to +125°C	20-Lead SOIC_IC	RI-20-1
ADuM4150ARIZ-RL	4	2	10	24	5000	−40°C to +125°C	20-Lead SOIC_IC, 13″ Tape and Reel	RI-20-1
ADuM4150BRIZ	4	2	17	13	5000	−40°C to +125°C	20-Lead SOIC_IC	RI-20-1
ADuM4150BRIZ-RL	4	2	17	13	5000	−40°C to +125°C	20-Lead SOIC_IC, 13″ Tape and Reel	RI-20-1
EVAL-ADuM3150Z							Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] The EVAL-ADuM3150Z uses a functionally equivalent device for evaluation. The pad layout on the EVAL-ADuM3150Z evaluation board does not support the 20-lead SOIC_IC package.

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