19-2267; Rev 1; 10/02

MAXIM

High-Efficiency, Wide Brightness Range, CCFL Backlight Controller

General Description

The MAX1996A integrated controller is optimized to drive cold-cathode fluorescent lamps (CCFLs) using synchronized full-bridge inverter architecture. Synchronized drive provides near sinusoidal waveforms over the entire input range to maximize the life of CCFLs. The controller also operates over a wide input-voltage range with high efficiency and broad dimming range.

The MAX1996A includes safety features that limit the transformer secondary voltage and protect against single-point fault conditions including lamp-out and short-circuit faults.

The MAX1996A regulates the CCFL brightness in three ways: linearly controlling the lamp current, digital pulse-width modulating (DPWM) the lamp current, or using both methods simultaneously to achieve the widest dimming range (>30:1). CCFL brightness can be controlled with either an analog voltage or a 2-wire SMBus™-compatible interface. The MAX1996A directly drives the four external N-channel power MOSFETs of the full bridge inverter. An internal 5.3V linear regulator powers the MOSFET drivers, the synchronizable DPWM oscillator, and most of the internal circuitry.

The MAX1996A has the same pin configuration as the MAX1895, but with modified SMBus slave address (0x58) and command bytes. In addition, the lamp-out protection timer has been reduced to approximately 1s and the DPWM frequency is guaranteed from 200Hz to 220Hz over the operating temperature range without external components or trimming. The MAX1996A is available in the space-saving 28-pin thin QFN package and operates over a -40°C to +85°C temperature range.

Applications

Notebook Computers

Multibulb LCD Monitors

Portable Display Electronics

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1996AETI	-40°C to +85°C	28 Thin QFN 5 × 5
MAX1996AEGI*	-40°C to +85°C	28 QFN 5 × 5

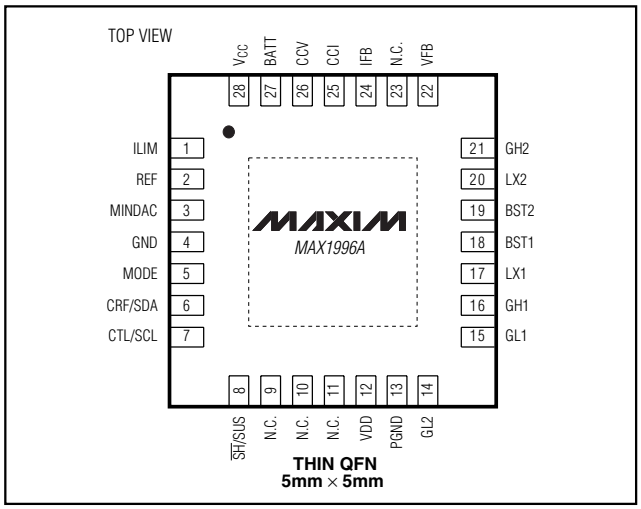
**Contact factory for availability.*

SMBus is a trademark of Intel Corp.

Features

- **SMBus Slave Address (0x58) for Wide Dimming Range Inverters**
- **Guaranteed 200Hz to 220Hz DPWM Frequency**
- **Externally Synchronizable DPWM Frequency**
- **Lamp-Out Protection with 1s Timeout**
- **Synchronized to Resonant Frequency**
  - **Good Crest Factor for Longer Lamp Life**
  - **Ensures Maximum Strike Capability**
- **High Power-to-Light Efficiency**
- **Wide Dimming Range (3 Methods)**
  - **Lamp Current Adjust: >3 to 1**
  - **DPWM: >10 to 1**
  - **Combined: >30 to 1**
- **Feed-Forward for Fast Response to Step Change of Input Voltage**
- **Wide Input-Voltage Range (4.6V to 28V)**
- **Transformer Secondary Voltage Limiting to Reduce Transformer Stress**
- **Protected Against Short-Circuit and Other Single-Point Faults**
- **Dual-Mode Brightness Control Interface**
- **Small Footprint 28-Pin Thin QFN (5mm × 5mm) Package**

Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

High-Efficiency, Wide Brightness Range, CCFL Backlight Controller

ABSOLUTE MAXIMUM RATINGS

BATT to GND .....-0.3V to +30V
BST1, BST2 to GND .....-0.3V to +36V
BST1 to LX1, BST2 to LX2 .....-0.3V to +6V
GH1 to LX1 .....-0.3V to (BST1 + 0.3V)
GH2 to LX2 .....-0.3V to (BST2 + 0.3V)
V_{CC}, V_{DD} to GND .....-0.3V to +6V
REF, ILIM to GND .....-0.3V to (V_{CC} + 0.3V)
GL1, GL2 to GND .....-0.3V to (V_{DD} + 0.3V)
MINDAC, IFB, CCV, CCI to GND .....-0.3V to +6V
MODE to GND .....-6V to +12V
VFB to GND .....-6V to +6V
CRF/SDA, CTL/SCL, $\overline{SH}$/SUS to GND .....-0.3V to +6V
PGND to GND .....-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
28-Pin QFN (derate 20.84mW/°C above +70°C) 1667mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{BATT} = 12V, MINDAC = GND, V_{CC} = V_{DD}, $V_{\overline{SH}/SUS}$ = 5.3V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BATT} Input Voltage Range	V_{CC} = V_{DD} = V_{BATT}		4.6		5.5	V
	V_{CC} = V_{DD} = open		5.5		28	
V_{BATT} Quiescent Current	$V_{\overline{SH}/SUS}$ = 5.5V	V_{BATT} = 28V		3.2	6.0	mA
		V_{BATT} = V_{CC} = 5V			6	
V_{BATT} Quiescent Current, Shutdown	$\overline{SH}$/SUS = 0			6	20	µA
V_{CC} Output Voltage, Normal Operation	$V_{\overline{SH}/SUS}$ = 5.5V, 6V < V_{BATT} < 28V 0 < I_{LOAD} < 20mA		5.00	5.35	5.50	V
V_{CC} Output Voltage, Shutdown	$\overline{SH}$/SUS = GND, no load		3.5	4.6	5.5	V
V_{CC} Undervoltage Lockout (UVLO) Threshold	V_{CC} rising (leaving lockout)				4.5	V
	V_{CC} falling (entering lockout)		4.0			
V_{CC} UVLO Lockout Hysteresis				200		mV
V_{CC} Power-On Reset (POR) Threshold	Rising edge		0.90	1.75	2.70	V
V_{CC} POR Hysteresis	Falling edge			50		mV
REF Output Voltage, Normal Operation	4.5V < V_{CC} < 5.5V, I_{LOAD} = 40µA		1.96	2.00	2.04	V
GH1, GH2, GL1, GL2 On-Resistance	I_{TEST} = 100mA, V_{CC} = V_{DD} = 5.3V			2	6	Ω
GH1, GH2, GL1, GL2 Maximum Output Current				1		A
BST1, BST2 Leakage Current	BST_ = 12V, LX_ = 7V				5	µA
Input Resonant Frequency	Guaranteed by design		20		300	kHz
Minimum Off-Time			210	315	420	ns
Maximum Off-Time			21.0	31.5	42.0	µs
Maximum Current-Limit Threshold LX1-GND, LX2-GND (Fixed)	ILIM = V_{CC}		180	200	220	mV
Maximum Current-Limit Threshold LX1-GND, LX2-GND (Adjustable)	V_{ILIM} = 0.5V		80	100	120	mV
	V_{ILIM} = 2.0V		370	400	430	

ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = 12V, MINDAC = GND, V_{CC} = V_{DD}, $V_{\overline{SH}/SUS}$ = 5.3V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Current-Crossing Threshold LX1-GND, LX2-GND				6		mV
Current-Limit Leading-Edge Blanking			210	315	420	ns
D/A Converter Resolution	Guaranteed monotonic		5			Bits
MINDAC Input Voltage Range			0		2	V
MINDAC Input Bias Current			-2		+2	µA
MINDAC Digital PWM Disable Threshold	MINDAC = V_{CC}		2.4	3.5	4.0	V
IFB Input Voltage Range			0		1.7	V
IFB Regulation Point	V_{MINDAC} = 0V, DAC code = 11111 binary		368	388	408	mV
	V_{MINDAC} = 0V, DAC code = 00100 binary		30	50	70	
	V_{MINDAC} = 1V, DAC code = 00000 binary		180	200	220	
IFB Input Bias Current			-2		+2	µA
IFB Lamp-Out Threshold			125	150	175	mV
IFB to CCI Transconductance	1V < V_{CCI} < 2.5V			100		µS
CCI Output Impedance				20		MΩ
V_{FB} Input Voltage Range			-2		+2	V
V_{FB} Input Bias Current	V_{FB} = 0V		-0.5		+0.5	µA
V_{FB} Regulation Point			490	510	530	mV
V_{FB} to CCV Transconductance	1V < V_{CCV} < 2.7V			40		µS
V_{FB} Zero-Voltage Crossing Threshold			-10		+10	mV
CCV Output Impedance				20		MΩ
Digital PWM Chop-Mode Frequency	No AC signal on MODE		200	210	220	Hz
	32kHz AC signal on MODE			250		
	100kHz AC signal on MODE			781		
MODE-to-DPWM Sync Ratio	f_{MODE}/f_{DPWM}			128		
Lamp-Out Detection Timeout Timer (Note 2)	V_{IFB} < 0.1V	No AC signal on MODE	1.14	1.22	1.30	s
		32kHz AC signal on MODE		1.02		
		100kHz AC signal on MODE		0.33		
MODE Operating Voltage Range			-5.5		11.0	V
MODE Input Current	MODE = GND or V_{CC}		-1		+1	µA
Positive Analog Interface Mode, MODE = GND Threshold ($V_{CTL/SCL}$ = 0V Sets Minimum Brightness)	Sync clock average value on MODE to sync DPWM oscillator, not in shutdown (Note 3)				0.6	V
Negative Analog Interface Mode, MODE = REF Threshold ($V_{CTL/SCL}$ = 0V Sets Maximum Brightness = 0V)	Sync clock average value on MODE to sync DPWM oscillator, not in shutdown (Note 3)		1.4		2.6	V
SMBus Interface Mode, MODE = V_{CC} Threshold	Sync clock average value on MODE to sync DPWM oscillator, not in shutdown (Note 3)		V_{CC} - 0.6			V

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ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = 12V, MINDAC = GND, V_{CC} = V_{DD}, $V_{\overline{SH}/SUS}$ = 5.3V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MODE AC Signal Amplitude	Peak-to-peak (Note 4)	2		5	V
MODE AC Signal Synchronization Range	Chopping oscillator synchronized to MODE	32		100	kHz
CRF/SDA Input Range		2.7		5.5	V
CRF/SDA Input Current	$V_{CRF/SDA}$ = 5.5V, $\overline{SH}$/SUS = V_{CC}			20	µA
	$V_{CRF/SDA}$ = 5.5V, $\overline{SH}$/SUS = 0V	-1		+1	
CTL/SCL Input Range		0		$V_{CRF/SDA}$	V
CTL/SCL Input Current	MODE = REF or GND	-1		+1	µA
A/D Converter Resolution	Guaranteed monotonic		5		Bits
A/D Converter Hysteresis			1		LSB
$\overline{SH}$/SUS Input Low Voltage				0.8	V
$\overline{SH}$/SUS Input High Voltage		2.1			V
$\overline{SH}$/SUS Input Hysteresis			300		mV
$\overline{SH}$/SUS Input Bias Current		-1		+1	µA
SDA, SCL Input Low Voltage				0.8	V
SDA, SCL Input High Voltage		2.1			V
SDA, SCL Input Hysteresis			300		mV
SDA Output Low Sink Current	$V_{CRF/SDA}$ = 0.4V	4			mA
SCL Serial Clock High Period	T_{HIGH}	4			µs
SCL Serial Clock Low Period	T_{LOW}	4.7			µs
Start Condition Setup Time	$t_{SU:STA}$	4.7			µs
Start Condition Hold Time	$t_{HD:STA}$	4			µs
SDA Valid to SCL Rising-Edge Setup Time, Slave Clocking in Data	$t_{SU:DAT}$	250			ns
SCL Falling Edge to SDA Transition	$t_{HD:DAT}$	0			ns
SCL Falling Edge to SDA Valid, Reading Out Data	T_{DV}		700		ns

ELECTRICAL CHARACTERISTICS

(V_{BATT} = 12V, MINDAC = GND, V_{CC} = V_{DD}, $V_{\overline{SH}/SUS}$ = 5.3V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BATT} Input Voltage Range	V_{CC} = V_{DD} = V_{BATT}		4.6		5.5	V
	V_{CC} = V_{DD} = open		5.5		28.0	
V_{BATT} Quiescent Current	$V_{\overline{SH}/SUS}$ = 5.5V	V_{BATT} = 28V			6	mA
		V_{BATT} = V_{CC} = 5V			6	
V_{BATT} Quiescent Current, Shutdown	$V_{\overline{SH}/SUS}$ = 0V				20	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = 12V, MINDAC = GND, V_{CC} = V_{DD}, $V_{\overline{SH}/SUS}$ = 5.3V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

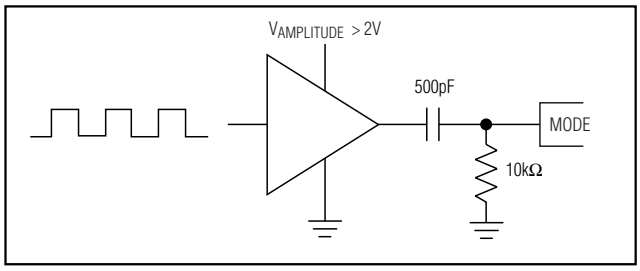
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Output Voltage, Normal Operation	$V_{\overline{SH}/SUS}$ = 5.5V, 6V < V_{BATT} < 28V, 0 < I_{LOAD} < 20mA	5.0		5.5	V
V_{CC} Output Voltage, Shutdown	$\overline{SH}$/SUS = GND, no load	3.5		5.5	V
V_{CC} UVLO Threshold	V_{CC} rising (leaving lockout)			4.5	V
	V_{CC} rising (entering lockout)	4			
V_{CC} POR Threshold	Rising edge	0.9		2.7	V
REF Output Voltage, Normal Operation	4.5V < V_{CC} < 5.5V, I_{LOAD} = 40µA	1.96		2.04	V
GH1, GH2, GL1, GL2 On-Resistance	I_{TEST} = 100mA			10	Ω
Maximum Current-Limit Threshold LX1-GND, LX2-GND (Fixed)	I_{LIM} = V_{CC}	180		220	mV
Maximum Current-Limit Threshold LX1-GND, LX2-GND (Adjustable)	V_{ILIM} = 0.5V	80		120	mV
	V_{ILIM} = 2.0V	360		440	
IFB Input Voltage Range		0		1.7	V
IFB Regulation Point	V_{MINDAC} = 0V, DAC code = 11111 binary	335		440	mV
IFB Input Bias Current		-2		+2	µA
IFB Lamp-Out Threshold		120		180	mV
VFB Input Voltage Range		-2		+2	V
VFB Input Bias Current	VFB = 0V	-0.5		0.5	µA
VFB Regulation Point		480		540	mV
VFB Zero-Voltage Crossing Threshold		-20		+20	mV
SHVSUS Input Low Voltage				0.8	V
SHVSUS Input High Voltage		2.1			V
SDA, SCL Input Low Voltage				0.8	V
SDA, SCL Input High Voltage		2.1			V
SDA Output Low Sink Current	$V_{CRF/SDA}$ = 0.4V	4			mA

Note 1: Specifications to -40°C are guaranteed by design based on final test characterization results.

Note 2: Corresponds to 256 DPWM cycles or 32768 MODE cycles.

Note 3: The MODE pin thresholds are only valid while the part is operating. When in shutdown, V_{REF} = 0 and the part only differentiates between SMB mode and ADC mode. When in shutdown and with ADC mode selected, the CRF/SDA and CTL/SCL pins are at high impedance and do not cause extra supply current when their voltages are not at GND or V_{CC}.

Note 4: The amplitude is measured with the following circuit:

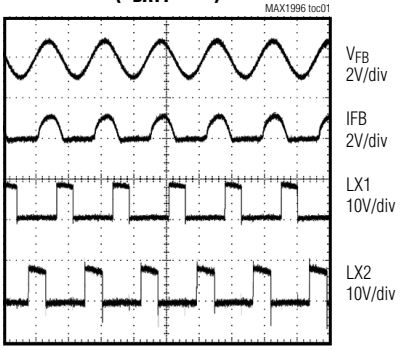


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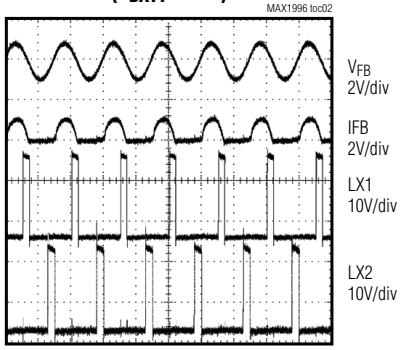
Typical Operating Characteristics

(V_{BATT} = 12V, V_{CTL} = V_{CRF}, V_{MINDAC} = 1V, MODE = GND, circuit of Figure 1, Table 4.)

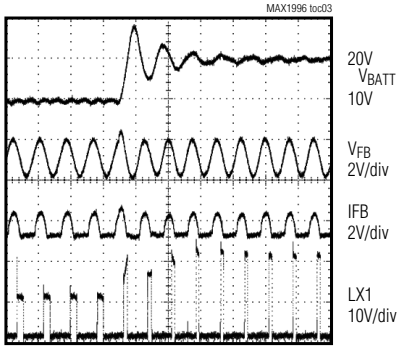
LOW INPUT-VOLTAGE OPERATION (V_{BATT} = 8V)



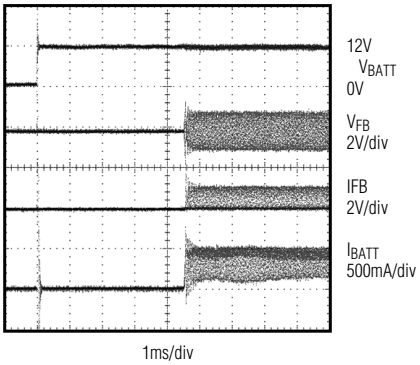
HIGH INPUT-VOLTAGE OPERATION (V_{BATT} = 20V)



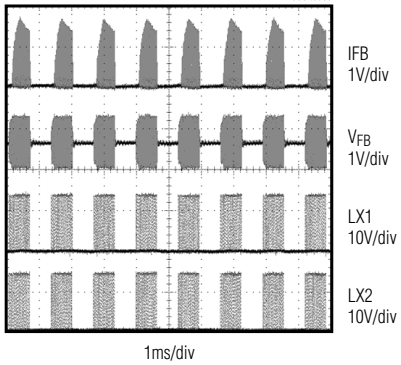
FEED-FORWARD COMPENSATION



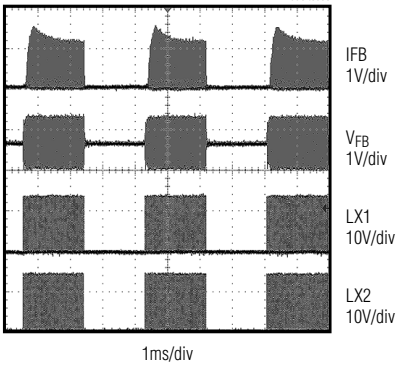
STARTUP



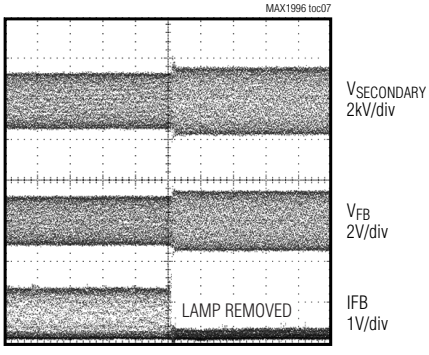
SYNCHRONIZED DPWM (f_{MODE} = 100kHz, DPWM = 50%)



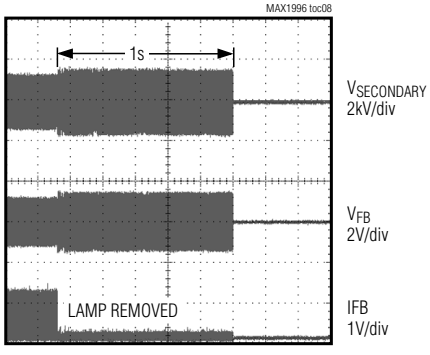
SYNCHRONIZED DPWM (f_{MODE} = 32kHz, DPWM = 50%)



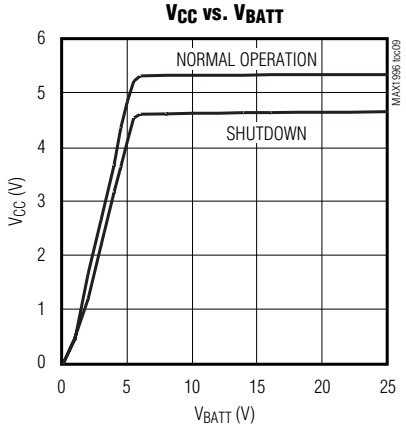
LAMP-OUT VOLTAGE LIMITING



LAMP-OUT PROTECTION

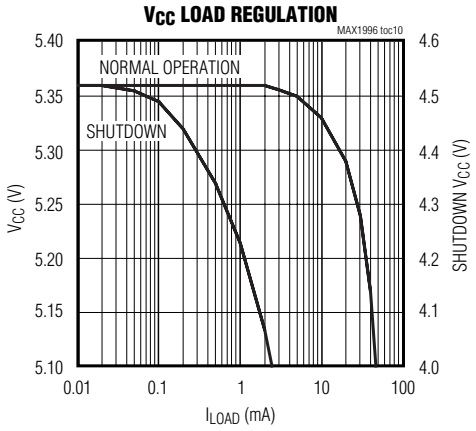


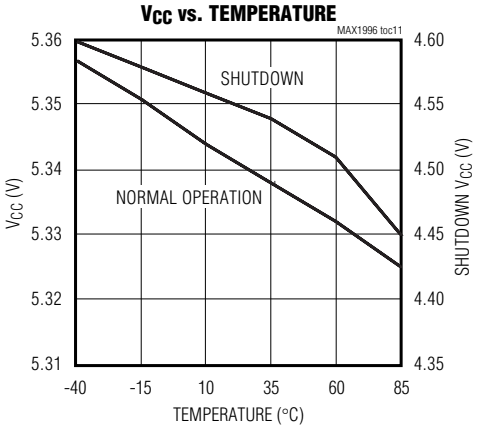
V_{CC} vs. V_{BATT}



Typical Operating Characteristics (continued)

(V_{BATT} = 12V, V_{CTL} = V_{CRF}, V_{MINDAC} = 1V, MODE = GND, circuit of Figure 1, Table 4.)





Pin Description

PIN	NAME	FUNCTION
1	ILIM	Current-Limit Threshold Adjustment. Bias ILIM with a resistive voltage-divider between REF or V_{CC} and GND. The current-limit threshold measured between LX_ and GND is 1/5th the voltage at ILIM; ILIM adjustment range is 0V to 3V. Connect ILIM to V_{CC} to set the default current-limit threshold to 0.2V.
2	REF	2V Reference Output. Bypass REF to GND with a 0.1µF capacitor. REF is discharged to GND when shut down.
3	MINDAC	DAC Zero-Scale Input. V_{MINDAC} sets the D/A converter's minimum-scale output voltage. Disable DPWM by connecting MINDAC to V_{CC}.
4	GND	System Ground. The GND input to the maximum and minimum current-limit comparators. The comparators sense the low-side FET NL1 and NL2 for zero-current crossing and current limit.
5	MODE	Interface Selection Input and Sync Input for DPWM Chopping. The average voltage on the MODE pin selects one of three CCFL brightness control interfaces: MODE = V_{CC} enables SMBus serial interface. MODE = GND enables the analog interface (positive analog interface mode), $V_{CTL/SCL}$ = 0V sets minimum brightness. MODE = REF enables the analog interface (reverse analog interface mode), $V_{CTL/SCL}$ = 0V sets maximum brightness. An AC clocking signal superimposed on the DC average MODE pin voltage can be used to synchronize the DPWM chopping frequency. See *Synchronizing the DPWM Frequency*.
6	CRF/SDA	Reference and Serial Data Input. In analog interface mode, pin 6 is the reference input to the 5-bit brightness control ADC. Bypass CRF to GND with a 0.1µF capacitor. In SMBus interface mode, SDA is an SMBus serial data input/open-drain output.

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Pin Description (continued)

PIN	NAME	FUNCTION
7	CTL/SCL	Brightness Control and Serial Clock Input. In analog interface mode, pin 7 is a CCFL brightness control input. CTL varies from 0V to REF to linearly control lamp brightness. In SMBus interface mode, SCL is an SMBus serial clock input.
8	$\overline{SH}$/SUS	Shutdown and Suspend Mode Control. In analog interface mode, pin 8 is an active-low shutdown input. In SMBus interface mode, pin 8 is an SMBus suspend control input.
9, 10, 11, 23	N.C.	No Connection. Not internally connected.
12	V_{DD}	Power Supply for Gate Drivers. Connect V_{DD} to the output of the linear regulator (V_{CC}). Bypass V_{DD} with a 0.1µF capacitor to PGND.
13	PGND	Power Ground. Gate-driver current flows through this pin.
14	GL2	Low-Side FET NL2 Gate-Driver Output
15	GL1	Low-Side FET NL1 Gate-Driver Output
16	GH1	High-Side FET NH1 Gate-Driver Output
17	LX1	Switching Node Connection. LX1 is the internal lower supply rail for the GH1 high-side gate driver. LX1 is also the sense input to the current comparators.
18	BST1	High-Side FET NH1 Driver Bootstrap Input. Connect BST1 through a diode to V_{DD} and through a 0.1µF capacitor to LX1 (Figure 1).
19	BST2	High-Side FET NH2 Driver Bootstrap Input. Connect BST2 through a diode to V_{DD} and through a 0.1µF capacitor to LX2 (Figure 1).
20	LX2	Switching Node Connection. LX2 is the internal lower supply rail for the GH2 high-side gate driver. LX2 is also the sense input to the current comparators.
21	GH2	High-Side FET NH2 Gate-Driver Output
22	VFB	Lamp-Output Feedback-Sense Input. The average value on VFB is regulated during startup and open-lamp conditions to 0.5V by controlling the on-time of high-side switches. A capacitive voltage-divider between the CCFL lamp output and GND is sensed to set the maximum average lamp output voltage.
24	IFB	Lamp Current-Sense Input. The voltage on IFB is used to regulate the lamp current. If the IFB input falls below 150mV for 1s, then the MAX1996A signals an open-lamp fault.
25	CCI	Current-Loop Compensation Pin. CCI is the output of the current-loop transconductance amplifier (GMI) that regulates the CCFL current. The CCI voltage controls the time interval in which full-bridge applies the input voltage (BATT) to transformer network. Connect CCI to GND through a 0.1µF capacitor. CCI is internally discharged to GND in shutdown.
26	CCV	Voltage-Loop Compensation Pin. CCV is the output of the voltage-loop transconductance amplifier (GMV) that regulates the maximum average secondary transformer voltage. Connect CCV to GND with a 10nF capacitor. The CCV voltage controls the time interval that the full bridge applies the input voltage (BATT) to transformer network. CCV is internally discharged to GND in shutdown.
27	BATT	Supply Input. Input to the internal 5.3V linear regulator that provides power (V_{CC}) to the chip. Bypass BATT to GND with a 0.1µF capacitor.
28	V_{CC}	5.3V Linear-Regulator Output. V_{CC} is the supply voltage for the MAX1996A. Bypass V_{CC} to GND with a 0.47µF ceramic capacitor. V_{CC} can also be connected to BATT if $V_{BATT} < 5.5V$.

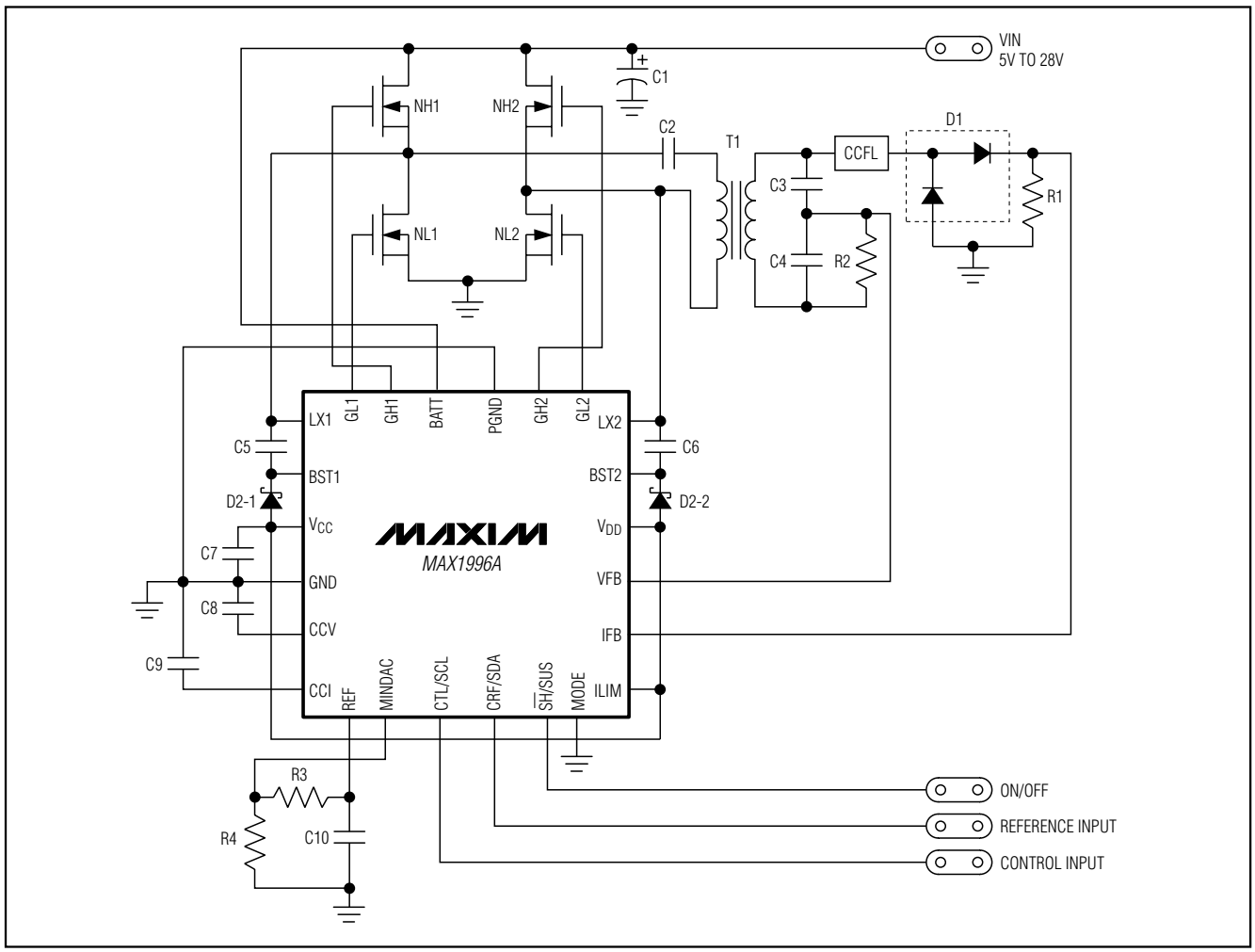


Figure 1. Standard Application Circuit

Detailed Description

The MAX1996A is optimized to drive CCFLs using a synchronized full-bridge inverter architecture. The drive to the full-bridge MOSFETs is synchronized to the resonant frequency of the tank circuit so that the CCFL's full-strike voltage develops for all operating conditions. The synchronized architecture provides near sinusoidal drive waveforms over the entire input range to maximize the life of CCFLs. The MAX1996A operates over a wide input voltage range (4.6V to 28V), achieves high efficiency, and maximizes dimming range.

The MAX1996A regulates the brightness of a CCFL in three ways:

1) Linearly controlling the lamp current.
2) Digitally pulse-width modulating (or chopping) the lamp current (DPWM).
3) Using both methods simultaneously for widest dimming range.

DPWM is implemented by pulse-width modulating the lamp current at a rate faster than the eye can detect.

The MAX1996A includes a 5.3V linear regulator to power the drivers for full-bridge switches, the synchronizable DPWM oscillator, and most of the internal circuitry. The MAX1996A is very flexible and can be controlled with an analog interface or with an SMBus interface.

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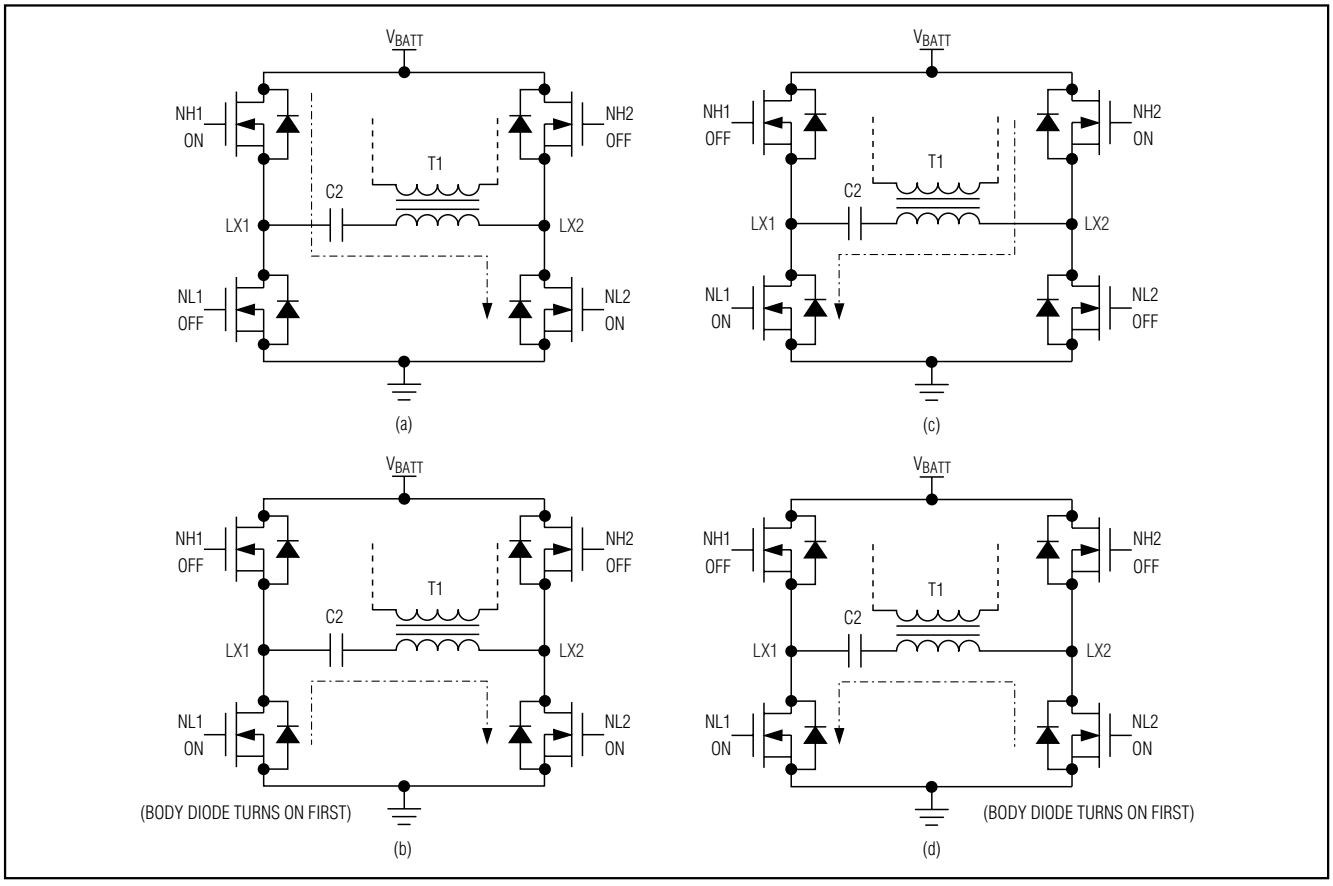


Figure 2. Resonant Operation

Resonant Operation

The MAX1996A drives the four N-channel power MOSFETs that make up the zero-voltage switching (ZVS) full-bridge inverter as shown in Figure 1. The LX1 and LX2 switching nodes are AC coupled to the primary side of the transformer.

Assume that NH1 and NL2 are turned on at the beginning of the cycle as shown in Figure 2(a). The primary current flows through MOSFET NH1, DC blocking cap C2, the primary side of transformer T1, and finally MOSFET NL2. During this interval, the primary current ramps up until the controller turns off NH1. When NH1 is off, the primary current forward biases the body diode of NL1 and brings the LX1 node down as shown in Figure 2(b). When the controller turns on NL1, its drain-to-source voltage is near zero because its forward-biased body diode clamps the drain. Since NL2 is still on, the primary current flows through NL1, C2, the primary side of T1, and finally NL2. Once the primary current drops to the minimum current threshold (6mV/R_{DSON}), the controller turns off NL2. The remaining energy in T1 charges up the LX2 node until the body diode of NH2 is forward biased. When NH2 turns on, it does so with near zero drain-to-source voltage. The primary current reverses polarity as shown in Figure 2(c), beginning a new cycle with the current flowing in the opposite direction, with NH2 and NL1 on. The primary current ramps up until the controller turns off NH2. When NH2 is off, the primary current forward biases the body diode of NL2, and brings the LX2 node down as shown in Figure 2(d). After the LX2 node goes low, the controller losslessly turns on NL2. Once the primary current drops to the minimum current threshold, the controller turns off NL1. The remaining energy charges up the LX1 node until the body diode of NH1 is forward biased. Finally, NH1 losslessly turns on, beginning a new cycle as shown in Figure 2(a).

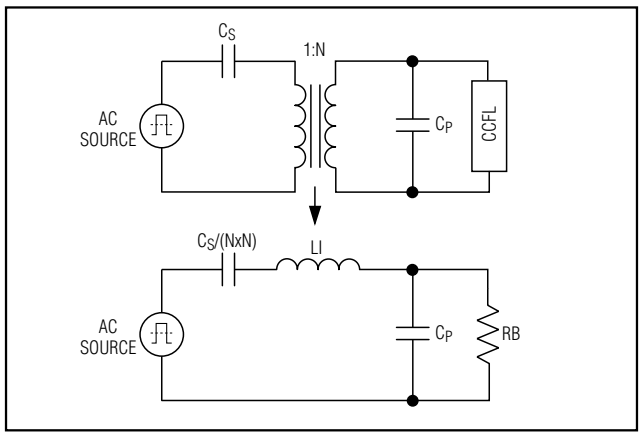


Figure 3. Equivalent Circuit

Note that switching transitions on all four power MOSFETs occur under ZVS conditions, which reduces transient power losses and EMI.

The equivalent circuit of the resonant tank is shown in Figure 3. The resonant frequency is determined by the RLC resonant tank elements: C_S, C_P, L_L, and RB. C_S is the series capacitance on the primary side of the transformer. C_P is the parallel cap on the transformer's secondary. L_L is the transformer secondary leakage inductance. RB is an idealized resistance that models the CCFL load in normal operation.

Current and Voltage-Control Loops

The MAX1996A uses a current loop and a voltage loop to control the energy applied to the CCFL. The current loop is the dominant control in setting the lamp brightness. The rectified lamp current is measured with a sense resistor in series with the CCFL. The voltage across this resistor is applied to the IFB input to regulate the average lamp current. The voltage loop controls the voltage across the lamp and is active during the beginning of DPWM on-cycles and the open-lamp fault condition. It limits the energy applied to the resonant network once the transformer secondary voltage is above the threshold of 500mV average measured at V_{FB}.

Both voltage and current circuits use transconductance-error amplifiers to compensate the loops. The voltage-error amplifier creates an error current based upon the voltage difference between V_{FB} and the internal reference level (typically 500mV) (Figure 4). The error current is then used to charge and discharge a capacitor at the CCV output to create an error voltage V_{CCV}. The current loop produces a similar signal at CCI based on the voltage difference between IFB and the dimming control signal. This signal is set by either the SMBus interface or the analog interface (see the *Dimming Range* section). This error voltage is called V_{CCI}. In normal operation, the current loop is in control of the regulator so long as V_{CCI} is less than V_{CCV}. The control signal is compared with an internal ramp signal to set the high-side switch on time (t_{ON}).

When DPWM is employed, the two control loops work together to limit the transformer voltage and to allow a wide dimming range with good line rejection. During the DPWM off-cycle, V_{CCV} is set to 1.2V and the current-loop error amplifier output is high impedance. V_{VFB} is set to 0.6V to create a soft-start at the beginning of each DPWM on-cycle in order to avoid overshoot on the transformer's secondary. When the transconductance amplifier in the current loop is high impedance, it acts like a sample-and-hold circuit to keep V_{CCI} from changing during the off-cycles. This action allows the current-control loop to regulate the average lamp current.

See the *Current-Sense Resistor* and the *Voltage-Sense Capacitors* sections for information regarding setting the current- and voltage-loop thresholds.

Startup

Operation during startup differs from the steady-state condition described in the *Current and Voltage-Control Loops* section. Upon power-up, V_{CCI} slowly rises, increasing the duty cycle, which provides soft-start. During this time, V_{CCV}, which is the faster control loop, is limited to 150mV above V_{CCI}. Once the secondary voltage reaches the strike voltage, the lamp current begins to increase. When the lamp current reaches the regulation point, V_{CCI} exceeds V_{CCV} and it reaches steady state. With MINDAC = V_{CC}, DPWM is disabled and the current loop remains in control regulating the lamp current.

Feed-Forward Control

The MAX1996A has a feed-forward control circuit, which influences both control loops. Feed-forward control instantly adjusts the t_{ON} time to changes in input voltage. This feature provides immunity to changes in input voltage at all brightness levels and makes compensation over wide input ranges easier. The feed-forward circuit improves line regulation for short DPWM on-times and makes startup transients less dependent on input voltage.

Feed-forward control is implemented by varying the internal voltage ramp rate. This has the effect of varying t_{ON} as a function of input voltage while maintaining about the same signal levels at V_{CCI} and V_{CCV}. Since the required voltage change across the compensation capacitors is minimal, the controller's response to change in V_{BATT} is essentially instantaneous.

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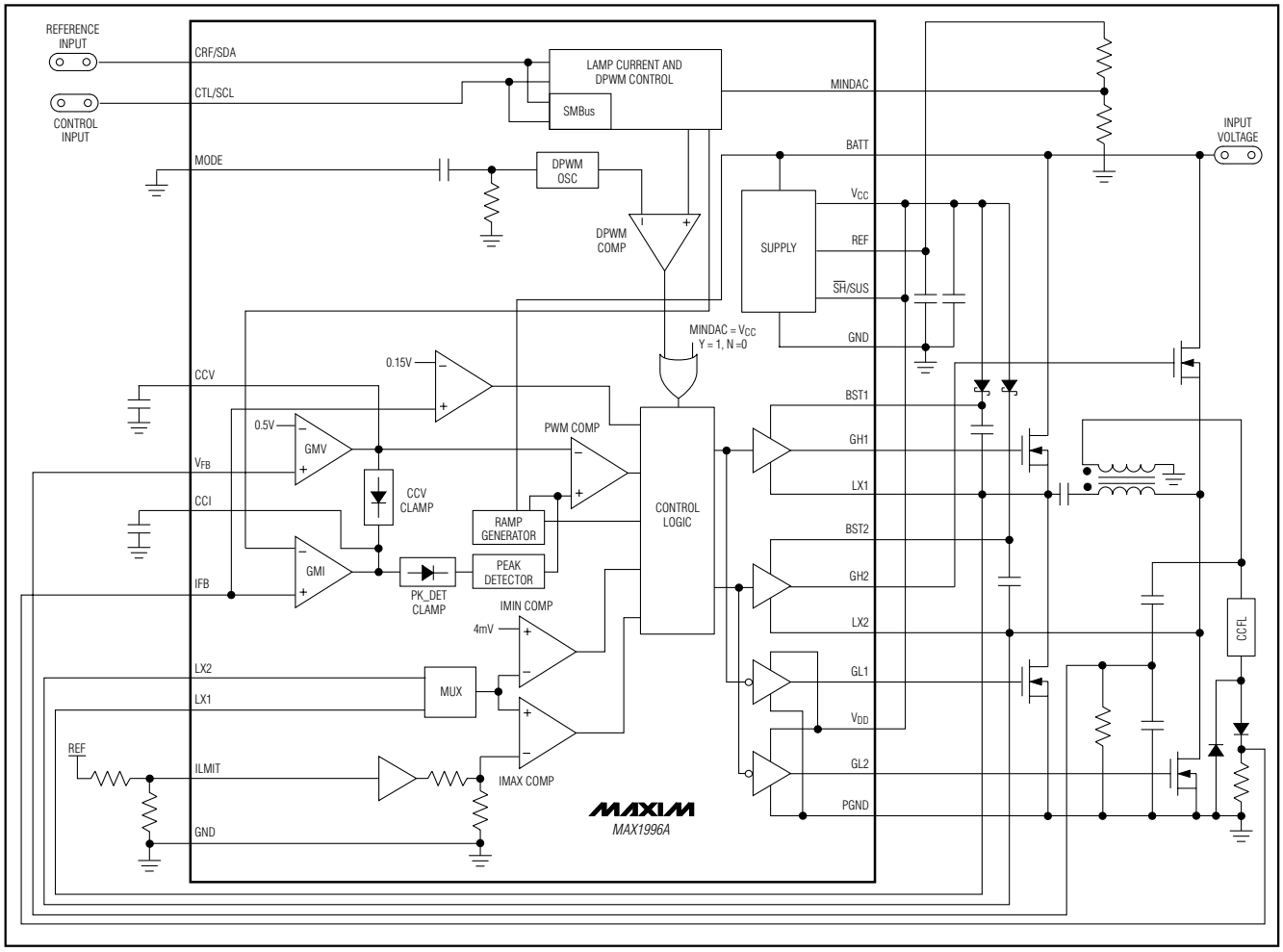


Figure 4. Functional Diagram

Transient Overvoltage Protection from Dropout

The MAX1996A is designed to maintain tight control of the transformer secondary under all transient conditions including dropout. To maximize run time, it is desirable to allow the circuit to operate in dropout at extremely low battery voltages where the backlight's performance is not critical. When V_{BATT} is very low, the controller can lose regulation and run at maximum duty cycle. Under these circumstances, a transient overvoltage condition can occur when the AC adapter is suddenly applied to power the circuit. The feed-forward circuitry minimizes variations in lamp voltage due to such input voltage steps. The regulator also clamps the voltage on V_{CCI}. Both features ensure that overvoltage transients do not appear on the transformer when leaving dropout.

The V_{CCI} clamp is unique in that it limits at the peaks of the voltage-ramp generator. As the circuit reaches dropout, V_{CCI} approaches the peaks of the ramp generator in order to reach maximum t_{ON}. If V_{BATT} decreases further, the control loop loses regulation and V_{CCI} tries to reach its positive supply rail. The clamp on V_{CCI} prevents this from happening and V_{CCI} rides just above the peaks of the PWM ramp. If V_{BATT} continues to decrease, the feed-forward PWM ramp generator loses amplitude and the clamp drags V_{CCI} down with it to a voltage below where V_{CCI} would have been if the circuit were not in dropout. When V_{BATT} suddenly steps out of dropout, V_{CCI} is still low and the MAX1996A maintains the drive on the transformer at the old dropout level. The control

Table 1. Interface Modes

PIN	DIGITAL INTERFACE	ANALOG INTERFACE	
	MODE = V_{CC}	**MODE = REF** **$V_{CTL/SCL}$ = 0 = maximum brightness**	**MODE = GND** **$V_{CTL/SCL}$ = 0 = minimum brightness**
$\overline{SH}$/SUS	SMBus suspend	Logic level shutdown control input	
CRF/SDA	SMBus data I/O	Reference input for minimum brightness	Reference input for maximum brightness
CTL/SCL	SMBus clock input	Analog control input to set brightness (range from 0 to CRF/SDA)	

loop then slowly corrects the lamp current by increasing V_{CCI}, which brings the circuit back into regulation.

Interface Selection

Table 1 describes the functionality of $\overline{SH}$/SUS, CRF/SDA, and CTL/SCL in each of the MAX1996A's three interface modes. The MAX1996A features both an SMBus digital interface and an analog interface. Note that the MODE signal can also synchronize the DPWM frequency. (See *Synchronizing the DPWM Frequency*.)

Dimming Range

The brightness is controlled by either the Analog Interface (see the *Analog Interface* section) or the SMBus Interface (see the *SMBus Interface* section). The brightness of the CCFL is adjusted in the following three ways:

1) Lamp-current control, where the magnitude of the average lamp current is adjusted.
2) DPWM control, where the average lamp current is pulsed to the set level with a variable duty cycle.
3) The combination of the first two methods.

In each of the three methods, a 5-bit brightness code is generated from the selected interface and is used to set the lamp current and/or DPWM duty cycle.

The 5-bit brightness code defines the lamp current level with 00000\b representing minimum lamp current and 11111\b representing maximum lamp current. The average lamp current is measured across an external sense resistor (see the *Current-Sense Resistor* section). The voltage on the sense resistor is measured at IFB. The brightness code adjusts the regulation voltage at IFB (V_{IFB}). The minimum average V_{IFB} is $V_{MINDAC}/5$, where V_{MINDAC} varies between 0 to 2V, and the maximum average is set by the following formula:

$$V_{IFB} = V_{REF} \times 31 / 160 + V_{MINDAC} / 160,$$

which is between 387.5mV and 400mV.

If V_{IFB} does not exceed 150mV peak (which is about 47.7mV/R1 RMS lamp current) for greater than 1s, the MAX1996A assumes a lamp-out condition and shuts down (see the *Lamp-Out Detection* section).

The equation relating brightness code to IFB regulation voltage is:

$$V_{IFB} = V_{REF} \times n / 160 + V_{MINDAC} \times (32 - n) / 160$$

where n is the brightness code.

To always use maximum average lamp current when using DPWM control, set V_{MINDAC} to V_{REF}.

DPWM control is similar to lamp-current control in that it also responds to the 5-bit brightness code. A brightness code of 00000\b corresponds to a 9% DPWM duty cycle and a brightness code of 11111\b corresponds to a 100% DPWM duty cycle. The duty cycle changes by 3.125% per step, but codes 00000\b to 00011\b all produce 9% (Figure 5).

To disable DPWM and always use 100% duty cycle, set V_{MINDAC} to V_{CC}. Note that with DPWM disabled, the equations shown above should assume V_{MINDAC} = 0 instead of $V_{MINDAC} = V_{CC}$. Table 2 describes MINDAC's functionality and Table 3 shows some typical settings for the brightness adjustment.

In normal operation, V_{MINDAC} is set between zero and V_{REF} and the MAX1996A uses both lamp-current control and DPWM control to vary the lamp brightness (Figure 6). In this mode, lamp-current control regulates the average lamp current during a DPWM on-cycle.

Analog Interface and Brightness Code

The MAX1996A's analog interface uses an internal ADC with 1-bit hysteresis to generate the brightness code used to dim the lamp (see the *Dimming Range* section). CTL/SCL is the ADC's input and CRF/SDA is its reference voltage. The ADC can operate in either positive-scale ADC mode or negative-scale ADC mode. In positive-scale ADC mode, the brightness code increases from 0 to 31 as V_{CTL} increases from zero to V_{CRF}.

In negative-scale mode, the brightness scale decreases from 31 to zero as V_{CTL} increases from zero to V_{CRF}.

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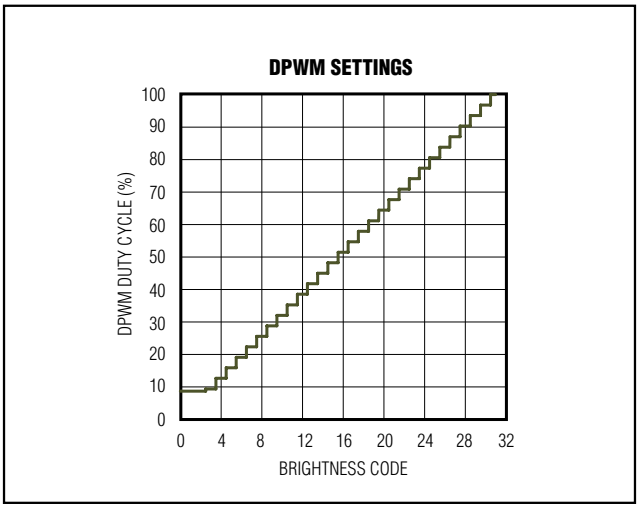


Figure 5. DPWM Settings

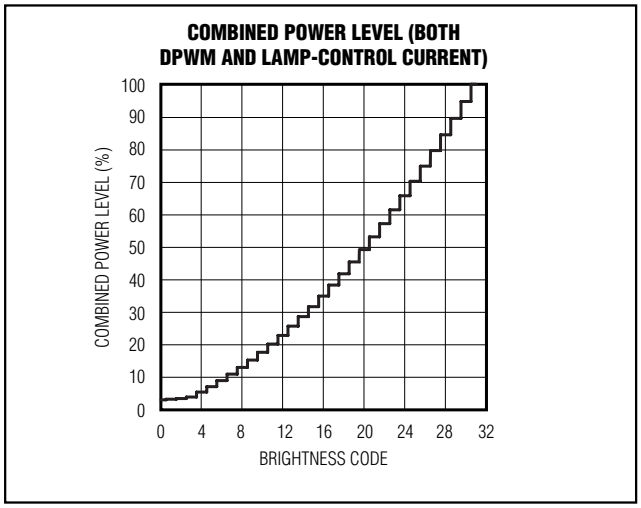


Figure 6. Combined Power Level

Table 2. MINDAC Functionality

CONDITION	FUNCTION
MINDAC = V_{CC}	DPWM disabled (always on 100% duty cycle). Operates in lamp-current control only. (Use V_{MINDAC} = 0 in the equations.)
MINDAC = REF	DPWM control enabled, duty cycle ranges from 9% to 100%. Lamp-current control is disabled (always maximum current).
$0 \le V_{MINDAC} < V_{REF}$	The device uses both lamp-current control and DPWM.

Table 3. Brightness Adjustment Ranges

RANGE	POSITIVE-SCALE ADC MODE	NEGATIVE-SCALE ADC MODE	SMBus	DAC OUTPUT	DPWM DUTY CYCLE (%)	COMBINED POWER LEVEL (%)
Maximum Brightness	MODE = GND, $V_{CRF/SDA}$ = $V_{CTL/SCL}$	MODE = REF, $V_{CRF/SDA}$ = 0	Bright [4:0] = 11111	Full-scale DAC output = 387.5mV	100	100
Minimum Brightness	MODE = GND, $V_{CRF/SDA}$ = 0, V_{MINDAC} = 1/3V_{REF}	MODE = REF, $V_{CRF/SDA}$ = $V_{CTL/SCL}$, V_{MINDAC} = 1/3V_{REF}	Bright [4:0] = 00000 V_{MINDAC} = 1/3V_{REF}	Zero-scale DAC output = V_{MINDAC}/5	9	3

Note: *The current level range is solely determined by the MINDAC to REF ratio and is externally set.*

The analog interface's internal ADC uses 1-bit hysteresis to keep the lamp from flickering between two codes. V_{CTL}'s positive threshold ($V_{CTL(TH)}$) is the voltage required to transition the brightness code as V_{CTL} increases and can be calculated as follows:

$V_{CTL(TH)} = (n + 2) / 33\ V_{CRF}$ (Positive-Scale ADC mode, MODE = GND)

$V_{CTL(TH)} = (33 - n) / 33\ V_{CRF}$ (Negative-Scale ADC mode, MODE = REF)

V_{CTL}'s negative threshold is the voltage required to transition the brightness code as V_{CTL} decreases and can be calculated as follows:

$V_{CTL(TH)} = n / 33\ V_{CRF}$ (Positive-Scale ADC mode, MODE = GND)

$V_{CTL(TH)} = (31 - n) / 33\ V_{CRF}$ (Negative-Scale ADC mode, MODE = REF)

where n is the brightness code. See Figure 7 for a graphical representation of the thresholds.

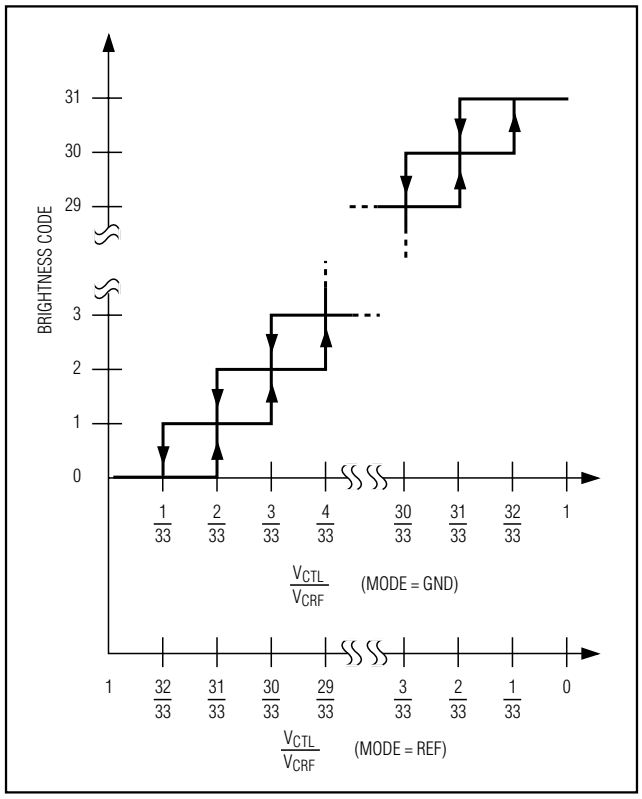


Figure 7. Brightness Code

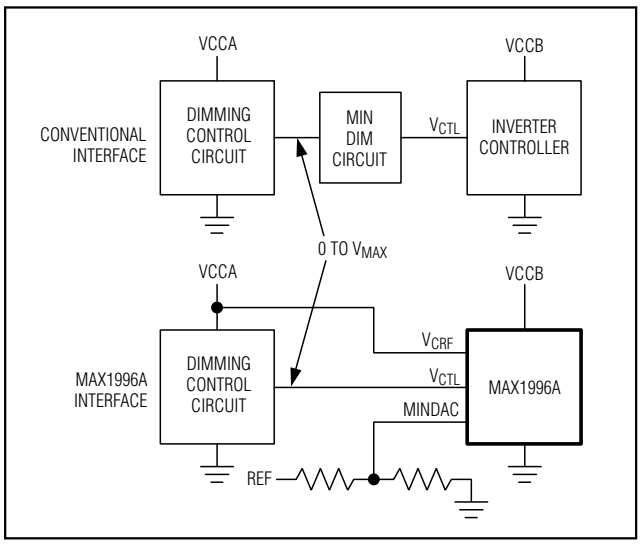


Figure 8. Analog Interface for Dimming

See the *Digital Interface* section for instructions on using the SMBus interface.

Unlike conventional dimming control circuits that have separate supplies and require additional minimum brightness circuitry, the MAX1996A provides dedicated pins for dimming control. The advantages of the MAX1996A's analog interface are illustrated in Figure 8. The analog interface is very simple in that the output voltage range of the dimming control circuit matches the input voltage range of the inverter control IC. With this method, it is possible to guarantee the maximum dimming range (Figure 9). For the conventional interface, the control voltage and the input voltage have different ranges. To avoid nonuniform lighting across the CCFL tube, or the thermometer effect, the lower limits of maximum and minimum control voltages have to be above the upper limits of the maximum and minimum input voltages, respectively. Therefore, the useful dimming range is reduced. For the MAX1996A's analog interface, the control voltage has the same range as the input voltage, so the useful dimming range is maximized.

Synchronizing the DPWM Frequency

MODE has two functions: one is to select the interface mode as described in the *Interface Selection* section and the other is to synchronize the DPWM chopping frequency to an external signal to prevent unwanted artifacts in the display screen.

To synchronize the DPWM frequency, connect MODE to V_{CC}, REF, or GND through a 10kΩ resistor. Then connect

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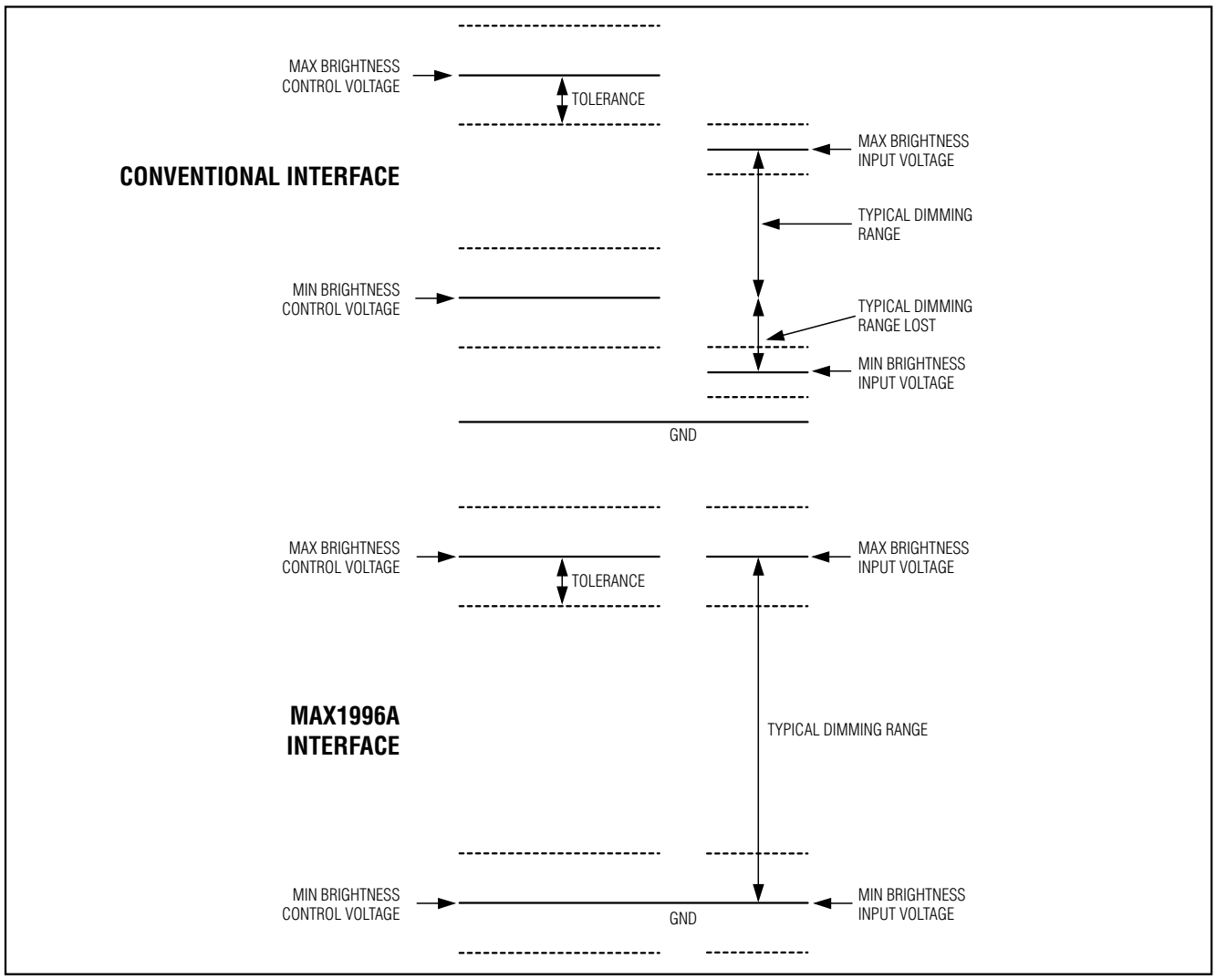


Figure 9. Useful Dimming Range

a 500pF capacitor from an AC signal source to MODE as shown in Figure 10. The amplitude of the AC signal must be at least $2V_{P-P}$ but no greater than $5V_{P-P}$ for accurate operation. The transition time of the AC signal should be less than 200µs. The synchronization range is 32kHz to 100kHz, which corresponds to a DPWM frequency range of 250Hz to 781Hz (128 MODE pulses per DPWM cycle). High DPWM frequencies limit the dimming range. See the *Loop Compensation* section for more information concerning high DPWM frequencies.

A simple oscillator circuit as shown in Figure 11 can be used to generate the synchronization signal. The core of the oscillator is the MAX9031, which is a low-cost, single-supply comparator in a 5-pin SC70 package. The V_{CC} and REF of the MAX1996A provide the supply voltage and the reference voltage for the oscillator. The positive threshold of the oscillator is: $V_{TH+} = (V_{CC} + V_{REF})/2$. The negative threshold is given by: $V_{TH-} = V_{REF}/2$. The frequency of the oscillator is:

$$f = \frac{1}{RC\ln\frac{V_{TH+}(V_{CC} - V_{TH-})}{V_{TH-}(V_{CC} - V_{TH+})}}$$

For C = 330pF and R = 13kΩ, the resulting oscillator frequency is 100kHz. For C = 330pF and R = 39kΩ, the oscillator frequency is 32kHz.

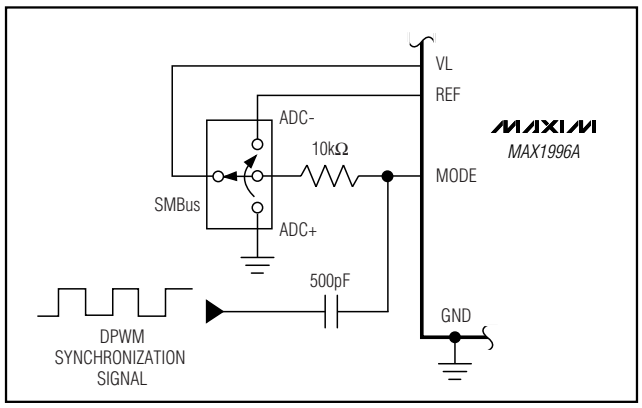


Figure 10. DPWM Synchronization

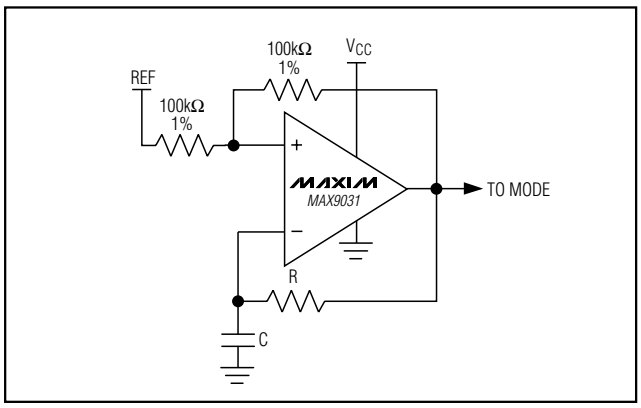


Figure 11. Simple RC Oscillator

POR and UVLO

The MAX1996A includes POR and UVLO circuits. The POR resets all internal registers such as DAC output, fault conditions, and all SMBus registers. POR occurs when V_{CC} is below 1.5V. The SMBus input-logic thresholds are only guaranteed to meet electrical characteristic limits for V_{CC} as low as 3.5V, but the interface continues to function down to the POR threshold.

The UVLO is activated and disables both high-side and low-side switch drivers when V_{CC} is below 4.2V (typ).

Low-Power Shutdown

When the MAX1996A is placed in shutdown, all functions of the IC are turned off except for the 5.3V linear regulator that powers all internal registers and the SMBus interface. The SMBus interface is accessible in shutdown. In shutdown, the linear regulator output voltage drops to about 4.5V and the supply current is 6µA (typ), which is the required power to maintain all internal register states. While in shutdown, lamp-out detection and short-circuit detection latches are reset. The device can be placed into shutdown by either writing to the shutdown mode register (SMBus mode only) or with $\overline{SH}$/SUS.

Lamp-Out Detection

For safety, the MAX1996A monitors the lamp current to detect the open-lamp fault. When the peak voltage on IFB drops below 150mV (IFB regulation point must be set above 48mV) the lamp-out timer starts. Before the timer times out, V_{CCI} increases the secondary voltage in an attempt to maintain lamp-current regulation. As V_{CCI} rises, V_{CCV} rises with it until the secondary voltage reaches its preset limit. At this point, V_{CCV} stops and limits the secondary voltage by limiting t_{ON}. Because V_{CCV} is limited to 150mV above V_{CCI}, the voltage control loop is able to quickly limit the secondary voltage. Without this clamping feature, the transformer voltage would overshoot to dangerous levels because V_{CCV} would take more time to slew down from its supply rail. If the peak voltage on IFB does not rise above 150mV before timeout, the MAX1996A shuts down the full bridge.

Overcurrent Fault Detection and Protection

The MAX1996A senses overcurrent faults on each switching cycle. The current comparator monitors the voltage drop from LX_ to GND. If the voltage exceeds the current-limit threshold, the regulator turns off the high-side switch to prevent the transformer primary current from increasing further.

Applications Information

The MAX1996A's standard application circuit, shown in Figure 1, regulates the current of a 4.5W CCFL. The IC's analog voltage interface sets the lamp brightness with a greater than 30 to 1 power adjustment range. This circuit operates from a wide supply voltage range of 4.6V to 28V. Typical applications for this circuit include notebook, desktop monitor, and car navigation displays. Table 4 shows the recommended components for the power stage of the 4.5W application. To select the correct component values, several C_{CFL} parameters (Table 6) and the DC input characteristics must be specified.

MOSFETs

The MAX1996A requires four external switches—NL1, NL2, NH1, and NH2—to form a full bridge to drive CCFL. The regulator senses drain-to-source voltage of NL1 and NL2 to detect the transformer primary minimum current crossing and overcurrent fault condition. R_{DSON} of NL1 and NL2 should be matched. Select a dual logic-level N-

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Table 4. Components for the Standard Application Circuit

DESIGNATION	DESCRIPTION	RECOMMENDED DEVICE	MANUFACTURER
C1	4.7µF, 25V X5R ceramic capacitor	TMK325BJ475MN	Taiyo Yuden www.t-yuden.com
		C3225X7R1E475M	TDK www.tdk.com
C2	1µF, 25V X7R ceramic capacitor	TMK316BJ105KL C3216X7R1E105K	Taiyo Yuden TDK
C3	15pF, 3.1kV high-voltage ceramic capacitor	GHM1038-SL-150J-3K	Murata www.murata.com
		C4520C0G3F150K	TDK
C4	0.015µF, 16V X7R ceramic capacitor	EMK105BJ153KV	Taiyo Yuden
		GRM36X7R153K016	Murata
C5–C8, C10	0.1µF,10V X5R ceramic capacitors	LMK105BJ104MV	Taiyo Yuden
		GRM36X5R104K010	Murata
		C10055R1A104K	TDK
C9	0.01µF, 16V X7R ceramic capacitor	ECJ-0EB1C103K	Panasonic www.panasonic.com
D1	100mA dual-series diode	MMBD4148SE	Fairchild Semiconductor www.fairchildsemi.com
		MMBD7000	General Semiconductor www.gensemi.com
		CMPD7000	Central Semiconductor www.centralsemi.com
D2	100mA dual Schottky diode common anode	BAT54AW	Diodes Incorporated www.diodes.com
		CMSSH-3A	Central Semiconductor
NH1/NL1, NH2/NL2	Dual N-channel MOSFETs (30V, 0.095Ω, SOT23-6)	FDC6561AN	Fairchild Semiconductor
		TPC6201	Toshiba www.toshiba.com
R1	150Ω ±1% resistor	—	—
R2	2kΩ ±5% resistor	—	—
R3	100kΩ ±1% resistor	—	—
R4	49.9kΩ ±1% resistor	—	—
T1	1:100 transformer	T912MG-1018	Toko www.tokoam.com

channel MOSFET with low R_{DSON} to minimize conduction loss for NL1/NL2 and NH1/NH2 (Fairchild FDC6561). The regulator softly turns on each of four switches in the full bridge. ZVS occurs when the external power MOSFETs are turned on while their respective drain-to-source voltages are near zero volts. ZVS effectively eliminates the MOSFET transition losses caused by C_{RSS} (drain-to-source capacitance) and parasitic capacitance discharge. ZVS improves efficiency and reduces switching-related EMI.

Current-Sense Resistor

The MAX1996A regulates the CCFL average current through sense resistor R1 in Figure 1. The voltage at

IFB is the half-wave rectified representation of the current through the lamp. The inverter regulates the average voltage at IFB, which is controlled by either the analog interface or the SMBus interface. To set the maximum lamp RMS current, determine R1 as follows: $R1 = 0.444V/I_{CCFL,\ RMS,\ MAX}$, where $I_{CCFL,\ RMS,\ MAX}$ is the maximum RMS lamp current. MINDAC and the wave shape influence the actual maximum RMS lamp current. If necessary, use an RMS current meter to make final adjustments to R1.

Voltage-Sense Capacitors

The MAX1996A limits the transformer secondary voltage during open-lamp fault through the capacitive divider C3/C4. The voltage of V_{FB} is proportional to CCFL voltage. To set the maximum RMS secondary transformer voltage, choose C3 around 10pF to 22pF, and select C4 such that $C4 = V_{T(MAX)}/1.11V \times C3$, where $V_{T(MAX)}$ comprises the maximum RMS secondary transformer voltage (above the strike voltage). R2 sets the V_{FB} DC bias point to zero volts. Choose $R2 = 10/(C4 \times 6.28 \times F_{SW})$, where F_{SW} is the nominal resonant operating frequency.

Loop Compensation

CCI sets the speed of the current loop that is used during startup, maintaining lamp-current regulation, and during transients, caused by changing the lamp-current settling. The typical CCI capacitor value is 0.1µF. Larger values limit lamp-current overshoot, but increase setting time. Smaller values speed up its response time, but extremely small values can lead to instability.

CCV sets the speed of the voltage loop that affects startup, DPWM transients, and operation in an open-tube fault condition. If DPWM is not used, the voltage control loop should only be active during startup or an open-lamp fault. The CCV capacitors typical value is 0.01µF. Use the smallest value of CCV capacitor necessary to set an acceptable fault-transient response and not cause excessive ringing at the beginning of a DPWM pulse. Larger CCV capacitor values reduce transient overshoot, but can degrade regulation at low DPWM duty cycles by increasing the delay to strike voltage.

Resonant Components

The MAX1996A works well with air-gap transformers with turns ratio N in the order of $N_P:N_S$ = 1:90 to 1:100 for most applications. The transformer secondary resonant frequency must be controlled. A low-profile CCFL transformer typically operates between 50kHz (F_{min}) and 200kHz (F_{max}). Transformer T1, DC blocking capacitor C2, parallel capacitor C3, and the CCFL lamp form a resonant tank. The resonant frequency is determined by the transformer secondary leakage inductance L, C2, and C3. The tank is a bandpass filter whose lower frequency is bounded by L, N, and C2. N is the transformer's turns ratio. Choose $C2 \le N^2 (10 \times F^2_{MIN} \times L)$. The upper frequency is bounded by L and C3. Choose $C3 \ge 1/(40 \times F^2_{MIN} \times L)$.

Other Components

The high-side MOSFET drivers (GH1 and GH2) are powered by the external bootstrap circuit formed by D2, C5, and C6. Connect BST1/BST2 through a dual signal-level Schottky diode D2 to V_{DD}, and connect it to LX1/LX2 with 0.1µF ceramic capacitors. Use a dual-series signal-level diode (D1) to generate the half-wave rectified current-sense voltage across R1. The current through these diodes is the lamp current.

Dual-Lamp Regulator

The MAX1996A can be used to drive two CCFL tubes as shown in Figure 12. See Table 5 for component selection. The circuit consists of two identical transformers with primary windings connected in parallel and secondary windings in series. The two transformers can also be replaced with a single transformer, which has one primary winding and two secondary windings. The advantage of the series secondary windings is that the same current flows through both lamps, resulting in approximately the same brightness.

In normal operation, C12 is charged to approximately 6V biasing N1 on, which permits current to flow in the loop as follows: in the first half cycle, current flows through the secondary winding of T1, CCFL1, diode D1, MOSFET N1, sense resistor R1, zener diode D4 (forward bias), CCFL2, and finally returning to T2. In the second half cycle, the lamp current flows through T2, CCFL2, D4 (breakdown), D3 (forward bias), CCFL1, and back to T1.

The roundabout path of current flow is necessary in order to detect an open-lamp condition when either CCFL is removed. If CCFL1 is open, the lamp current cannot flow through sense resistor R1. When IFB drops below 150mV, the controller detects the condition and shuts down after a 1s delay. During the delay, current can flow from T2 through CCFL2, D4 (breakdown), and R6 back to T2. If CCFL2 is removed, the voltage across D4 drops to zero and C11 is discharged through R5. N1 is biased off, which forces the voltage at IFB to drop to zero once again. During the 1s turn-off delay, current flows from T1 to CCFL1 through D3 (breakdown) and R6 back to T1. D3 clamps the drain of N1 enabling the use of a MOSFET with modest breakdown characteristics.

High-Efficiency, Wide Brightness Range, CCFL Backlight Controller

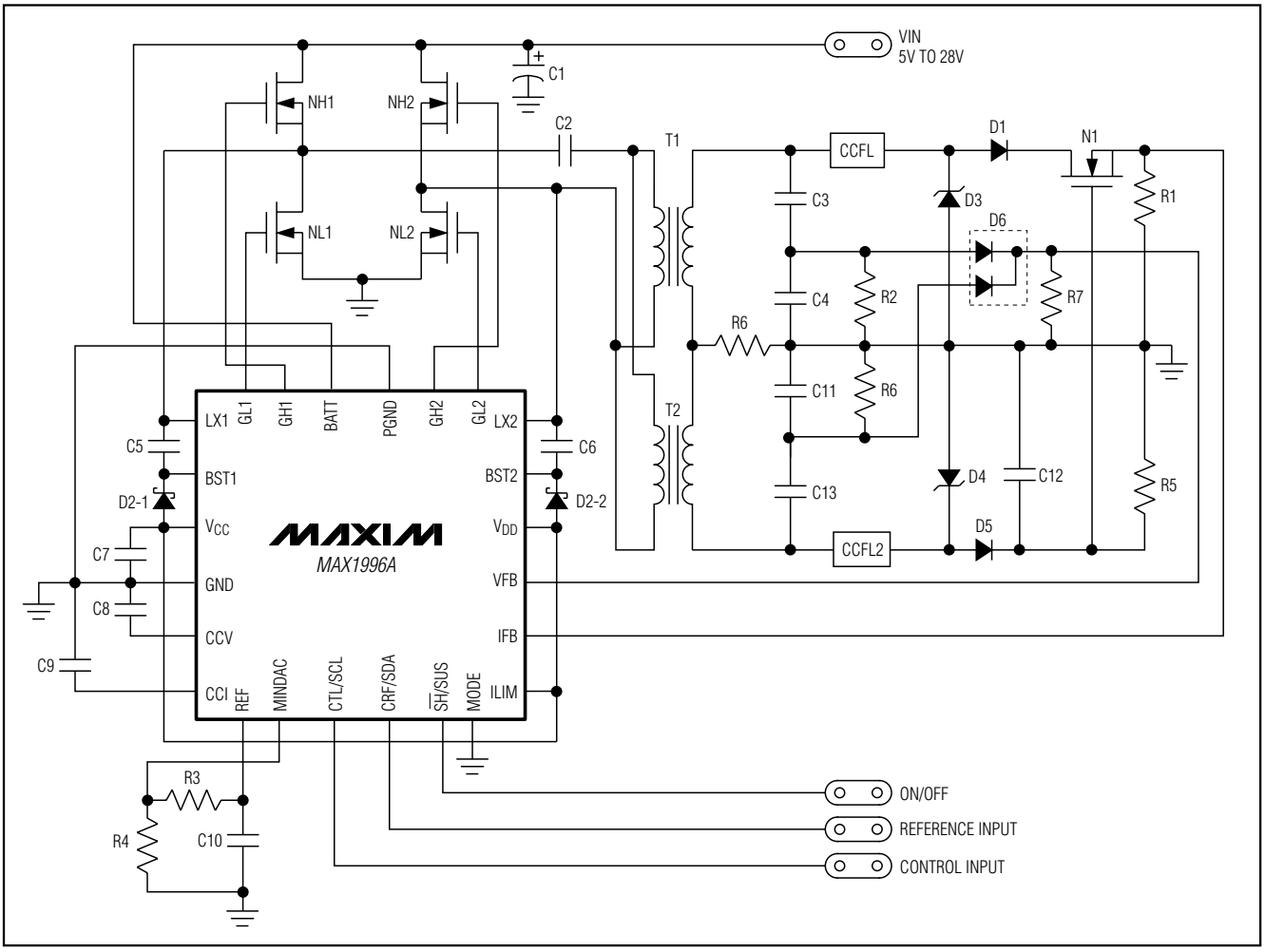


Figure 12. Dual-Lamp Application Circuit

The secondary voltages of both transformers are monitored through the two identical capacitive voltage-dividers (C3/C4 and C13/C11). Dual-diode D6 rectifies the two sensed voltages and passes the signal to the VFB pin. A full-wave rectified sinusoidal waveform appears at the VFB pin. The RMS value of this new VFB signal is greater than the half-wave rectified signal in the single-lamp application. To compensate for the waveform change and the forward-voltage drop in the diodes, the capacitive voltage-divider ratio must be decreased. Choose C3 around 10pF to 22pF, and select C4 according to $C4 = V_{T,\,MAX}/1.33V \times C3$, where $V_{T,\,MAX}$ is the maximum transformer secondary RMS voltage.

Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The high-voltage and switching-power stages require particular attention (Figure 13). The high-voltage sections of the layout need to be well separated from the control circuit. Most layouts are constrained to long narrow PC boards, so this separation occurs naturally.

Follow these guidelines for good PC board layout:

1) Keep the high-current paths short and wide, especially at the ground terminals. This is essential for stable, jitter-free operation, and high efficiency.

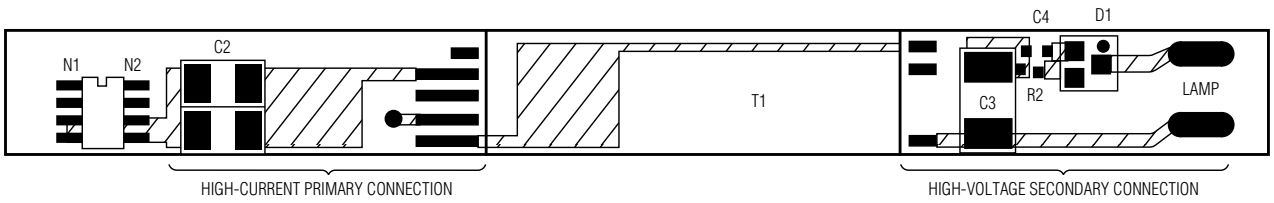
Table 5. Components for the Dual-Lamp Application Circuit

DESIGNATION	DESCRIPTION	RECOMMENDED DEVICE	MANUFACTURER
C1	4.7µF, 25V X5R ceramic capacitor	TMK325BJ475MN	Taiyo Yuden www.t-yuden.com
		C3225X7R1E475M	TDK www.tdk.com
C2	1µF, 25V X7R ceramic capacitor	TMK316BJ105KL	Taiyo Yuden
		C3216X7R1E105K	TDK
C3, C13	15pF, 3.1kV high-voltage ceramic capacitors	GHM1038-SL-150J-3K	Murata www.murata.com
		C4520C0G3F150K	TDK
C4, C11	0.015µF, 16V X7R ceramic capacitors	EMK105BJ153KV	Taiyo Yuden
		GRM36X7R153K016	Murata
C5–C8, C10, C12	0.1µF, 10V X5R ceramic capacitors	LMK105BJ104MV	Taiyo Yuden
		GRM36X5R104K010	Murata
		C1005X5R1A104K	TDK
C9	0.01µF, 16V X7R ceramic capacitor	ECJ-0EB1C103K	Panasonic www.panasonic.com
D1, D5	100mA diodes	MMBD4148	Fairchild Semiconductor www.fairchildsemi.com
		IMBD4148	General Semiconductor www.gensemi.com
		MMBD4148	Diodes Incorporated www.diodes.com
D2	100mA dual Schottky diode, common anode	BAT54AW	Diodes Incorporated
		CMSSH-3A	Central Semiconductor www.centralsemi.com
D3, D4	6.2V zener diodes	CMPZ5234B	Central Semiconductor
		BZX84C6V2	Diodes Incorporated
D6	Dual diode, common cathode	CMPD2838	Central Semiconductor
		BAV70	Diodes Incorporated
N1	N-channel MOSFET (SOT23)	2N7002	Fairchild Semiconductor
		2N7002	General Semiconductor
		2N7002	Central Semiconductor
NH1/NL1, NH2/NL2	Dual N-channel MOSFETs (30V, 0.095Ω, SOT23-6)	FDC6561AN	Fairchild Semiconductor
		TPC6201	Toshiba www.toshiba.com
R1	150Ω ±1% resistor	—	—
R2, R6	2kΩ ±5% resistors	—	—
R3	100kΩ ±1% resistor	—	—
R4	49.9kΩ ±1% resistor	—	—

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Table 5. Components for the Dual-Lamp Application Circuit

DESIGNATION	DESCRIPTION	RECOMMENDED DEVICE	MANUFACTURER
R5	1kΩ ±5% resistor	—	—
R7	20kΩ ±5% resistor	—	—
T1, T2	1:100 transformers	T912MG-1018	Toko www.tokoam.com



NOTE: DUAL MOSFET N2 IS MOUNTED ON THE BOTTOM SIDE OF THE PC BOARD DIRECTLY UNDER N1.

Figure 13. Layout Example

Table 6. CCFL Specifications

SPECIFICATION	SYMBOL	UNITS	DESCRIPTION
CCFL Minimum Strike Voltage (Kick-Off Voltage)	V_S	V_{RMS}	Although CCFLs typically operate at <550V_{RMS}, a higher voltage (up to 1000V_{RMS} and beyond) is required initially to start the tube. The strike voltage is typically higher at cold temperatures and at the end of the life of the tube.
CCFL Typical Operating Voltage (Lamp Voltage)	V_L	V_{RMS}	Once a CCFL has been struck, the voltage is required to maintain light output falls to approximately 550V_{RMS}. Shorter tubes may operate on as little as 250V_{RMS}. The operating voltage of the CCFL stays relatively constant, even as the tube's brightness is varied.
CCFL Maximum Operating Current (Lamp Current)	I_L	mA_{RMS}	The maximum AC current through a CCFL is typically 5mA_{RMS}. DC current is not allowed through CCFLs. The maximum lamp current is set by sense resistor R1 and the maximum brightness setting. $R1 = 2.2 \times V_{IFBMAX}/I_{LMAX}$.
CCFL Maximum Frequency (Lamp Frequency)	f_L	kHz	The maximum AC lamp-current frequency. The MAX1996A is designed to operate between 20kHz and 300kHz.

2) Utilize a star ground configuration for power and analog grounds. The power ground and analog ground should be completely isolated—meeting only at the center of the star. The center should be placed at the backside contact to the QFN package. Using separate copper planes for these planes may simplify this task. Quiet analog ground is used for REF, CCV, CCI, RX, and MINDAC (if a resistive voltage-divider is used).
3) Route high-speed switching nodes away from sensitive analog areas (IFB, VFB, REF, ILIM). Make all pin-strap control input connections (ILIM, etc.) to analog ground or V_{CC}, rather than power ground or V_{DD}.
4) Mount the decoupling capacitor from V_{CC} to GND as close as possible to the IC with dedicated traces that are not shared with other signal paths.
5) The current-sense paths for LX1 and LX2 to GND must be made using Kelvin-sense connections to guarantee the current-limit accuracy. With 8-pin SO MOSFETs, this is best done by routing power to the MOSFETs from outside using the top copper layer, while connecting GND and LX inside (underneath) the 8-pin SO package.
6) Ensure the feedback connections are short and direct. To the extent possible, IFB and V_{FB} connec-

Write-Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	DATA	ACK	P
	7 bits	1b	1b	8 bits	1b	8 bits	1b	

Slave Address

Command Byte: selects which register you are writing to

Data Byte: data goes into the register set by the command byte

Read-Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	S	ADDRESS	RD	ACK	DATA	///	P
	7 bits	1b	1b	8 bits	1b		7 bits	1b	1b	8 bits	1b	

Slave Address

Command Byte: selects which register you are reading from

Slave Address: repeated due to change in data-flow direction

Data Byte: reads from the register set by the command byte

Send-Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	P
	7 bits	1b	1b	8 bits	1b	

Command Byte: sends command with no data; usually used for one-shot command

Receive-Byte Format

S	ADDRESS	RD	ACK	DATA	///	P
	7 bits	1b	1b	8 bits	1b	

Slave Address

Data Byte: reads data from the register commanded by the last read-byte or write-byte transmission; also used for SMBus Alert Response return address

S = Start condition
P = Stop condition
Shaded = Slave transmission
Ack= Acknowledged = 0
/// = Not acknowledged = 1
WR = Write = 0
RD = Read =1

Figure 14. SMBus Protocols

tions should be far away from the high-voltage traces and the transformer.

7) To the extent possible, high-voltage trace clearance on the transformer's secondary should be widely separated. The high-voltage traces should also be separated from adjacent ground planes to prevent capacitive coupling losses.

8) The traces to the capacitive voltage-divider on the transformer's secondary need to be widely separated to prevent arcing. Moving these traces to opposite sides of the board can be beneficial in some cases (Figure 13).

Digital Interface

With MODE connected to V_{CC}, the CRF/SDA and CTL/SCL pins no longer behave as analog inputs; instead, they function as an Intel SMBus-compatible 2-wire digital interface. CRF/SDA is the bidirectional data line and CTL/SCL is the clock line of the 2-wire interface corresponding respectively to the SMBDATA and SMBCLK lines of the SMBus. The MAX1996A uses the Write-Byte, Read-Byte, Send-Byte, and Receive-Byte protocols (Figure 14). The SMBus protocols are documented in System Management Bus Specification v1.08 and are available at www.sbs-forum.org.

The MAX1996A is a slave-only device and responds to the 7-bit address 0b0101100 (i.e., with the R/$\overline{W}$ bit clear indicating a write, this corresponds to 0x58). The MAX1996A has three functional registers: a 5-bit brightness register (BRIGHT4–BRIGHT0), a 3-bit shutdown mode register (SHMD2–SHMDE0), and a 2-bit status register (STATUS1–STATUS0). In addition, the device has three identification (ID) registers: an 8-bit chip ID register, an 8-bit chip revision register, and an 8-bit manufacturer ID register.

CRF/SDA and CTL/SCL pins have Schmitt-trigger inputs that can accommodate slow edges; however, the rising and falling edges should still be faster than 1µs and 300ns, respectively.

Communication starts with the master signaling the beginning of a transmission with a START condition, which is a high-to-low transition on CRF/SDA, while CTL/SCL is high. When the master has finished com-

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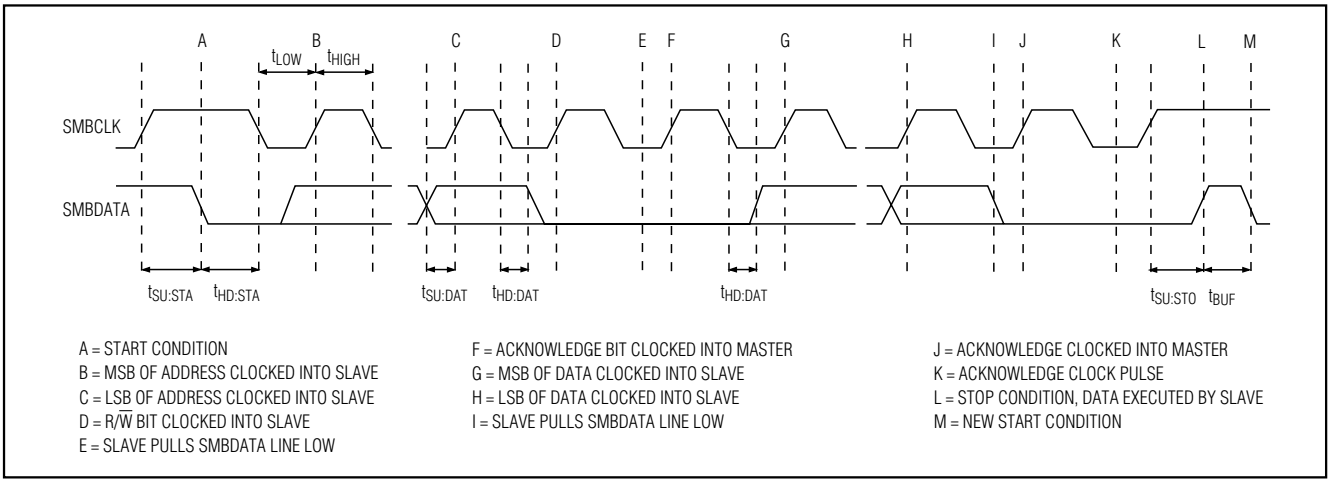


Figure 15. SMBus Write Timing

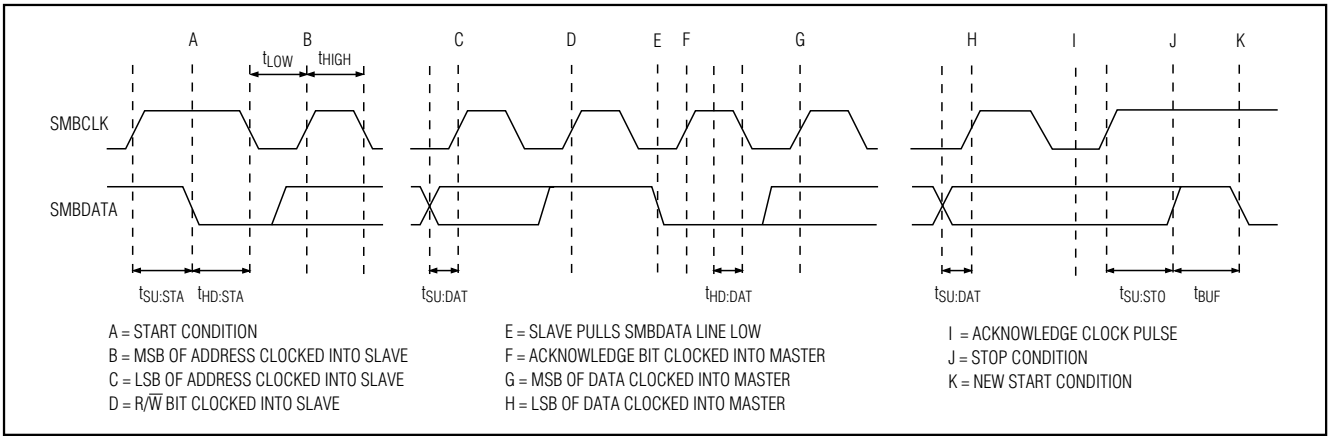


Figure 16. SMBus Read Timing

municating with the slave, the master issues a STOP condition (P), which is low-to-high transition on CRF/SDA, while CTL/SCL is high. The bus is then free for another transmission. Figures 15 and 16 show the timing diagram for signals on the 2-wire interface. The address-byte, command-byte, and data-byte are transmitted between the START and STOP conditions. The CRF/SDA state is allowed to change only while CTL/SCL is low, except for the START and STOP conditions. Data is transmitted in 8-bit words and is sampled on the rising edge of CTL/SCL. Nine clock cycles are required to transfer each byte in or out of the MAX1996A since either the master or the slave acknowledges the receipt of the correct byte during the ninth clock. If the MAX1996A receives its correct slave address followed by R/$\overline{W}$ = 0, it expects to receive 1 or 2 bytes of information (depending on the protocol). If the device detects a START or STOP condition prior to clocking in the bytes of data, it considers this an error condition and disregards all the data. If the transmission is completed correctly, the registers are updated immediately after a STOP (or RESTART) condition. If the MAX1996A receives its correct slave address followed by R/$\overline{W}$ = 1, it expects to clock out the register data selected by the previous command byte.

SMBus Commands

The MAX1996A registers are accessible through several different redundant commands (i.e., the command-byte in the read-byte and write-byte protocols), which can be used to read or write the brightness, SHMD_, status, or ID registers.

Table 6 summarizes the command-byte's register assignments, as well as each register's power-on state.

Table 7. Command Byte Description

SMBus PROTOCOL	COMMAND BYTE*	POR STATE	DATA REGISTER BIT ASSIGNMENT							
			BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
Read and Write	0x01 0b0XXX XX01	0x17	0	0	0	BRIGHT4 (MSB)	BRIGHT3	BRIGHT2	BRIGHT1	BRIGHT0 (LSB)
Read and Write	0x02 0b0XXX XX10	0xF9	STATUS1	STATUS0	1	1	1	SHMD2	SHMD1	SHMD0
Read Only	0x03 0b0XXX XX11	0x0C	ChipID7 0	ChipID6 0	ChipID5 0	ChipID4 0	ChipID3 1	ChipID2 1	ChipID1 0	ChipID0 0
Read Only	0x04 0b0XXX XX00	0x00	ChipRev7 0	ChipRev6 0	ChipRev5 0	ChipRev4 0	ChipRev3 0	ChipRev2 0	ChipRev1 0	ChipRev0 0
Read and Write	0xAA 0b10XX XXX0	0x40	$\overline{\text{BRIGHT4}}$ (MSB)	$\overline{\text{BRIGHT3}}$	$\overline{\text{BRIGHT2}}$	$\overline{\text{BRIGHT1}}$	$\overline{\text{BRIGHT0}}$ (LSB)	0	$\overline{\text{STATUS1}}$	$\overline{\text{STATUS0}}$
Read and Write	0xA9 0b10XX XXX1	0x40	$\overline{\text{BRIGHT4}}$ (MSB)	$\overline{\text{BRIGHT3}}$	$\overline{\text{BRIGHT2}}$	$\overline{\text{BRIGHT1}}$	$\overline{\text{BRIGHT0}}$ (LSB)	0	$\overline{\text{STATUS1}}$	$\overline{\text{STATUS0}}$
Read Only	0xFE 0b11XX XXX0	0x4D	MfgID7 0	MfgID6 1	MfgID5 0	MfgID4 0	MfgID3 1	MfgID2 1	MfgID1 0	MfgID0 1
Read Only	0xFF 0b11XX XXX1	0x0C	ChipID7 0	ChipID6 0	ChipID5 0	ChipID4 0	ChipID3 1	ChipID2 1	ChipID1 0	ChipID0 0

**The hexadecimal command byte shown is recommended for maximum forward compatibility with future products.*
X = Don't care.

The MAX1996A also supports the receive-byte protocol for quicker data transfers. This protocol accesses the register configuration pointed to by the last command byte. Immediately after power-up, the data-byte returned by the receive-byte protocol is the contents of the brightness register, left justified (i.e., BRIGHT4 is in the most significant bit position of the data byte) with the remaining bits containing a one, STATUS1, and STATUS0. Use caution with the shorter protocols in multimaster systems, since a second master could overwrite the command byte without informing the first master. During shutdown the serial interface remains fully functional.

Brightness Register [BRIGHT4–BRIGHT0] (POR = 0b10111)

The 5-bit brightness register corresponds with the 5-bit brightness code used in the dimming control (see the *Dimming Control* section). BRIGHT4–BRIGHT0 = 0b00000 sets minimum brightness and BRIGHT4–BRIGHT0 = 0b11111 sets maximum brightness. Note that the brightness register bit assignment of command bytes 0xA9 and 0xAA is inverted from the bit assignment of command byte 0x01. The SMBus interface does not control whether the device regulates the current by analog dimming, DPWM dimming or both; this is done by MINDAC (see *Pin Description*).

Shutdown Mode Register [SHMD2–SHMD0] (POR = 0b001)

The 3-bit shutdown mode register configures the operation of the device when $\overline{\text{SH}}$/SUS pin is toggled as described in Table 8. The shutdown mode register can also be used to directly shut off the CCFL regardless of the state of $\overline{\text{SH}}$/SUS (Table 9).

Status Register [STATUS1–STATUS0] (POR = 0b11)

The status register returns information on fault conditions. If a lamp is not connected to the secondary of the transformer, the MAX1996A detects that the lamp current has not exceeded the IFB detection threshold and after 1s clears the STATUS1 bit (see the *Lamp-Out Detection* section). The STATUS1 bit is latched; i.e., it remains 0 even if the lamp-out condition goes away. When STATUS1 = 0, the lamp is forced off. STATUS0 reports 1 as long as no overcurrent conditions are detected. If an overcurrent condition is detected in any given digital PWM period, STATUS0 is cleared for the

Table 8. SHMD Register Bit Descriptions

BIT	NAME	POR STATE	DESCRIPTION
2	SHMD2	0	SHMD2 = 1 forces the lamp off and sets STATUS1. SHMD2 = 0 allows the lamp to operate although it may still be shut down by the /SH\/SUS pin (depending on the state of SHMD1 and SHMD0).
1	SHMD1	0	When $\overline{SH}$/SUS = 0, this bit has no effect. $\overline{SH}$/SUS = 1 and SHMD1 = 1 forces the lamp off and sets STATUS1. $\overline{SH}$/SUS = 1 and SHMD1 = 0 allows the lamp to operate although it may still be shut down by the SHMD2 bit.
0	SHMD0	1	When $\overline{SH}$/SUS = 1, this bit has no effect. $\overline{SH}$/SUS = 0 and SHMD0 = 1 forces the lamp off and sets STATUS1. $\overline{SH}$/SUS = 0 and SHMD0 = 0 allows the lamp to operate although it may still be shut down by the SHMD2 bit.

Table 9. $\overline{SH}$/SUS and SHMD Register Truth Table

$\overline{SH}$/SUS	SHMD2	SHMD1	SHMD0	OPERATING MODE
0	0	X	0	Operate
0	0	X	1	Shutdown, STATUS1 set
1	0	0	X	Operate
1	0	1	X	Shutdown, STATUS1 set
X	1	X	X	Shutdown, STATUS1 set

X = Don't care.

Table 10. Status Register Bit Descriptions (Read Only/Writes Have No Effect)

BIT	NAME	POR STATE	DESCRIPTION
1	STATUS1	1	STATUS1 = zero means that a lamp-out condition has been detected. The STATUS1 bit stays clear even after the lamp-out condition has gone away. The only way to set STATUS1 is to shut off the lamp by programming the mode register or by toggling SHB/SUS.
0	STATUS0	1	STATUS0 = zero means that an overcurrent condition was detected during the previous digital PWM period. STATUS0 = 1 means that no overcurrent condition was detected during the previous digital PWM period.

duration of the following digital PWM period. If an overcurrent condition is not detected in any given digital PWM period, STATUS0 is set for the duration of the following digital PWM period. Forcing the CCFL lamp off by entering shutdown, writing to the mode register, or by toggling SHB/SUS sets STATUS1. Note that the status register bit assignment of command byte 0xA9 is inverted from the bit assignment of command byte 0x80.

ID Registers

The ID registers return information on the manufacturer, the chip ID, and the chip revision number. The MAX1996A is the first-generation advanced CCFL controller and its ChipRev is 0x00. Reading from MfgID register returns 0x4D, which is the ASCII code for M (for Maxim), the ChipID register returns 0x0C. Writing to these registers has no effect.

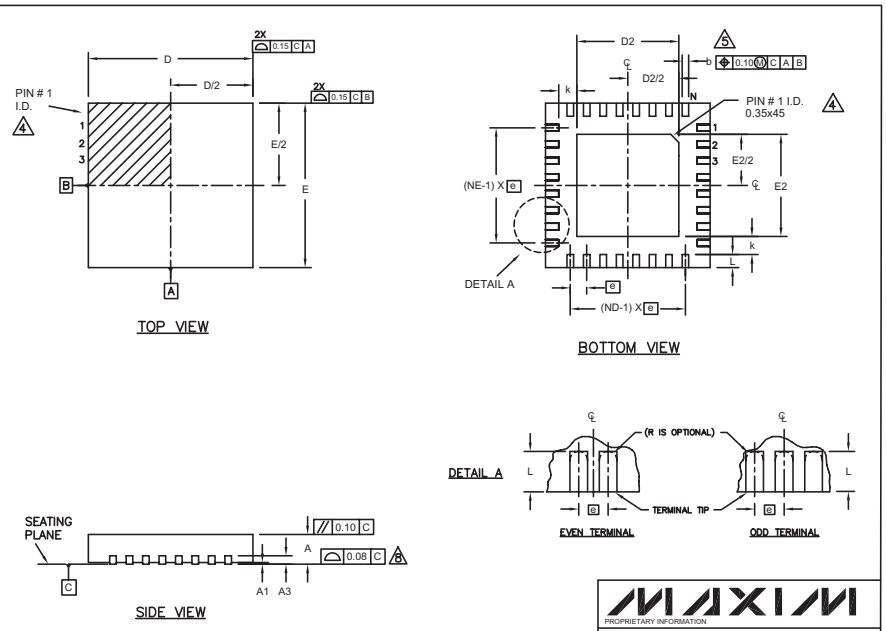
Chip Information

TRANSISTOR COUNT: 7364

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QFN THIN 5x5x0.8 .EPS



PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm

APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. C | 1/2

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm

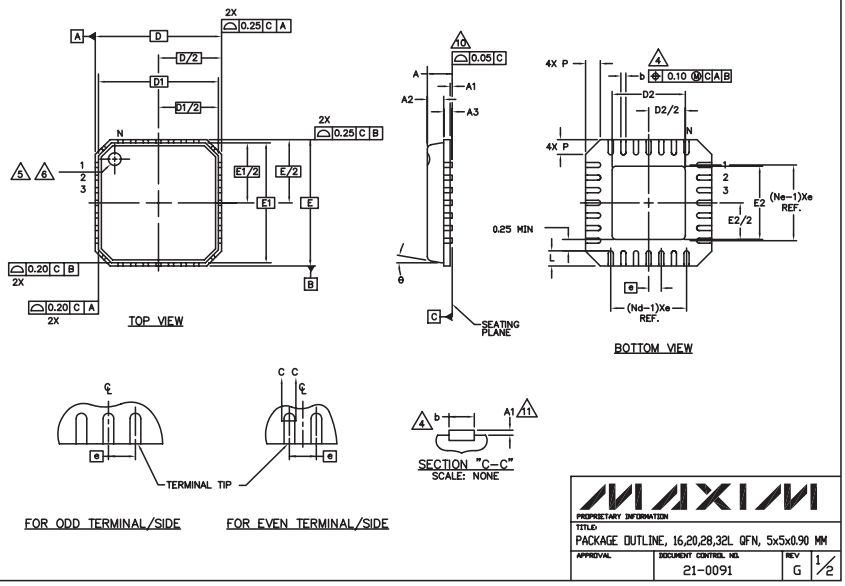
APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. C | 2/2

High-Efficiency, Wide Brightness Range, CCFL Backlight Controller

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

32L QFN .EPS



PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM
APPROVAL | DOCUMENT CONTROL NO. 21-0091 | REV G | 1/2

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/ LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES) AND TO SAW SINGULATION (STRAIGHT SIDES) QFN STYLES.

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	1.00	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
E		5.00 BSC		
E1		4.75 BSC		
θ	0°	–	12°	
P	0		0.60	
D2	1.25	–	3.25	
E2	1.25	–	3.25	

SYMBOL	PITCH VARIATION B MIN.	NOM.	MAX.	NOTE
e		0.80 BSC		
N		16		3
Nd		4		3
Ne		4		3
L	0.35	0.55	0.75	
b	0.28	0.33	0.40	4

SYMBOL	PITCH VARIATION B MIN.	NOM.	MAX.	NOTE
e		0.65 BSC		
N		20		3
Nd		5		3
Ne		5		3
L	0.35	0.55	0.75	
b	0.23	0.28	0.35	4

SYMBOL	PITCH VARIATION C MIN.	NOM.	MAX.	NOTE
e		0.50 BSC		
N		28		3
Nd		7		3
Ne		7		3
L	0.35	0.55	0.75	
b	0.18	0.23	0.30	4

SYMBOL	PITCH VARIATION D MIN.	NOM.	MAX.	NOTE
e		0.50 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4

PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM
APPROVAL | DOCUMENT CONTROL NO. 21-0091 | REV G | 2/2

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