Rev 2; 10/06

# DS2065W 3.3V Single-Piece 8Mb Nonvolatile SRAM



## General Description

The DS2065W is a 8Mb reflowable nonvolatile (NV) SRAM, which consists of a static RAM (SRAM), an NV controller, and an internal rechargeable manganese lithium (ML) battery. These components are encased in a surface-mount module with a 256-ball BGA footprint. Whenever $V_{CC}$ is applied to the module, it recharges the ML battery, powers the SRAM from the external power source, and allows the contents of the SRAM to be modified. When $V_{CC}$ is powered down or out-of-tolerance, the controller write-protects the SRAM's contents and powers the SRAM from the battery. The DS2065W also contains a power-supply monitor output, $\overline{RST}$, which can be used as a CPU supervisor for a microprocessor.

## Applications

| | |
|---|---|
| RAID Systems and Servers | POS Terminals |
| Industrial Controllers | Routers/Switches |
| Data-Acquisition Systems | Fire Alarms |
| Gaming | PLC |

## Features

- **Single-Piece, Reflowable, 27mm² PBGA Package Footprint**
- **Internal ML Battery and Charger**
- **Unconditionally Write-Protects SRAM when $V_{CC}$ is Out-of-Tolerance**
- **Automatically Switches to Battery Supply when $V_{CC}$ Power Failures Occur**
- **Internal Power-Supply Monitor Detects Power Fail Below Nominal $V_{CC}$ (3.3V)**
- **Reset Output can be Used as a CPU Supervisor for a Microprocessor**
- **Industrial Temperature Range (-40°C to +85°C)**
- **UL Recognized**

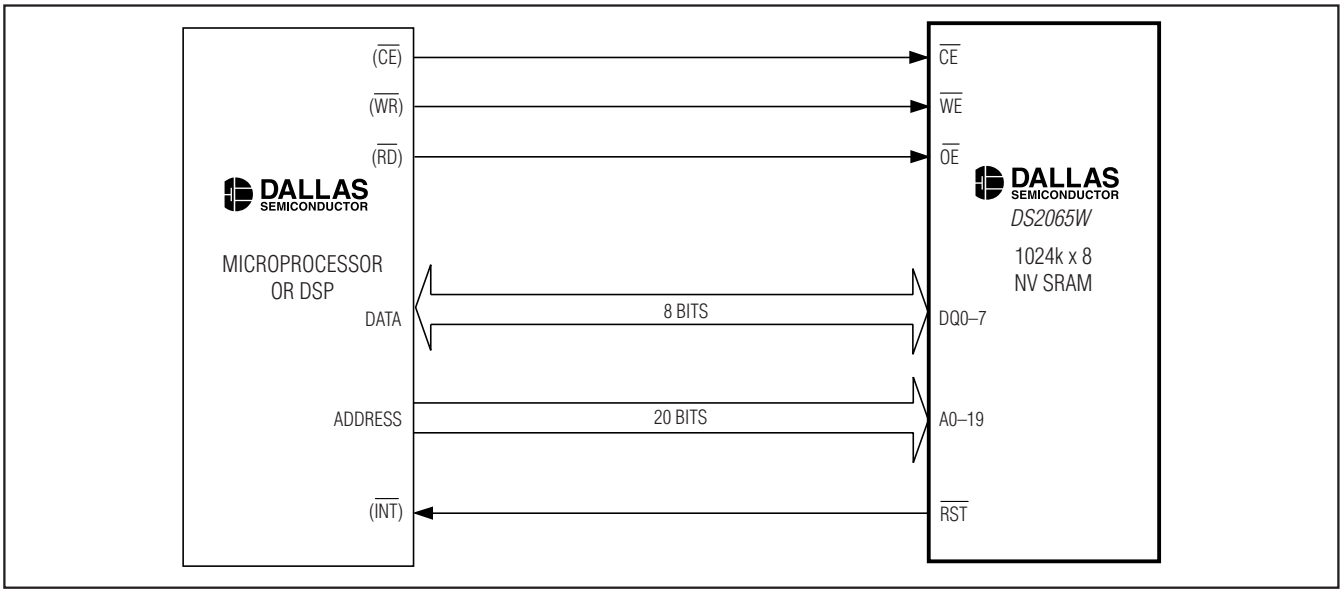
***Pin Configuration appears at end of data sheet.***

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | SPEED (ns) | SUPPLY TOLERANCE |
|---|---|---|---|---|
| DS2065W-100# | -40°C to +85°C | 256 Ball 27mm² BGA Module | 100 | 3.3V ±0.3V |

*#Denotes a RoHS-compliant device that may include lead that is exempt under the RoHS requirements.*

## Typical Operating Circuit






***For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.***

# DS2065W 3.3V Single-Piece 8Mb Nonvolatile SRAM

## ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to Ground .....-0.3V to +4.6V
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-40°C to +85°C
Soldering Temperature .....See IPC/JEDEC J-STD-020

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## RECOMMENDED OPERATING CONDITIONS

($T_A$ = -40°C to +85°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | 3.0 | 3.3 | 3.6 | V |
| Input Logic 1 | $V_{IH}$ | | 2.2 | | $V_{CC}$ | V |
| Input Logic 0 | $V_{IL}$ | | 0 | | 0.4 | V |

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 3.3V ±0.3V, $T_A$ = -40°C to +85°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | | -1.0 | | +1.0 | µA |
| I/O Leakage Current | $I_{IO}$ | $\overline{CE}$ = $V_{CC}$ | -1.0 | | +1.0 | µA |
| Output-Current High | $I_{OH}$ | At 2.4V | -1.0 | | | mA |
| Output-Current Low | $I_{OL}$ | At 0.4V | 2.0 | | | mA |
| Output-Current Low $\overline{RST}$ | $I_{OL}$ $\overline{RST}$ | At 0.4V (Note 1) | 10.0 | | | mA |
| Standby Current | $I_{CCS1}$ | $\overline{CE}$ = 2.2V | | 0.5 | 7 | mA |
| | $I_{CCS2}$ | $\overline{CE}$ = $V_{CC}$ - 0.2V | | 0.2 | 5 | |
| Operating Current | $I_{CCO1}$ | $t_{RC}$ = 200ns, outputs open | | | 50 | mA |
| Write-Protection Voltage | $V_{TP}$ | | 2.8 | 2.9 | 3.0 | V |

## CAPACITANCE

($T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | Not tested | | 7 | | pF |
| Input/Output Capacitance | $C_{OUT}$ | Not tested | | 7 | | pF |

## AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 3.3V ±0.3V, $T_A$ = -40°C to +85°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | | 100 | | ns |
| Access Time | $t_{ACC}$ | | | 100 | ns |
| $\overline{OE}$ to Output Valid | $t_{OE}$ | | | 50 | ns |
| $\overline{CE}$ to Output Valid | $t_{CO}$ | | | 100 | ns |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | (Note 2) | 5 | | ns |
| Output High Impedance from Deselection | $t_{OD}$ | (Note 2) | | 35 | ns |
| Output Hold from Address Change | $t_{OH}$ | | 5 | | ns |
| Write Cycle Time | $t_{WC}$ | | 100 | | ns |
| Write Pulse Width | $t_{WP}$ | (Note 3) | 75 | | ns |
| Address Setup Time | $t_{AW}$ | | 0 | | ns |
| Write Recovery Time | $t_{WR1}$ | (Note 4) | 5 | | ns |
| | $t_{WR2}$ | (Note 5) | 20 | | |
| Output High Impedance from $\overline{WE}$ | $t_{ODW}$ | (Note 2) | | 35 | ns |
| Output Active from $\overline{WE}$ | $t_{OEW}$ | (Note 2) | 5 | | ns |
| Data Setup Time | $t_{DS}$ | (Note 6) | 40 | | ns |
| Data Hold Time | $t_{DH1}$ | (Note 4) | 0 | | ns |
| | $t_{DH2}$ | (Note 5) | 20 | | |

## POWER-DOWN/POWER-UP TIMING

($T_A$ = -40°C to +85°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{CC}$ Fail Detect to $\overline{CE}$ and $\overline{WE}$ Inactive | $t_{PD}$ | (Note 7) | | | 1.5 | µs |
| $V_{CC}$ Slew from $V_{TP}$ to 0V | $t_F$ | | 150 | | | µs |
| $V_{CC}$ Slew from 0V to $V_{TP}$ | $t_R$ | | 150 | | | µs |
| $V_{CC}$ Valid to $\overline{CE}$ and $\overline{WE}$ Inactive | $t_{PU}$ | | | | 2 | ms |
| $V_{CC}$ Valid to End of Write Protection | $t_{REC}$ | | | | 125 | ms |
| $V_{CC}$ Fail Detect to $\overline{RST}$ Active | $t_{RPD}$ | (Note 1) | | | 3.0 | µs |
| $V_{CC}$ Valid to $\overline{RST}$ Inactive | $t_{RPU}$ | (Note 1) | 225 | 350 | 525 | ms |

## DATA RETENTION

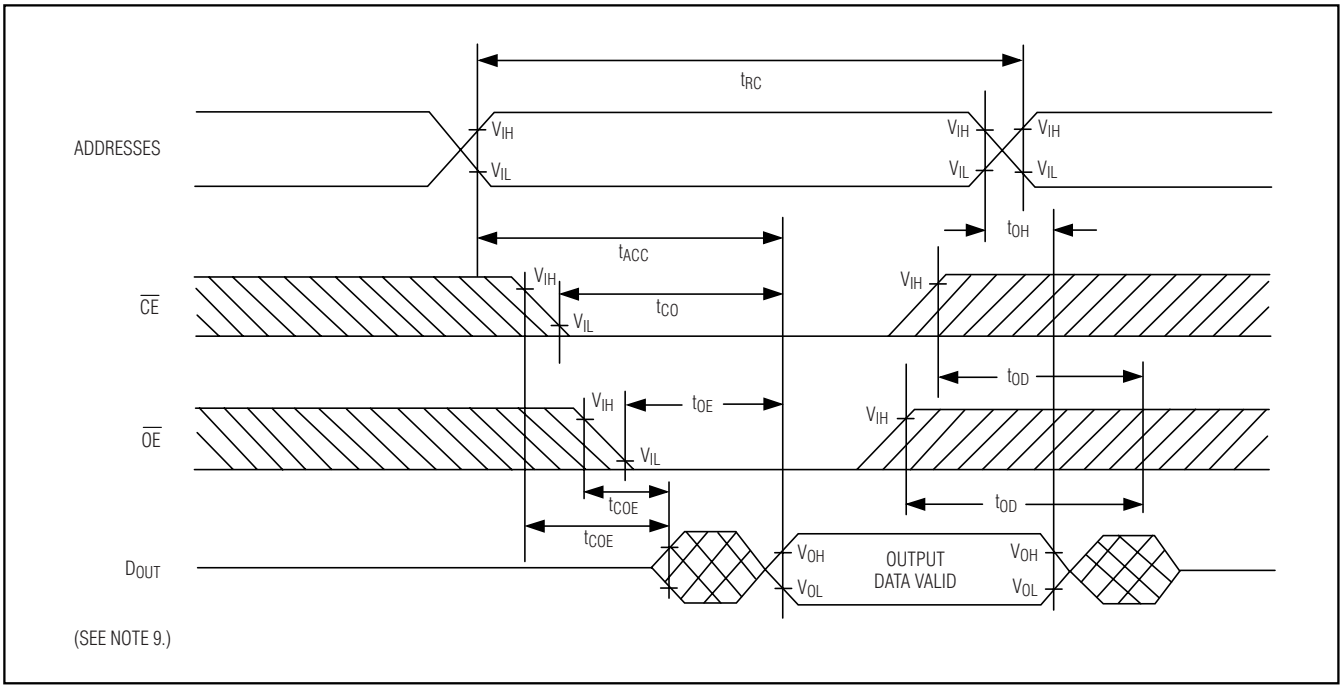
($T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Expected Data-Retention Time (Per Charge) | $t_{DR}$ | (Note 8) | 2 | 3 | | years |

## AC TEST CONDITIONS

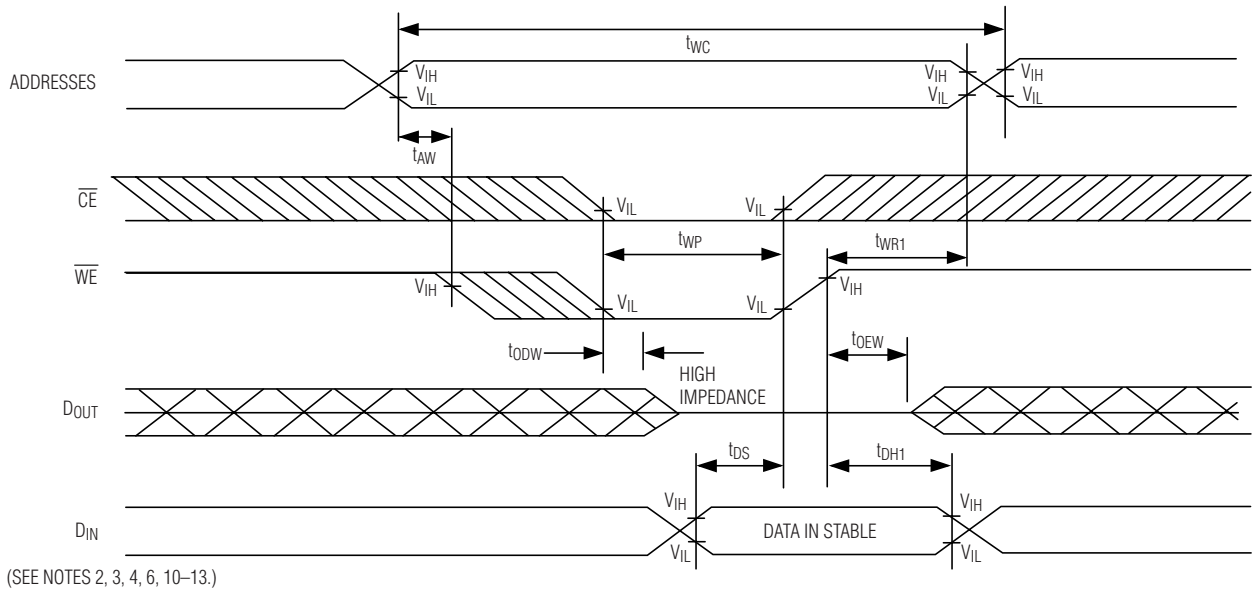
| | |
|---|---|
| Input Pulse Levels: | $V_{IL}$ = 0.0V, $V_{IH}$ = 2.7V |
| Input Pulse Rise and Fall Times: | 5ns |
| Input and Output Timing Reference Level: | 1.5V |
| Output Load: | 1 TTL Gate + $C_L$ (100pF) including scope and jig |

## Read Cycle


tRC
ADDRESSES
VIH
VIL
tACC
tOH
CE
tCO
OE
tOE
tOD
tCOE
DOUT
VOH
VOL
OUTPUT
DATA VALID
(SEE NOTE 9.)

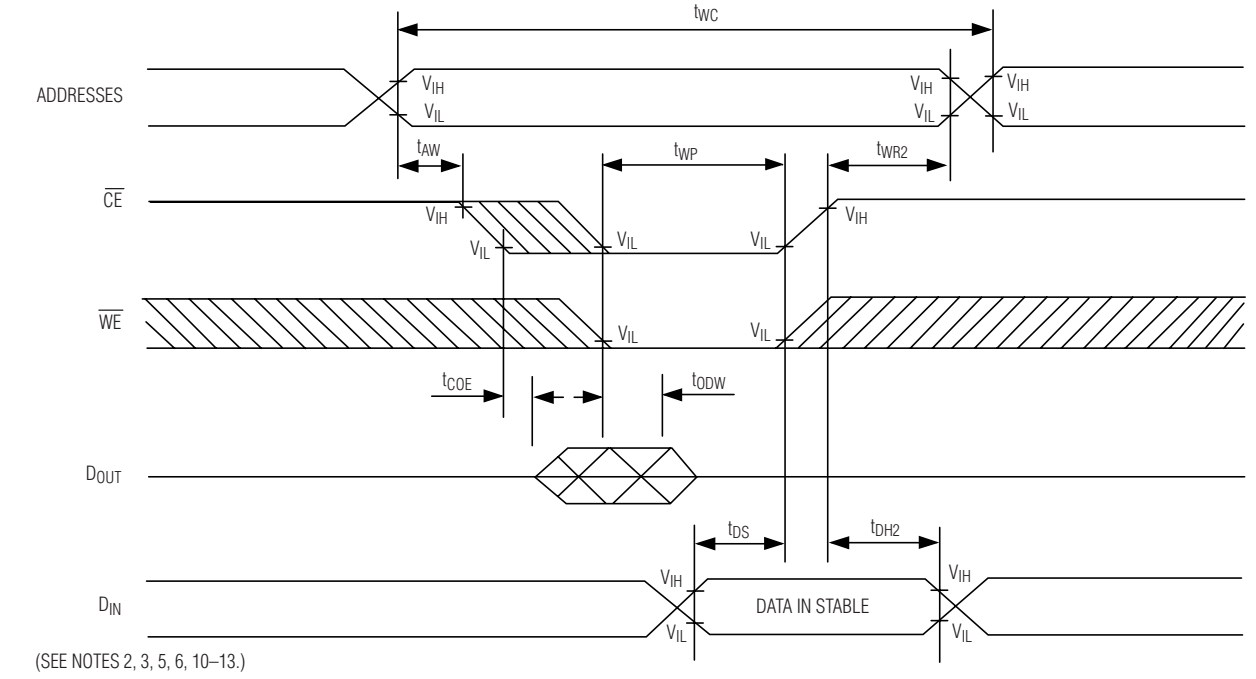
# DS2065W 3.3V Single-Piece 8Mb Nonvolatile SRAM

## Write Cycle 1




(SEE NOTES 2, 3, 4, 6, 10–13.)

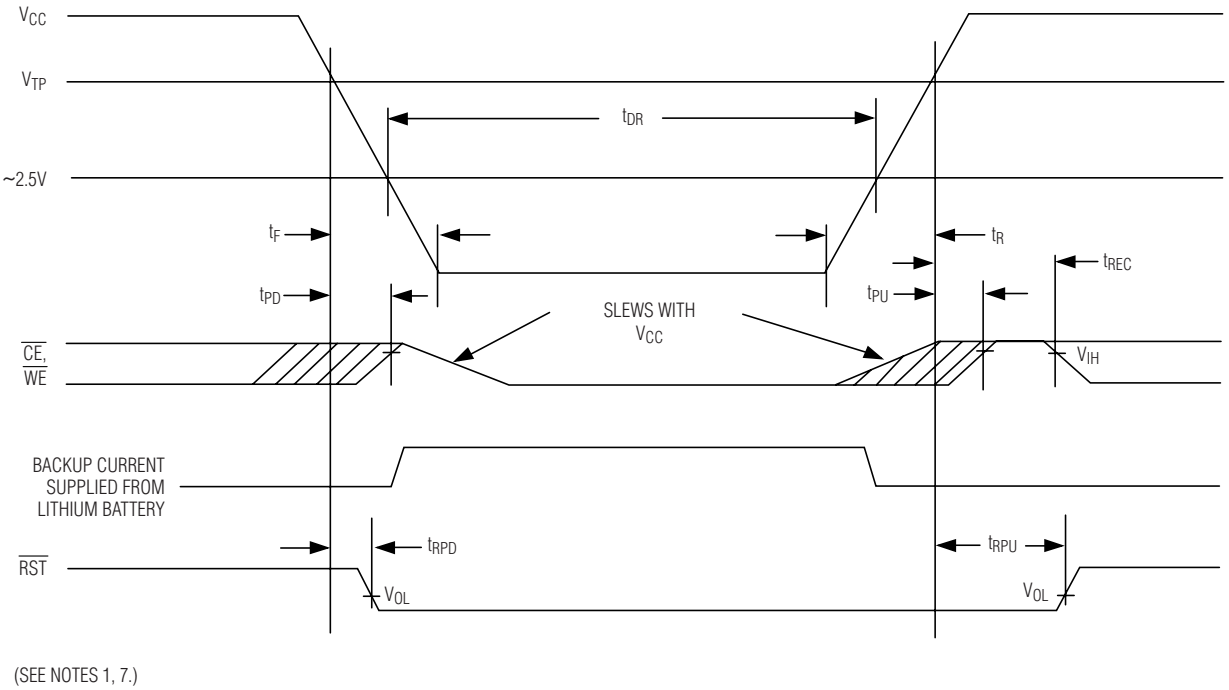
## Write Cycle 2




(SEE NOTES 2, 3, 5, 6, 10–13.)

# DS2065W 3.3V Single-Piece 8Mb Nonvolatile SRAM

## Power-Down/Power-Up Condition




(SEE NOTES 1, 7.)

**Note 1:** $\overline{RST}$ is an open-drain output and cannot source current. An external pullup resistor should be connected to this pin to realize a logic-high level.

**Note 2:** These parameters are sampled with a 5pF load and are not 100% tested.

**Note 3:** $t_{WP}$ is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

**Note 4:** $t_{WR1}$ and $t_{DH1}$ are measured from $\overline{WE}$ going high.

**Note 5:** $t_{WR2}$ and $t_{DH2}$ are measured from $\overline{CE}$ going high.

**Note 6:** $t_{DS}$ is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

**Note 7:** In a power-down condition, the voltage on any pin cannot exceed the voltage on $V_{CC}$.

**Note 8:** The expected $t_{DR}$ is defined as accumulative time in the absence of $V_{CC}$ starting from the time power is first applied by the user. Minimum expected data-retention time is based on a maximum of two +230°C convection solder reflow exposures, followed by a fully charged cell. Full charge occurs with the initial application of $V_{CC}$ for a minimum of 96 hours. This parameter is assured by component selection, process control, and design. It is not measured directly in production testing.

**Note 9:** $\overline{WE}$ is high for a read cycle.

**Note 10:** $\overline{OE}$ = $V_{IH}$ or $V_{IL}$. If $\overline{OE}$ = $V_{IH}$ during write cycle, the output buffers remain in a high-impedance state.

**Note 11:** If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition, the output buffers remain in a high-impedance state during this period.

**Note 12:** If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high-impedance state during this period.

**Note 13:** If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high-impedance state during this period.

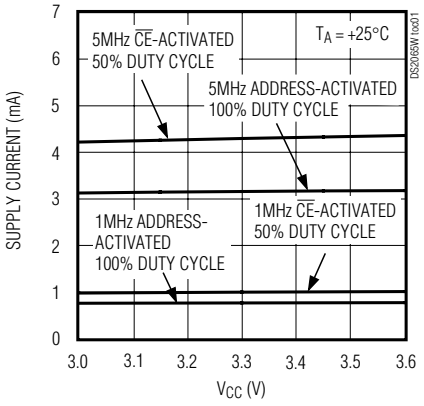
**Note 14:** DS2065W BGA modules are recognized by Underwriters Laboratory (UL) under file E99151.

# DS2065W 3.3V Single-Piece 8Mb Nonvolatile SRAM

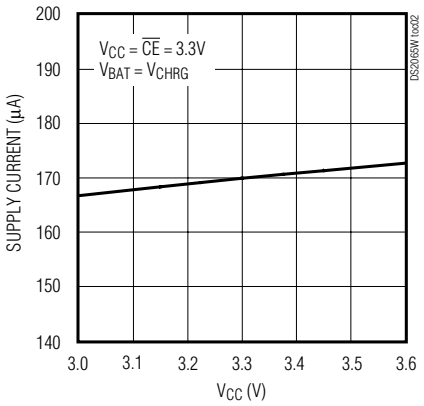
## Typical Operating Characteristics

($V_{CC}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.)

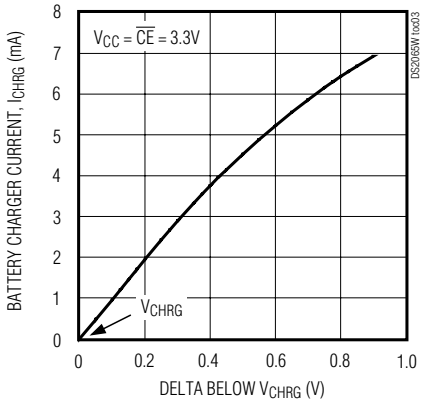
**SUPPLY CURRENT vs. OPERATING FREQUENCY**



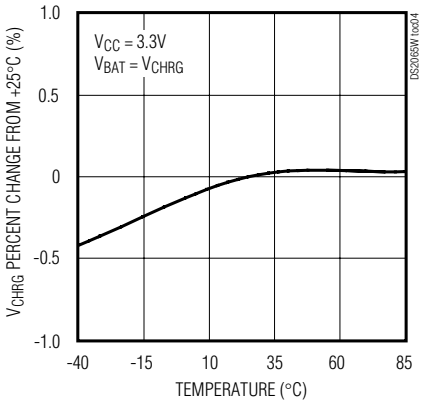

**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



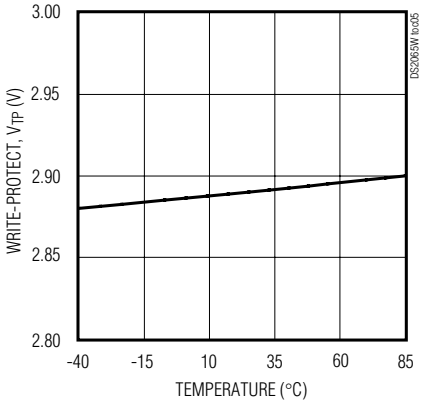

**BATTERY CHARGER CURRENT vs. BATTERY VOLTAGE**



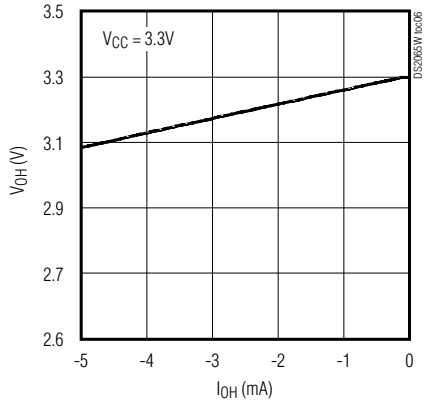

**$V_{CHRG}$ PERCENT CHANGE vs. TEMPERATURE**



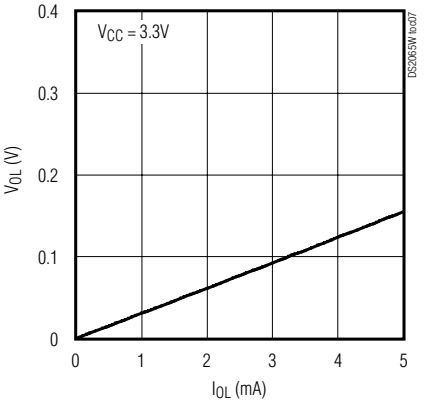

**$V_{TP}$ vs. TEMPERATURE**



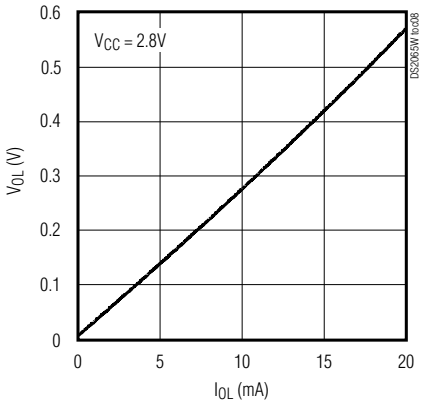

**DQ OUTPUT-VOLTAGE HIGH vs. DQ OUTPUT-CURRENT HIGH**



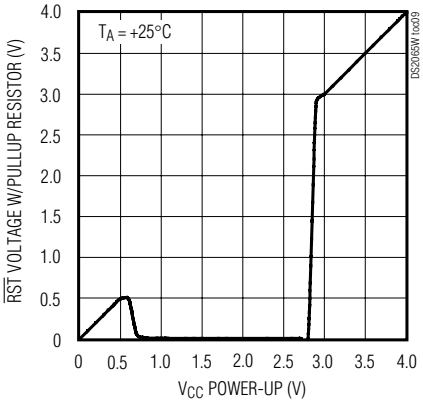

**DQ OUTPUT-VOLTAGE LOW vs. DQ OUTPUT-CURRENT LOW**




**$\overline{RST}$ OUTPUT-VOLTAGE LOW vs. OUTPUT-CURRENT LOW**




**$\overline{RST}$ VOLTAGE vs. $V_{CC}$ DURING POWER-UP**



# DS2065W 3.3V Single-Piece 8Mb Nonvolatile SRAM

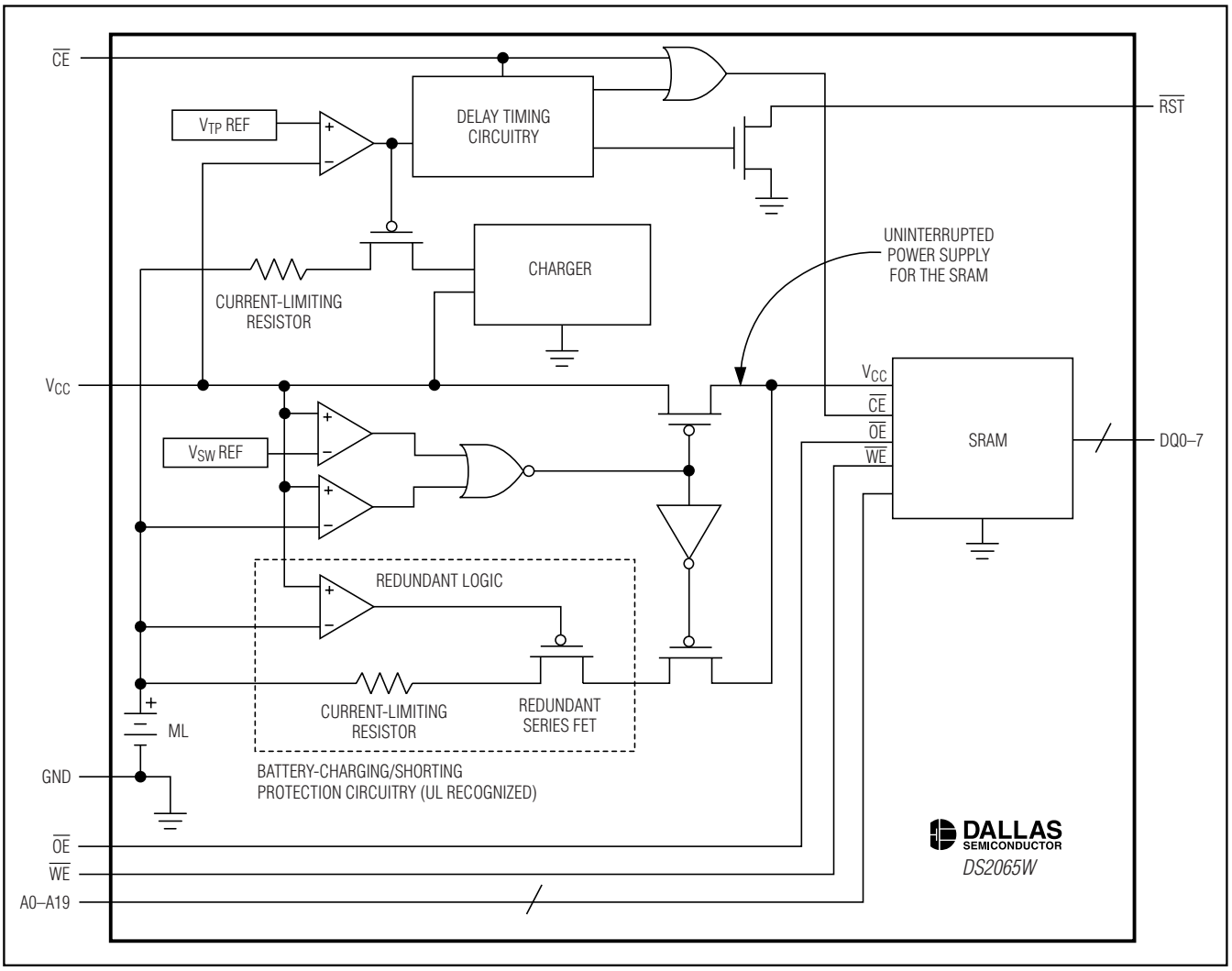
## Pin Description

| BALLS | NAME | DESCRIPTION |
|---|---|---|
| A1, A2, A3, A4 | GND | Ground |
| B1, B2, B3, B4 | N.C. | No Connection |
| C1, C2, C3, C4 | A15 | Address Input 15 |
| D1, D2, D3, D4 | A16 | Address Input 16 |
| E1, E2, E3, E4 | $\overline{RST}$ | Open-Drain Reset Output |
| F1, F2, F3, F4 | $V_{CC}$ | Supply Voltage |
| G1, G2, G3, G4 | $\overline{WE}$ | Write-Enable Input |
| H1, H2, H3, H4 | $\overline{OE}$ | Output-Enable Input |
| J1, J2, J3, J4 | $\overline{CE}$ | Chip-Enable Input |
| K1, K2, K3, K4 | DQ7 | Data Input/Output 7 |
| L1, L2, L3, L4 | DQ6 | Data Input/Output 6 |
| M1, M2, M3, M4 | DQ5 | Data Input/Output 5 |
| N1, N2, N3, N4 | DQ4 | Data Input/Output 4 |
| P1, P2, P3, P4 | DQ3 | Data Input/Output 3 |
| R1, R2, R3, R4 | DQ2 | Data Input/Output 2 |
| T1, T2, T3, T4 | DQ1 | Data Input/Output 1 |
| U1, U2, U3, U4 | DQ0 | Data Input/Output 0 |
| V1, V2, V3, V4 | GND | Ground |
| W1, W2, W3, W4 | GND | Ground |
| Y1, Y2, Y3, Y4 | GND | Ground |
| A17, A18, A19, A20 | GND | Ground |
| B17, B18, B19, B20 | A18 | Address Input 18 |
| C17, C18, C19, C20 | A17 | Address Input 17 |
| D17, D18, D19, D20 | A14 | Address Input 14 |
| E17, E18, E19, E20 | A13 | Address Input 13 |
| F17, F18, F19, F20 | A12 | Address Input 12 |
| G17, G18, G19, G20 | A11 | Address Input 11 |
| H17, H18, H19, H20 | A10 | Address Input 10 |
| J17, J18, J19, J20 | A9 | Address Input 9 |
| K17, K18, K19, K20 | A8 | Address Input 8 |
| L17, L18, L19, L20 | A7 | Address Input 7 |
| M17, M18, M19, M20 | A6 | Address Input 6 |

| BALLS | NAME | DESCRIPTION |
|---|---|---|
| N17, N18, N19, N20 | A5 | Address Input 5 |
| P17, P18, P19, P20 | A4 | Address Input 4 |
| R17, R18, R19, R20 | A3 | Address Input 3 |
| T17, T18, T19, T20 | A2 | Address Input 2 |
| U17, U18, U19, U20 | A1 | Address Input 1 |
| V17, V18, V19, V20 | A0 | Address Input 0 |
| W17, W18, W19, W20 | GND | Ground |
| Y17, Y18, Y19, Y20 | GND | Ground |
| A5, B5, C5, D5 | N.C. | No Connection |
| A6, B6, C6, D6 | N.C. | No Connection |
| A7, B7, C7, D7 | N.C. | No Connection |
| A8, B8, C8, D8 | N.C. | No Connection |
| A9, B9, C9, D9 | N.C. | No Connection |
| A10, B10, C10, D10 | N.C. | No Connection |
| A11, B11, C11, D11 | N.C. | No Connection |
| A12, B12, C12, D12 | N.C. | No Connection |
| A13, B13, C13, D13 | N.C. | No Connection |
| A14, B14, C14, D14 | N.C. | No Connection |
| A15, B15, C15, D15 | A19 | Address Input 19 |
| A16, B16, C16, D16 | N.C. | No Connection |
| U5, V5, W5, Y5 | N.C. | No Connection |
| U6, V6, W6, Y6 | N.C. | No Connection |
| U7, V7, W7, Y7 | N.C. | No Connection |
| U8, V8, W8, Y8 | N.C. | No Connection |
| U9, V9, W9, Y9 | N.C. | No Connection |
| U10, V10, W10, Y10 | N.C. | No Connection |
| U11, V11, W11, Y11 | N.C. | No Connection |
| U12, V12, W12, Y12 | N.C. | No Connection |
| U13, V13, W13, Y13 | N.C. | No Connection |
| U14, V14, W14, Y14 | N.C. | No Connection |
| U15, V15, W15, Y15 | N.C. | No Connection |
| U16, V16, W16, Y16 | N.C. | No Connection |

# DS2065W 3.3V Single-Piece 8Mb Nonvolatile SRAM

## Functional Diagram




## Detailed Description

The DS2065W is a 8Mb (1024kb x 8 bits) fully static, NV memory similar in function and organization to the DS1265W NV SRAM, but containing a rechargeable ML battery. The DS2065W NV SRAM constantly monitors $V_{CC}$ for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. There is no limit to the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing. This device can be used in place of SRAM, EEPROM, or flash components.

The DS2065W assembly consists of a low-power SRAM, an ML battery, and an NV controller with a battery charger, integrated on a standard 256-ball, 27mm$^2$ BGA substrate. Unlike other surface-mount NV memory modules that require the battery to be removable for soldering, the internal ML battery can tolerate exposure to convection reflow soldering temperatures allowing this single-piece component to be handled with standard BGA assembly techniques.

The DS2065W also contains a power-supply monitor output, $\overline{RST}$, which can be used as a CPU supervisor for a microprocessor.

# DS2065W 3.3V Single-Piece 8Mb Nonvolatile SRAM

## Memory Operation Truth Table

| $\overline{WE}$ | $\overline{CE}$ | $\overline{OE}$ | MODE | $I_{CC}$ | OUTPUTS |
|---|---|---|---|---|---|
| 1 | 0 | 0 | Read | Active | Active |
| 1 | 0 | 1 | Read | Active | High Impedance |
| 0 | 0 | X | Write | Active | High Impedance |
| X | 1 | X | Standby | Standby | High Impedance |

*X = Don't care.*

### Read Mode

The DS2065W executes a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (chip enable) is active (low). The unique address specified by the 20 address inputs (A0 to A19) defines which of the 1,048,576 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within $t_{ACC}$ (access time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{CE}$ and $\overline{OE}$ access times are not satisfied, then data access must be measured from the later-occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either $t_{CO}$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$, rather than address access.

### Write Mode

The DS2065W executes a write cycle whenever the $\overline{CE}$ and $\overline{WE}$ signals are active (low) after address inputs are stable. The later-occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers have been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{ODW}$ from its falling edge.

### Data-Retention Mode

The DS2065W provides full functional capability for $V_{CC}$ greater than 3.0V and write-protects by 2.8V. Data is maintained in the absence of $V_{CC}$ without additional support circuitry. The NV static RAM constantly monitors $V_{CC}$. Should the supply voltage decay, the NV SRAM automatically write-protects itself. All inputs become "don't care", and all data outputs become high impedance. As $V_{CC}$ falls below approximately 2.5V ($V_{SW}$), the power-switching circuit connects the lithium energy source to the RAM to retain data. During power-up, when $V_{CC}$ rises above $V_{SW}$, the power-switching circuit connects external $V_{CC}$ to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after $V_{CC}$ exceeds $V_{TP}$ for a minimum duration of $t_{REC}$.

### Battery Charging

When $V_{CC}$ is greater than $V_{TP}$, an internal regulator charges the battery. The UL-approved charger circuit includes short-circuit protection and a temperature-stabilized voltage reference for on-demand charging of the internal battery. Typical data-retention expectations of 3 years *per charge cycle* are achievable.

A maximum of 96 hours of charging time is required to fully charge a depleted battery.

### System Power Monitoring

When the external $V_{CC}$ supply falls below the selected out-of-tolerance trip point, the output $\overline{RST}$ is forced active (low). Once active, the $\overline{RST}$ is held active until the $V_{CC}$ supply has fallen below that of the internal battery. On power-up, the $\overline{RST}$ output is held active until the external supply is greater than the selected trip point and one reset timeout period ($t_{RPU}$) has elapsed. This is sufficiently longer than $t_{REC}$ to ensure that the SRAM is ready for access by the microprocessor.

### Freshness Seal and Shipping

The DS2065W is shipped from Dallas Semiconductor with the lithium battery electrically disconnected, guaranteeing that no battery capacity has been consumed during transit or storage. As shipped, the lithium battery is ~60% charged, and no preassembly charging operations should be attempted.

When $V_{CC}$ is first applied at a level greater than $V_{TP}$, the lithium battery is enabled for backup operation. A 96 hour initial battery charge time is recommended for new system installations.

## Recommended Reflow Temperature Profile

| PROFILE FEATURE | Sn-Pb EUTECTIC ASSEMBLY |
|---|---|
| Average ramp-up rate ($T_L$ to $T_P$) | 3°C/second max |
| Preheat<br>- Temperature min ($T_{Smin}$)<br>- Temperature max ($T_{Smax}$)<br>- Time (min to max) (ts) | <br>100°C<br>150°C<br>60 to 120 seconds |
| $T_{Smax}$ to $T_L$<br>- Ramp-up rate | |
| Time maintained above:<br>- Temperature ($T_L$)<br>- Time ($t_L$) | <br>183°C<br>60 to 150 seconds |
| Peak temperature ($T_P$) | 225 +0/-5°C |
| Time within 5°C of actual peak temperature ($T_P$) | 10 to 30 seconds |
| Ramp-down rate | 6°C/second max |
| Time 25°C to peak temperature | 6 minutes max |

***Note:*** *All temperatures refer to top side of the package, measured on the package body surface.*

### Recommended Cleaning Procedures

The DS2065W may be cleaned using aqueous-based cleaning solutions. No special precautions are needed when cleaning boards containing a DS2065W module.

Removal of the topside label violates the environmental integrity of the package and voids the warranty of the product.

## Applications Information

### Power-Supply Decoupling

To achieve the best results when using the DS2065W, decouple the power supply with a 0.1µF capacitor. Use a high-quality, ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, while ceramic capacitors have adequately high frequency response for decoupling applications.

### Using the Open-Drain $\overline{RST}$ Output

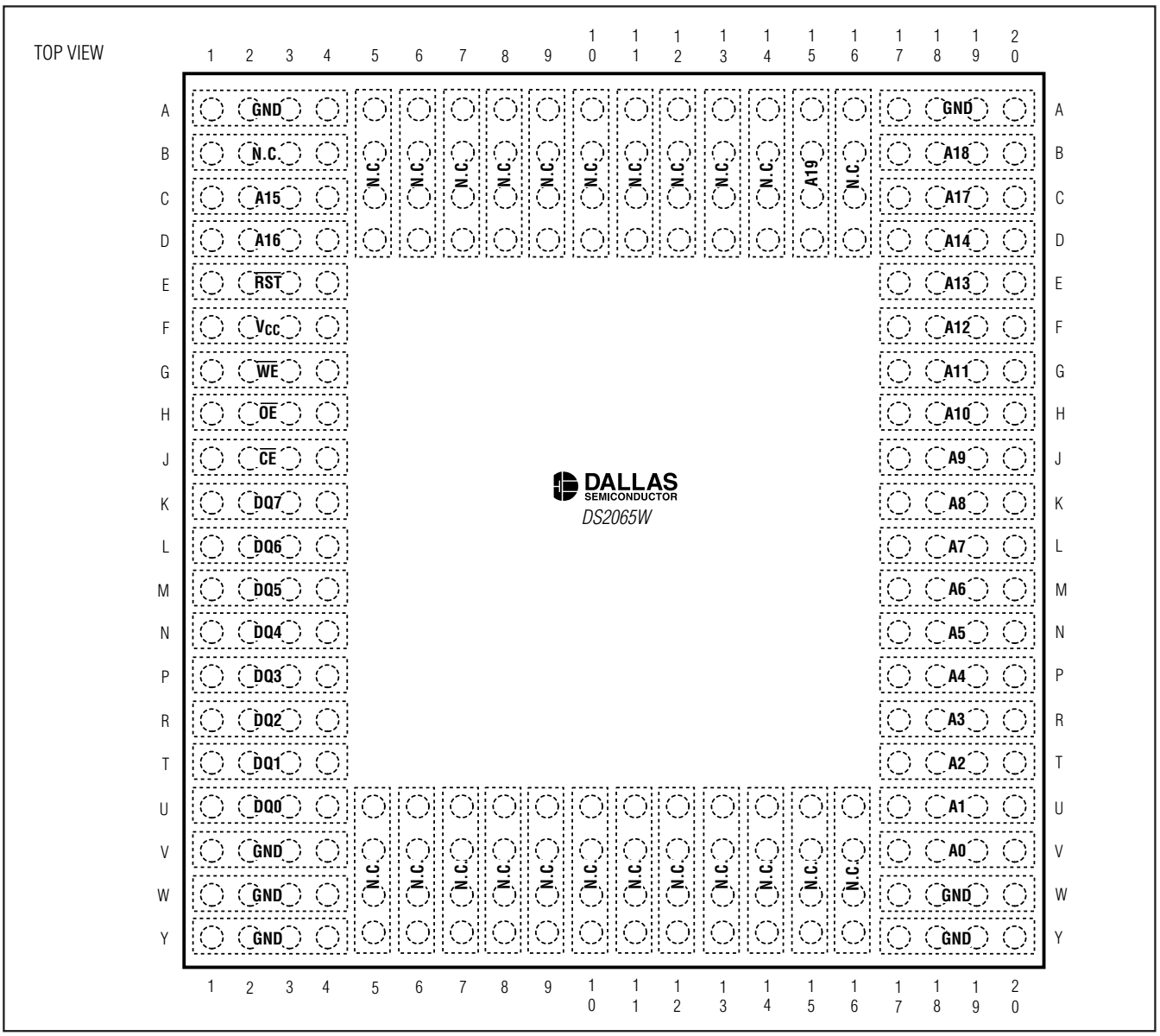
The $\overline{RST}$ output is open drain, and therefore requires a pullup resistor to realize a high logic output level. Pullup resistor values between 1kΩ and 10kΩ are typical.

### Battery Charging/Lifetime

The DS2065W charges an ML battery to maximum capacity in approximately 96 hours of operation when $V_{CC}$ is greater than $V_{TP}$. Once the battery is charged, its lifetime depends primarily on the $V_{CC}$ duty cycle. The DS2065W can maintain data from a single, initial charge for up to 3 years. Once recharged, this deep-discharge cycle can be repeated up to 20 times, producing a worst-case service life of 60 years. More typical duty cycles are of shorter duration, enabling the DS2065W to be charged hundreds of times, therefore extending the service life well beyond 60 years.

# DS2065W 3.3V Single-Piece 8Mb Nonvolatile SRAM

## Pin Configuration




## Revision History

Pages changed at Rev 2: 1, 3, 12

## Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.

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