Dual-Port, Differential VDSL2 Line Driver Amplifiers

FEATURES

- **Low Power Consumption:**
  - **21mA/Port Full Bias Mode**
  - **16.2mA/Port Mid Bias Mode**
  - **11.2mA/Port Low Bias Mode**
  - **Low-Power Shutdown Mode**
  - **I_{ADJ} Pin for Variable Bias**
- **Low Noise:**
  - **2.5nV/√Hz Voltage Noise**
  - **17pA/√Hz Inverting Current Noise**
  - **1.2pA/√Hz Noninverting Current Noise**
- **Low MTPR Distortion:**
  - **70dB with +20.5dBm G.993.2—Profile 8b**
- **–89dBc HD3 (1MHz, 100Ω Differential)**
- **High Output Current: > 424mA (25Ω Load)**
- **Wide Output Swing: 43.2V_{PP} (±12V, 100Ω Differential)**
- **Wide Bandwidth: 150MHz (Gain = 10V/V)**
- **Port-To-Port Separation of 90dB at 1MHz**
- **PSRR of 50dB at 1MHz for Good Isolation**
- **Wide Power-Supply Range: 10V to 28V**

APPLICATIONS

- **Ideal For VDSL2 Systems**
- **Backward-Compatible with ADSL/ADSL2+/ADSL2++ Systems**

DESCRIPTION

The THS6204 is a dual-port, current-feedback architecture, differential line driver amplifier system ideal for xDSL systems. The device is targeted for use in VDSL2 (very-high-bit-rate digital subscriber line 2) line driver systems that enable greater than +20.5dBm line power up to 8.5MHz with good linearity supporting the G.993.2 VDSL2 8b profile. It is also fast enough to support central-office transmission of +14.5dBm line power up to 18.1MHz—Profile 30a.

The unique architecture of the THS6204 allows quiescent current to be minimal while still achieving very high linearity. Differential distortion, under full bias conditions, is –89dBc at 1MHz and reduces to only –73dBc at 10MHz. Fixed multiple bias settings of the amplifiers allows for enhanced power savings for line lengths where the full performance of the amplifier is not required. To allow for even more flexibility and power savings, an I_{ADJ} pin is available to further lower the bias currents.

The wide output swing of 43.2V_{PP} (100Ω differentially) with ±12V power supplies, coupled with over 425mA current drive (25Ω), allows for wide dynamic headroom, keeping distortion minimal.

The THS6204 is available in a QFN-24 or a TSSOP-24 PowerPAD™ package.

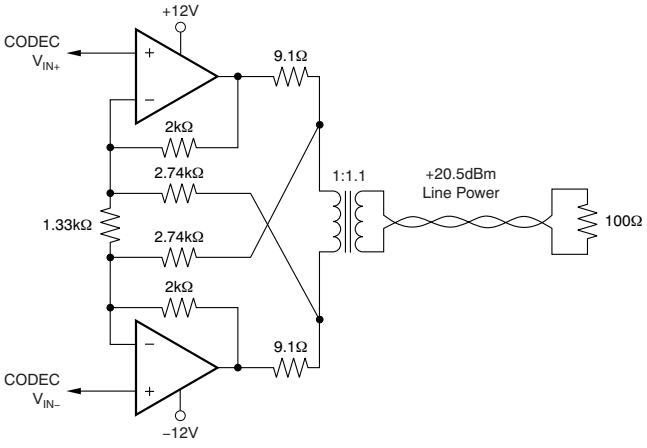


Figure 1. Typical VDSL2 Line Driver Circuit Utilizing One Port of the THS6204

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT(2)	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY
THS6204IRHFT	QFN-24	RHF	6204	Tape and Reel, 250
THS6204IRHFR				Tape and Reel, 3000
THS6204IPWP	TSSOP-24	PWP	THS6204	Rails, 60
THS6204IPWPR				Tape and Reel, 2000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) The PowerPAD is electrically isolated from all other pins.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		THS6204	UNIT
Supply voltage, V_{S-} to V_{S+}		28	V
Input voltage, V_I		$\pm V_S$	
Differential input voltage, V_{ID}		±2	V
Output current, I_O—static dc(2)		±100	mA
Continuous power dissipation		See Dissipation Ratings table	
Maximum junction temperature, any condition, T_J(3)		+150	°C
Maximum junction temperature, continuous operation, long-term reliability, T_J(4), QFN package		+130	°C
Maximum junction temperature, continuous operation, long-term reliability, T_J(4), TSSOP package		+140	°C
Storage temperature range, T_{STG}		–65 to +150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		+300	°C
ESD ratings	Human body model (HBM)	2000	V
	Charged device model (CDM)	500	V
	Machine model (MM)	100	V

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) The THS6204 incorporates a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD thermally-enhanced package. Under high-frequency ac operation (> 10kHz), the short-term output current capability is much greater than the continuous dc output current rating. This short-term output current rating is about 8.5X the dc capability, or about ±850mA.
(3) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(4) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)(1)(2)	POWER RATING(3) (T_J = +130°C)	
			T_A = +25°C	T_A = +85°C
QFN-24 (RHF)	1.7	32	3.28W	1.4W
HTSSOP-24 (PWP)	0.92	31	3.39W	1.45W

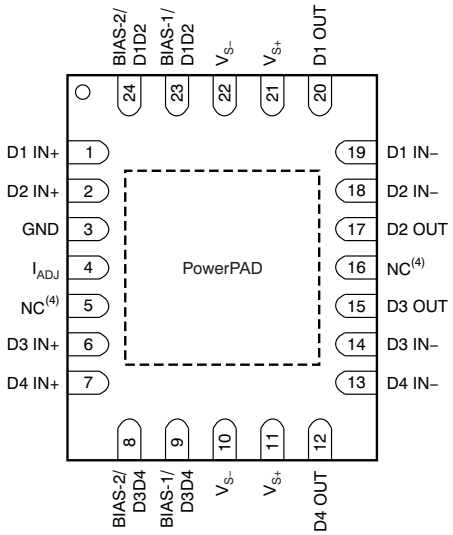
(1) This data was taken using a 4-layer, 3in × 3in (76.2mm × 76.2mm) test PCB with the PowerPAD soldered to the PCB. If the PowerPAD is not soldered to the PCB, θ_{JA} increases to +74°C/W for the RHF package and +62°C/W for the PWP package.
(2) For high-power dissipation applications, soldering the PowerPAD to the PCB is required. Failure to do so may result in reduced reliability and/or lifetime of the device. See TI technical brief SLMA002 for more information about utilizing the PowerPAD thermally enhanced package.
(3) Power rating is determined with a junction temperature of +130°C. This is the point where distortion starts to substantially increase and long-term reliability starts to be reduced. Thermal management of the final PCB should strive to keep the junction temperature at or below +130°C for best performance and reliability.

RECOMMENDED OPERATING CONDITIONS

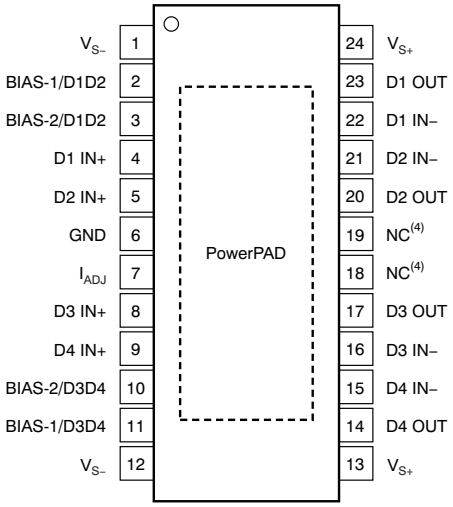
		THS6204		UNIT
		MIN	MAX	
Supply voltage, V_{S-} to V_{S+}	Dual supply	±5	±14	V
	Single supply	10	28	V
Operating free-air temperature, T_A		–40	+85	°C
Operating junction temperature, continuous operating temperature, T_J, QFN package		–40	+130	°C
Operating junction temperature, continuous operating temperature, T_J, TSSOP package		–40	+140	°C
Normal storage temperature, T_{STG}		–40	+85	°C

PIN CONFIGURATIONS(1)(2)(3)

QFN-24(4)
RHF PACKAGE
(TOP VIEW)



HTSSOP-24(4)
PWP PACKAGE
(TOP VIEW)



(1) The PowerPAD is electrically isolated from all other pins and can be connected to any potential voltage range from V_{S-} to V_{S+}. Typically, the PowerPAD is connected to the GND plane as this plane tends to physically be the largest and is able to dissipate the most amount of heat.
(2) The THS6204 defaults to shutdown mode if no signal is present on the bias pins.
(3) The GND pin range is from V_{S-} to (V_{S+} – 5V).
(4) NC = no connection.

ELECTRICAL CHARACTERISTICS: V_S = ±12V

At T_A = +25°C, R_F = 1.24kΩ, R_L = 100Ω differential, G_{Diff} = 10V/V differential, G_{CM} = 1V/V common-mode, and full bias, unless otherwise noted. Each port is independently tested.

PARAMETER	CONDITIONS		THS6204IRHF, IPWP TYP +25°C	THS6204IRHF, IPWP OVER TEMPERATURE +25°C(2)	THS6204IRHF, IPWP OVER TEMPERATURE 0°C to +70°C(3)	THS6204IRHF, IPWP OVER TEMPERATURE –40°C to +85°C(3)	UNITS	MIN/ MAX	TEST LEVEL(1)
AC PERFORMANCE									
Small-signal bandwidth, –3dB (V_O = 2V_{PP})	G_{DIFF} = 5V/V differential, R_F = 1.5kΩ, V_O = 2V_{PP}		160				MHz	Typ	C
	G_{DIFF} = 10V/V differential, R_F = 1.24kΩ, V_O = 2V_{PP}		150	120	110	100	MHz	Min	B
0.1dB bandwidth flatness	G_{DIFF} = 10V/V differential, R_F = 1.24kΩ		114				MHz	Typ	C
Large-signal bandwidth	G_{DIFF} = 10V/V differential, V_O = 20V_{PP}		120				MHz	Typ	C
Slew rate (10% to 90% level)	G_{DIFF} = 10V/V, V_O = 20V step, differential		3800	3200	3100	3000	V/µs	Min	B
Rise and fall time	G_{DIFF} = +5V/V, V_O = 2V_{PP}, differential		5				ns	Typ	C
Harmonic distortion									
2nd harmonic	G_{DIFF} = 10V/V, V_O = 2V_{PP}, f = 1MHz, R_L = 100Ω	Full bias	–100	–95	–92	–90	dBc	Min	B
		Low bias	–96				dBc	Typ	C
3rd harmonic		Full bias	–89	–85	–82	–80	dBc	Min	B
		Low bias	–85				dBc	Typ	C
2nd harmonic	G_{DIFF} = 10V/V, V_O = 2V_{PP}, f = 10MHz, R_L = 100Ω	Full bias	–75	–70	–68	–65	dBc	Min	B
		Low bias	–72				dBc	Typ	C
3rd harmonic		Full bias	–73	–65	–61	–53	dBc	Min	B
		Low bias	–58				dBc	Typ	C
Multi-tone power ratio (MTPR) G ≈ 11, active termination, SF ≈ 4.	VDSL2 8b profile +20.5dBm		–70				dBc	Typ	C
	VDSL2 17a profile +14.5dBm; power supply = ±7.5V		–65				dBc	Typ	C
Differential input voltage noise	f = 1MHz		2.5	3.0	3.2	3.3	nV/√Hz	Max	B
Differential inverting current noise	f = 1MHz		17	20	22	24	pA/√Hz	Max	B
Differential noninverting current noise	f = 1MHz		1.2	1.4	1.5	1.6	pA/√Hz	Max	B
DC PERFORMANCE									
Open-loop transimpedance gain	R_L = 100Ω		700	**330**	320	300	kΩ	Typ	A
Input offset voltage			±15	**±50**	±55	±60	mV	Max	A
Input offset voltage drift					±110	±155	µV/°C	Max	B
Input offset voltage matching	Channels 1 to 2 and 3 to 4 only		±0.5	**±5**	±6	±7	mV	Max	A
Noninverting input bias current			±1	**±3**	±4	±5	µA	Max	A
Noninverting input bias current drift					±25	±30	nA/°C	Max	B
Inverting input bias current			±8	**±40**	±45	±50	µA	Max	A
Inverting input bias current drift					±115	±135	nA/°C	Max	B
Inverting input bias current matching			±8	**±25**	±30	±35	µA	Max	A
INPUT CHARACTERISTICS									
Common-mode input range	Each amplifier		±9.5	**±9**	±8.8	±8.6	V	Min	A
Common-mode rejection ratio	Each amplifier		65	**53**	50	49	dB	Min	A
Noninverting input resistance			500 || 2				kΩ || pF	Typ	C
Inverting input resistance			50				Ω	Typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.

ELECTRICAL CHARACTERISTICS: V_S = ±12V (continued)

At T_A = +25°C, R_F = 1.24kΩ, R_L = 100Ω differential, G_{Diff} = 10V/V differential, G_{CM} = 1V/V common-mode, and full bias, unless otherwise noted. Each port is independently tested.

PARAMETER	CONDITIONS		THS6204IRHF, IPWP TYP +25°C	THS6204IRHF, IPWP OVER TEMPERATURE +25°C(2)	THS6204IRHF, IPWP OVER TEMPERATURE 0°C to +70°C(3)	THS6204IRHF, IPWP OVER TEMPERATURE –40°C to +85°C(3)	UNITS	MIN/ MAX	TEST LEVEL(1)
OUTPUT CHARACTERISTICS(4)									
Output voltage swing	R_L = 100Ω, each output, linear output		±10.9				V	Typ	C
	R_L = 50Ω, each output, linear output		±10.8	**±10.6**	±10.5	±10.4	V	Min	A
	R_L = 25Ω, each output, linear output		±10.4	**±10.2**	±10.1	±10.0	V	Min	A
Output current (sourcing, sinking)	R_L = 25Ω, each output		±416	**±408**	±404	±400	mA	Min	A
Short-circuit output current			±1				A	Typ	C
Output impedance	f = 1MHz, differential		0.2				Ω	Typ	C
Crosstalk	f = 1MHz, V_{OUT} = 2V_{PP}	Port 1 to port 2	–90				dB	Typ	C
POWER SUPPLY									
Operating voltage			±12				V	Typ	C
Maximum operating voltage				**±14**	±14	±14	V	Max	A
Minimum operating voltage				**±5**	±5	±5	V	Min	B
Maximum I_{S+} quiescent current	Per port, full bias (Bias-1 = 0, Bias-2 = 0)		21	**22.5**	23.5	24	mA	Max	A
	Per port, mid bias (Bias-1 = 1, Bias-2 = 0)		16.2	**17.7**	18.5	19	mA	Max	A
	Per port, mid bias ; R_{ADJ} = 604Ω		12.6	**14.1**	15	15.5	mA	Max	A
	Per port, low bias (Bias-1 = 0, Bias-2 = 1)		11.2	**12.7**	13.4	13.9	mA	Max	A
	Per port, bias off (Bias-1 = 1, Bias-2 = 1)		0.5	**0.8**	0.9	1	mA	Max	A
Minimum I_{S+} quiescent current	Per port, full bias (Bias-1 = 0, Bias-2 = 0)		21	**19.5**	18.5	17	mA	Min	A
	Per port, mid bias (Bias-1 = 1, Bias-2 = 0)		16.2	**14.7**	13.7	13	mA	Min	A
	Per port, low bias (Bias-1 = 0, Bias-2 = 1)		11.2	**9.7**	9.1	7.6	mA	Min	A
Maximum $I_{S–}$ quiescent current	Per port, full bias (Bias-1 = 0, Bias-2 = 0)		20.5	**21.5**	22.5	23	mA	Max	A
	Per port, mid bias (Bias-1 = 1, Bias-2 = 0)		15.7	**16.7**	17.4	17.8	mA	Max	A
	Per port, mid bias ; R_{ADJ} = 604Ω		12.1	**13.1**	14	14.5	mA	Max	A
	Per port, low bias (Bias-1 = 0,Bias-2 = 1)		10.7	**11.7**	12.1	12.4	mA	Max	A
	Per port, bias off (Bias-1 = 1, Bias-2 = 1)		0.1	**0.3**	0.6	0.8	mA	Max	A
Minimum $I_{S–}$ quiescent current	Per port, full bias (Bias-1 = 0, Bias-2 = 0)		20.5	**19.5**	18.5	17.5	mA	Min	A
	Per port, mid bias (Bias-1 = 1, Bias-2 = 0)		15.7	**14.7**	13.8	13.6	mA	Min	A
	Per port, low bias (Bias-1 = 0, Bias-2 = 1)		10.7	**9.7**	9.4	9.1	mA	Min	A
Current through GND pin			0.5				mA	Typ	C
Power-supply rejection ratio (+PSRR)			66	**54**	53	52	dB	Min	A
Power-supply rejection ratio (–PSRR)			65	**52**	51	50	dB	Min	A

(4) Test circuit is shown in Figure 2.

ELECTRICAL CHARACTERISTICS: V_S = ±12V (continued)

At T_A = +25°C, R_F = 1.24kΩ, R_L = 100Ω differential, G_{Diff} = 10V/V differential, G_{CM} = 1V/V common-mode, and full bias, unless otherwise noted. Each port is independently tested.

PARAMETER	CONDITIONS	THS6204IRHF, IPWP				UNITS	MIN/ MAX	TEST LEVEL(1)
		TYP	OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to +70°C(3)	–40°C to +85°C(3)			
LOGIC								
Bias control pin logic threshold	Logic 1, with respect to GND(5)		1.9	1.9	1.9	V	Min	B
	Logic 0, with respect to GND(5)		0.8	0.8	0.8	V	Max	B
Bias pin quiescent current	Bias-X = 0.5V (logic 0)	20	**30**	33	35	µA	Max	A
	Bias-X = 3.3V (logic 1)	0.3	**1**	1.1	1.2	µA	Max	A
Turn-on time delay (t_{ON})	Time for I_S to reach 50% of final value	1				µs	Typ	C
Turn-off time delay (t_{OFF})		1				µs	Typ	C
Bias pin input impedance		50				kΩ	Typ	C
Amplifier output impedance	Off bias (Bias-1 = 1, Bias-2 = 1)	10 || 5				kΩ || pF	Typ	C

(5) The GND pin usable range is from $V_{S–}$ to (V_{S+} – 5V).

Table 1. Logic Table

BIAS-1	BIAS-2	FUNCTION	DESCRIPTION
0	0	Full bias mode	Amplifiers on with lowest distortion possible
1	0	Mid bias mode	Amplifiers on with power savings and a reduction in distortion performance
0	1	Low bias mode	Amplifiers on with enhanced power savings and a reduction of performance
1	1	Shutdown mode	Amplifiers off and output has high impedance (default state if left floating)

ELECTRICAL CHARACTERISTICS: V_S = ±6V

At T_A = +25°C, R_F = 1.5kΩ, R_L = 100Ω differential, G_{Diff} = 10V/V differential, G_{CM} = 1V/V common-mode, and full bias, unless otherwise noted. Each port is independently tested.

PARAMETER	CONDITIONS		THS6204IRHF, IPWP TYP +25°C	THS6204IRHF, IPWP OVER TEMPERATURE +25°C(2)	THS6204IRHF, IPWP OVER TEMPERATURE 0°C to +70°C(3)	THS6204IRHF, IPWP OVER TEMPERATURE –40°C to +85°C(3)	UNITS	MIN/ MAX	TEST LEVEL(1)
AC PERFORMANCE									
Small-signal bandwidth, –3dB (V_O = 2V_{PP})	G = 5V/V differential, R_F = 1.82kΩ		140				MHz	Typ	C
	G = 10V/V differential, R_F = 1.5kΩ		140	110	100	95	MHz	Min	B
0.1dB bandwidth flatness	G = 10V/V differential, R_F = 1.5kΩ		12				MHz	Typ	C
Large-signal bandwidth	G = 10V/V differential, V_O = 20V_{PP}		140				MHz	Typ	C
Slew rate (10% to 90% level)	G = 10V/V, V_O = 20V step, differential		1600	1200	1100	1000	V/µs	Min	B
Rise and fall time	G = +5V/V, V_O = 2V_{PP}, differential		5				ns	Typ	C
Harmonic distortion									
2nd harmonic	G = 10V/V, V_O = 2V_{PP}, f = 1MHz, R_L = 100Ω differential	Full bias	–98	–92	–89	–87	dBc	Min	B
		Low bias	–93				dBc	Typ	C
3rd harmonic		Full bias	–93	–84	–81	–79	dBc	Min	B
		Low bias	–89				dBc	Typ	C
2nd harmonic	G = 10V/V, V_O = 2V_{PP}, f = 10MHz, R_L = 100Ω differential	Full bias	–80	–75	–70	–68	dBc	Min	B
		Low bias	–74				dBc	Typ	C
3rd harmonic		Full bias	–66	–60	–58	–54	dBc	Min	B
		Low bias	–55				dBc	Typ	C
Multi-tone power ratio (MTPR) G ≈ 11, active termination, SF ≈ 4.	VDSL2 8b profile +20.5dBm		–70				dBc	Typ	C
	VDSL2 17a profile +14.5dBm; power supply = ±7.5V		–65				dBc	Typ	C
Differential input voltage noise	f = 1MHz		2.5	3.0	3.2	3.3	nV/√Hz	Max	B
Differential inverting current noise	f = 1MHz		17	20	22	24	pA/√Hz	Max	B
Differential noninverting current noise	f = 1MHz		1.2	1.4	1.5	1.6	pA/√Hz	Max	B
DC PERFORMANCE									
Open-loop transimpedance gain	R_L = 100Ω		650	**330**	320	300	kΩ	Typ	A
Input offset voltage			±10	**±45**	±50	±55	mV	Max	A
Input offset voltage drift					±110	±155	µV/°C	Max	B
Input offset voltage matching	Channels 1 to 2 and 3 to 4 only		±0.5	**±5**	±6	±7	mV	Max	A
Noninverting input bias current			±1	**±3**	±4	±5	µA	Max	A
Noninverting input bias current drift					±25	±30	nA/°C	Max	B
Inverting input bias current			±8	**±40**	±45	±50	µA	Max	A
Inverting input bias current drift					±115	±135	nA/°C	Max	B
Inverting input bias current matching			±8	**±25**	±30	±35	µA	Max	A
INPUT CHARACTERISTICS									
Common-mode input range	Each amplifier		±3.0	**±2.9**	±2.8	±2.7	V	Min	A
Common-mode rejection ratio	Each amplifier		62	**51**	48	47	dB	Min	A
Noninverting input resistance			500 || 2				kΩ || pF	Typ	C
Inverting input resistance			55				Ω	Typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.

ELECTRICAL CHARACTERISTICS: V_S = ±6V (continued)

At T_A = +25°C, R_F = 1.5kΩ, R_L = 100Ω differential, G_{Diff} = 10V/V differential, G_{CM} = 1V/V common-mode, and full bias, unless otherwise noted. Each port is independently tested.

PARAMETER	CONDITIONS		THS6204IRHF, IPWP TYP +25°C	THS6204IRHF, IPWP OVER TEMPERATURE 0°C to +70°C(3)	THS6204IRHF, IPWP OVER TEMPERATURE –40°C to +85°C(3)	UNITS	MIN/ MAX	TEST LEVEL(1)
OUTPUT CHARACTERISTICS(4)								
Output voltage swing	R_L = 100Ω, each output, linear output		±4.9			V	Typ	C
	R_L = 50Ω, each output, linear output		±4.9	**±4.75**	±4.65	±4.6	V	Min	A
	R_L = 25Ω, each output, linear output		±4.7	**±4.55**	±4.45	±4.4	V	Min	A
Output current (sourcing, sinking)	R_L = 25Ω, each output		±188	**±182**	±178	±176	mA	Min	A
Short-circuit output current			±1				A	Typ	C
Output impedance	f = 1MHz, differential		0.2				Ω	Typ	C
Crosstalk	f = 1MHz, V_{OUT} = 2V_{PP}	Port 1 to port 2	–90				dB	Typ	C
POWER SUPPLY								
Operating voltage			±6				V	Typ	C
Maximum operating voltage				**±14**	±14	±14	V	Max	A
Minimum operating voltage				**±5**	±5	±5	V	Min	B
Maximum I_{S+} quiescent current	Per port, full bias (Bias-1 = 0, Bias-2 = 0)		17	**21**	21.5	22	mA	Max	A
	Per port, mid bias (Bias-1 = 1, Bias-2 = 0)		13.2	**16.8**	16.9	17	mA	Max	A
	Per port, low bias (Bias-1 = 0, Bias-2 = 1)		9.4	**12.2**	12.3	12.4	mA	Max	A
	Per port, bias off (Bias-1 = 1, Bias-2 = 1)		0.5	**0.8**	0.9	0.9	mA	Max	A
Minimum I_{S+} quiescent current	Per port, full bias (Bias-1 = 0, Bias-2 = 0)		17	**13**	11.5	10	mA	Min	A
	Per port, mid bias (Bias-1 = 1, Bias-2 = 0)		13.2	**9.8**	9.3	8.9	mA	Min	A
	Per port, low bias (Bias-1 = 0, Bias-2 = 1)		9.4	**6.7**	6.4	6.0	mA	Min	A
Maximum $I_{S–}$ quiescent current	Per port, full bias (Bias-1 = 0, Bias-2 = 0)		16.5	**20.5**	21	21.5	mA	Max	A
	Per port, mid bias (Bias-1 = 1, Bias-2 = 0)		12.7	**16.3**	16.4	16.5	mA	Max	A
	Per port, low bias (Bias-1 = 0,Bias-2 = 1)		8.9	**11.7**	11.8	11.9	mA	Max	A
	Per port, bias off (Bias-1 = 1, Bias-2 = 1)		0.1	**0.3**	0.4	0.5	mA	Max	A
Minimum $I_{S–}$ quiescent current	Per port, full bias (Bias-1 = 0, Bias-2 = 0)		16.5	**12.5**	11	9.5	mA	Min	A
	Per port, mid bias (Bias-1 = 1, Bias-2 = 0)		12.7	**9.3**	8.8	8.4	mA	Min	A
	Per port, low bias (Bias-1 = 0, Bias-2 = 1)		8.9	**6.2**	5.9	5.5	mA	Min	A
Current through GND pin			0.5				mA	Typ	C
Power-supply rejection ratio (+PSRR)			64	**54**	53	52	dB	Min	A
Power-supply rejection ratio (–PSRR)			63	**52**	51	50	dB	Min	A

(4) Test circuit is shown in Figure 2.

ELECTRICAL CHARACTERISTICS: V_S = ±6V (continued)

At T_A = +25°C, R_F = 1.5kΩ, R_L = 100Ω differential, G_{Diff} = 10V/V differential, G_{CM} = 1V/V common-mode, and full bias, unless otherwise noted. Each port is independently tested.

PARAMETER	CONDITIONS	THS6204IRHF, IPWP				UNITS	MIN/ MAX	TEST LEVEL(1)
		TYP	OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to +70°C(3)	–40°C to +85°C(3)			
LOGIC								
Bias control pin logic threshold	Logic 1, with respect to GND(5)				1.9	V	Min	B
	Logic 0, with respect to GND(5)				0.8	V	Max	B
Bias pin quiescent current	Bias-X = 0.5V (logic 0)	20	**30**	33	35	µA	Max	A
	Bias-X = 3.3V (logic 1)	0.3	**1**	1.1	1.2	µA	Max	A
Turn-on time delay (t_{ON})	Time for I_S to reach 50% of final value	1				µs	Typ	C
Turn-off time delay (t_{OFF})		1				µs	Typ	C
Bias pin input impedance		50				kΩ	Typ	C
Amplifier output impedance	Off bias (Bias-1 = 1, Bias-2 = 1)	10 || 5				kΩ || pF	Typ	C

(5) The GND pin usable range is from $V_{S–}$ to (V_{S+} – 5V).

Table 2. Logic Table

BIAS-1	BIAS-2	FUNCTION	DESCRIPTION
0	0	Full bias mode	Amplifiers on with lowest distortion possible
1	0	Mid bias mode	Amplifiers on with power savings and a reduction in distortion performance
0	1	Low bias mode	Amplifiers on with enhanced power savings and a reduction of performance
1	1	Shutdown mode	Amplifiers off and output has high impedance (default state if left floating)

TYPICAL CHARACTERISTICS: V_S = ±12V, Full Bias

At T_A = +25°C, G_{DIFF} = +10V/V, G_{CM} = 1V/V, R_{ADJ} = 0Ω, R_F = 1.24kΩ, and R_L = 100Ω, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

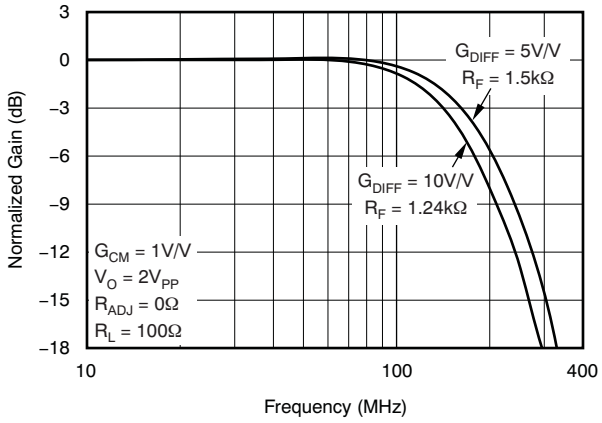


Figure 2.

SMALL-SIGNAL FREQUENCY RESPONSE vs BIAS MODE

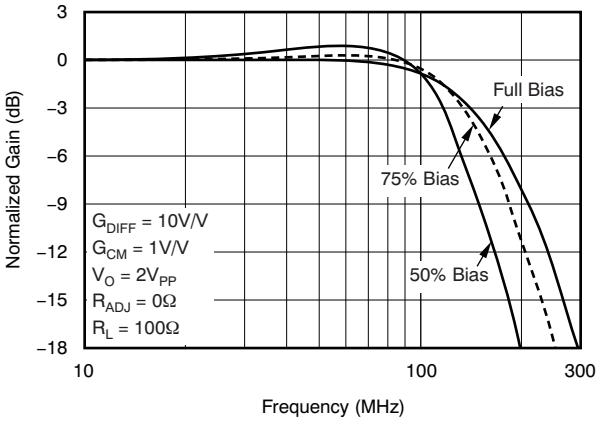


Figure 3.

LARGE SIGNAL FREQUENCY RESPONSE

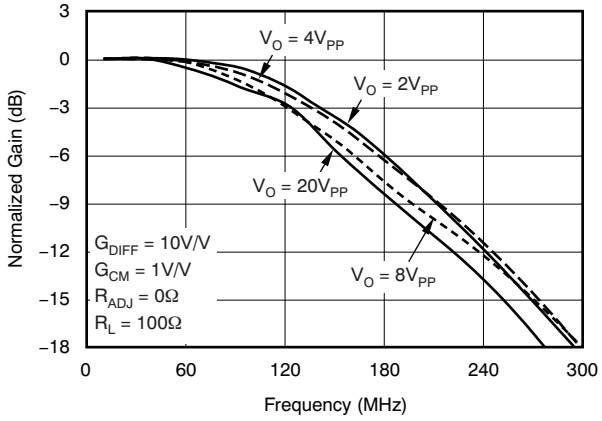


Figure 4.

SMALL-SIGNAL AND LARGE-SIGNAL PULSE RESPONSE

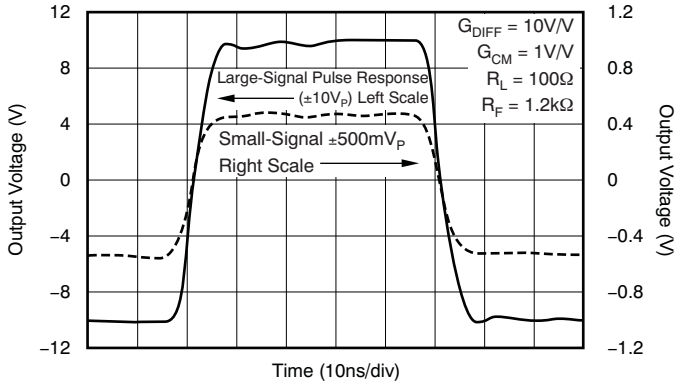


Figure 5.

RECOMMENDED R_S vs CAPACITIVE LOAD

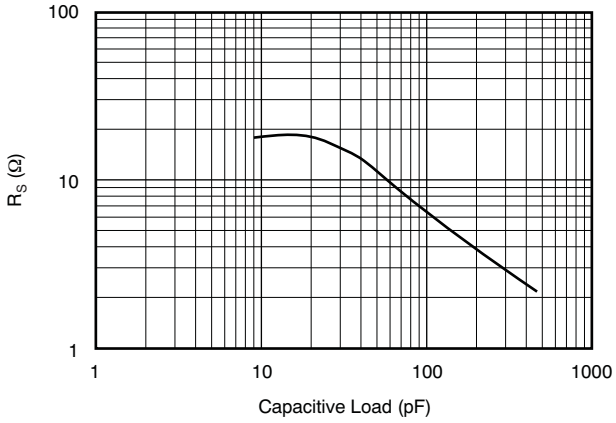


Figure 6.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

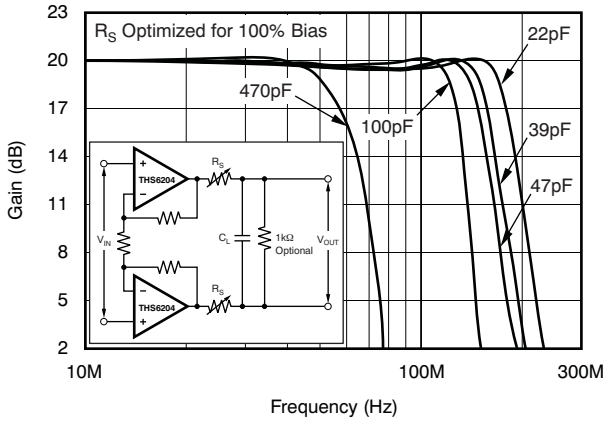


Figure 7.

TYPICAL CHARACTERISTICS: V_S = ±12V, Full Bias (continued)

At T_A = +25°C, G_{DIFF} = +10V/V, G_{CM} = 1V/V, R_{ADJ} = 0Ω, R_F = 1.24kΩ, and R_L = 100Ω, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

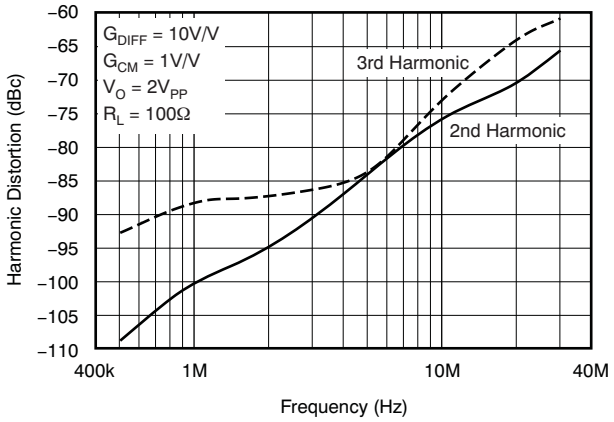


Figure 8.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

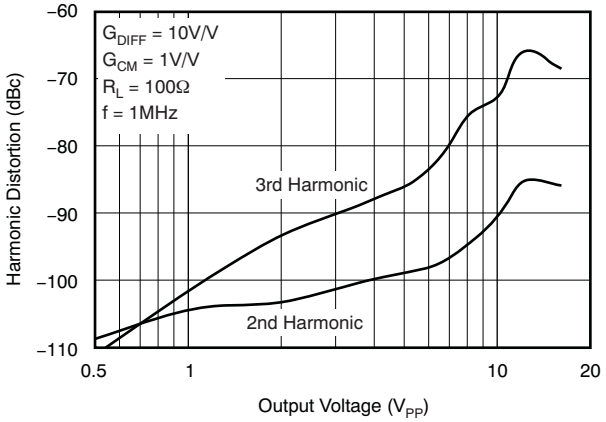


Figure 9.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

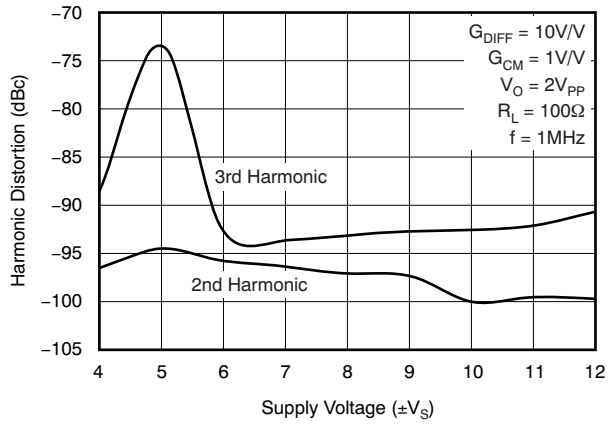


Figure 10.

HARMONIC DISTORTION vs LOAD RESISTANCE

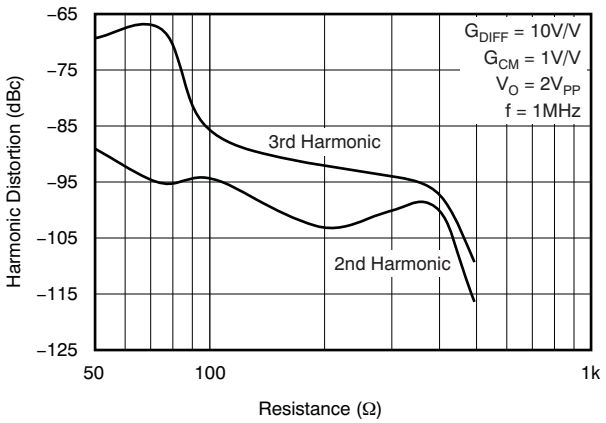


Figure 11.

HARMONIC DISTORTION vs NONINVERTING GAIN

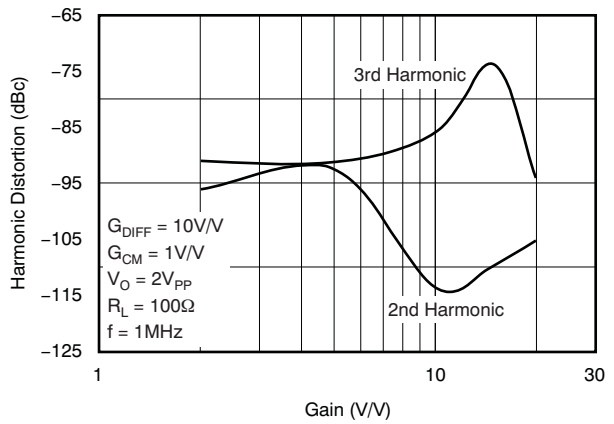


Figure 12.

2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

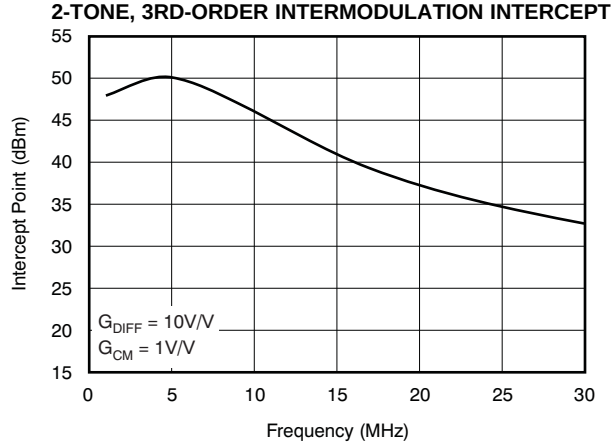


Figure 13.

TYPICAL CHARACTERISTICS: V_S = ±12V, Full Bias (continued)

At T_A = +25°C, G_{DIFF} = +10V/V, G_{CM} = 1V/V, R_{ADJ} = 0Ω, R_F = 1.24kΩ, and R_L = 100Ω, unless otherwise noted.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

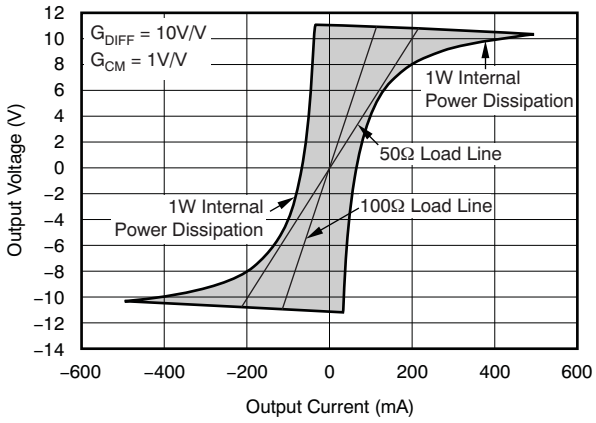


Figure 14.

INPUT VOLTAGE AND CURRENT NOISE DENSITY

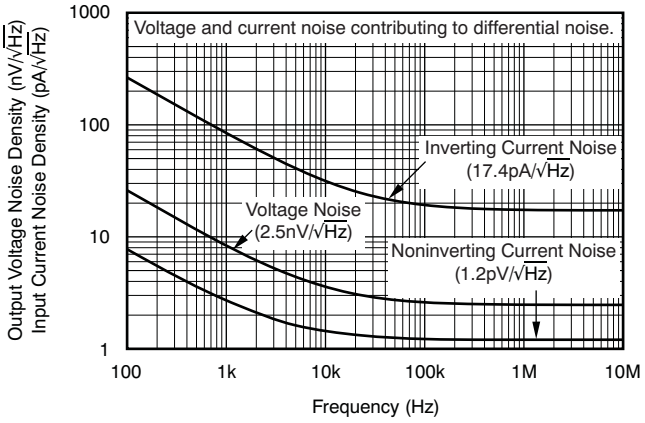


Figure 15.

SUPPLY CURRENT FOR FULL BIAS SETTINGS vs R_{ADJ}

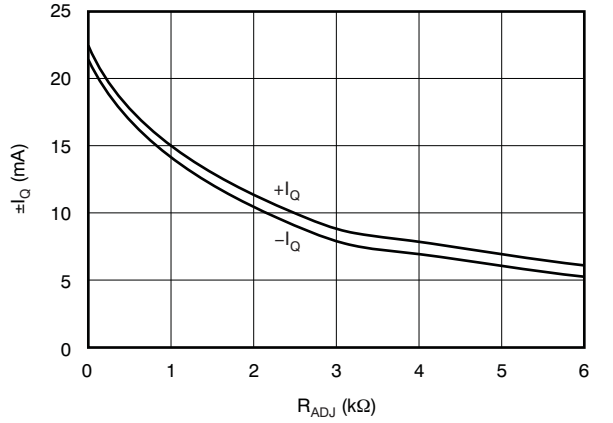


Figure 16.

PSRR vs FREQUENCY

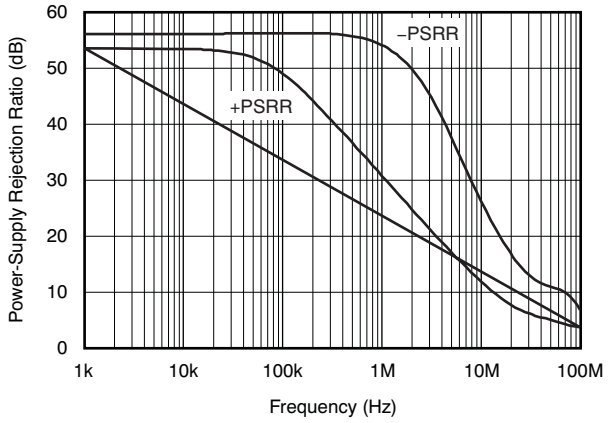


Figure 17.

OPEN-LOOP GAIN AND PHASE

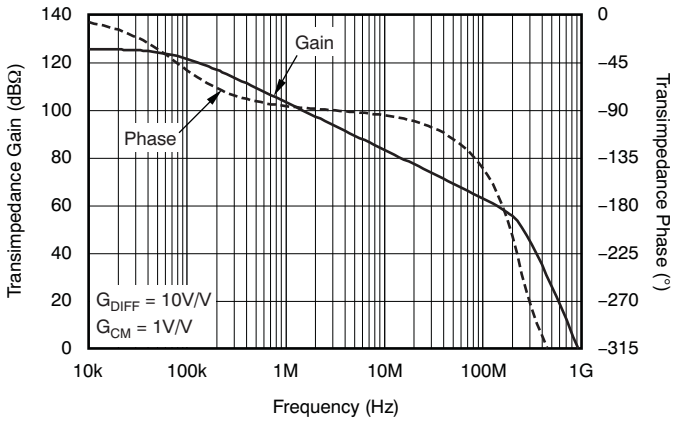


Figure 18.

CLOSED-LOOP OUTPUT IMPEDANCE

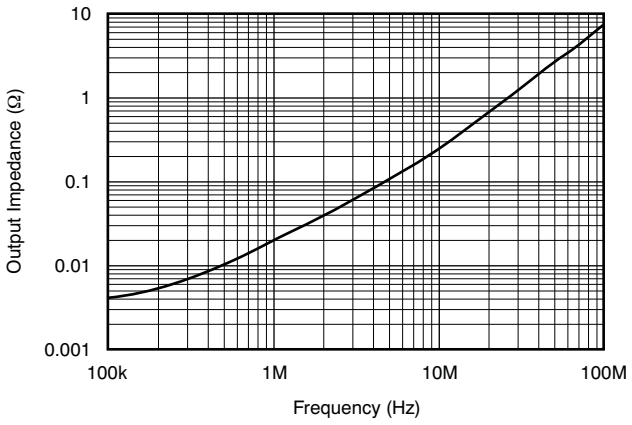


Figure 19.

TYPICAL CHARACTERISTICS: V_S = ±12V, 75% Bias

At T_A = +25°C, G_{DIFF} = +10V/V, G_{CM} = 1V/V, R_{ADJ} = 0Ω, R_F = 1.24kΩ, and R_L = 100Ω, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

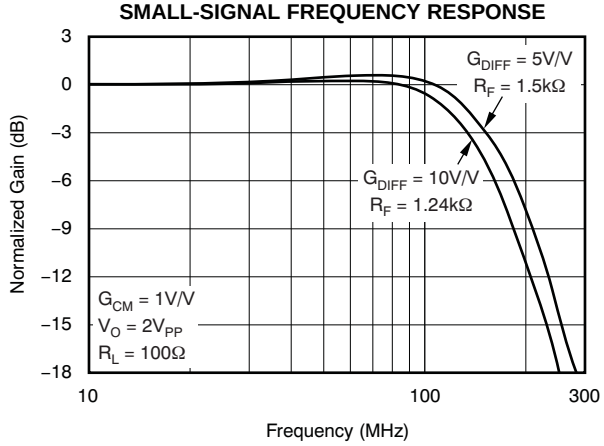


Figure 20.

LARGE-SIGNAL FREQUENCY RESPONSE

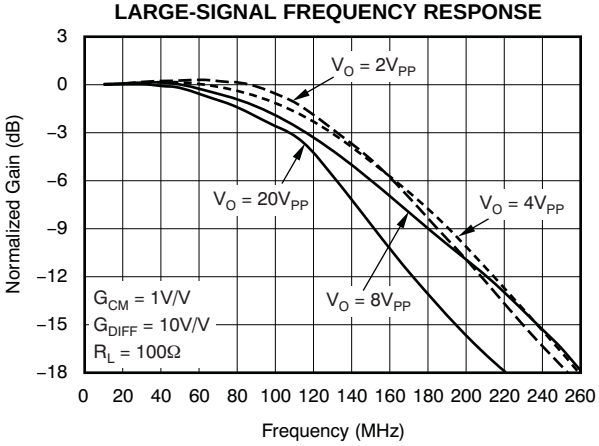


Figure 21.

DIFFERENTIAL SMALL-SIGNAL AND LARGE-SIGNAL PULSE RESPONSE

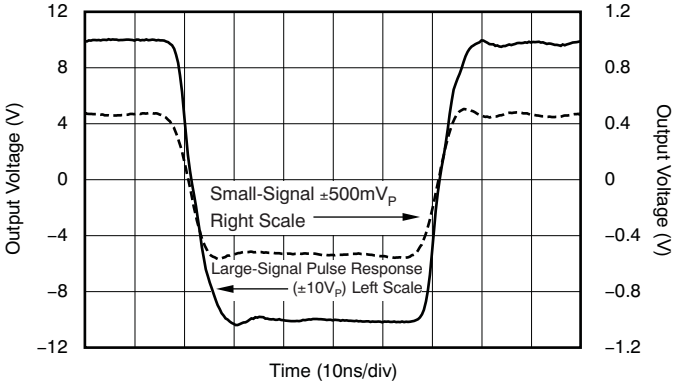


Figure 22.

SUPPLY CURRENT FOR FULL BIAS SETTINGS vs R_{ADJ}

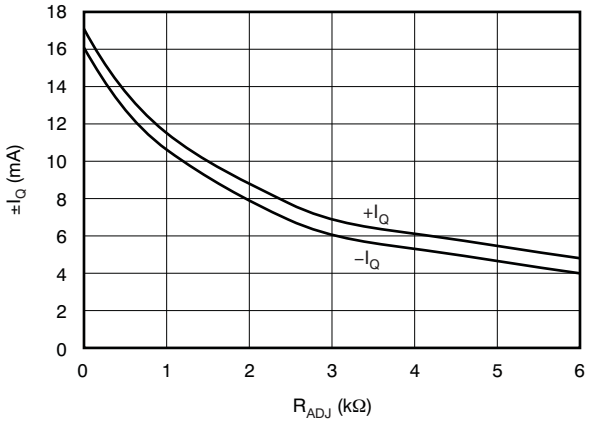


Figure 23.

RECOMMENDED R_S vs CAPACITIVE LOAD

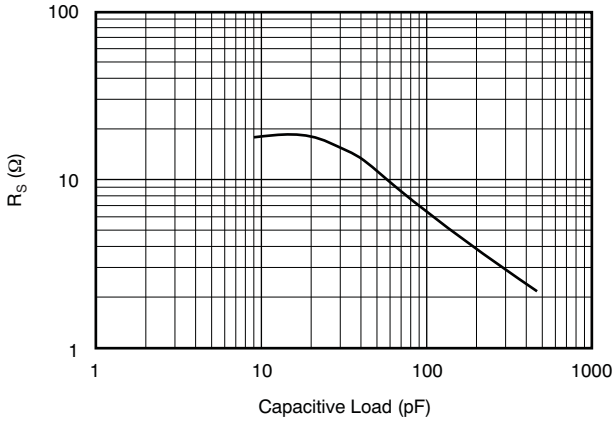


Figure 24.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

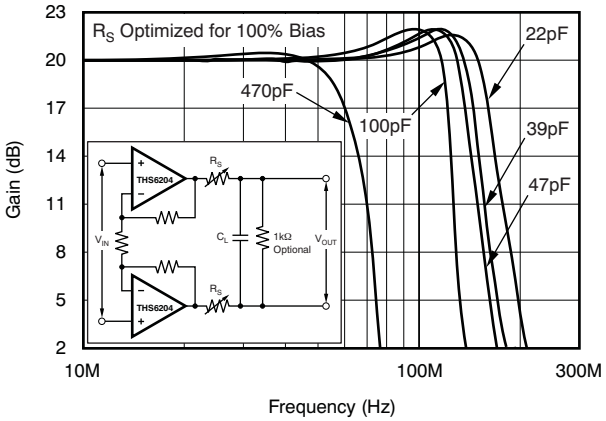


Figure 25.

TYPICAL CHARACTERISTICS: V_S = ±12V, 75% Bias (continued)

At T_A = +25°C, G_{DIFF} = +10V/V, G_{CM} = 1V/V, R_{ADJ} = 0Ω, R_F = 1.24kΩ, and R_L = 100Ω, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

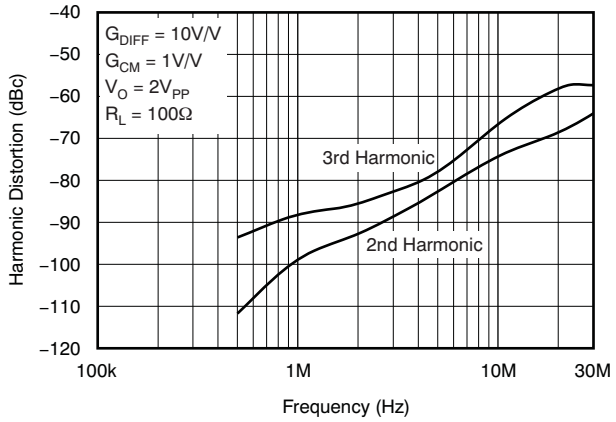


Figure 26.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

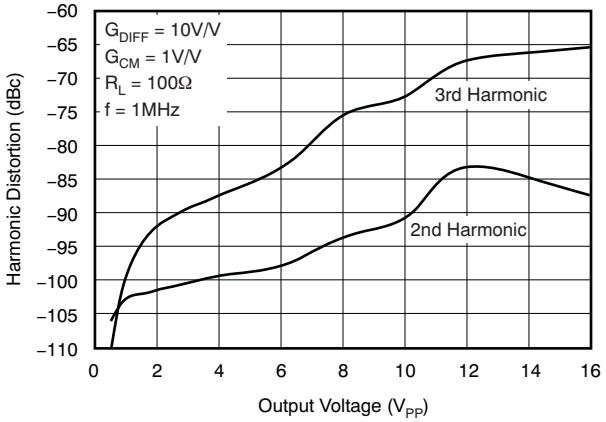


Figure 27.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

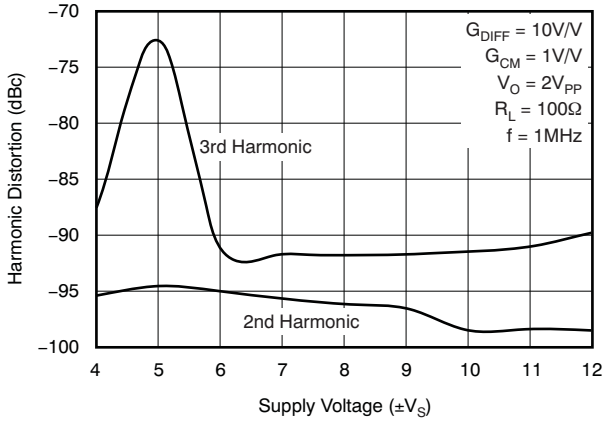


Figure 28.

HARMONIC DISTORTION vs LOAD RESISTANCE

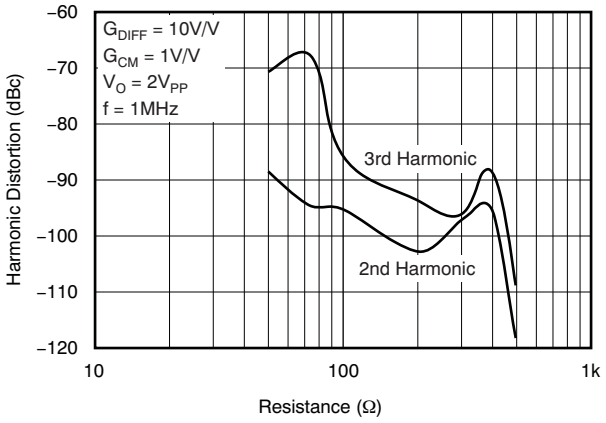


Figure 29.

HARMONIC DISTORTION vs NONINVERTING GAIN

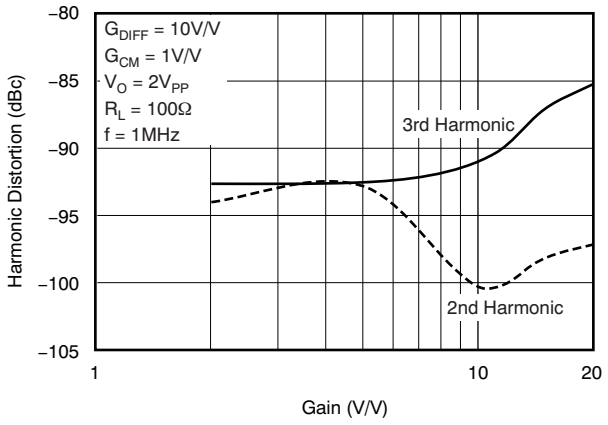


Figure 30.

2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

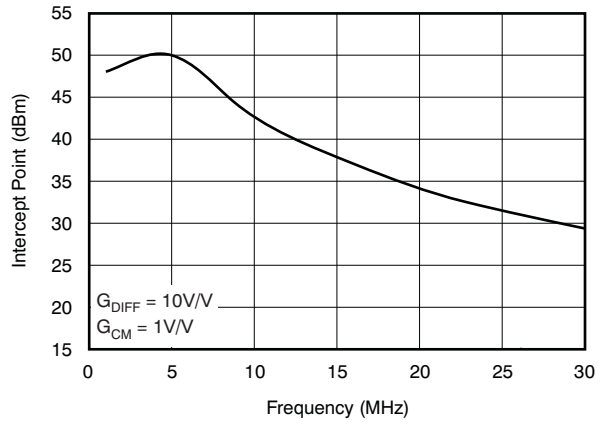


Figure 31.

TYPICAL CHARACTERISTICS: V_S = ±12V, 50% Bias

At T_A = +25°C, G_{DIFF} = +10V/V, G_{CM} = 1V/V, R_{ADJ} = 0Ω, R_F = 1.24kΩ, and R_L = 100Ω, unless otherwise noted.

50% BIAS FREQUENCY RESPONSE

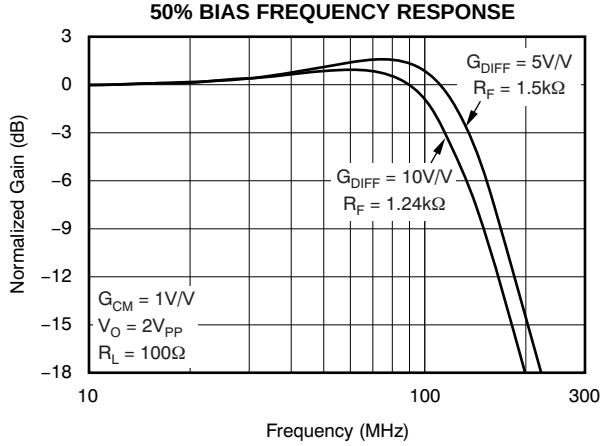


Figure 32.

LARGE-SIGNAL FREQUENCY RESPONSE

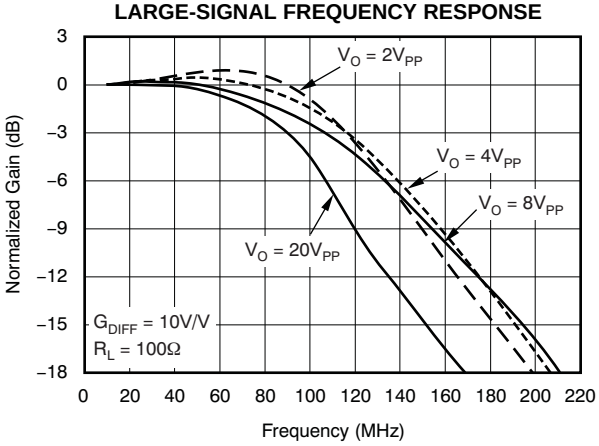


Figure 33.

DIFFERENTIAL PULSE RESPONSE

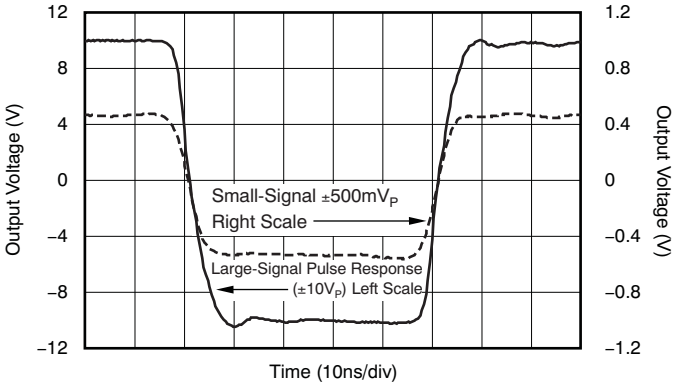


Figure 34.

SUPPLY CURRENT FOR FULL BIAS SETTINGS vs R_{ADJ}

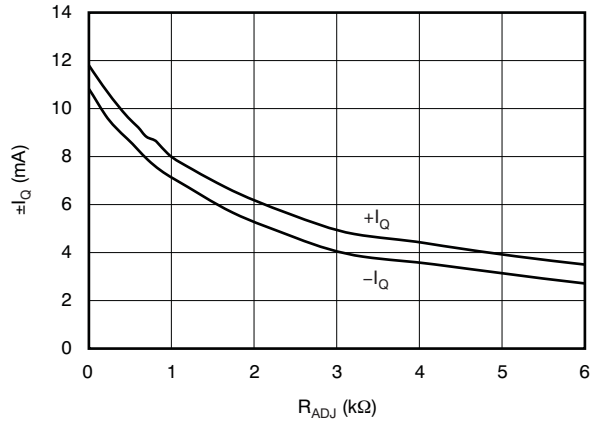


Figure 35.

RECOMMENDED R_S vs CAPACITIVE LOAD

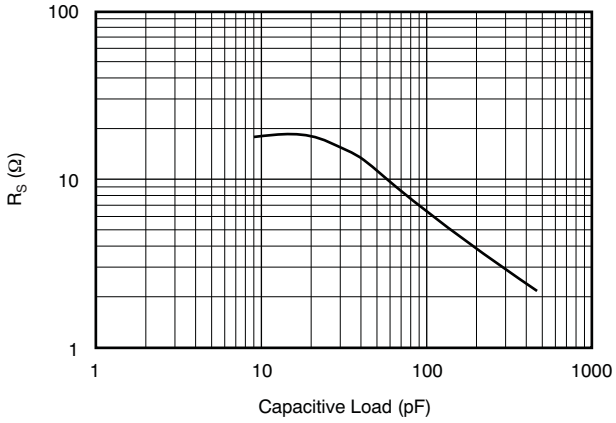


Figure 36.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

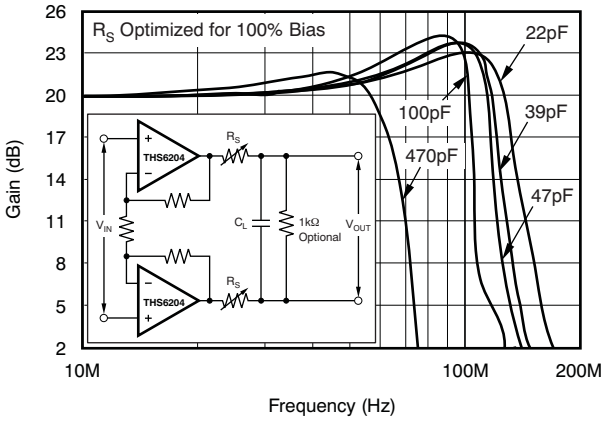


Figure 37.

TYPICAL CHARACTERISTICS: V_S = ±12V, 50% Bias (continued)

At T_A = +25°C, G_{DIFF} = +10V/V, G_{CM} = 1V/V, R_{ADJ} = 0Ω, R_F = 1.24kΩ, and R_L = 100Ω, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

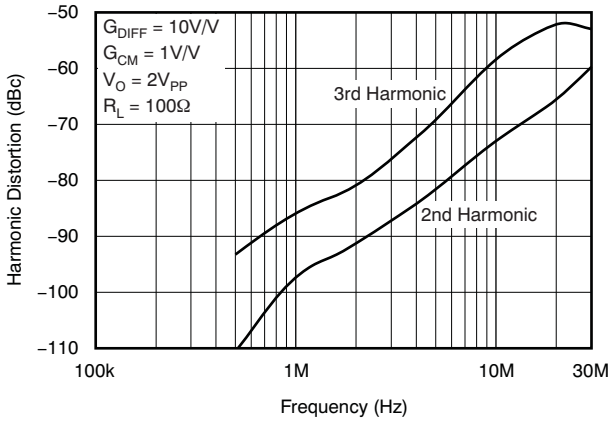


Figure 38.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

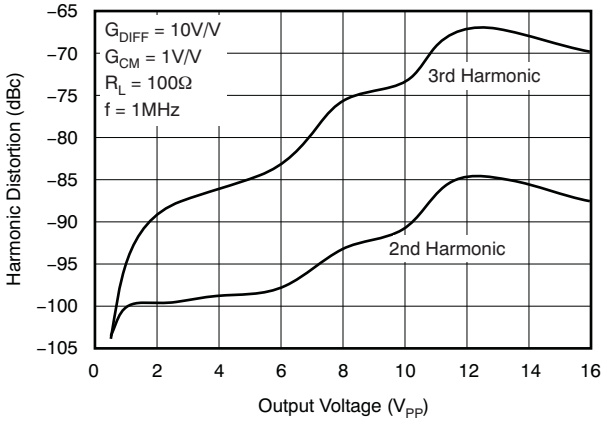


Figure 39.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

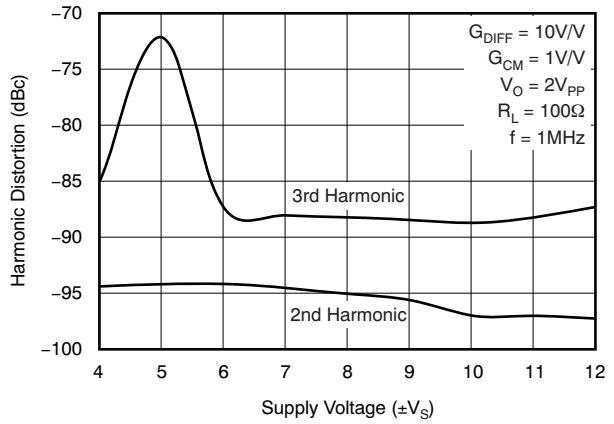


Figure 40.

HARMONIC DISTORTION vs LOAD RESISTANCE

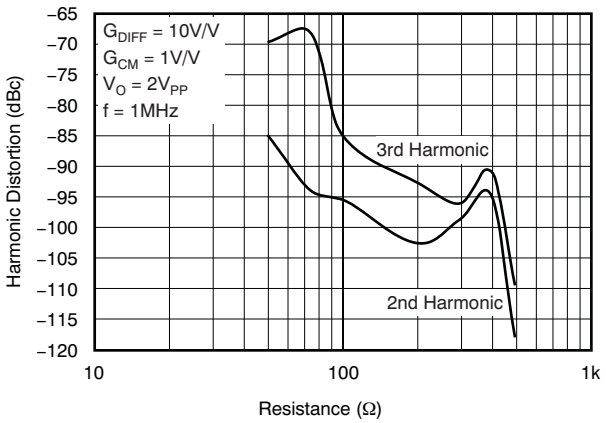


Figure 41.

HARMONIC DISTORTION vs NONINVERTING GAIN

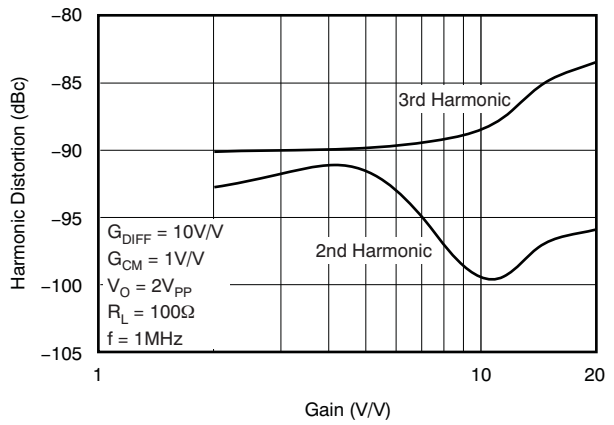


Figure 42.

2-TONE, 3RD-ORDER, INTERMODULATION INTERCEPT

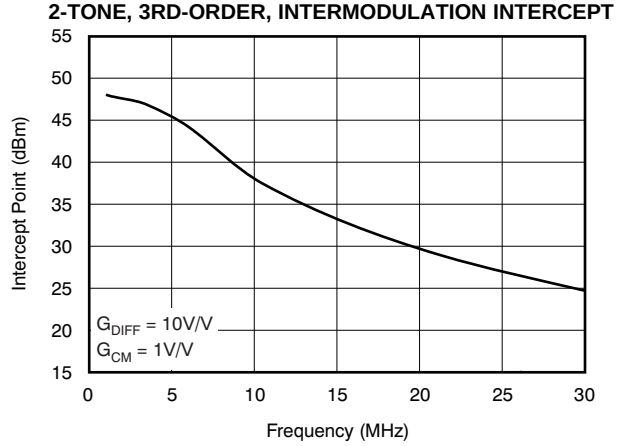


Figure 43.

TYPICAL CHARACTERISTICS: V_S = ±6V, Full Bias

At T_A = +25°C, G_{DIFF} = +5V/V, G_{CM} = 1V/V, R_{ADJ} = 0Ω, R_F = 1.82kΩ, and R_L = 100Ω, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

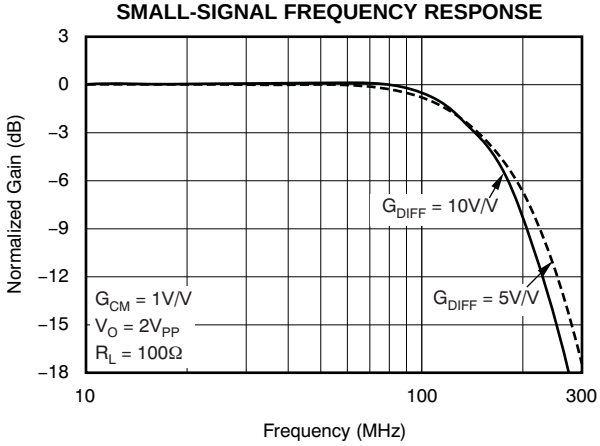


Figure 44.

FULL BIAS FREQUENCY RESPONSE

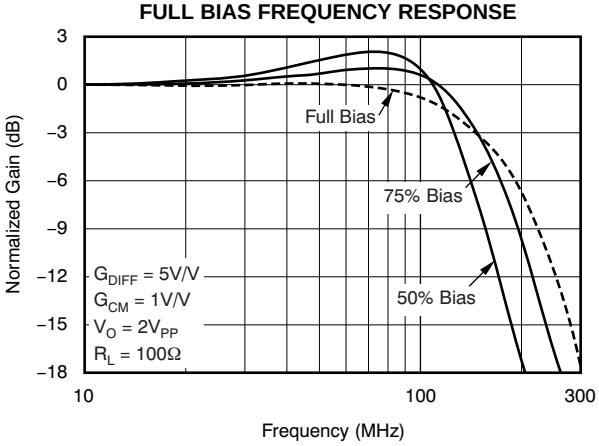


Figure 45.

LARGE-SIGNAL FREQUENCY RESPONSE

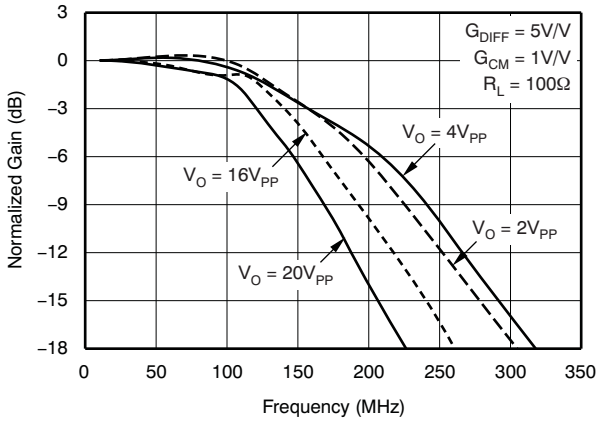


Figure 46.

SMALL-SIGNAL AND LARGE-SIGNAL PULSE RESPONSE

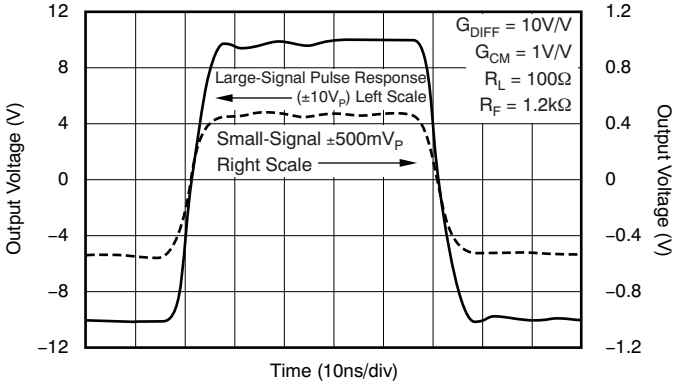


Figure 47.

DIFFERENTIAL R_S vs CAPACITIVE LOAD

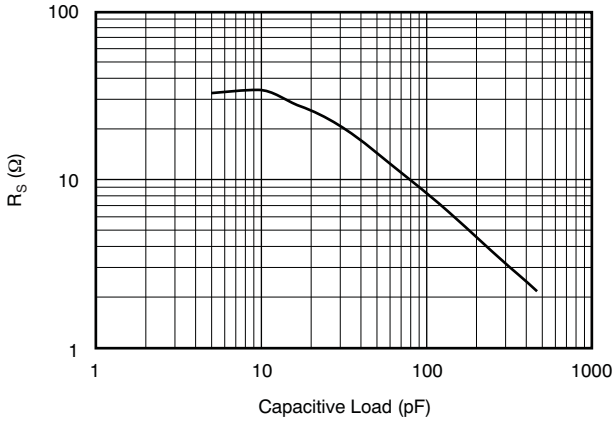


Figure 48.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

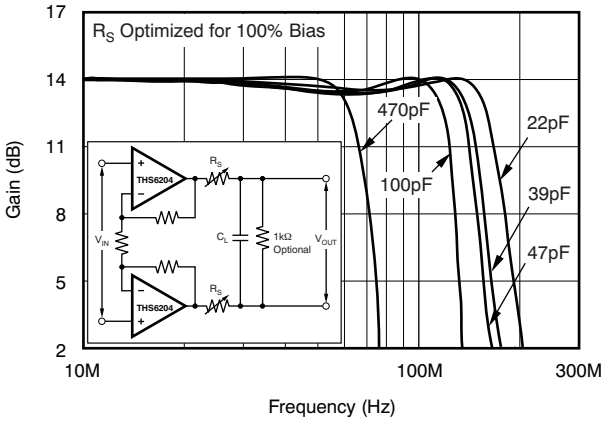


Figure 49.

TYPICAL CHARACTERISTICS: V_S = ±6V, Full Bias (continued)

At T_A = +25°C, G_{DIFF} = +5V/V, G_{CM} = 1V/V, R_{ADJ} = 0Ω, R_F = 1.82kΩ, and R_L = 100Ω, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

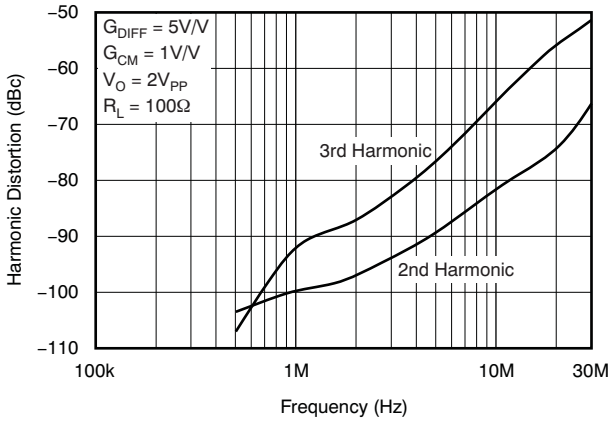


Figure 50.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

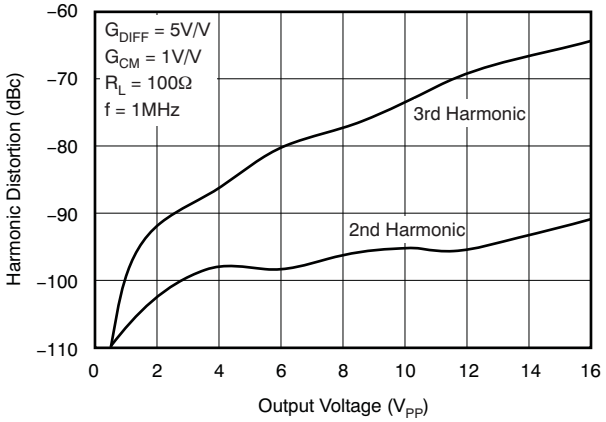


Figure 51.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

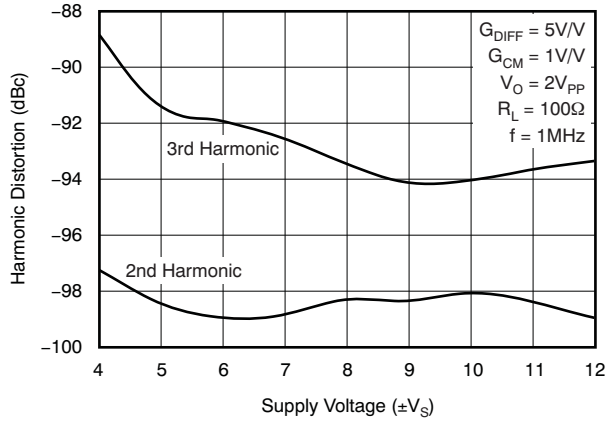


Figure 52.

HARMONIC DISTORTION vs LOAD RESISTANCE

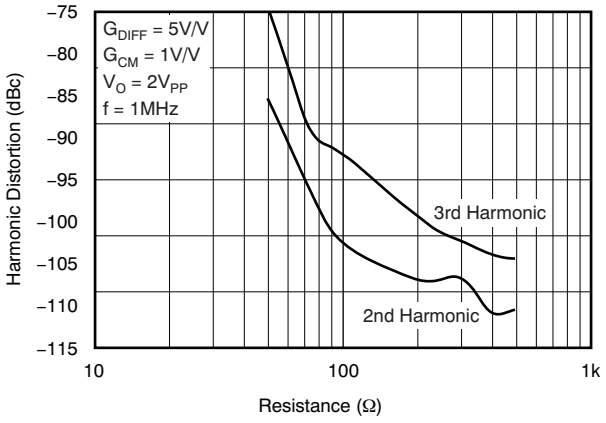


Figure 53.

HARMONIC DISTORTION vs NONINVERTING GAIN

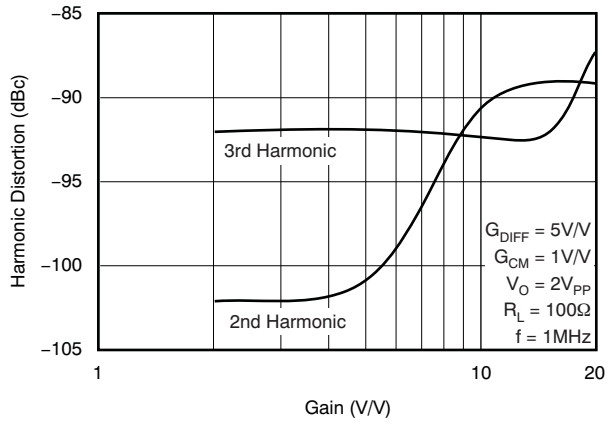


Figure 54.

2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

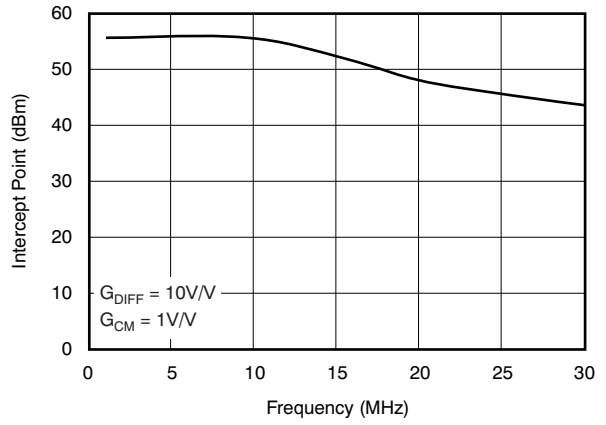


Figure 55.

TYPICAL CHARACTERISTICS: V_S = ±6V, Full Bias (continued)

At T_A = +25°C, G_{DIFF} = +5V/V, G_{CM} = 1V/V, R_{ADJ} = 0Ω, R_F = 1.82kΩ, and R_L = 100Ω, unless otherwise noted.

SUPPLY CURRENT FOR FULL BIAS SETTING vs R_{ADJ}

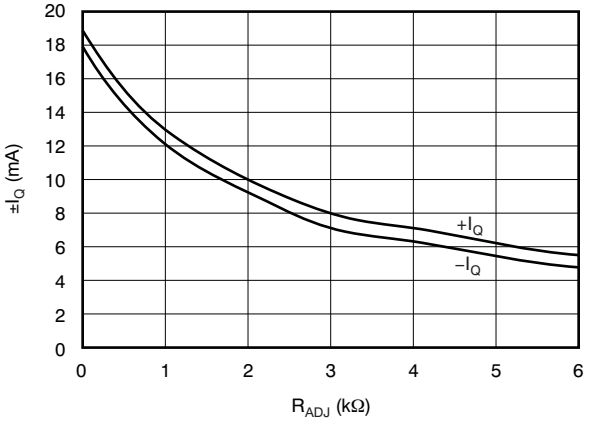


Figure 56.

TYPICAL CHARACTERISTICS: V_S = ±6V, 75% Bias

At T_A = +25°C, G_{DIFF} = +5V/V, G_{CM} = 1V/V, R_{ADJ} = 0Ω, R_F = 1.82kΩ, and R_L = 100Ω, unless otherwise noted.

75% BIAS FREQUENCY RESPONSE

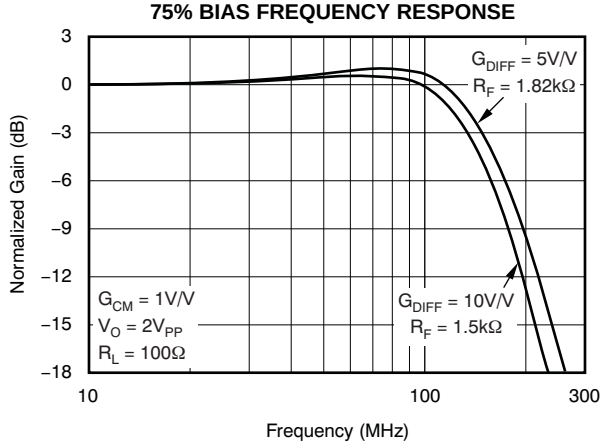


Figure 57.

LARGE-SIGNAL FREQUENCY RESPONSE

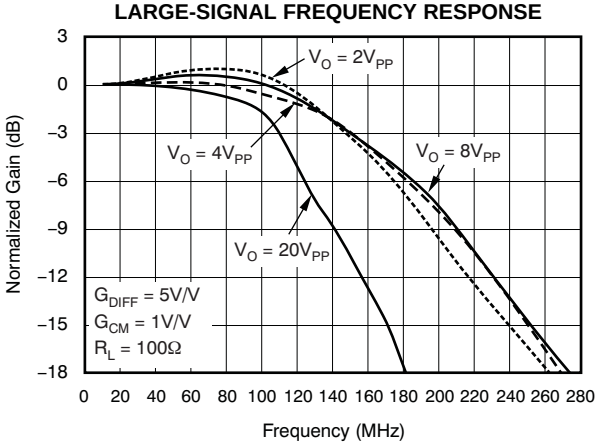


Figure 58.

DIFFERENTIAL SMALL-SIGNAL AND LARGE-SIGNAL PULSE RESPONSE

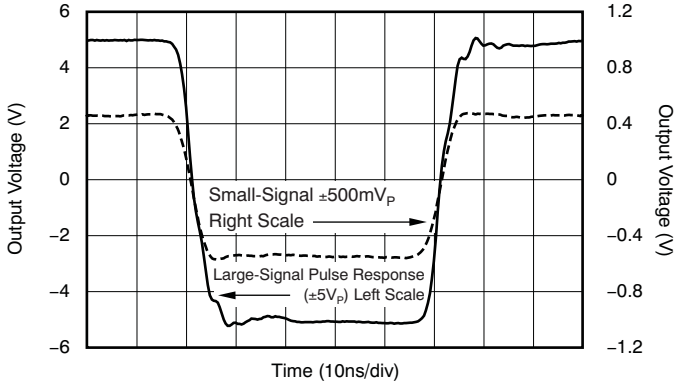


Figure 59.

SUPPLY CURRENT FOR FULL BIAS SETTING vs R_{ADJ}

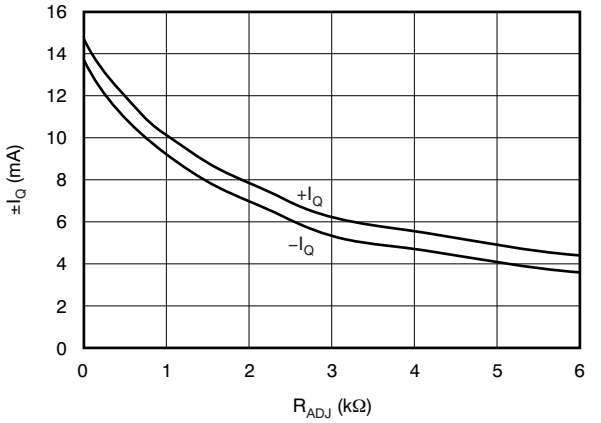


Figure 60.

DIFFERENTIAL R_S vs CAPACITIVE LOAD

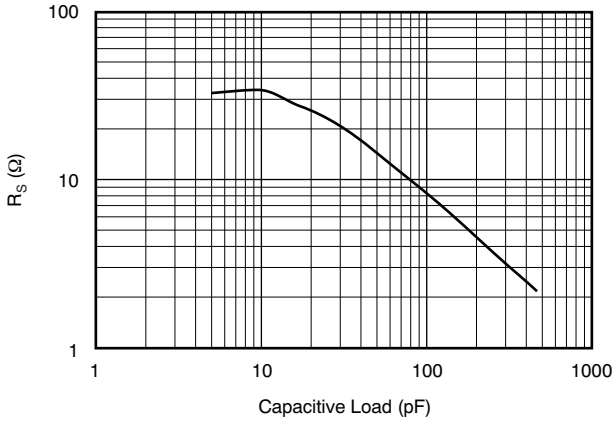


Figure 61.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

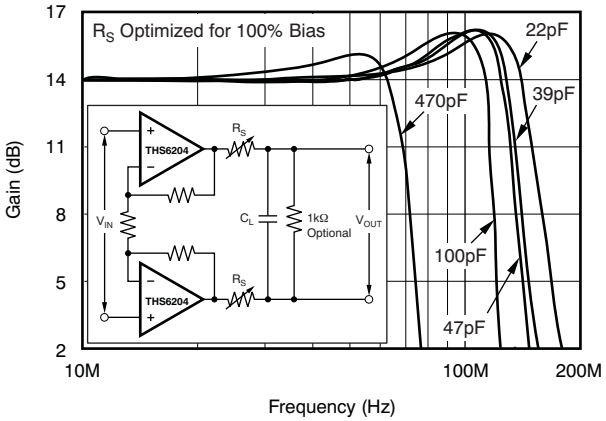


Figure 62.

TYPICAL CHARACTERISTICS: V_S = ±6V, 75% Bias (continued)

At T_A = +25°C, G_{DIFF} = +5V/V, G_{CM} = 1V/V, R_{ADJ} = 0Ω, R_F = 1.82kΩ, and R_L = 100Ω, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

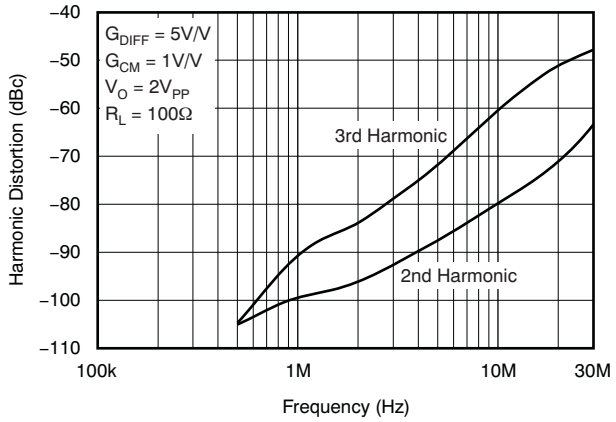


Figure 63.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

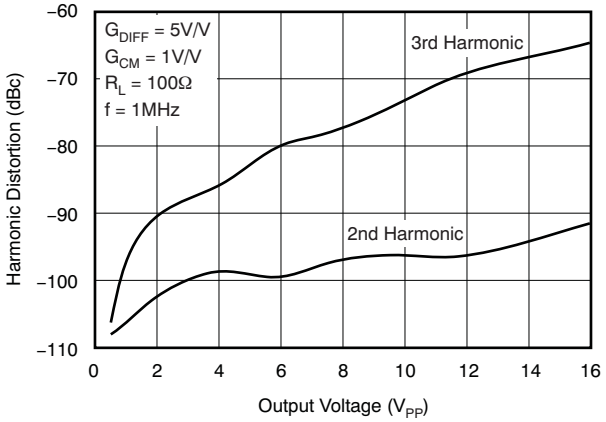


Figure 64.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

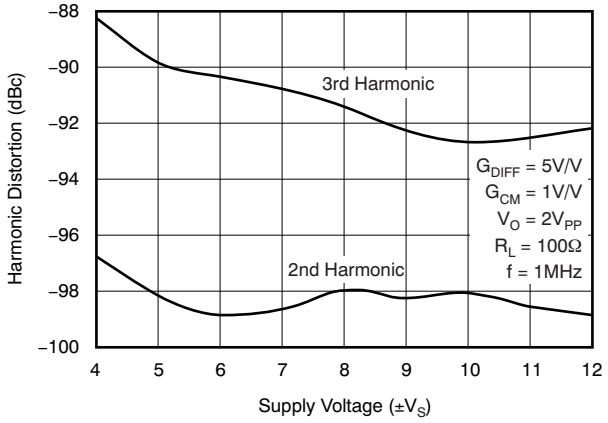


Figure 65.

HARMONIC DISTORTION vs LOAD RESISTANCE

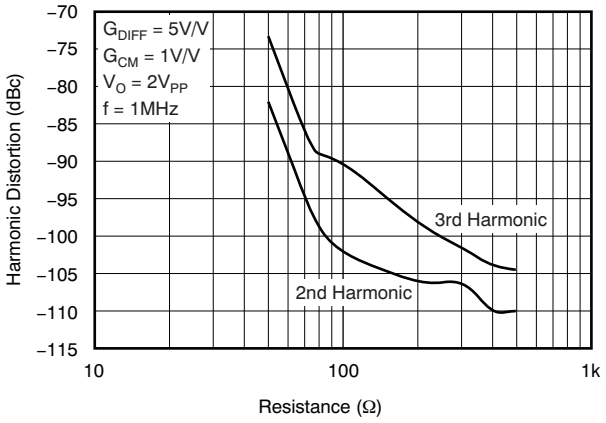


Figure 66.

HARMONIC DISTORTION vs NONINVERTING GAIN

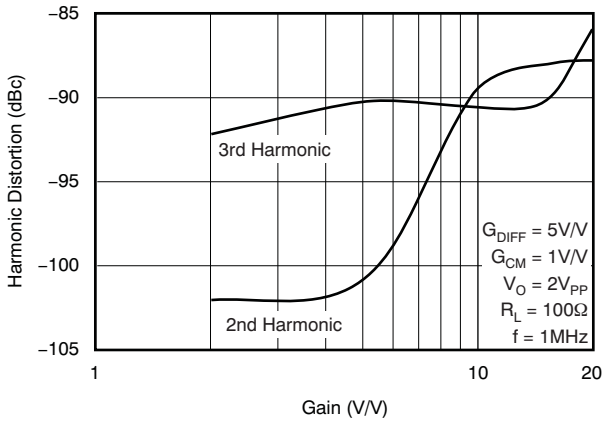


Figure 67.

2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

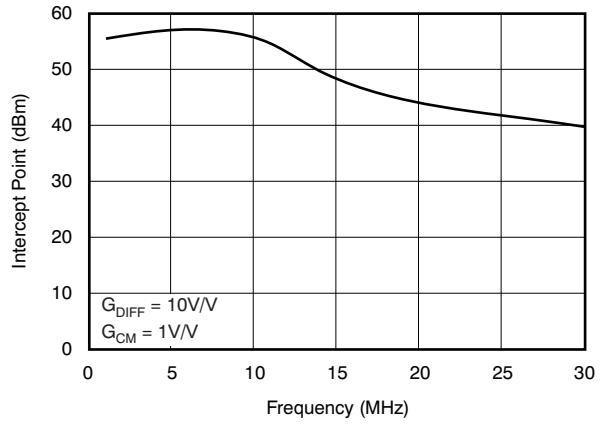


Figure 68.

TYPICAL CHARACTERISTICS: V_S = ±6V, 50% Bias

At T_A = +25°C, G_{DIFF} = +5V/V, G_{CM} = 1V/V, R_{ADJ} = 0Ω, R_F = 1.82kΩ, and R_L = 100Ω, unless otherwise noted.

50% BIAS FREQUENCY RESPONSE

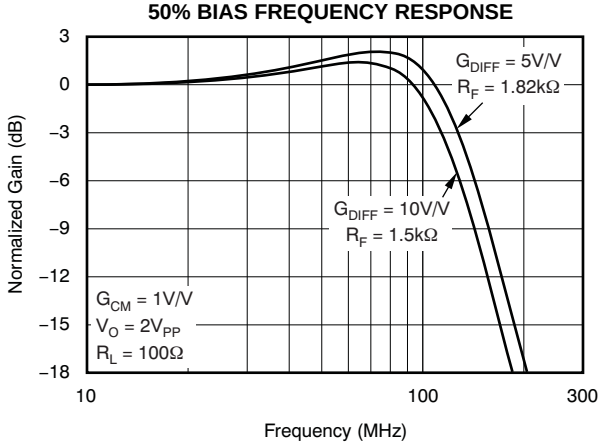


Figure 69.

LARGE-SIGNAL FREQUENCY RESPONSE

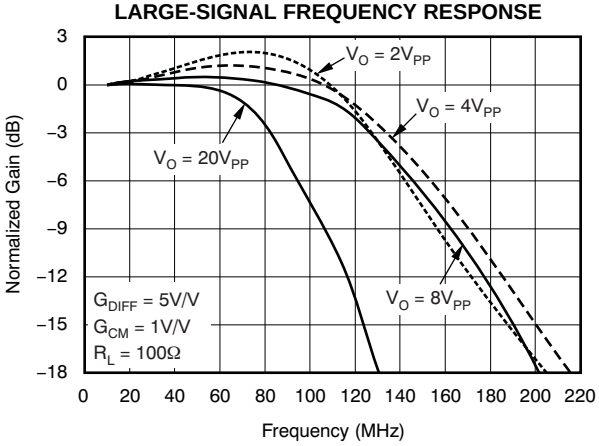


Figure 70.

DIFFERENTIAL PULSE RESPONSE

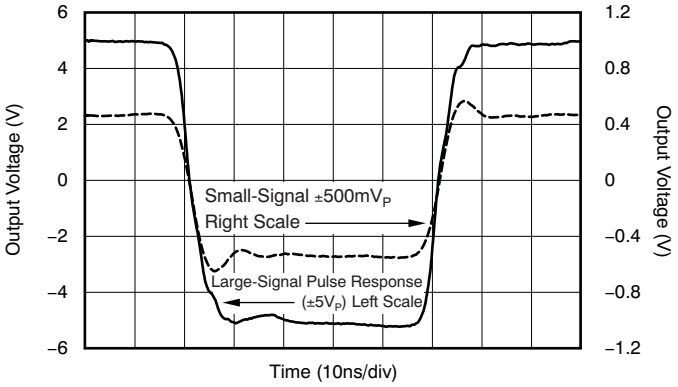


Figure 71.

SUPPLY CURRENT FPR FULL BIAS SETTING vs R_{ADJ}

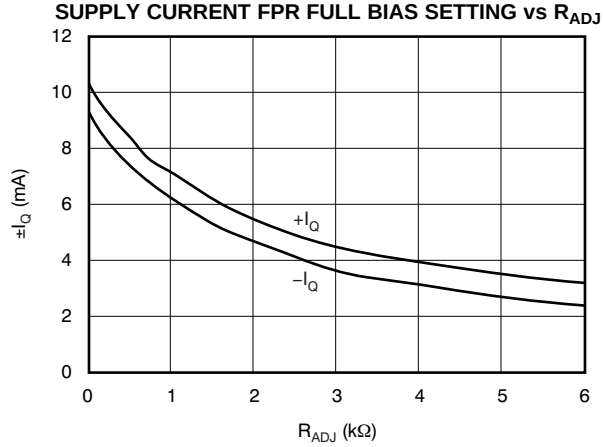


Figure 72.

DIFFERENTIAL R_S vs CAPACITIVE LOAD

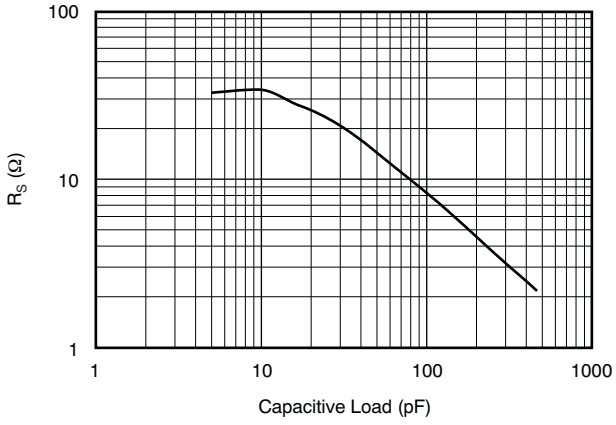


Figure 73.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

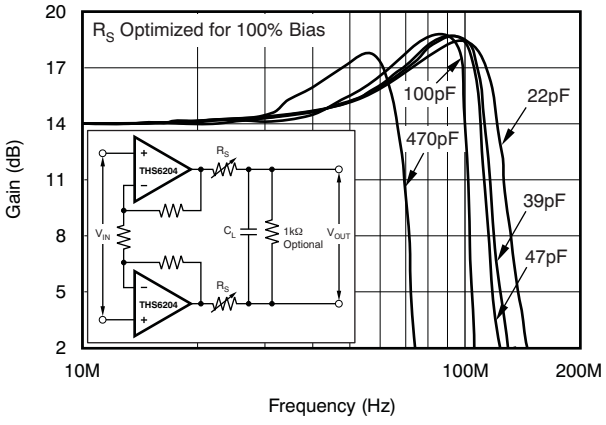


Figure 74.

TYPICAL CHARACTERISTICS: V_S = ±6V, 50% Bias (continued)

At T_A = +25°C, G_{DIFF} = +5V/V, G_{CM} = 1V/V, R_{ADJ} = 0Ω, R_F = 1.82kΩ, and R_L = 100Ω, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

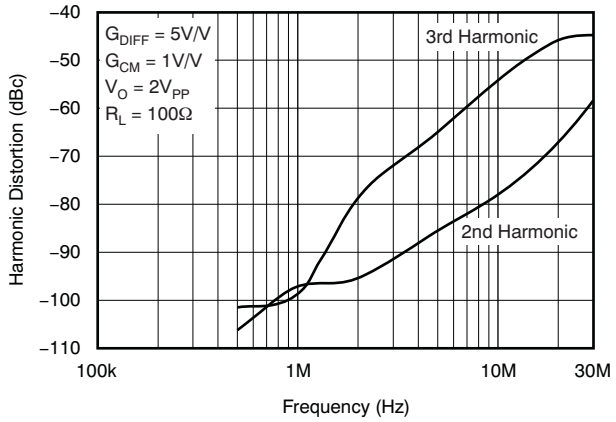


Figure 75.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

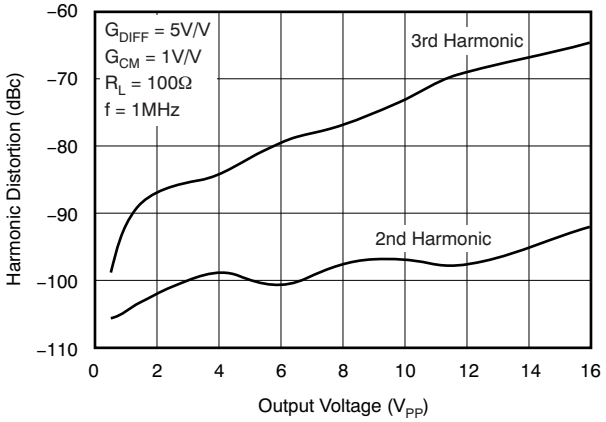


Figure 76.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

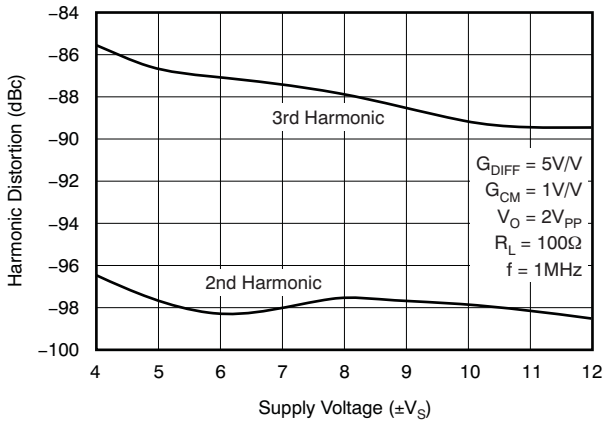


Figure 77.

HARMONIC DISTORTION vs LOAD RESISTANCE

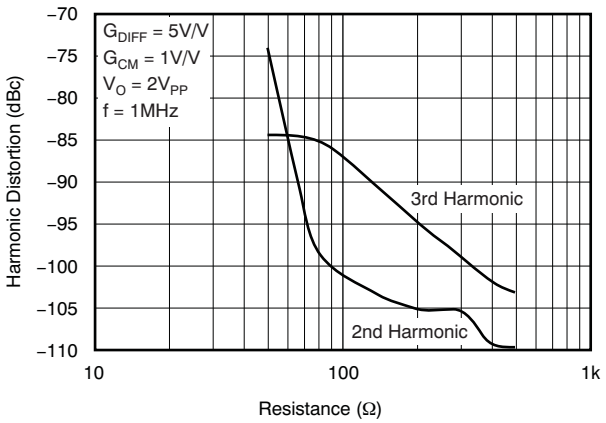


Figure 78.

HARMONIC DISTORTION vs NONINVERTING GAIN

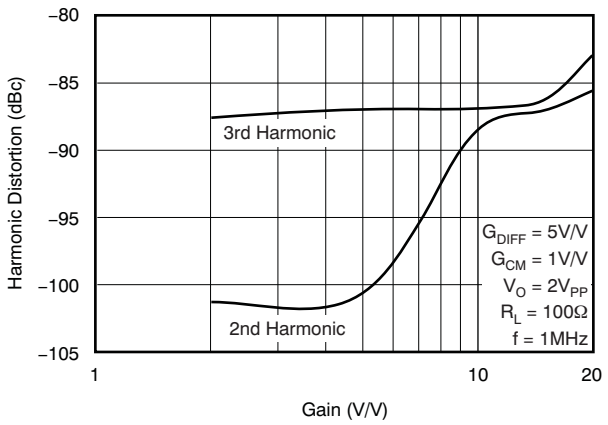


Figure 79.

2-TONE, 3RD-ODER INTERMODULATION INTERCEPT

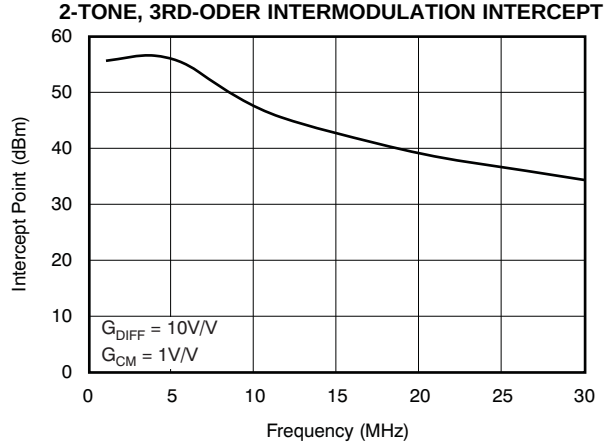


Figure 80.

APPLICATION INFORMATION

WIDEBAND CURRENT-FEEDBACK OPERATION

The THS6204 gives the exceptional ac performance of a wideband current-feedback op amp with a highly linear, high-power output stage. Requiring only 9mA/ch quiescent current, the THS6204 swings to within 1V of either supply rail and delivers in excess of 380mA at room temperature. This low-output headroom requirement, along with supply voltage independent biasing, gives remarkable ±6V supply operation. The THS6204 delivers greater than 145MHz bandwidth driving a $2V_{PP}$ output into 100Ω on a ±6V supply. Previous boosted output stage amplifiers typically suffer from very poor crossover distortion as the output current goes through zero. The THS6204 achieves a comparable power gain with much better linearity. The primary advantage of a current-feedback op amp over a voltage-feedback op amp is that ac performance (bandwidth and distortion) is relatively independent of signal gain. Figure 81 shows the dc-coupled, gain of +10V/V, dual power-supply circuit configuration used as the basis of the ±12V Electrical and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the electrical characteristics are taken directly at the input and output pins, whereas load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 81, the total effective load is 100Ω || 1.24kΩ || 1.24kΩ = 86.1Ω.

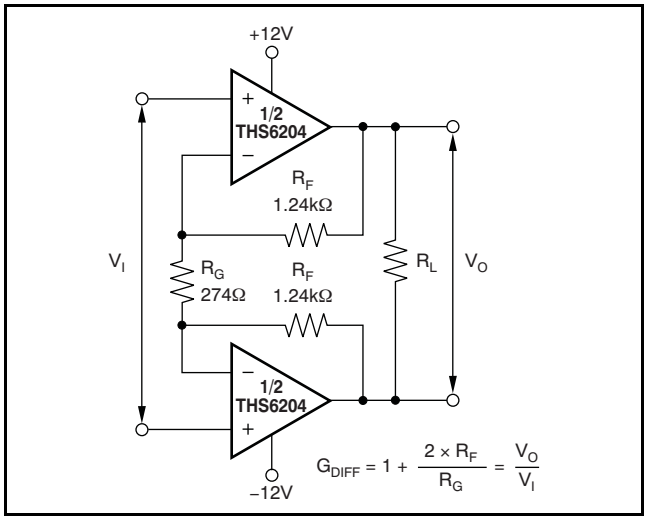


Figure 81. Noninverting Differential I/O Amplifier

This approach provides for a source termination impedance at the input that is independent of the signal gain. For instance, simple differential filters may be included in the signal path right up to the noninverting inputs without interacting with the gain setting. The differential signal gain for the circuit of Figure 81 is:

$$A_D = 1 + 2 \times \frac{R_F}{R_G} \quad (1)$$

Because the THS6204 is a current feedback (CFB) amplifier, its bandwidth is primarily controlled with the feedback resistor value; Figure 81 shows a value of 274Ω for the A_D = +10V/V design. The differential gain, however, may be adjusted with considerable freedom using just the R_G resistor. In fact, R_G may be a reactive network providing a very isolated shaping to the differential frequency response.

Various combinations of single-supply or ac-coupled gain can also be delivered using the basic circuit of Figure 81. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of +1V/V since an equal dc voltage at each inverting node creates no current through R_G. This circuit does show a common-mode gain of +1V/V from input to output. The source connection should either remove this common-mode signal if undesired (using an input transformer can provide this function), or the common-mode voltage at the inputs can be used to set the output common-mode bias. If the low common-mode rejection of this circuit is a problem, the output interface may also be used to reject that common-mode. For instance, most modern differential input ADCs reject common-mode signals very well, while a line driver application through a transformer will also attenuate the common-mode signal through to the line.

DUAL-SUPPLY VDSL DOWNSTREAM

Figure 82 shows an example of a dual-supply VDSL downstream driver. Both channels of the THS6204 are configured as a differential gain stage to provide signal drive to the primary winding of the transformer (here, a step-up transformer with a turns ratio of 1:1.1). The main advantage of this configuration is the cancellation of all even harmonic distortion products. Another important advantage for VDSL is that each amplifier needs only to swing half of the total output required driving the load.

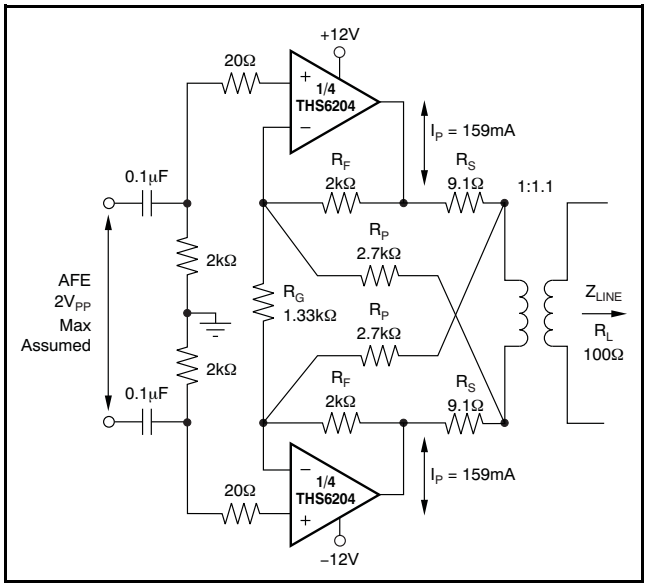


Figure 82. Dual-Supply VDSL Downstream Driver

The analog front end (AFE) signal is ac-coupled to the driver, and the noninverting input of each amplifier is biased to the mid-supply voltage (ground in this case). In addition to providing the proper biasing to the amplifier, this approach also provides a high-pass filtering with a corner frequency, set here at 5kHz. As the signal bandwidth starts at 26kHz, this high-pass filter does not generate any problem and has the advantage of filtering out unwanted lower frequencies.

The input signal is amplified with a gain set by the following equation:

$$G_D = 1 + \frac{2 \times R_F}{R_G} \quad (2)$$

With R_F = 2kΩ and R_G = 1.33kΩ, the gain for this differential amplifier is R_P = 2.1kΩ. This gain boosts the AFE signal, assumed to be a maximum of $2V_{PP}$, to a maximum of $3V_{PP}$.

The two back-termination resistors (9.1Ω each) added at each terminal of the transformer make the impedance of the modem match the impedance of the phone line, and also provide a means of detecting the received signal for the receiver. The value of these resistors (R_M) is a function of the line impedance and the transformer turns ratio (n), given by the following equation:

$$R_M = \frac{Z_{LINE}}{2n^2} \quad (3)$$

LINE DRIVER HEADROOM MODEL

The first step in a transformer-coupled, twisted-pair driver design is to compute the peak-to-peak output voltage from the target specifications. This is done using the following equations:

$$P_L = 10 \times \log \frac{V_{RMS}^2}{(1mW) \times R_L} \quad (4)$$

with P_L power at the load, V_{RMS} voltage at the load, and R_L load impedance; this gives the following:

$$V_{RMS} = \sqrt{(1mW) \times R_L \times 10^{\frac{P_L}{10}}} \quad (5)$$

$$V_P = \text{CrestFactor} \times V_{RMS} = CF \times V_{RMS} \quad (6)$$

with V_P peak voltage at the load and CF Crest Factor.

$$V_{LPP} = 2 \times CF \times V_{RMS} \quad (7)$$

with V_{LPP}: peak-to-peak voltage at the load.

Consolidating Equation 4 through Equation 7 allows expressing the required peak-to-peak voltage at the load as a function of the crest factor, the load impedance, and the power at the load. Thus,

$$V_{LPP} = 2 \times CF \times \sqrt{(1mW) \times R_L \times 10^{\frac{P_L}{10}}} \quad (8)$$

This V_{LPP} is usually computed for a nominal line impedance and may be taken as a fixed design target.

The next step in the design is to compute the individual amplifier output voltage and currents as a function of V_{PP} on the line and transformer turns ratio. As this turns ratio changes, the minimum allowed supply voltage changes along with it. The peak current in the amplifier output is given by:

$$\pm I_P = \frac{1}{2} \times \frac{2 \times V_{LPP}}{n} \times \frac{1}{4R_M} \quad (9)$$

with V_{PP} as defined in Equation 8, and R_M as defined in Equation 3 and shown in Figure 83.

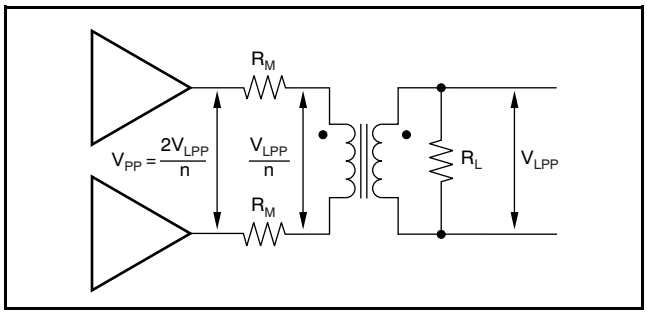


Figure 83. Driver Peak Output Voltage

With the previous information available, it is now possible to select a supply voltage and the turns ratio desired for the transformer as well as calculate the headroom for the THS6204.

The model, shown in Figure 84, can be described with the following set of equations:

1. As available output swing:

$$V_{PP} = V_{CC} - (V_1 + V_2) - I_P \times (R_1 + R_2) \quad (10)$$

2. Or as required supply voltage:

$$V_{CC} = V_{PP} + (V_1 + V_2) + I_P \times (R_1 + R_2) \quad (11)$$

The minimum supply voltage for a power and load requirement is given by Equation 11.

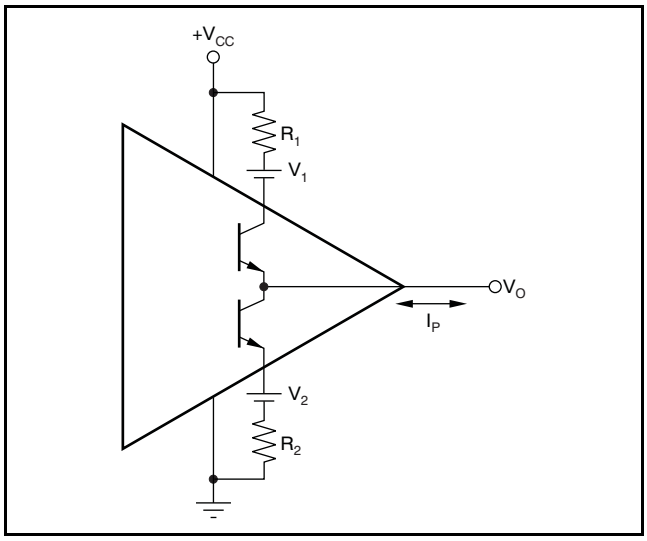


Figure 84. Line Driver Headroom Model

V_1, V_2, R_1, and R_2 are given in Table 3 for ±12V operation.

Table 3. Line Driver Headroom Model Values

	V_1	R_1	V_2	R_2
±12V	1V	0.6V	1V	1.2V

When using a synthetic output impedance circuit, such as the one shown in Figure 82, a significant drop is noticed in bandwidth from the bandwidth appearing in the Electrical Characteristics tables. This apparent drop in bandwidth for the differential signal is a result of the apparent increase in the feedback transimpedance as seen for each amplifier. This feedback transimpedance equation is given below.

$$Z_{FB} = R_F \times \frac{1 + 2 \times \frac{R_S}{R_L} + \frac{R_S}{R_P}}{1 + 2 \times \frac{R_S}{R_L} + \frac{R_S}{R_P} - \frac{R_F}{R_P}} \quad (12)$$

To increase 0.1dB flatness to the frequency of interest, adding a serial R-C in parallel with the gain resistor may be needed, as shown in Figure 85.

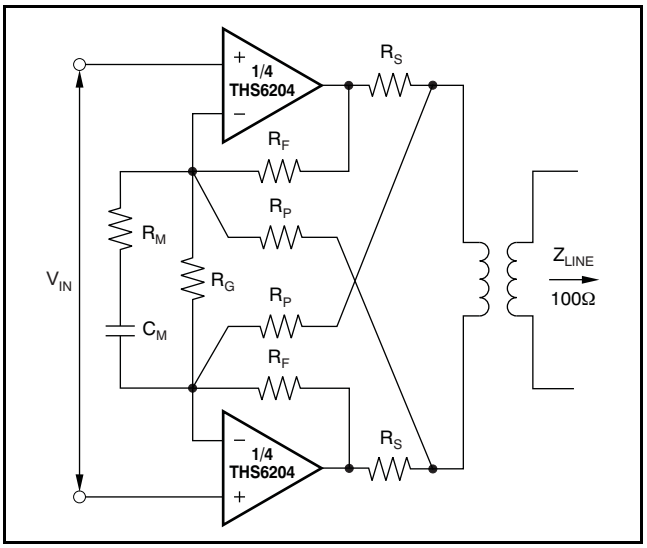


Figure 85. 0.1dB Flatness Compensation Circuit

TOTAL DRIVER POWER FOR xDSL APPLICATIONS

The total internal power dissipation for the THS6204 in an xDSL line driver application will be the sum of the quiescent power and the output stage power. The THS6204 holds a relatively constant quiescent current versus supply voltage—giving a power contribution that is simply the quiescent current times the supply voltage used (the supply voltage will be greater than the solution given in Equation 11). The total output stage power may be computed with reference to Figure 86.

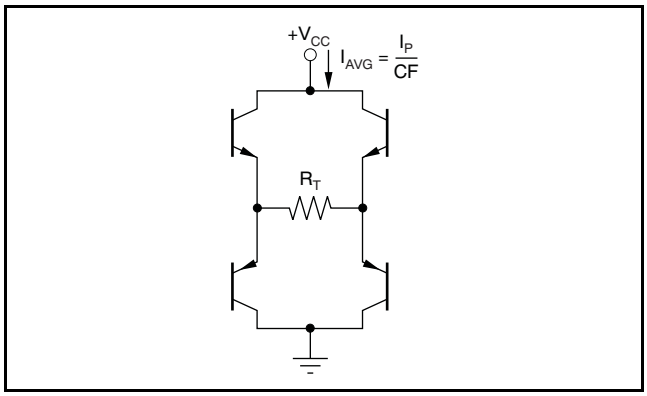


Figure 86. Output Stage Power Model

The two output stages used to drive the load of Figure 83 can be seen as an H-Bridge in Figure 86. The average current drawn from the supply into this H-Bridge and load will be the peak current in the load given by Equation 9 divided by the crest factor (CF) for the xDSL modulation. This total power from the supply is then reduced by the power in R_T to leave the power dissipated internal to the drivers in the four output stage transistors. That power is simply the target line power used in Equation 4 plus the power lost in the matching elements (R_M). In the examples here, a perfect match is targeted giving the same power in the matching elements as in the load. The output stage power is then set by Equation 12.

$$P_{OUT} = \frac{I_P}{CF} \times V_{CC} - 2P_L \quad (13)$$

The total amplifier power is then:

$$P_{TOT} = I_Q \times V_{CC} + \frac{I_P}{CF} \times V_{CC} - 2P_L \quad (14)$$

For the ADSL CO driver design of Figure 82, the peak current is 159mA for a signal that requires a crest factor of 5.6 with a target line power of 20.5dBm into 100Ω (115mW). With a typical quiescent current of 21mA and a nominal supply voltage of ±12V, the total internal power dissipation for the solution of Figure 82 will be:

$$P_{TOT} = 21mA\ (24V) + \frac{159mA}{5.6}\ (24V) - 2(115mW) = 955mW \quad (15)$$

OUTPUT CURRENT AND VOLTAGE

The THS6204 provides output voltage and current capabilities that are unsurpassed in a low-cost dual monolithic op amp. Under no-load conditions at +25°C, the output voltage typically swings closer than 1.1V to either supply rail; tested at +25°C swing limit is within 1.4V of either rail into a 100Ω differential load. Into a 25Ω load (the minimum tested load), it delivers more than ±408mA continuous and > ±1A peak output current.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage times current (or V-I product) that is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot (Figure 14) in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the THS6204 output drive capabilities, noting that the graph is bounded by a safe operating area of 1W maximum internal power dissipation (in this case for 1 channel only). Superimposing resistor load lines onto the plot shows that the THS6204 can drive ±10.9V into 100Ω or ±10.5V into 50Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±12V output swing capability, as shown in the Electrical Characteristics tables. The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the Electrical Characteristics tables. As the output transistors deliver power, the junction temperatures increases, decreasing the V_{BE}s (increasing the available output voltage swing), and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications, since the output stage junction temperatures will be higher than the minimum specified operating ambient. To maintain maximum output stage linearity, no output short-circuit protection is provided. This is normally not a problem because most applications include a series-matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin (24-pin package), will in most cases, destroy the amplifier. If additional short-circuit protection is required, a small

series resistor may be included in the supply lines. Under heavy output loads this will reduce the available output voltage swing. A 5Ω series resistor in each power-supply lead will limit the internal power dissipation to less than 1W for an output short circuit while decreasing the available output voltage swing only 0.5V for up to 100mA desired load currents. Always place the 0.1μF power-supply decoupling capacitors after these supply current limiting resistors directly on the supply pins.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance that may be recommended to improve the ADC linearity. A high-speed, high open-loop gain amplifier such as the THS6204 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested.

When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability. The Typical Characteristics show the recommended R_S vs Capacitive Load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the THS6204. Long printed-circuit board (PCB) traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the THS6204 output pin (see the *Board Layout Guidelines* section).

DISTORTION PERFORMANCE

The THS6204 provides good distortion performance into a 100Ω load on ±12V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operation on a dual ±6V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the second harmonic dominates the distortion with a negligible third harmonic component. Focusing then on the second harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 81), this is the sum of R_F + R_G, whereas in the inverting configuration it is just R_F. Also, providing an additional supply decoupling capacitor (0.01μF) between the supply pins (for bipolar operation) improves the second-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The Typical Characteristics show the second harmonic increasing at a little less than the expected 2x rate whereas the third harmonic increases at a little less than the expected 3x rate. Where the test power doubles, the difference between it and the second harmonic decreases less than the expected 6dB, whereas the difference between it and the third harmonic decreases by less than the expected 12dB. This also shows up in the two-tone, third-order intermodulation spurious (IM3) response curves. The third-order spurious levels are extremely low at low-output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly.

DIFFERENTIAL NOISE PERFORMANCE

As the THS6204 is used as a differential driver in xDSL applications, it is important to analyze the noise in such a configuration. Figure 87 shows the op amp noise model for the differential configuration.

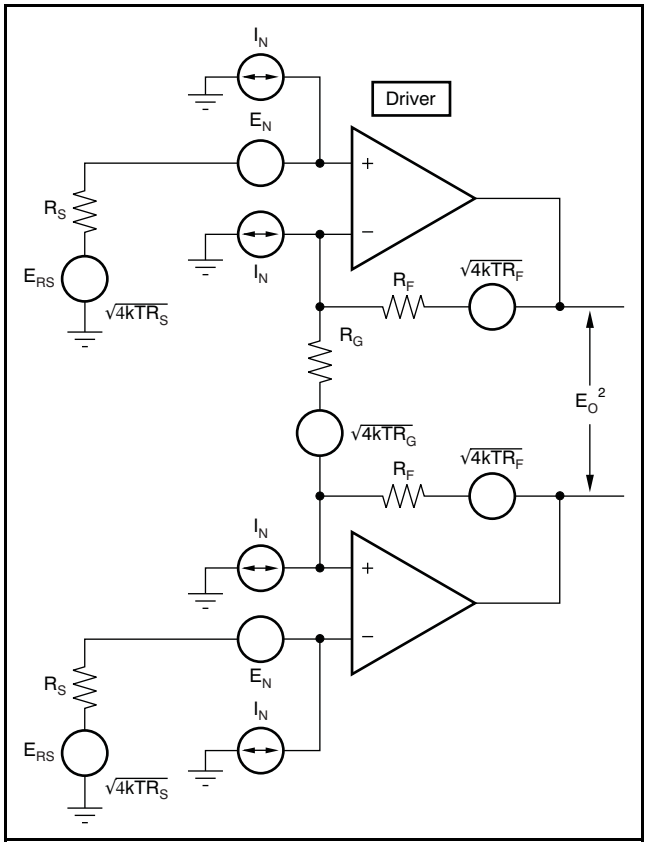


Figure 87. Differential Op Amp Noise Analysis Model

As a reminder, the differential gain is expressed as:

$$G_D = 1 + \frac{2 \times R_F}{R_G} \quad (16)$$

The output noise can be expressed as shown below:

$$E_O = \sqrt{2 \times G_D^2 \times \left[e_N^2 + (i_N \times R_S)^2 + 4kTR_S \right] + 2(i_I R_F)^2 + 2(4kTR_F G_D)} \quad (17)$$

Dividing this expression by the differential noise gain (G_D = (1 + $2R_F/R_G$)) gives the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 18.

$$E_O = \sqrt{2 \times \left[e_N^2 + (i_N \times R_S)^2 + 4kTR_S \right] + 2\left[\frac{i_I R_F}{G_D} \right]^2 + 2\left[\frac{4kTR_F}{G_D} \right]} \quad (18)$$

Evaluating these equations for the THS6204 ADSL circuit and component values of Figure 82 gives a total output spot noise voltage of 38.9nV/√Hz and a total equivalent input spot noise voltage of 7nV/√Hz.

In order to minimize the output noise due to the noninverting input bias current noise, it is recommended to keep the noninverting source impedance as low as possible.

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp such as the THS6204 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate dc accuracy. The Electrical Characteristics show an input offset voltage comparable to high-speed, voltage-feedback amplifiers; however, the two input bias currents are somewhat higher and are unmatched. While bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output dc offset for wideband current-feedback op amps. Because the two input bias currents are unrelated in both magnitude and polarity, matching the input source impedance to reduce error contribution to the output is ineffective. Evaluating the configuration of Figure 81, using worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

V_{OFF} = ± (NG × $V_{OS(MAX)}$) + (I_{BN} × R_S/2 × NG) ± (I_{BI} × R_F)

where NG = noninverting signal gain

= ± (10 × 5mV) + (3µA × 25Ω × 10) ± (1.24kΩ × 40µA)

= ±50mV + 0.75mV ± 49.6mV

V_{OFF} = –98.85mV to +100.35mV

POWER CONTROL OPERATION

The THS6204 provides a power control feature that may be used to reduce system power. The four modes of operation for this power control feature are full-power, power cutback, idle state, and power shutdown. These four operating modes are set through two logic lines A0 and A1. Table 4 shows the different modes of operation.

Table 4. Power Control Mode of Operation

MODE OF OPERATION	BIAS 1	BIAS 2
Full bias mode	0	0
Mid bias mode	1	0
Low bias mode	0	1
Shutdown	1	1

The full-power mode is used for normal operating condition. The power cutback mode brings the quiescent power to 13.5mA. The idle state mode keeps a low output impedance but reduces output power and bandwidth. The shutdown mode has a high output impedance as well as the lowest quiescent power (0.5mA).

If the Bias 1 and Bias 2 pins are left unconnected, the THS6204 shuts down.

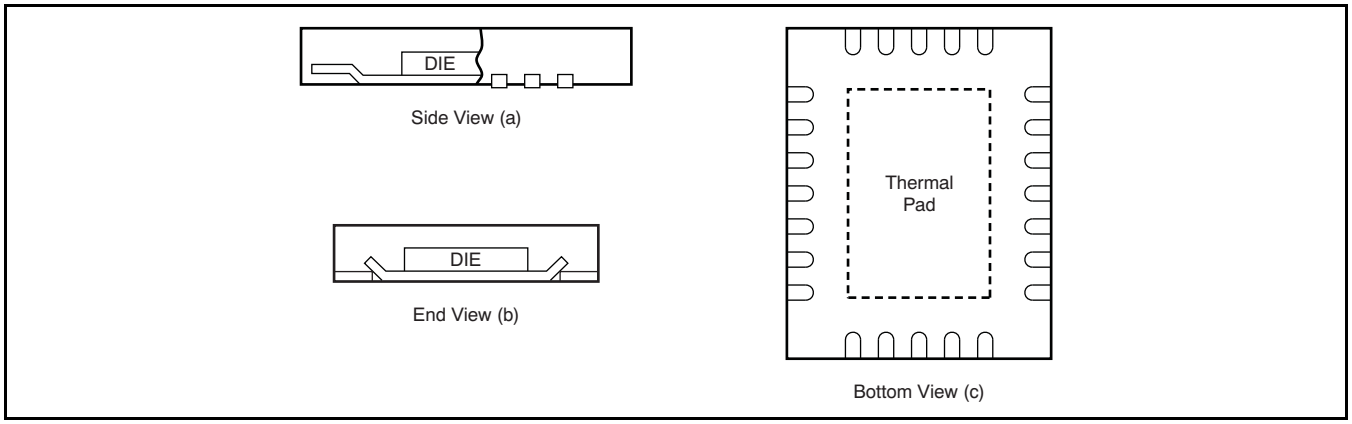
DEVICE PROTECTION FEATURE

The THS6204 has a built-in thermal protection feature. Should the internal junction temperature rise above approximately +160°C, the device automatically shuts down. Such a condition could exist with improper heat sinking or if the output is shorted to ground. When the abnormal condition is fixed, the internal thermal shutdown circuit automatically turns the device back on. This occurs at approximately +145°C, junction temperature. Note that the THS6204 does not have short-circuit protection and care should be taken to minimize the output current below the absolute maximum ratings.

THERMAL INFORMATION

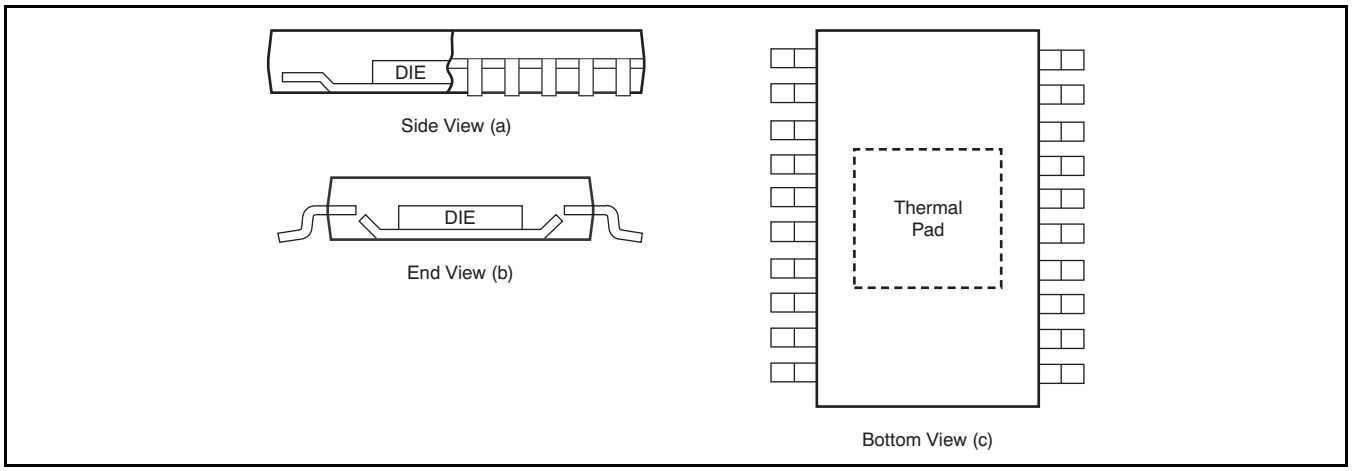
The THS6204 is available in thermally-enhanced RHF and PWP packages, which are members of the PowerPAD family of packages. These packages are constructed using leadframes upon which the dies are mounted (see Figure 88 for the RHF package and Figure 89 for the PWP package). This arrangement results in the lead frames being exposed as thermal pads on the underside of their respective packages. Because a thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad. Note that the PowerPAD is electronically isolated from the active circuitry and any pins. Thus, the PowerPAD can be connected to any potential voltage within the absolute maximum voltage range. Ideally, connection of the PAD to the most negative supply plane is preferred.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. This is discussed in more detail in the PCB design considerations section of this document.



(1) The thermal pad is electrically isolated from all terminals in the package.

Figure 88. Views of Thermally-Enhanced RHF Package (Representative Only—Not to Scale)



(1) The thermal pad is electrically isolated from all terminals in the package.

Figure 89. Views of Thermally-Enhanced PWP Package (Representative Only—Not to Scale)

THERMAL ANALYSIS

Due to the high output power capability of the THS6204, heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature sets the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +130°C. Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipation in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. A P_{DL} depends on the required output signal and load; using the previously developed model described in the *Total Driver Power for xDSL Applications* section, compute the maximum T_J using a THS6204 QFN-24 in the circuit of Figure 81 operating at the maximum specified ambient temperature of +85°C.

$$\text{Maximum } T_J = +85°C + (0.955 \times 32°C/W) = 115.5°C \quad (19)$$

Although this is still well below the specified maximum junction temperature, system reliability considerations may require lower tested junction temperatures. The highest possible internal dissipation will occur if the load requires current to be forced into the output for positive output voltages or sourced from the output for negative output voltages. This puts a high current through a large internal voltage drop in the output transistors. The output V-I plot shown in the Typical Characteristics includes a boundary for 1W maximum internal power dissipation under these conditions.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the THS6204 requires careful attention to board layout parasitic and external component types. Recommendations that optimize performance include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves second-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These can be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components preserve the high-frequency performance of the THS6204. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high-frequency performance.

Again, keep leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Although the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value as described previously. Increasing the value reduces the bandwidth, whereas decreasing it gives a more peaked frequency response. The 1.24kΩ feedback resistor used in the Typical Characteristics at a gain of +10V/V on ±12V supplies is a good starting point for design. Note that a 1.5kΩ feedback resistor, rather than a direct short, is recommended for the unity-gain follower application. A current-feedback op amp requires a feedback resistor even in the unity-gain follower configuration to control stability.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs Capacitive Load* (Figure 6, Figure 24, and Figure 36). Low parasitic capacitive loads (< 5pF) may not need an R_S because the THS6204 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board; in fact, a higher impedance environment improves distortion (see the distortion versus load plots). With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS6204 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device.

This total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the THS6204 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only.

Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of *R_S vs Capacitive Load* (Figure 6, Figure 24, and Figure 36). However, this does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the THS6204 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS6204 directly onto the board.

f) Use the $-V_S$ plane to conduct heat out of the QFN-24 and TSSOP-24 PowerPAD packages. These packages attach the die directly to an exposed thermal pad on the bottom, which should be soldered to the board. This pad must be connected electrically to the same voltage plane as the most negative supply applied to the THS6204 (in Figure 82, this would be –12V).

INPUT AND ESD PROTECTION

The THS6204 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices and are reflected in the absolute maximum ratings table. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 90.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the THS6204), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, since high values degrade both noise performance and frequency response.

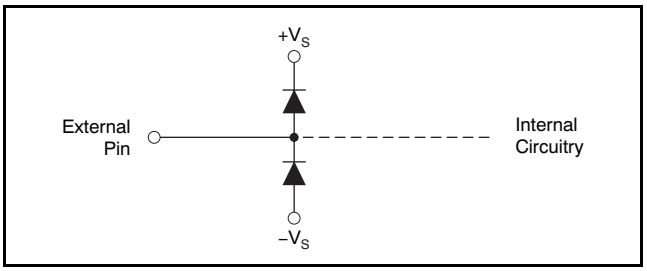


Figure 90. Internal ESD Protection

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2008) to Revision C **Page**

- Added TSSOP package operating junction temperature row to Absolute Maximum Ratings table 2
- Added TSSOP package operating junction temperature row to Recommended Operating Conditions table 3
- Changed footnote 2 of *Pin Configurations* 3
- Updated Figure 13 11
- Updated Figure 14 12
- Updated Figure 18 12
- Updated Figure 31 14
- Updated Figure 43 16
- Updated Figure 55 18
- Updated Figure 68 21
- Updated Figure 80 23

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS6204IPWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS6204	Samples
THS6204IRHFR	ACTIVE	VQFN	RHF	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS6204	Samples
THS6204IRHFT	ACTIVE	VQFN	RHF	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS6204	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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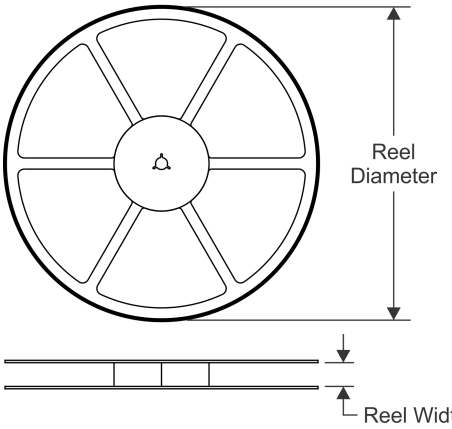
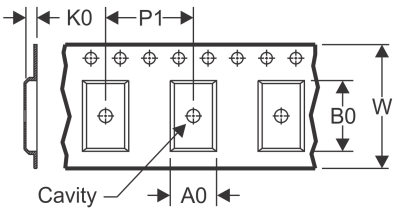
TAPE AND REEL INFORMATION

REEL DIMENSIONS

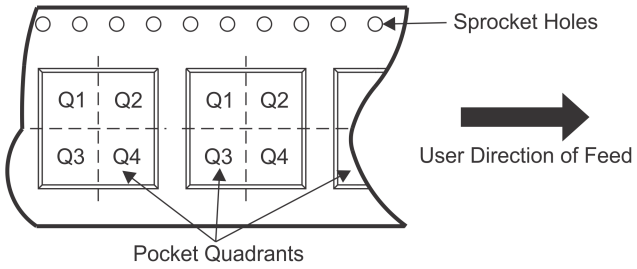


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

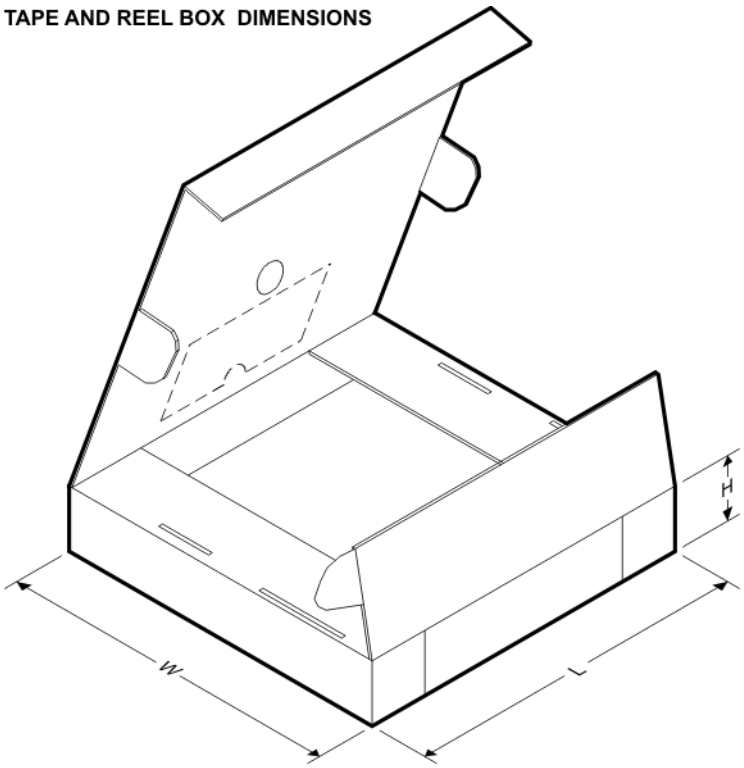
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6204IRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
THS6204IRHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6204IRHFR	VQFN	RHF	24	3000	367.0	367.0	35.0
THS6204IRHFT	VQFN	RHF	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

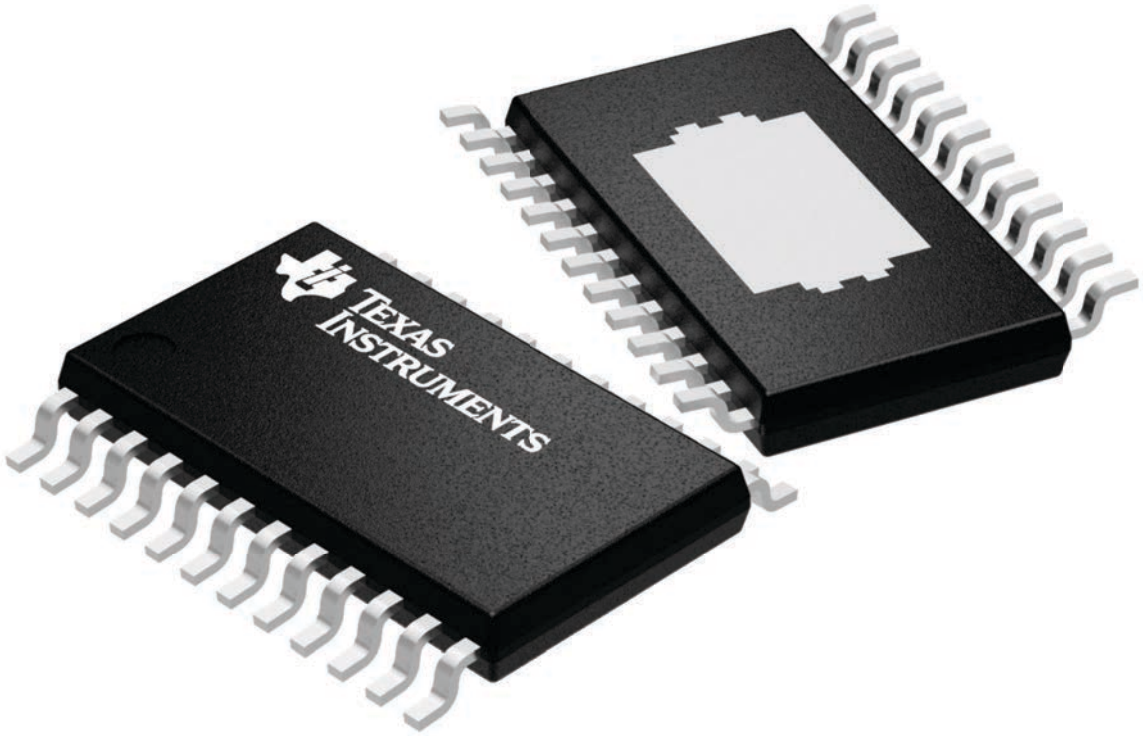
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



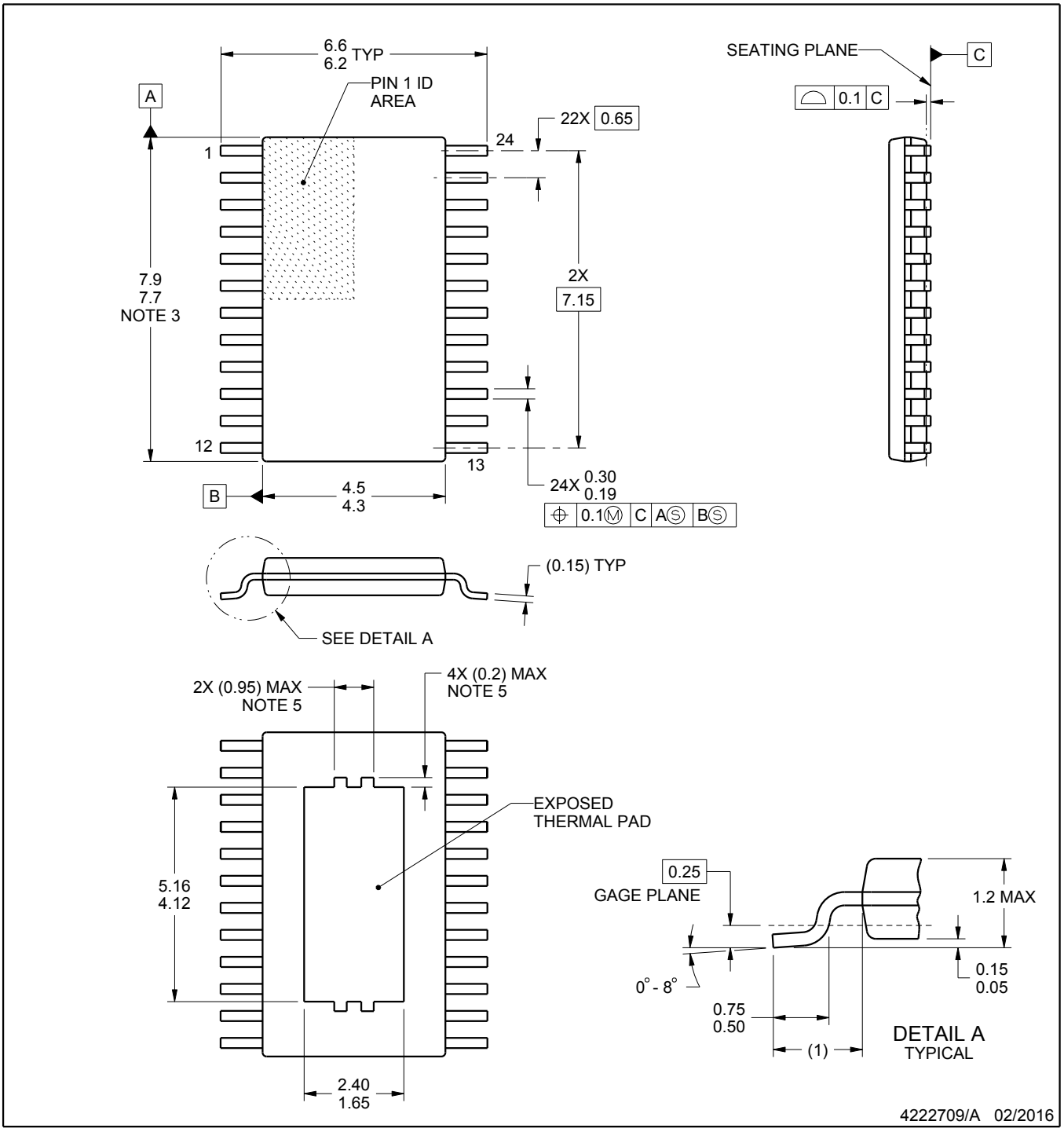
4224742/B

PACKAGE OUTLINE

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

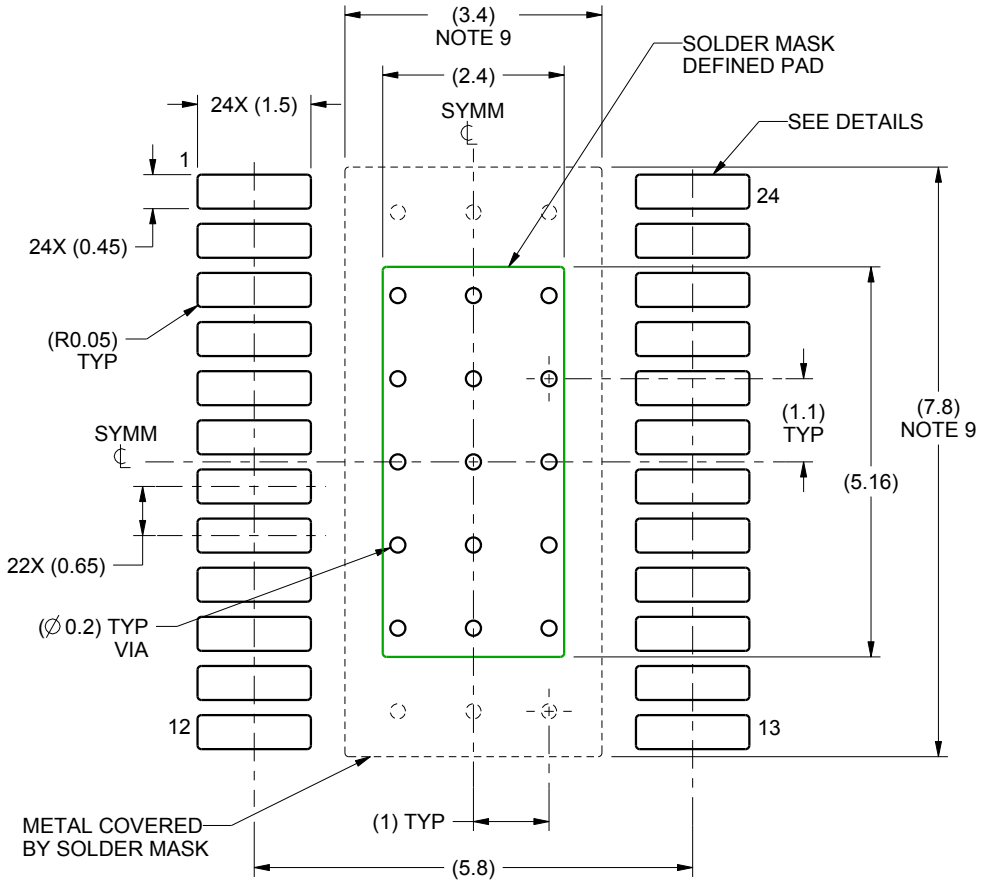
PLASTIC SMALL OUTLINE



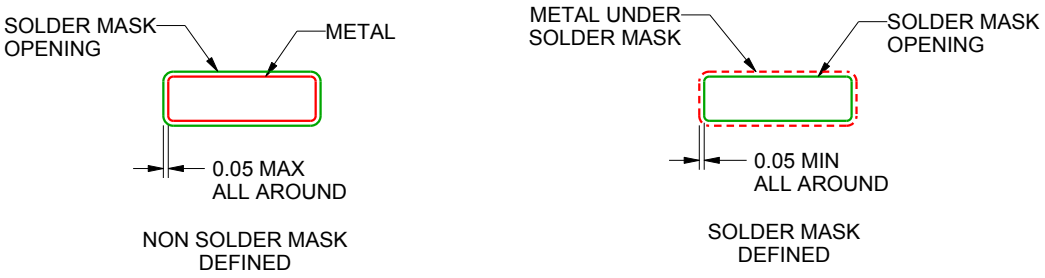
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.



LAND PATTERN EXAMPLE
SCALE:10X

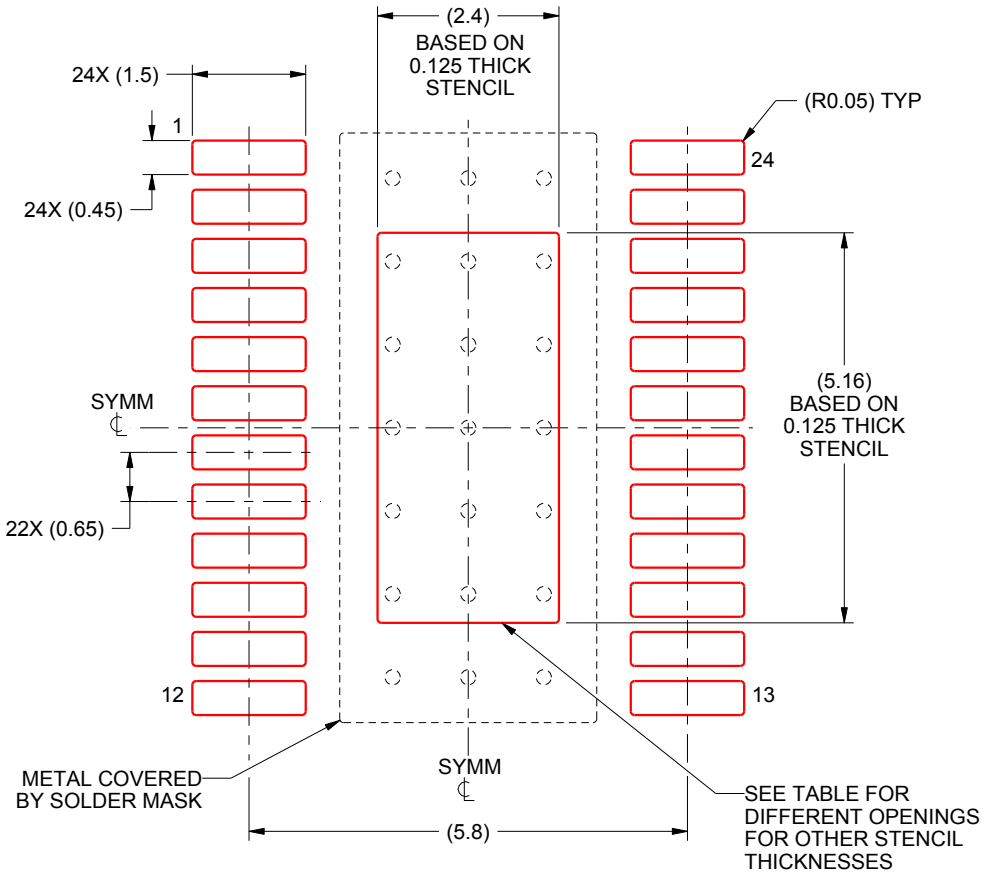


SOLDER MASK DETAILS
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

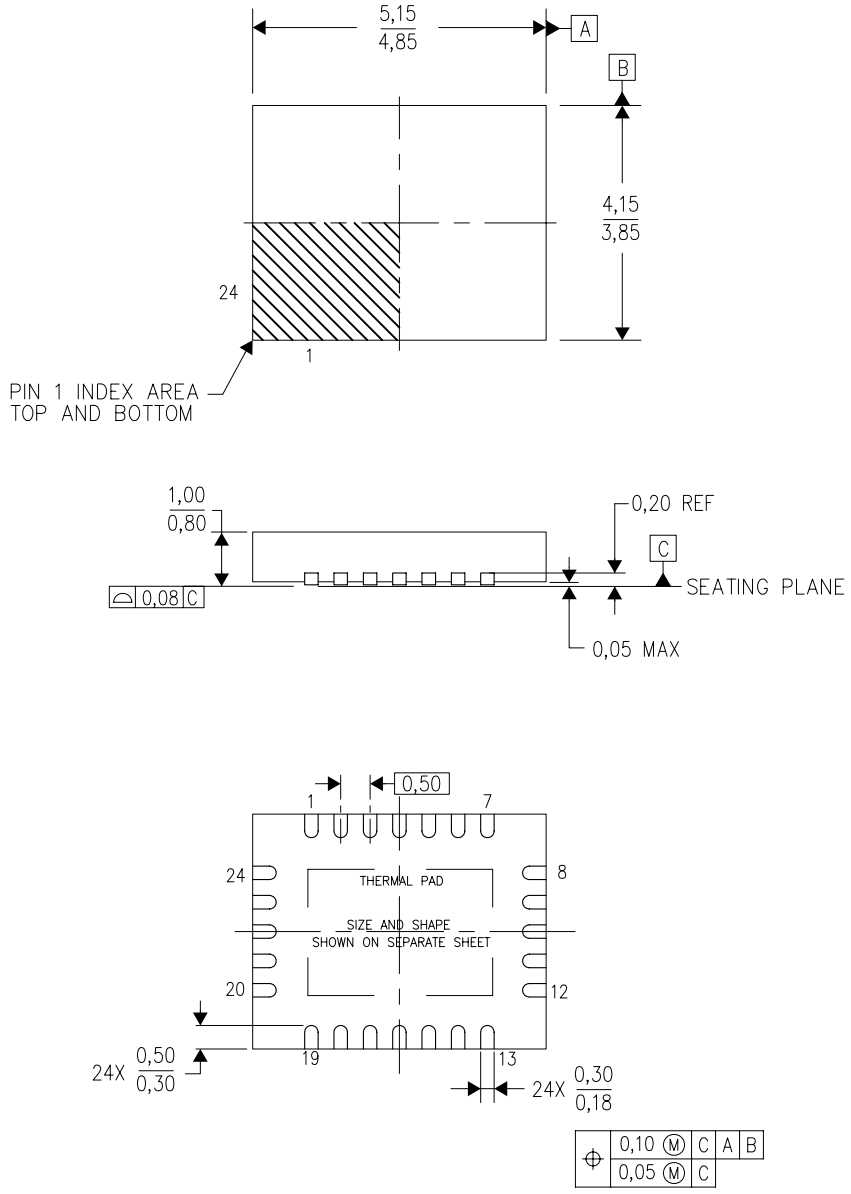
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

4222709/A 02/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



4204845–2/H 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

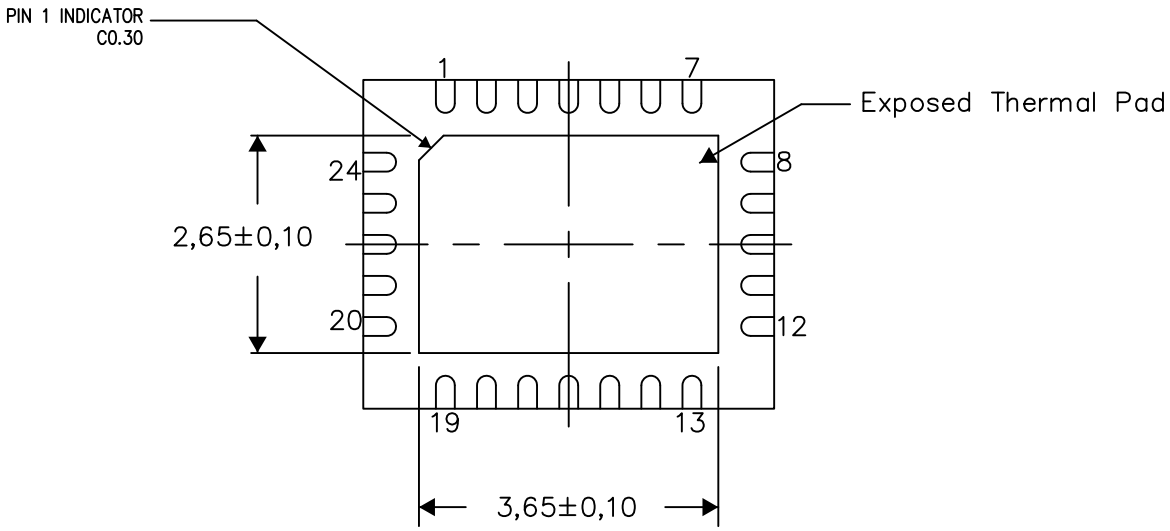
RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



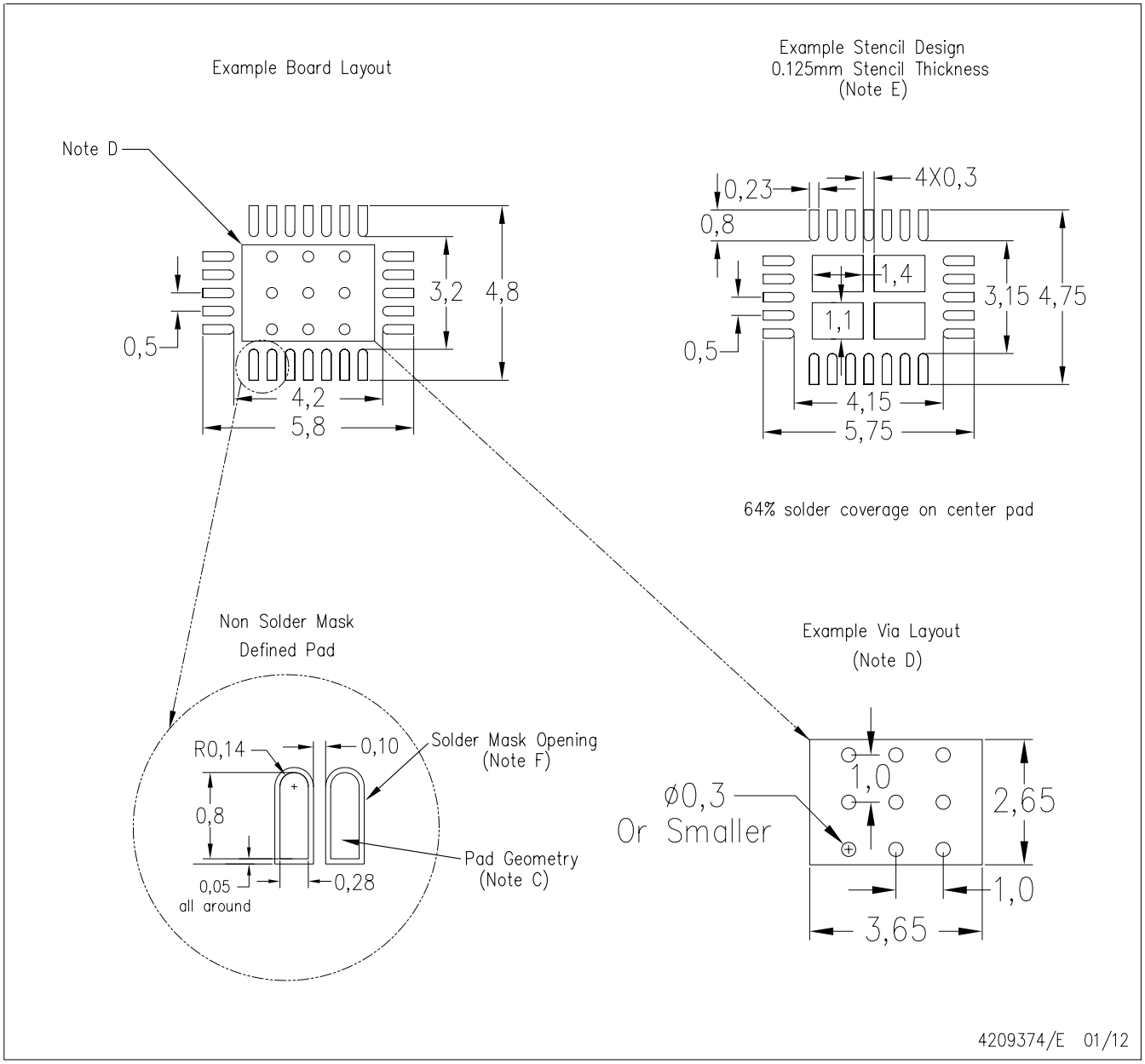
Bottom View

Exposed Thermal Pad Dimensions

4206360–3/K 02/14

NOTE: All linear dimensions are in millimeters

RHF (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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