0.01 GHz to 10 GHz, GaAs, pHEMT, MMIC, Low Noise Amplifier

Data Sheet **HMC8410**

FEATURES

Low noise figure: 1.1 dB typical
High gain: 19.5 dB typical
High output third-order intercept (IP3): 33 dBm typical
6-lead, 2 mm × 2 mm LFCSP package

APPLICATIONS

Software defined radios
Electronic warfare
Radar applications

FUNCTIONAL BLOCK DIAGRAM

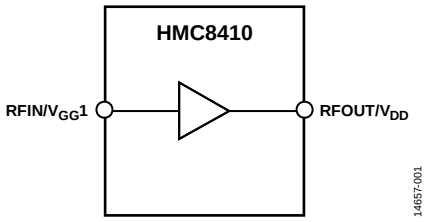


Figure 1.

GENERAL DESCRIPTION

The HMC8410 is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT), low noise wideband amplifier that operates from 0.01 GHz to 10 GHz. The HMC8410 provides a typical gain of 19.5 dB, a 1.1 dB typical noise figure, and a typical output IP3 of 33 dBm, requiring only 65 mA from a 5 V supply voltage. The saturated output power (P_{SAT}) of up to 22.5 dBm enables the low noise amplifier (LNA) to function as a local oscillator (LO) driver for many of Analog Devices, Inc., balanced, I/Q or image rejection mixers.

The HMC8410 also features inputs/outputs (I/Os) that are internally matched to 50 Ω, making it ideal for surface-mounted technology (SMT)-based, high capacity microwave radio applications.

The HMC8410 is housed in a RoHS-compliant, 2 mm × 2 mm, LFCSP package.

Multifunction pin names can be referenced by their relevant function only.

Rev. D **Document Feedback**
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REVISION HISTORY

6/2019—Rev. C to Rev. D

Changes to Table 4 ... 5
Changes to Figure 11 ... 7
Changes to Figure 25 ... 10

1/2019—Rev. B to Rev. C

Changes to Figure 11 ... 7
Added Figure 16, Renumbered Sequentially ... 8
Updated Outline Dimensions ... 17

9/2018—Rev. A to Rev. B

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11/2017—Rev. 0 to Rev. A

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Changes to Figure 18 and Figure 20 Caption ... 9
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Added Figure 36; Renumbered Sequentially ... 12
Updated Outline Dimensions ... 17
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7/2016—Revision 0: Initial Version

ELECTRICAL SPECIFICATIONS

0.01 GHz TO 3 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 65 mA, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		0.01		3	GHz	
GAIN		17.5	19.5		dB	
Gain Variation Over Temperature			0.01		dB/°C	
NOISE FIGURE			1.1	1.6	dB	0.3 GHz to 3 GHz
RETURN LOSS						
Input			15		dB	
Output			24		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	19.0	21.0		dBm	
Saturated Output Power	P_{SAT}		22.5		dBm	
Output Third-Order Intercept	IP3		33		dBm	
SUPPLY CURRENT	I_{DQ}		65	80	mA	Adjust V_{GG1} to achieve I_{DQ} = 65 mA typical
SUPPLY VOLTAGE	V_{DD}	2	5	6	V	

3 GHz TO 8 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 65 mA, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		3		8	GHz	
GAIN		15.5	18		dB	
Gain Variation Over Temperature			0.01		dB/°C	
NOISE FIGURE			1.4	1.9	dB	
RETURN LOSS						
Input			10		dB	
Output			16		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	18.0	21.0		dBm	
Saturated Output Power	P_{SAT}		22.5		dBm	
Output Third-Order Intercept	IP3		31.5		dBm	
SUPPLY CURRENT	I_{DQ}		65	80	mA	Adjust V_{GG1} to achieve I_{DQ} = 65 mA typical
SUPPLY VOLTAGE	V_{DD}	2	5	6	V	

8 GHz TO 10 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 65 mA, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		8		10	GHz	
GAIN		13	16		dB	
Gain Variation Over Temperature			0.01		dB/°C	
NOISE FIGURE			1.7	2.2	dB	
RETURN LOSS						
Input			8		dB	
Output			7		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	17.5	19.5		dBm	
Saturated Output Power	P_{SAT}		21.5		dBm	
Output Third-Order Intercept	IP3		33		dBm	
SUPPLY CURRENT	I_{DQ}		65	80	mA	Adjust V_{GG1} to achieve I_{DQ} = 65 mA typical
SUPPLY VOLTAGE	V_{DD}	2	5	6	V	

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter[1]	Rating
Drain Bias Voltage (V_{DD})	7 V dc
Radio Frequency (RF) Input Power (RFIN)	20 dBm
Continuous Power Dissipation (P_{DISS}), T = 85°C (Derate 7.8 mW/°C above 85°C)	0.7 W
Channel Temperature	175°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Thermal Resistance (Channel to Ground Paddle)	128.92°C/W
Maximum Peak Reflow Temperature (MSL3)[2]	260°C
ESD Sensitivity	
Human Body Model (HBM)	Class1B Passed 500 V

[1] When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed. For the full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.
[2] See the Ordering Guide section for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

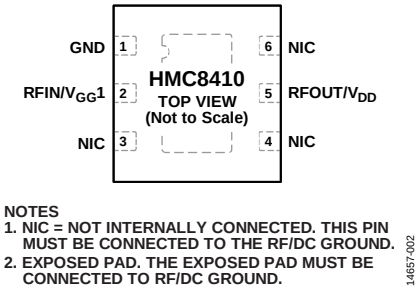


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground. This pin must be connected to the RF/dc ground. See Figure 3 for the interface schematic.
2	RFIN/V_{GG}1	RF Input (RFIN). This pin is ac-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
		Gate Bias of the Amplifier (V_{GG}1). This pin is ac-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
3, 4, 6	NIC	Not Internally Connected. This pin must be connected to the RF/dc ground.
5	RFOUT/V_{DD}	RF Output (RFOUT). This pin is ac-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.
		Drain Bias for Amplifier (V_{DD}). This pin is ac-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS



Figure 3. GND Interface Schematic

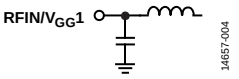


Figure 4. RFIN/V_{GG}1 Interface Schematic

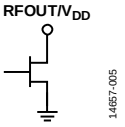


Figure 5. RFOUT/V_{DD} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

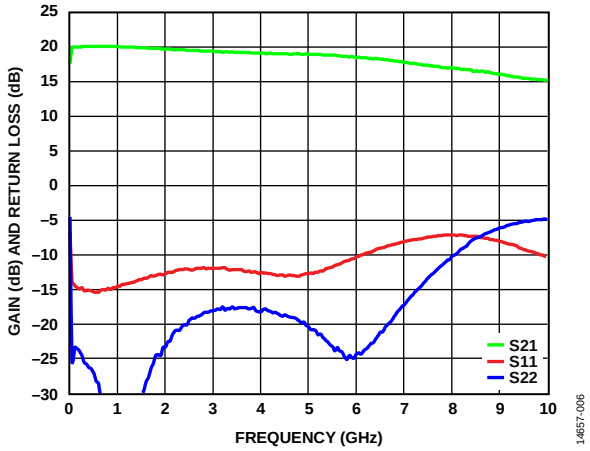


Figure 6. Gain and Return Loss vs. Frequency

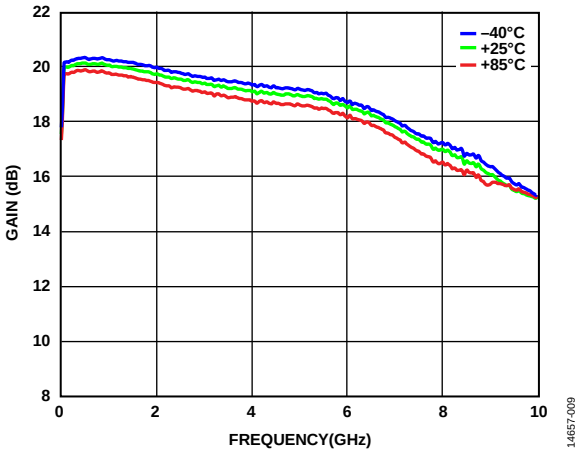


Figure 9. Gain vs. Frequency for Various Temperatures

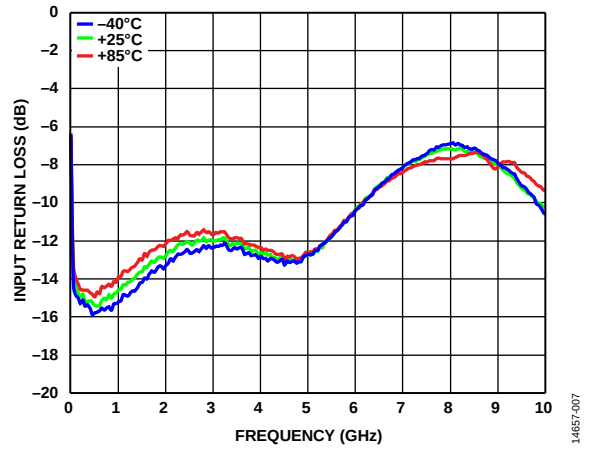


Figure 7. Input Return Loss vs. Frequency for Various Temperatures

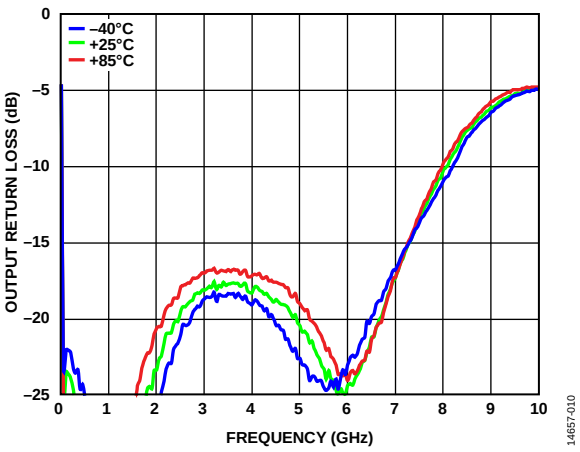


Figure 10. Output Return Loss vs. Frequency for Various Temperatures

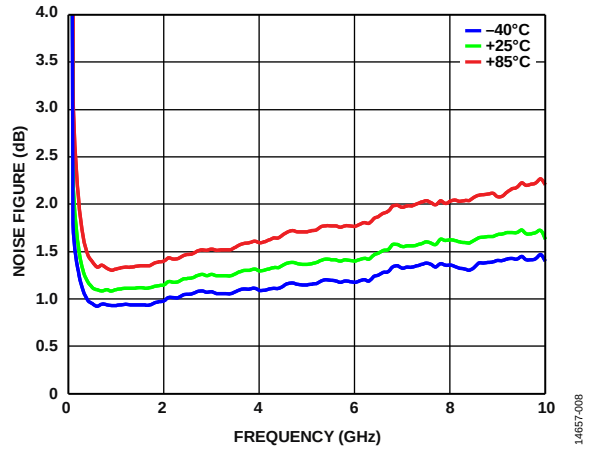


Figure 8. Noise Figure vs. Frequency for Various Temperatures

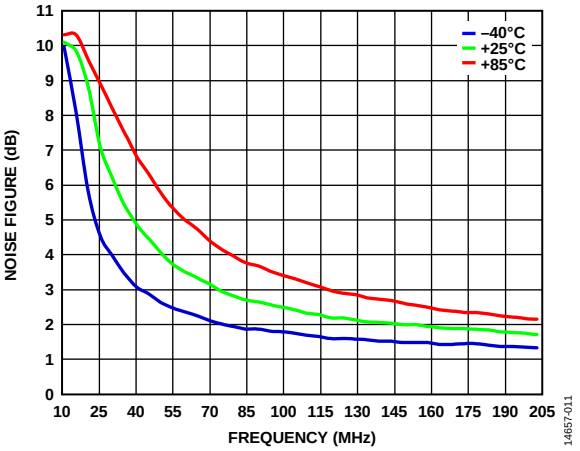


Figure 11. Noise Figure vs. Frequency for Various Temperatures, 10 MHz to 200 MHz

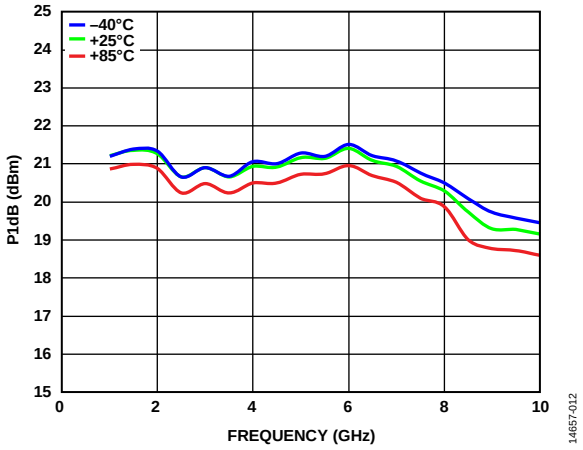


Figure 12. P1dB vs. Frequency for Various Temperatures

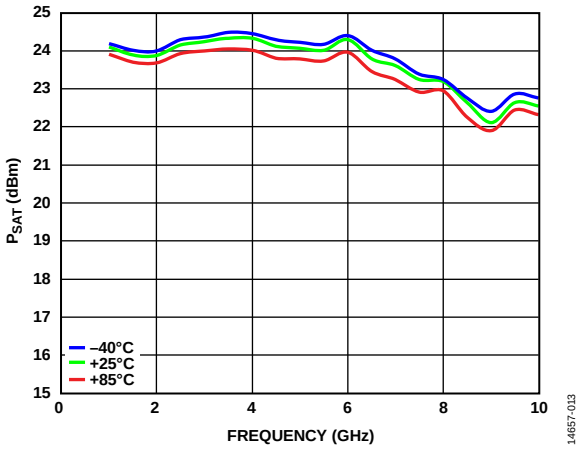


Figure 13. P_{SAT} vs. Frequency for Various Temperatures

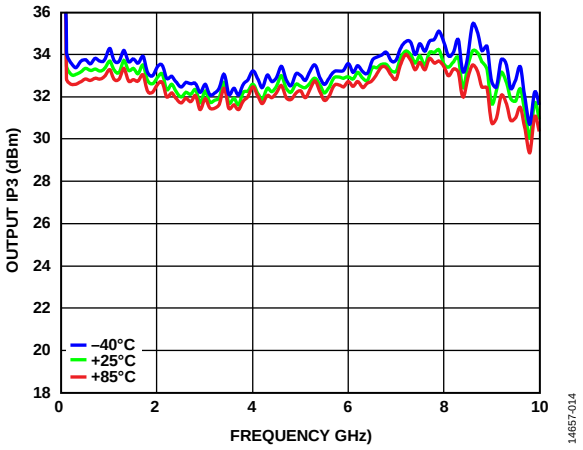


Figure 14. Output IP3 vs. Frequency for Various Temperatures, Output Power (P_{OUT})/Tone = 5 dBm

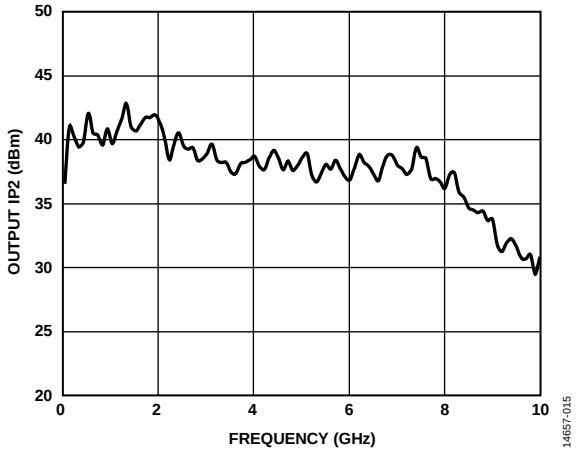


Figure 15. Output IP2 vs. Frequency at P_{OUT}/Tone = 5 dBm

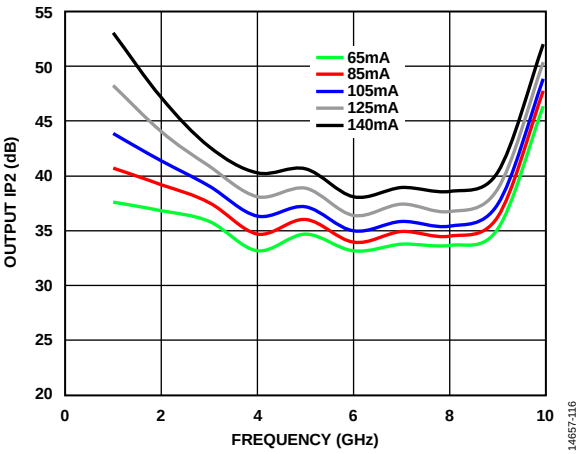


Figure 16. Output IP2 vs. Frequency for Various Supply Currents (IDQ), P_{OUT}/Tone=5 dBm, V_{DD} = 5 V

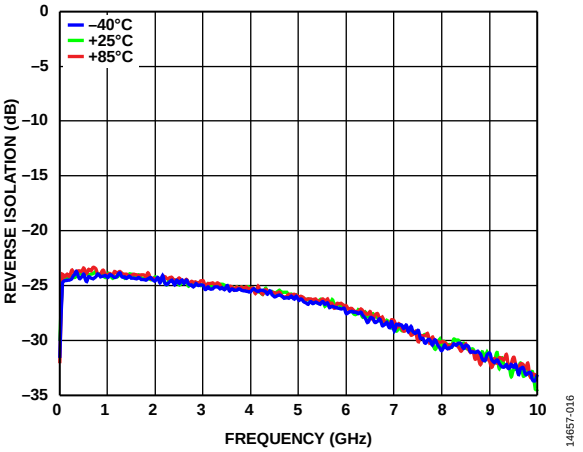


Figure 17. Reverse Isolation vs. Frequency for Various Temperatures

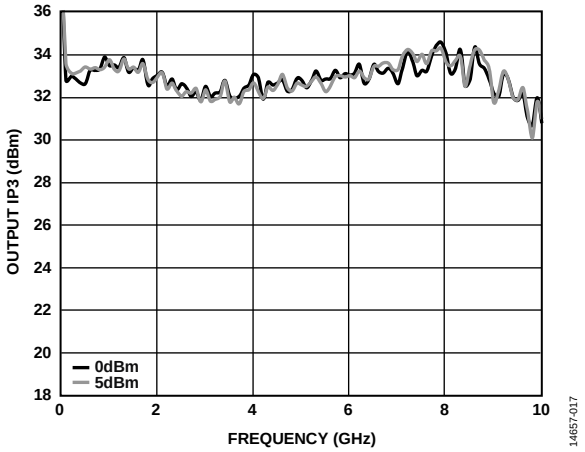


Figure 18. Output IP3 vs. Frequency for Various P_{OUT}/Tone

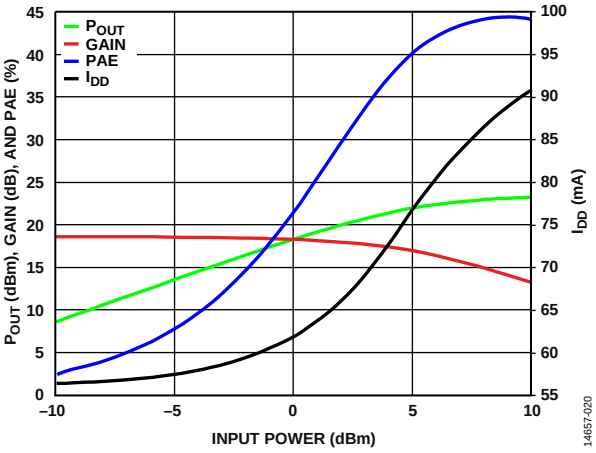


Figure 21. P_{OUT}, Gain, PAE, and Supply Current with RF Applied (I_{DD}) vs. Input Power at 5 GHz

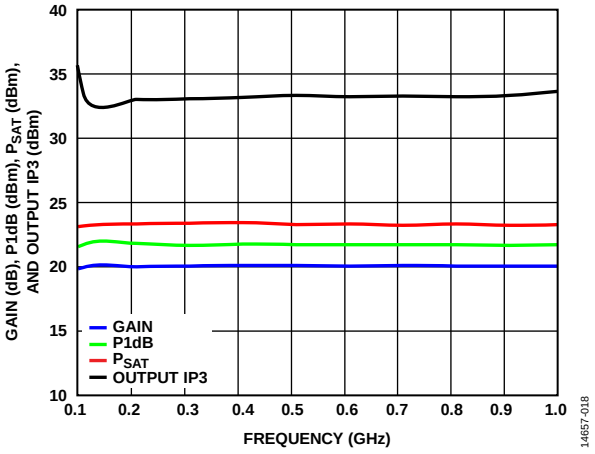


Figure 19. Gain, P1dB, P_{SAT}, and Output IP3 vs. Frequency

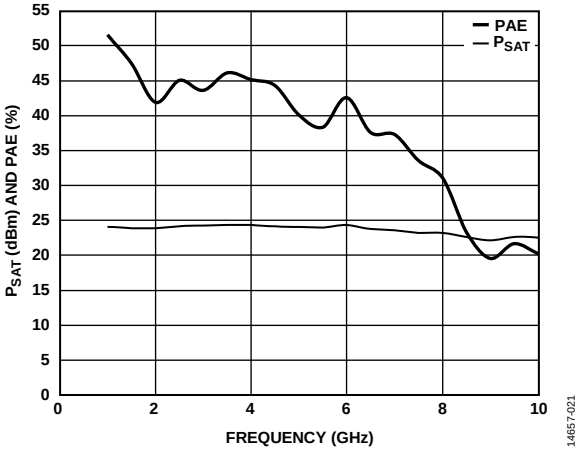


Figure 22. P_{SAT} and PAE vs. Frequency

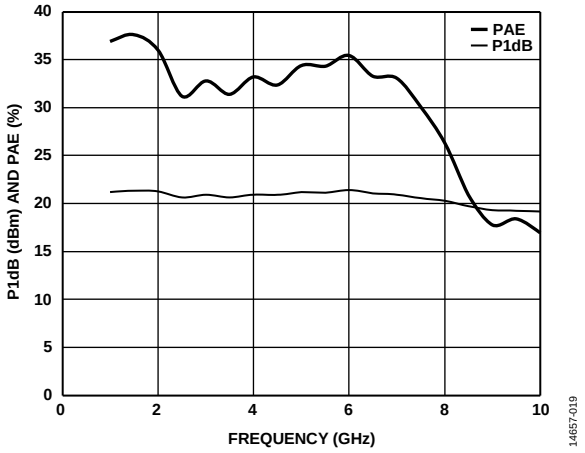


Figure 20. P1dB and Power Added Efficiency (PAE) vs. Frequency

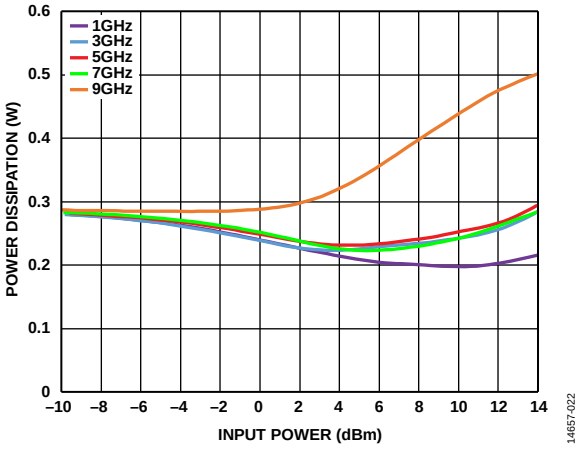


Figure 23. Power Dissipation at 85°C vs. Input Power at Various Frequencies

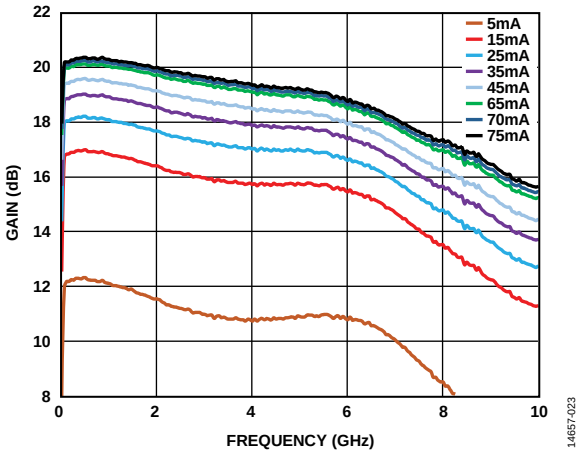


Figure 24. Gain vs. Frequency for Various Supply Currents, V_{DD} = 5 V

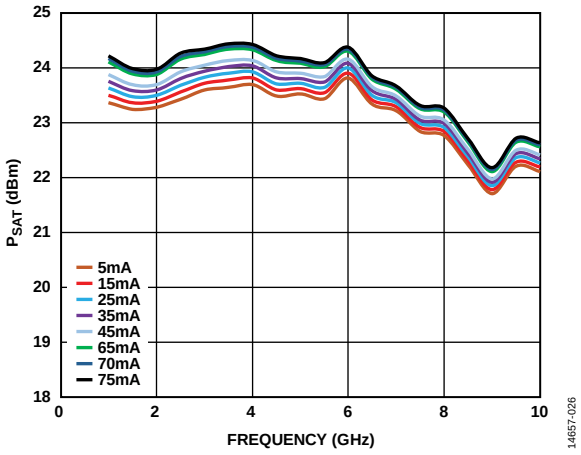


Figure 27. P_{SAT} vs. Frequency for Various Supply Currents (I_{DQ}), V_{DD} = 5 V

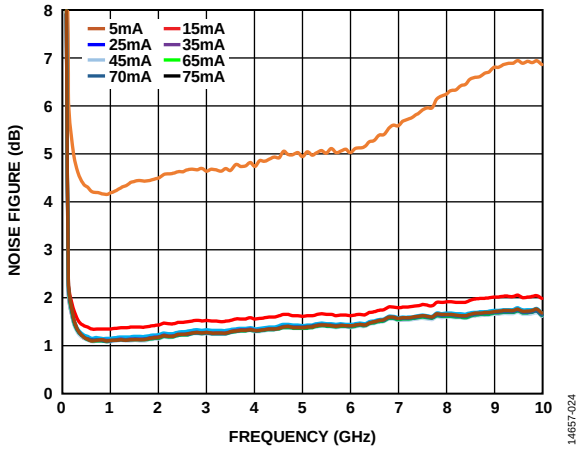


Figure 25. Noise Figure vs. Frequency for Various Supply Currents (I_{DQ}), V_{DD} = 5 V

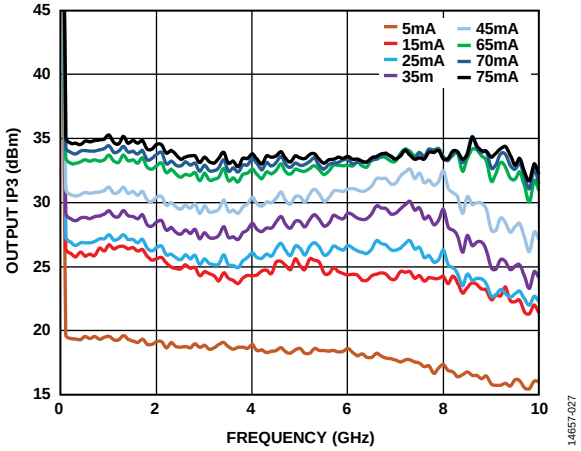


Figure 28. Output IP3 vs. Frequency for Various Supply Currents (I_{DQ}), P_{OUT}/Tone = 5 dBm, V_{DD} = 5 V

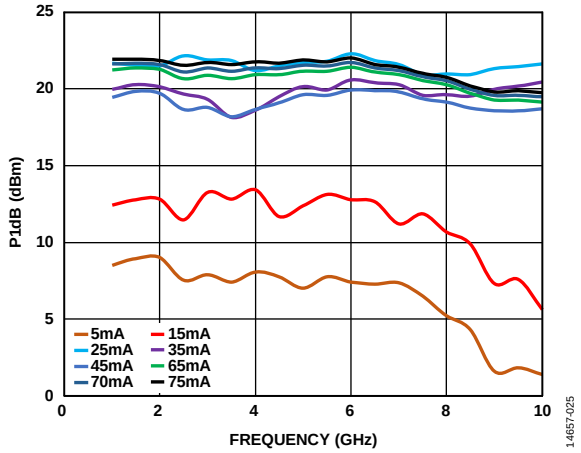


Figure 26. P1dB vs. Frequency for Various Supply Currents (I_{DQ}), V_{DD} = 5 V

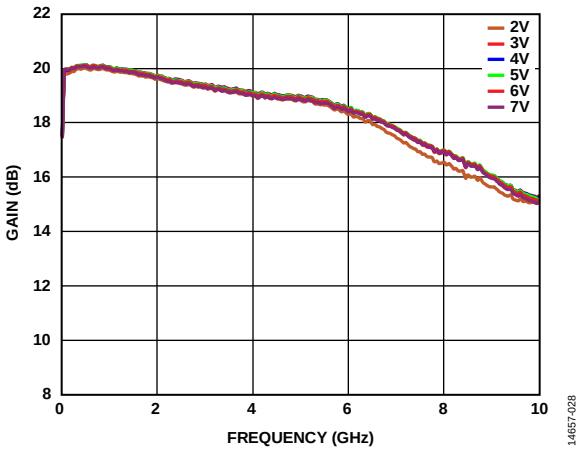


Figure 29. Gain vs. Frequency for Various Supply Voltages, I_{DQ} = 65 mA

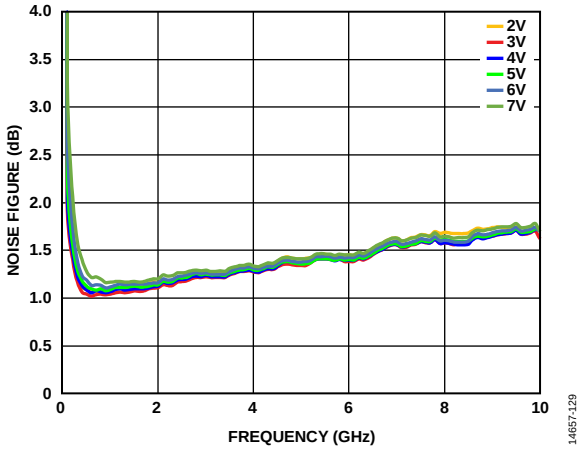


Figure 30. Noise Figure vs. Frequency for Various Supply Voltages, I_{DQ} = 65 mA

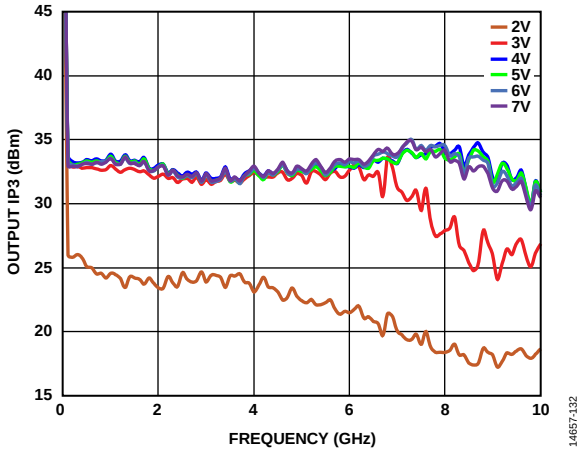


Figure 33. Output IP3 vs. Frequency for Various Supply Voltages, P_{OUT}/Tone = 5 dBm

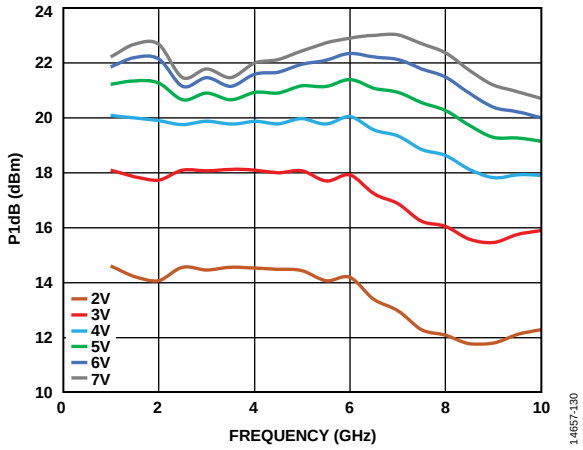


Figure 31. P1dB vs. Frequency for Various Supply Voltages, I_{DQ} = 65 mA

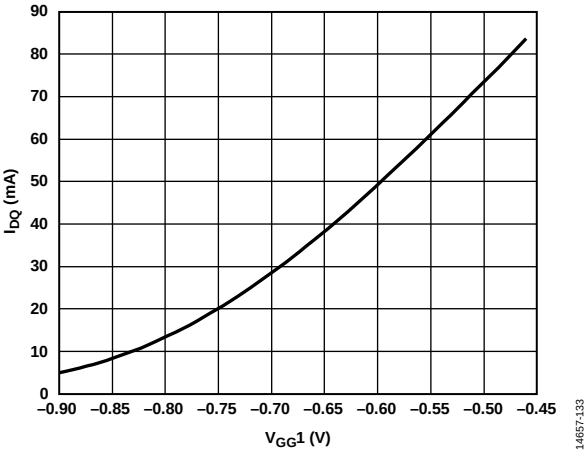


Figure 34. Supply Current (I_{DQ}) vs. $V_{GG}1$, V_{DD} = 5 V, Representative of a Typical Device

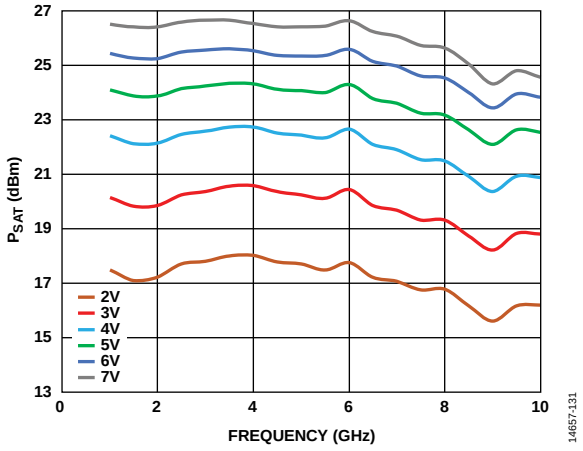


Figure 32. P_{SAT} vs. Frequency for Various Supply Voltages, I_{DQ} = 65 mA

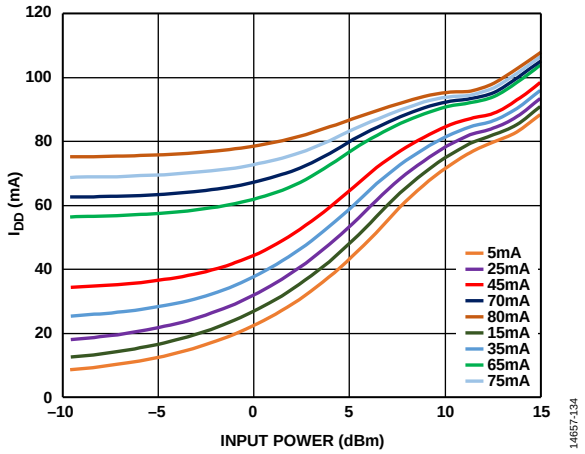


Figure 35. Supply Current with RF Applied (I_{DD}) vs. Input Power for Various Supply Currents (I_{DQ}) at 5 GHz, V_{DD} = 5 V

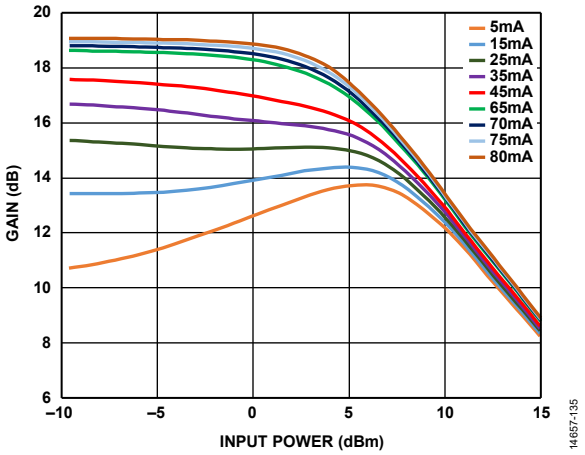


Figure 36. Gain vs. Input Power for Various Supply Currents (I_{DQ}) at 5 GHz, V_{DD} = 5 V

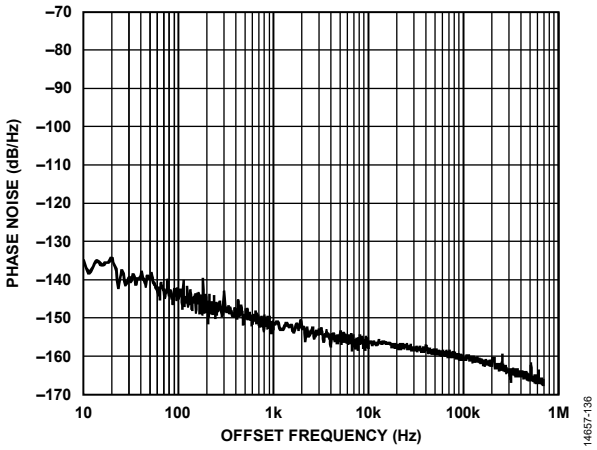


Figure 37. Additive Phase Noise vs. Offset Frequency, RF Frequency = 5 GHz, RF Input Power = 3 dBm (P1dB)

THEORY OF OPERATION

The HMC8410 is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic (pHEMT), low noise wideband amplifier.

The cascode amplifier uses a fundamental cell of two field effect transistors (FETs) in series, source to drain. The basic schematic for the cascode cell is shown in Figure 38, which forms a low noise amplifier operating from 0.01 GHz to 10 GHz with excellent noise figure performance.

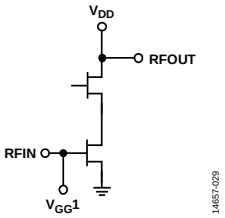


Figure 38. Basic Schematic for the Cascode Cell

The HMC8410 has single-ended input and output ports whose impedances are nominally equal to 50 Ω over the 0.01 GHz to 10 GHz frequency range. Consequently, it can directly insert into a 50 Ω system with no required impedance matching circuitry, which also means that multiple HMC8410 amplifiers can be cascaded back to back without the need for external matching circuitry.

The input and output impedances are sufficiently stable vs. variations in temperature and supply voltage that no impedance matching compensation is required.

Note that it is critical to supply very low inductance ground connections to the ground pins as well as to the backside exposed paddle to ensure stable operation.

To achieve optimal performance from the HMC8410 and prevent damage to the device, do not exceed the absolute maximum ratings.

APPLICATIONS INFORMATION

Figure 39 shows the basic connections for operating the HMC8410. AC couple the input and output of the HMC8410 with appropriately sized capacitors. DC block capacitors and RF choke inductors are supplied on the RFIN and RFOUT pins of the HMC8410 evaluation board. See Table 6 for additional information. These dc block capacitors and RF choke inductors form wideband bias tees on the input and output ports to provide both ac coupling and the necessary supply voltages to the RFIN and RFOUT pins. A 5 V dc bias is supplied to the amplifier through the choke inductor connected to the RFOUT pin, and the negative $V_{GG}1$ voltage is supplied to the RFIN pin through the choke inductor.

RECOMMENDED BIAS SEQUENCING

To not damage the amplifier, follow the recommended bias sequencing.

During Power-Up

The recommended bias sequence during power-up for the HMC8410 follows:

1. Connect to GND.
2. Set $V_{GG}1$ to −2 V.
3. Set V_{DD} to 5 V.
4. Increase $V_{GG}1$ to achieve a typical supply current (I_{DQ}) = 65 mA.
5. Apply the RF signal.

During Power-Down

The recommended bias sequence during power-down for the HMC8410 follows:

1. Turn off the RF signal.
2. Decrease $V_{GG}1$ to −2 V to achieve a typical I_{DQ} = 0 mA.
3. Decrease V_{DD} to 0 V.
4. Increase $V_{GG}1$ to 0 V.

The bias conditions previously listed (V_{DD} = 5 V and I_{DQ} = 65 mA) are the recommended operating points to achieve optimum performance. The data used in this data sheet was taken with the recommended bias conditions. When using the HMC8410 with different bias conditions, different performance than what is shown in the Typical Performance Characteristics section can result.

Figure 19, Figure 31, and Figure 32 show that increasing the voltage from 2 V to 7 V typically increases P1dB and P_{SAT} at the expense of power consumption with minor degradation on noise figure (NF).

TYPICAL APPLICATION CIRCUIT

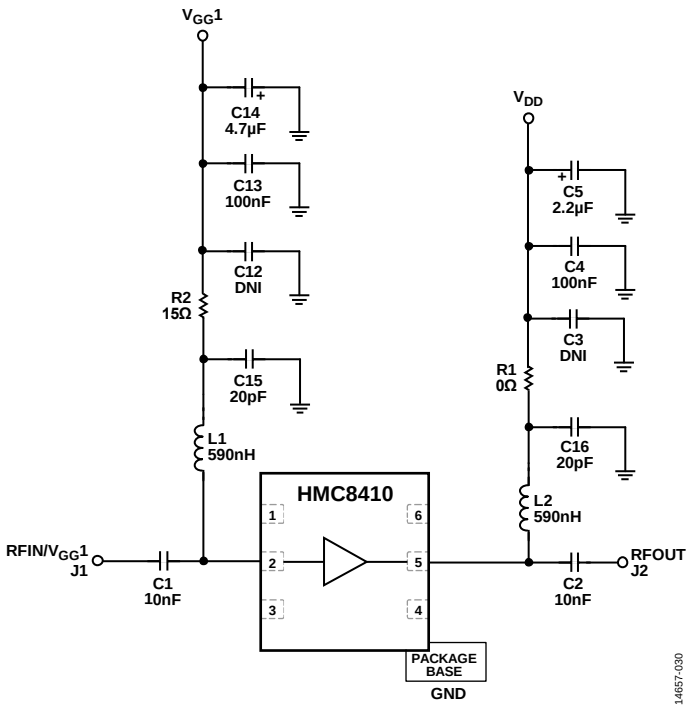


Figure 39. Typical Application Circuit

EVALUATION BOARD

The HMC8410 evaluation board is a 4-layer board fabricated using a Rogers 4350 and the best practices for high frequency RF design. The RF input and RF output traces have a 50 Ω characteristic impedance.

The HMC8410 evaluation board and populated components operate over the −40°C to +85°C ambient temperature range. For proper bias sequence, see the Applications Information section.

The HMC8410 evaluation board schematic is shown in Figure 41. A fully populated and tested evaluation printed circuit board (PCB) is available from Analog Devices, Inc., upon request (see Figure 40).

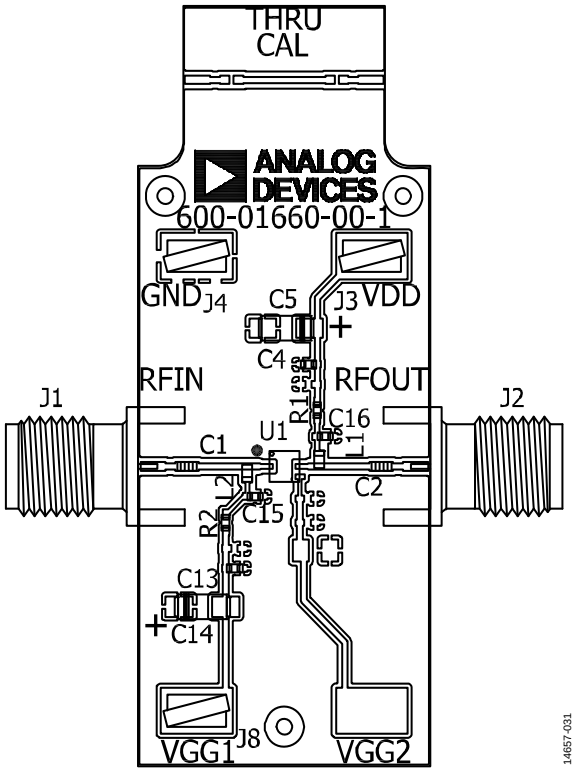


Figure 40. HMC8410 Evaluation PCB

EVALUATION BOARD SCHEMATIC

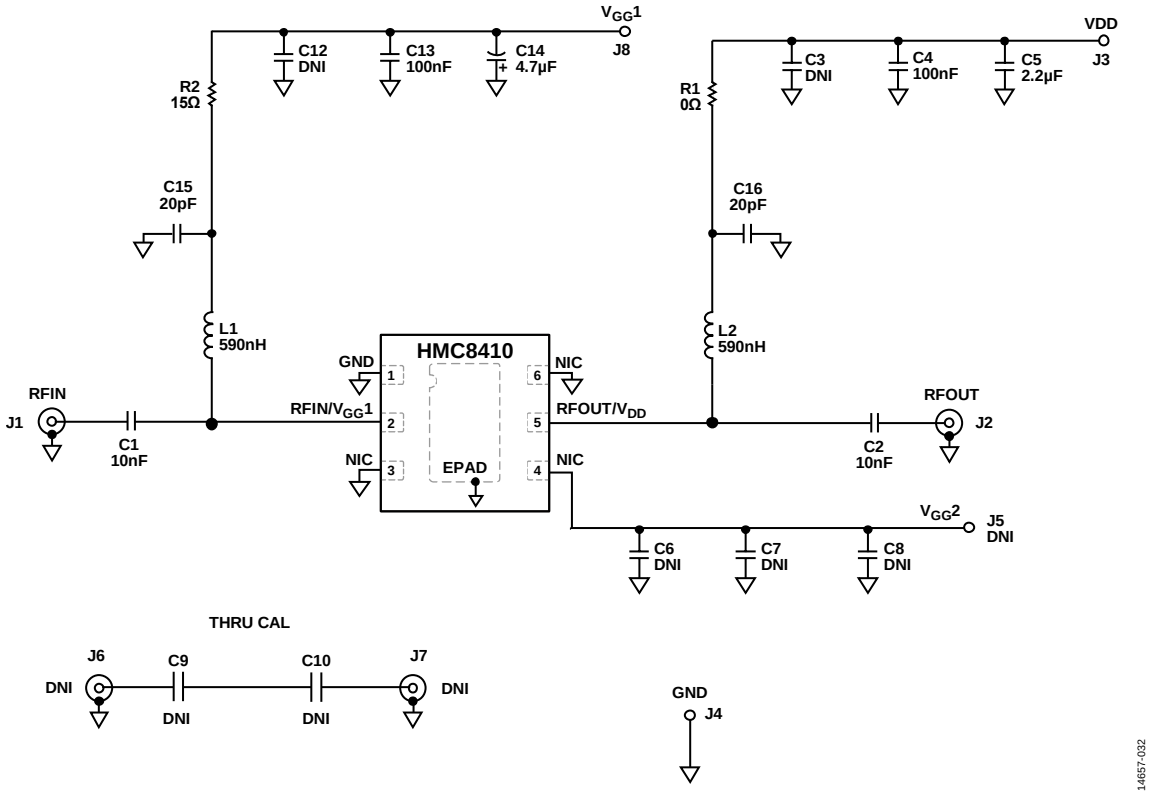


Figure 41. HMC8410 Evaluation Board Schematic

Table 6. Bill of Materials for Evaluation PCB EV1HMC8410LP2F

Item	Description
J1, J2	PCB mount SMA RF connectors, SRI 21-146-1000-01
J3, J4, J8	DC bias test points
C1, C2	Capacitors, broadband, 10 nF and 82 pF, 0502, 160 kHz and 40 GHz; Presidio Components MBB0502X103MLP5N8L
C3, C6 to C10, C12, J5 to J7	Do not install (DNI)
C4, C13	Capacitors, ceramic, 100 nF, 0402 package
C5	Capacitor, tantalum, 2.2 µF, Size A
C14	Capacitor, tantalum, 4.7 µF, 3216 package
C15, C16	Capacitors, ceramic, 20 pF, 0402 package
L1, L2	Inductors, 590 nH, 0402, 5%, ferrite DF, Coilcraft 0402DF-591XJRU
R1	0 Ω resistor
R2	15 Ω resistor, 0402 package
U1	Amplifier, HMC8410
Heat sink	Heat sink
PCB	600-01660-00 evaluation PCB; circuit board material: Rogers 4350

OUTLINE DIMENSIONS

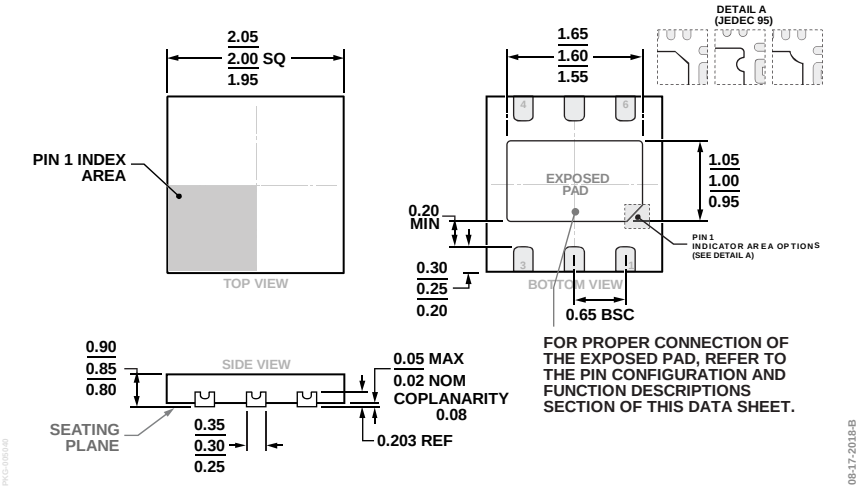


Figure 42. 6-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2 mm Body and 0.85 mm Package Height
(CP-6-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Lead Finish	Package Description	Package Option
HMC8410LP2FE	−40°C to +85°C	MSL3	100% Matte Sn	6-Lead LFCSP	CP-6-9
HMC8410LP2FETR	−40°C to +85°C	MSL3	100% Matte Sn	6-Lead LFCSP	CP-6-9
EV1HMC8410LP2F				Evaluation PCB	

[1] The HMC8410LP2FE and HMC8410LP2FETR are RoHS Compliant Parts.
[2] See the Absolute Maximum Ratings section for additional information.

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