

PIC18F87J93 Family Silicon Errata and Data Sheet Clarification

The PIC18F87J93 family devices that you have received conform functionally to the current Device Data Sheet (DS39948A) and its “parent” data sheet (“PIC18F87J90 Family Data Sheet”, DS39933), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F87J93 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICKIT™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICKIT™ 3.
2. From the main menu in MPLAB IDE, select Configure>Select Device, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (Debugger>Select Tool).
4. Perform a “Connect” operation to the device (Debugger>Connect). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVID:REVID values for the various PIC18F87J93 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾		
		A1		
PIC18F66J93	0101 0000 010	0 0001		
PIC18F67J93	0101 0000 011			
PIC18F86J93	0101 0000 110			
PIC18F87J93	0101 0000 111			

Note 1: The Device IDs (DEVID and REVID) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format “DEVID:REVID”.

2: Refer to the “PIC18F6XJXX/8XJXX Family Flash Microcontroller Programming Specification” (DS39644) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾		
				A1		
MSSP	I ² C™ Slave	1.	If the SSPBUF register is not read within a window after the SSPIF interrupt, the module may not receive the correct data.	X		
EUSART	Enable/Disable	2.	If interrupts are enabled, disabling and re-enabling the module requires a 2 Tcy delay.	X		
RTCC	INTRC clock	3.	The INTRC clock is not automatically enabled when it is selected.	X		
MSSP	I ² C™ Mode	4.	If a Stop condition occurs in the middle of an address or data reception, there will be issues with the SCL clock stream and RCEN bit.	X		

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: MSSP (I²C™ Slave)

In extremely rare cases when configured for I²C™ slave reception, the MSSP module may not receive the correct data. This occurs only if the Serial Receive/Transmit Buffer register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

Work around

The issue can be resolved in either of these ways:

- Prior to the I²C slave reception, enable the clock stretching feature.

This is done by setting the SEN bit (SSPCON2<0>).

- Each time the SSPIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

Affected Silicon Revisions

A1								
X								

2. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (SPEN bit (RCSTAx<7>) = 0)
- The EUSART is re-enabled (RCSTAx<7> = 1)
- A two-cycle instruction is executed

Work around

Add a 2 Tcy delay after re-enabling the EUSART.

1. Disable receive interrupts (RCxIE bit (PIE1<5>) = 0).
2. Disable the EUSART (RCSTAx<7> = 0).
3. Re-enable the EUSART (RCSTAx<7> = 1).
4. Re-enable receive interrupts (PIE1<5> = 1).

(This is the first Tcy delay.)

5. Execute a NOP instruction.

(This is the second Tcy delay.)

Affected Silicon Revisions

A1								
X								

3. Module: Real-Time Clock and Calendar (RTCC)

The INTRC is not automatically enabled as the clock source for the RTCC module when the INTRC clock is selected (CONFIG3L<1> = 0) and the RTCC module is enabled (RTCCFG<7> = 1).

Work around

In order to enable the INTRC, at least one of the following has to be enabled:

1. Watchdog Timer Enable bit (WDTEN, CONFIG1L<0>).
2. Two-Speed Start-up Enable bit (IESO, CONFIG2L<7>).
3. Fail-Safe Clock Monitor Enable bit (FCMEN, CONFIG2L<6>).

Affected Silicon Revisions

A1								
X								

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4. Module: MSSP (I²C™ Mode)

In Master I²C Receive mode, if a Stop condition occurs in the middle of an address or data reception, the SCL clock stream will continue endlessly and the RCEN bit of the SSPCON2 register will remain set improperly. When a Start condition occurs after the improper Stop condition, nine additional clocks will be generated followed by the RCEN bit going low.

Work around

Use low-impedance pull-ups on the SDA line to reduce the possibility of noise glitches that may trigger an improper Stop event. Use a time-out event timer to detect the unexpected Stop condition and subsequently stuck RCEN bit. Clear the stuck RCEN bit by clearing SSPEN bit of SSPCON1.

Affected Silicon Revisions

A1							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39948A). For corrections and clarifications for the “parent” data sheet, see the silicon errata and data sheet clarification document for the PIC18F87J90 family.

Note: Corrections are shown in bold. Where possible, the original bold text formatting has been removed for clarity.

None.

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APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2009)

Initial release of this document. Silicon issues 1 (MSSP – I²C Slave), 2 (EUSART), 3 (RTCC) and 4 (MSSP – I²C Mode). No data sheet clarifications.

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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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