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November 2014

# FL7734
# Single-Stage Primary-Side-Regulation PWM Controller for PFC and Phase Cut Dimmable LED Driving

## Features

- Excellent Dimmer Compatibility by Active Dimming Control
- Programmable Dimming Curve and Input Current Management
- Constant LED Current Regulation in Large Phase Angle Range
- Cost-Effective Solution without Input Bulk Capacitor and Feedback Circuitry
- Accurate Constant-Current (CC) Control, Independent on Line Voltage, Output Voltage, Magnetizing Inductance Variation
- Power Factor Correction (PFC)
- Fast Startup utilizing Bleeding Circuit
- Open-LED Protection
- Short-LED Protection
- Sensing Resistor Short Protection
- Cycle-by-Cycle Current Limiting
- Over-Temperature Protection with Auto Restart

## Applications

- LED Lighting System

## Description

The FL7734 is a highly integrated PWM controller with advanced Primary-Side-Regulation (PSR) technique to minimize components for low power LED lighting solutions. Using the innovative TRUECURRENT® technology for tight constant-current control, it enables designs with constant-current (CC) tolerance of less than ±1% in the wide line voltage range to meet stringent LED brightness requirements.

FL7734 can operate with all types of phase cut dimmers. Phase cut dimming is managed smoothly by Fairchild's proprietary constant input current control and bleeding current control to achieve excellent dimmer compatibility without visible flicker.

The controller can automatically detect whether there is a dimmer connection. In non dimming mode, the operating mode is set to optimize power factor and THD by enabling linear frequency control and voltage mode based on DCM.

An external high-voltage bleeding circuit is utilized to implement fast startup and high system efficiency. The FL7734 also provides powerful protections, such as LED open / short, sensing resistor shorted, and over-temperature for high system reliability. The FL7734 is available in 16-pin Small-Outline Package (SOP).

## Related Resources

*FL7734 Product Folder*

## Ordering Information

| Part Number | Operating Temperature Range | Package | Packing Method |
|---|---|---|---|
| FL7734MX | -40°C to +125°C | 16-Lead, Small Outline Package (SOP-16) | Tape & Reel |



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## Application Diagram

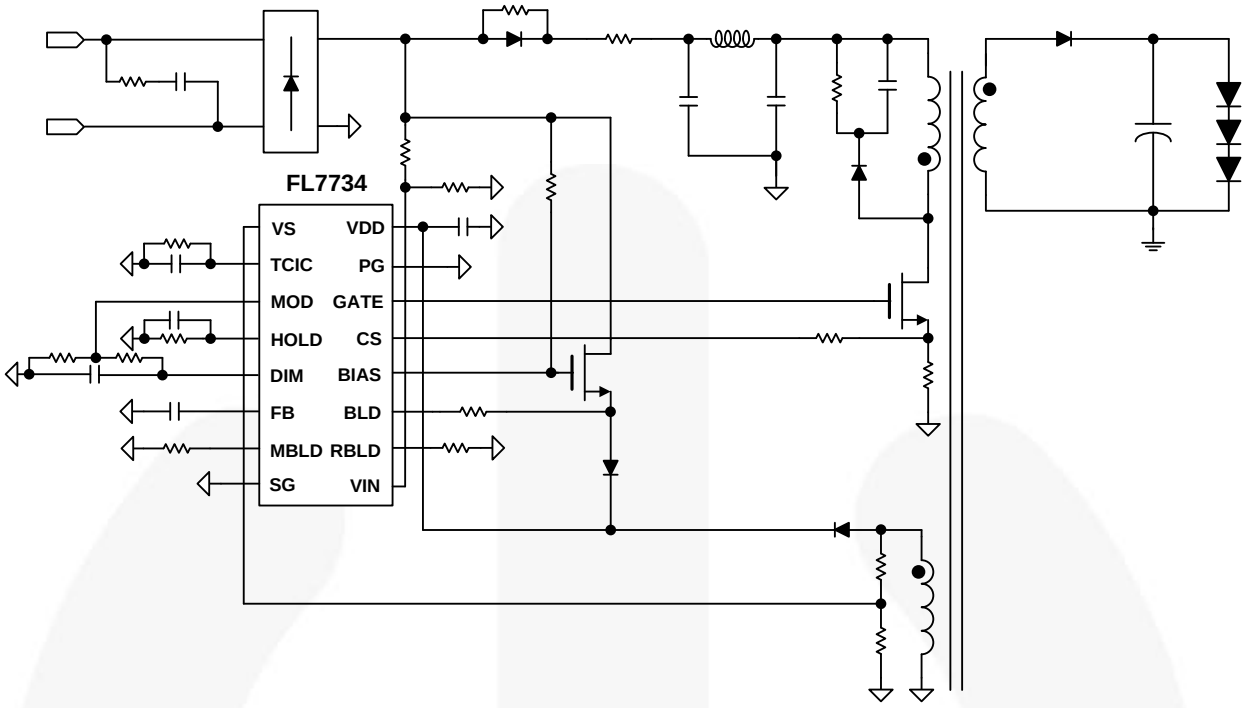



**Figure 1. Typical Application**

## Internal Block Diagram

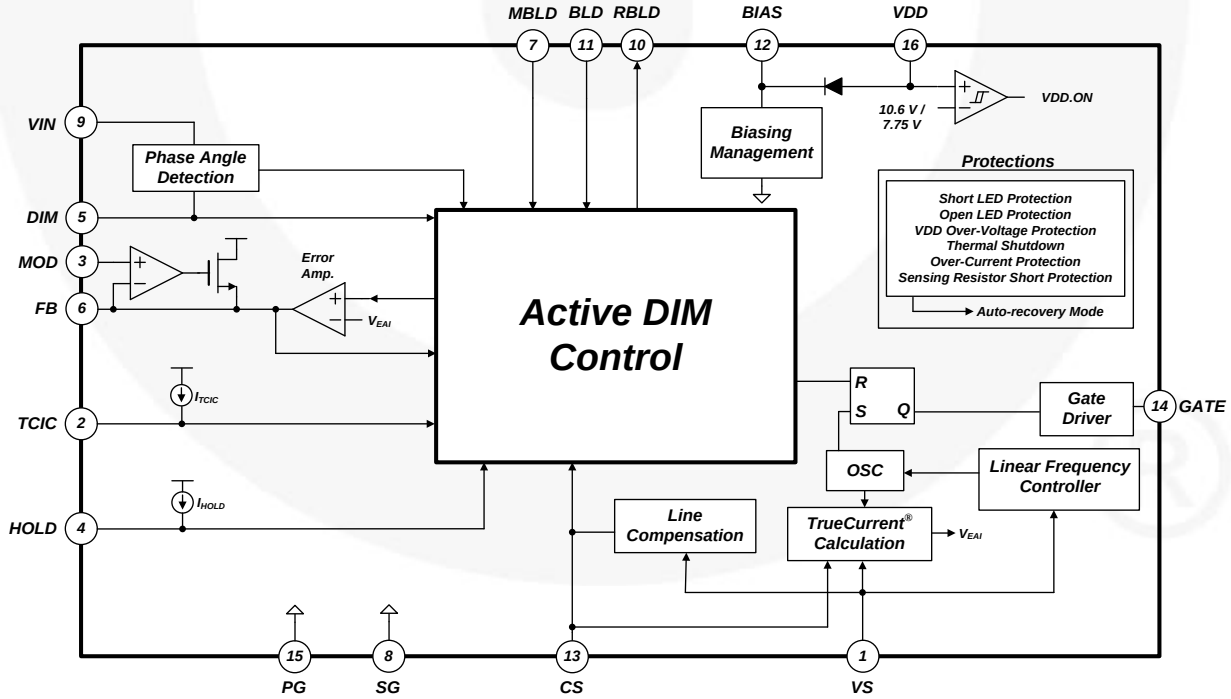
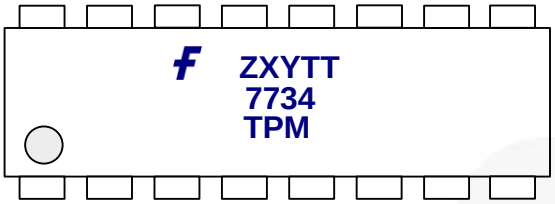



**Figure 2. Functional Block Diagram**

## Marking Information




*F*: Fairchild Logo
Z: Plant Code
X: 1-Digit Year Code
Y: 1-Digit Week Code
TT: 2-Digit Die Run Code
T: Package Type (M=SOP)
P: Z: Pb free, Y: Green package
M: Manufacture Flow Code

**Figure 3. Top Mark**

## Pin Configuration

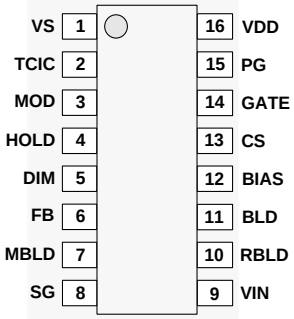



**Figure 4. Pin Configuration**

## Pin Definitions

| Pin # | Name | Description |
|---|---|---|
| 1 | VS | **Voltage Sense**. VS pin detects the output voltage for linear frequency control and discharge time for output current regulation. VS voltage detection protects LED open and short conditions. |
| 2 | TCIC | **Constant Input Current**. TCIC manages switching mode control. |
| 3 | MOD | **Modulation**. Min. FB is clamped by MOD voltage. |
| 4 | HOLD | **Holding Current**. External HOLD resistor sets the level of constant input current. |
| 5 | DIM | **Phase Angle Sense**. DIM voltage indicates the amount of phase angle. It is the reference voltage of the error amplifier in the feedback loop. |
| 6 | FB | **Feedback**. FB is the output of the error amplifier. |
| 7 | MBLD | **Maximum Bleeding**. Resistor connected to MBLD determines maximum bleeding current. |
| 8 | SG | **Signal Ground**. |
| 9 | VIN | **Input Voltage Sense**. VIN pin detects input voltage for phase angle detection. |
| 10 | RBLD | **Bleeding Control Resistor**. RBLD current set by external resistor decides the amount of bleeding current. |
| 11 | BLD | **Bleeding Control**. BLD flows current into RBLD. |
| 12 | BIAS | **Bleeding Circuit BIAS**. External bleeding switch is biased by an internal clamping circuit via BIAS pin. |
| 13 | CS | **Current Sense**. CS pin connects a current-sense resistor to detect the MOSFET current for the output current regulation. Over-current protection and sensing resistor short protection are triggered by this pin. |
| 14 | GATE | **PWM Signal Output**. Gate driver in this pin switches power MOSFET. |
| 15 | PG | **Power Ground**. |
| 16 | VDD | **Power Supply**. Connects to a decoupling capacitor. IC operating current and MOSFET driving current are supplied from this pin. |

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## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{VDD}$ | DC Supply Voltage[1,2] | | -0.3 | 30 | V |
| $V_{DIM}$ | DIM Pin Input Voltage | | -0.3 | 6.0 | V |
| $V_{MOD}$ | MOD Pin Input Voltage | | -0.3 | 6.0 | V |
| $V_{HOLD}$ | HOLD Pin Input Voltage | | -0.3 | 6.0 | V |
| $V_{TCIC}$ | TCIC Pin Input Voltage | | -0.3 | 6.0 | V |
| $V_{FB}$ | FB Pin Input Voltage | | -0.3 | 6.0 | V |
| $V_{RBLD}$ | RBLD Pin Input Voltage | | -0.3 | 6.0 | V |
| $V_{BIAS}$ | BIAS Pin Input Voltage | | -0.3 | 30.0 | V |
| $V_{BLD}$ | BLD Pin Input Voltage | | -0.3 | 30.0 | V |
| $V_{MBLD}$ | MBLD Pin Input Voltage | | -0.3 | 6.0 | V |
| $V_{VS}$ | VS Pin Input Voltage | | -0.3 | 6.0 | V |
| $V_{CS}$ | CS Pin Input Voltage | | -0.3 | 6.0 | V |
| $V_{GATE}$ | GATE Pin Input Voltage | | -0.3 | 30.0 | V |
| $V_{VIN}$ | VIN Pin Input Voltage | | -0.3 | 30.0 | V |
| $P_D$ | Power Dissipation ($T_A < 50°C$) | | | 909 | mW |
| $\theta_{JA}$ | Thermal Resistance (Junction to Air) | | | 110 | °C /W |
| $T_J$ | Maximum Junction Temperature | | | 150 | °C |
| $T_{STG}$ | Storage Temperature Range | | -55 | 150 | °C |
| $T_L$ | Lead Temperature (Soldering, 10 Seconds) | | | 260 | °C |
| ESD | Electrostatic Discharge Capability | Human Body Model, ANSI/ESDA/JEDEC JS-001-2012 | | 5 | kV |
| | | Charged Device Model, JESD22-C101 | | 2 | |

**Notes:**
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to the GND pin.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_A$ | Operating Ambient Temperature | -40 | 125 | °C |

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## Electrical Characteristics

$V_{DD}$=20 V and $T_J$=-40 ~ 125°C unless otherwise specified.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **VDD Section** | | | | | | |
| $V_{DD-ON}$ | Turn-On Threshold Voltage | | 9.1 | 10.6 | 12.1 | V |
| $V_{DD-OFF}$ | Turn-Off Threshold Voltage | | 6.75 | 7.75 | 8.75 | V |
| $I_{DD-OP}$ | Operating Current | $C_{LOAD}$=1 nF | 4 | 5 | 6 | mA |
| $I_{DD-ST}$ | Startup Current | $V_{DD}$=6 V | - | 2 | 10 | µA |
| $V_{DD-OVP}$ | $V_{DD}$ Over-Voltage-Protection | | 25 | 27 | 29 | V |
| $V_{BIAS-VDD-OFF}$ | BIAS Clamp Voltage at VDD-OFF | $V_{IN}$[3]=30 V, $R_{BIAS}$=20 kΩ | 21.3 | 24.4 | 27.5 | V |
| $V_{BIAS-VDD-ON}$ | BIAS Clamp Voltage at VDD-ON | $V_{IN}$[3]=30 V, $R_{BIAS}$=20 kΩ | 17.6 | 19.5 | 21.4 | V |
| **Gate Section** | | | | | | |
| $V_{OL}$ | Output Voltage Low | $I_{GATE}$=-1 mA | | | 1.5 | V |
| $V_{OH}$ | Output Voltage High | $I_{GATE}$=+1 mA, $V_{DD}$=10 V | 5 | | | V |
| $I_{source}$ | Peak Sourcing Current[4] | | | 60 | | mA |
| $I_{sink}$ | Peak Sinking Current[4] | | | 180 | | mA |
| $t_r$ | Rising Time | $C_{LOAD}$=1 nF | 100 | 150 | 200 | ns |
| $t_f$ | Falling Time | $C_{LOAD}$=1 nF | 20 | 60 | 100 | ns |
| $V_{GATE-CLAMP}$ | GATE Clamp Voltage | $V_{DD}$=20 V | 12 | 15 | 18 | V |
| **Oscillator Section** | | | | | | |
| $f_D$ | Operating Frequency at D.Mode | $T_J$=25°C | 65 | 70 | 75 | kHz |
| $f_{ND-MAX}$ | Max. Frequency at ND.Mode | $T_J$=25°C | 65 | 70 | 75 | kHz |
| $f_{ND-MIN}$ | Min. Frequency at ND.Mode | $T_J$=25°C | 26 | 29.5 | 33 | kHz |
| $t_{ON-MAX}$ | Maximum Turn-On Time | $T_J$=25°C | 10.4 | 12.4 | 14.4 | µs |
| $t_{ON-MIN}$ | Minimum Turn-On Time[4] | $V_{FB}$=0 V | | 600 | | ns |
| **Current Sense Section** | | | | | | |
| $t_{LEB}$ | Leading-Edge Blanking Time[4] | | | 300 | | ns |
| $t_{PD}$ | Propagation Delay to GATE | | 50 | 100 | 150 | ns |
| $V_{CS}/I_{VS}$ | Line Compensation Ratio[4] | | | 21.5 | | V/A |
| **Voltage Sense Section** | | | | | | |
| $t_{DIS-BNK}$ | $t_{DIS}$ Blanking Time at VS Sampling[4] | | | 1.5 | | µs |
| $I_{VS-BNK}$ | VS Current for VS Blanking | | 67 | 80 | 93 | µA |
| $V_{VS-CLAMP}$ | VS Clamping Voltage | $I_{VS}$=1 mA | -0.1 | | | V |
| | | $I_{VS}$=10 µA | | | 0.35 | V |

**Notes:**

3. $V_{IN}$ is external voltage source and $R_{BIAS}$ is connected between $V_{IN}$ and BIAS pin.
4. This parameter, although design-guaranteed, is not tested in production.

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## Electrical Characteristics

$V_{DD}$=20 V and $T_J$=-40 ~ 125°C unless otherwise specified.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Feedback Section** | | | | | | |
| $g_M$ | Transconductance | | 14 | 18 | 22 | μmho |
| $I_{FB-SINK}$ | FB Sink Current | $T_J$=25°C, $V_{EAI}$=2 V, $V_{FB}$=2.5 V | 14 | 18 | 22 | μA |
| $I_{FB-SOURCE}$ | FB Source Current | $V_{EAI}$=0 V, $V_{FB}$=2.5 V | 14 | 18 | 22 | μA |
| $V_{FB-HGH}$ | FB High Voltage(4) | | 4.7 | | | V |
| $V_{FB-LOW}$ | FB Low Voltage(4) | | | | 0.1 | V |
| **Start Sequence Section** | | | | | | |
| $t_{SS1-MIN}$ | Minimum Start Sequence Time 1 | | 10.8 | 12.0 | 13.2 | ms |
| $t_{SS3-MIN}$ | Minimum Start Sequence Time 3 | | 13.5 | 15.0 | 16.5 | ms |
| $V_{FB-ADJ-NDM}$ | FB Adjustment Voltage in ND.MODE | | 1.26 | 1.40 | 1.54 | V |
| **Protection Section** | | | | | | |
| $V_{CS-HIGH-CL}$ | High Current Limit Threshold | | 1.08 | 1.20 | 1.32 | V |
| $V_{CS-LOW-CL}$ | Low Current Limit Threshold | | 0.15 | 0.20 | 0.25 | V |
| $V_{CS-OCP}$ | Over Current Protection Voltage | | | 1.8 | | V |
| $V_{VS-LOW-CL-H}$ | Low Current Limit Hys. Voltage 'H'(4) | | 0.45 | 0.50 | 0.55 | V |
| $V_{VS-LOW-CL-L}$ | Low Current Limit Hys. Voltage 'L'(4) | | 0.35 | 0.40 | 0.45 | V |
| $V_{VS-SLP-TH}$ | VS Threshold Voltage for SLP | | 0.35 | 0.40 | 0.45 | V |
| $V_{VS-OVP}$ | VS Threshold Voltage for OVP | | 2.9 | 3.0 | 3.1 | V |
| $t_{AR-DELAY}$ | Auto Restart Delay Time(4) | | | 4.0 | | s |
| $V_{CS-SRSP}$ | CS Threshold Voltage for SRSP | | 0.05 | 0.10 | 0.15 | V |
| $T_{OTP}$ | Threshold Temperature for OTP(4)(5) | | | 150 | | °C |
| $T_{OTP-HYS}$ | Junction Temperature Hysteresis(4) | | | 10 | | °C |
| **Dimming Control Section** | | | | | | |
| $I_{DIM}$ | DIM Sourcing Current | $V_{DIM}$=3 V | 36 | 40 | 44 | μA |
| $V_{VIN-DIM}$ | DIM Current On/Off Voltage(4) | | | 3.00 | | V |
| $V_{DIM-CLAMP}$ | DIM Clamping Voltage | | | 3.25 | | V |
| $K_{HOLD}$ | HOLD Conversion Coefficient | $T_J$=25°C, $V_{CS}$=0.5 V, $R_{HOLD}$=31.5 kΩ | | 510 | | /mA |
| $I_{HOLD}$ | HOLD Sourcing Current | $V_{HOLD}$=3.5 V | 36 | 40 | 44 | μA |
| $I_{TCIC}$ | TCIC Sourcing Current | | 13.5 | 15.0 | 16.5 | μA |
| $V_{TCIC-MIN-DIS}$ | Minimum TCIC Discharging Voltage | | 0.9 | 1.0 | 1.1 | V |
| $V_{RBLD-CLAMP}$ | Clamped RBLD Voltage | $V_{VIN}$=5 V, $R_{RBLD}$=40 Ω | 0.45 | 0.50 | 0.55 | V |
| $I_{MBLD}$ | MBLD Current | $V_{MBLD}$=3.5 V | 36 | 40 | 44 | μA |

**Note:**

5. If over-temperature protection is activated, the power system enters Auto Recovery Mode and output is disabled. Device operation above the maximum junction temperature is NOT guaranteed.

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## Typical Performance Characteristics

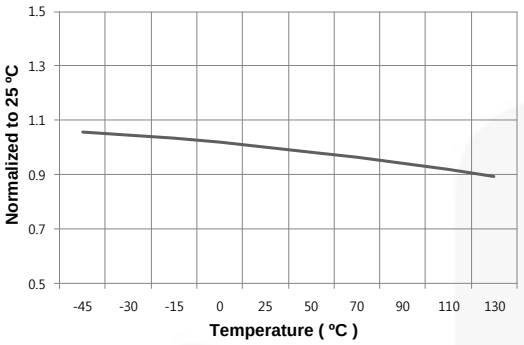


**Figure 5. $V_{DD-ON}$ vs. Temperature**

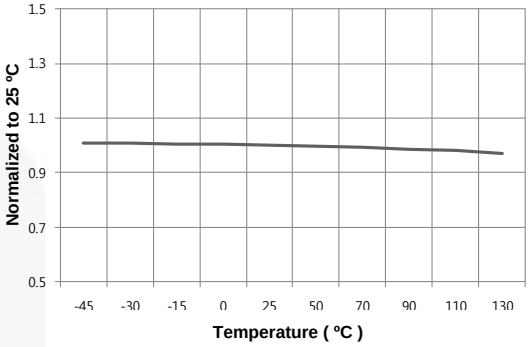


**Figure 6. $V_{DD-OFF}$ vs. Temperature**

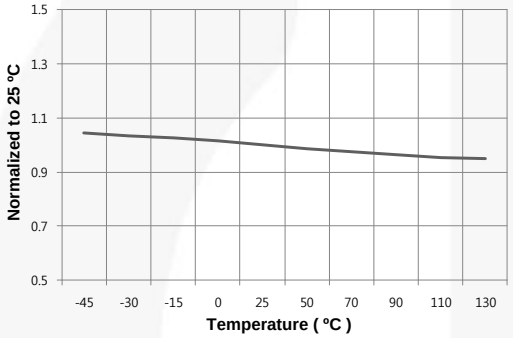


**Figure 7. $I_{DD-OP}$ vs. Temperature**

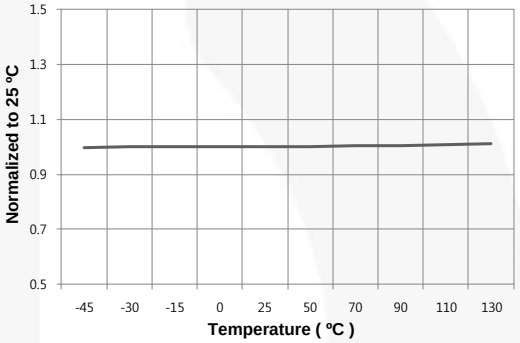


**Figure 8. $V_{DD-OVP}$ vs. Temperature**

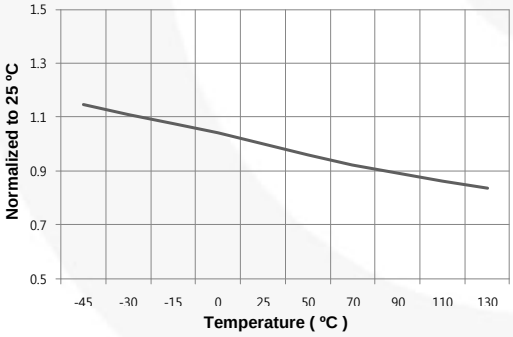


**Figure 9. $f_{ND-MAX}$ vs. Temperature**

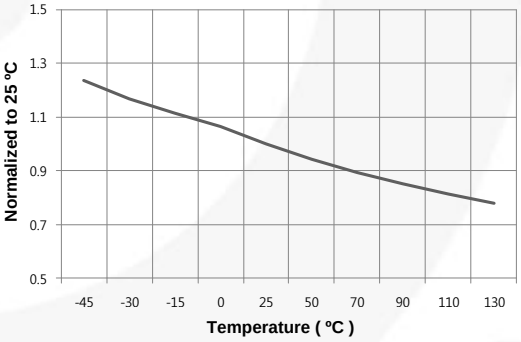


**Figure 10. $f_{ND-MIN}$ vs. Temperature**

## Typical Performance Characteristics

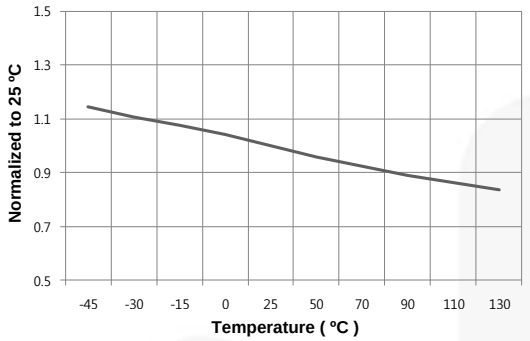


**Figure 11. $f_D$ vs. Temperature**

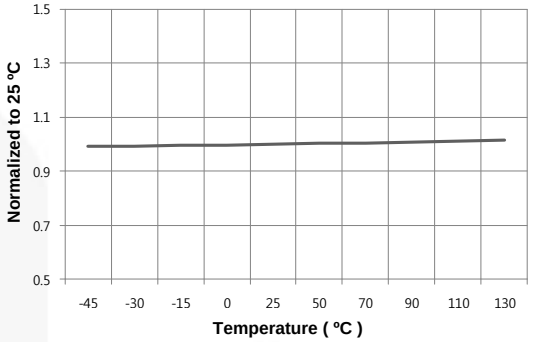


**Figure 12. $V_{CS\text{-}HIGH\text{-}CL}$ vs. Temperature**

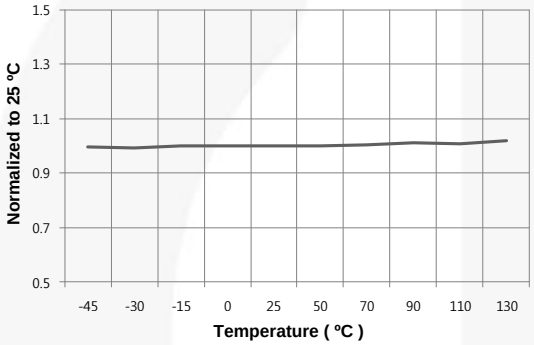


**Figure 13. $V_{VS\text{-}SLP\text{-}TH}$ vs. Temperature**

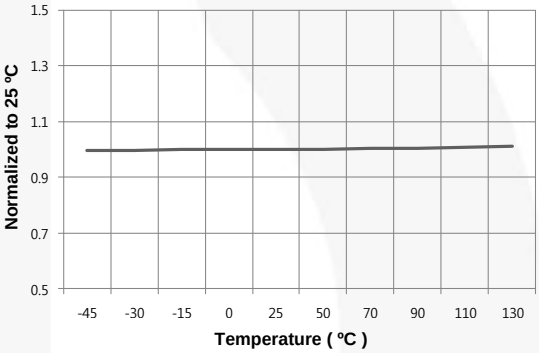


**Figure 14. $V_{VS\text{-}OVP}$ vs. Temperature**

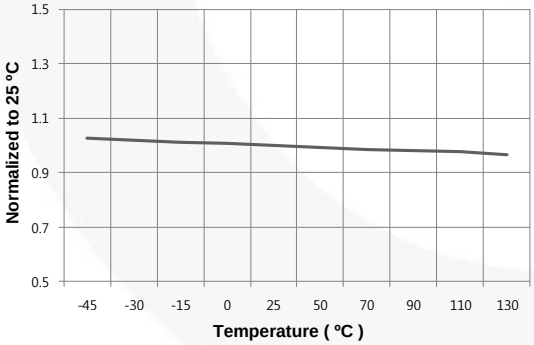


**Figure 15. $K_{HOLD}$ vs. Temperature**

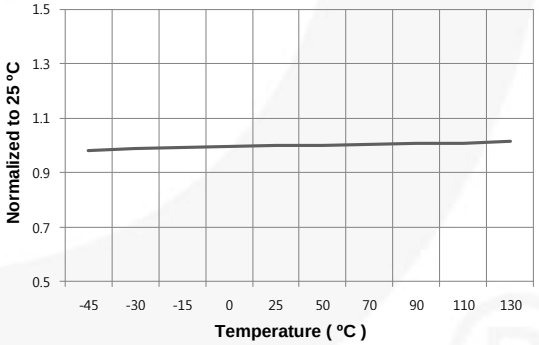


**Figure 16. $I_{HOLD}$ vs. Temperature**

## Functional Description

FL7734 is a phase-cut dimmable PWM controller for LED lighting applications. Accurate LED current regulation independent of input voltage, output voltage and magnetizing inductance variations is implemented by TRUECURRENT® technique. The controller features programmable dimming curve which ensures that the constant maximum LED current can be met at the various maximum phase angle conditions of each dimmer and low LED current can be set at the minimum phase angle condition with wide dimming range. Fairchild's proprietary constant input current control provides excellent dimmer compatibility by maintaining input current higher than TRIAC holding current. The linear frequency control and DCM operation with minimized turn-on time ripple implements best power factor and THD in a single-stage topology. A variety of protections; such as short-LED protection, open-LED protection, sensing resistor open/short protection, over-temperature protection, and cycle-by-cycle current limitation stabilize system operation and protect external components.

### Startup

An external bleeding MOSFET is utilized for fast startup. Once power is on, BIAS voltage is quickly lifted to $V_{BIAS-VDD-OFF}$ (24.4 V) so the bleeding MOSFET can charge the VDD capacitor higher than $V_{DD-ON}$ voltage (10.6 V). Once $V_{DD}$ is higher than $V_{DD-ON}$, Startup Sequence (SS1) begins with maximum bleeding current to stabilize dimmer operation. SS1 ends when $V_{IN}$ reaches the line voltage zero crossing after $t_{SS1-MIN}$ (12 ms).

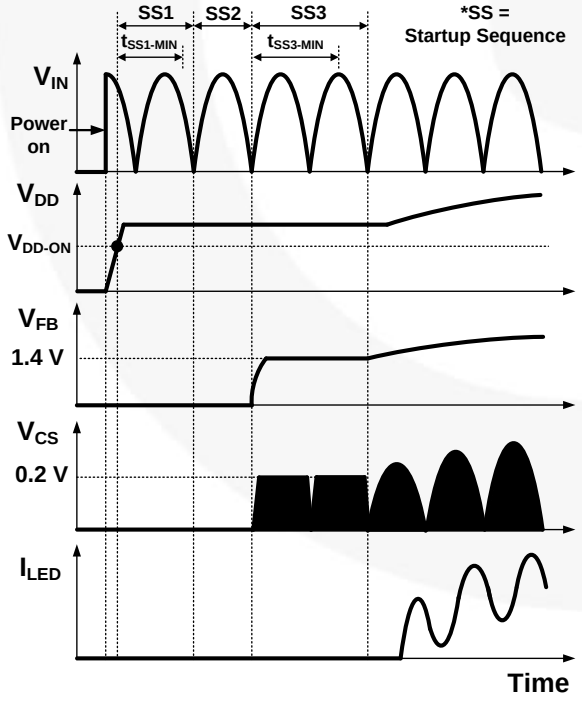


**Figure 17. Startup Sequence**

During SS2 which is defined as a half line period, FL7734 determines whether phase-cut dimmer is connected in the line. From SS3, internal operation is set as either dimming mode or non-dimming mode. SS3 time is set longer than $t_{SS3-MIN}$ which is counted except for phase-cut time and finishes synchronized with $V_{IN}$ zero crossing. 0.2 V current-mode is activated during SS3 so that output voltage reaches a level higher than threshold for short-LED protection, which is enabled after SS3. In the mean time, FB voltage is clamped to 1.4 V at non-dimming mode or a certain level proportional to phase angle at dimming mode to set the voltage closer to steady-state level. The maximum bleeding current is disabled after SS3 and voltage mode control is enabled at non-dimming mode and constant input current control is enabled at dimming mode.

### Constant-Current Regulation

The output current is estimated using the peak drain current and inductor current discharge time because output current is same as the average of the diode current in steady-state. The peak value of the drain current is determined by the CS pin. The inductor discharge time ($t_{dis}$) is sensed by a $t_{dis}$ detector. Using three sources of information; peak drain current, inductor discharging time, and operating switching period, the TRUECURRENT® block calculates the estimated output current. The output of the calculation is compared with an internal precise reference to generate an error voltage ($V_{FB}$). With Fairchild's innovative TRUECURRENT® technique, constant LED current can be precisely controlled.

### Constant Input Current Control

Fairchild's proprietary Constant Input Current (CIC) control generates switching duty to form input current proportional to the external resistor value at HOLD pin. Filtered switch current is the system input current and the system input current is adjusted by the calculation of CS average voltage. Input current is determined by equation (1) where $K_{HOLD}$ is coefficient of internal calculation.

$$I_{IN} = \frac{R_{HOLD}}{R_{CS} \cdot K_{HOLD}} \quad (1)$$

Fairchild's CIC control offers superior accurate and stable current management than other input current control technologies.

### Dimming Control

Phase angle is detected by comparing VIN voltage and 3 V threshold voltage ($V_{VIN-DIM}$). When VIN voltage is higher than 3 V, DIM sourcing current ($I_{DIM}$) is connected to the DIM pin and the current flows into external resistors ($R_{DIM1}$ and $R_{DIM2}$) and capacitor ($C_{DIM}$). Therefore, the DIM voltage filtered by $C_{DIM}$ indicates the amount of phase angle controlled by phase-cut dimmer.

$$V_{DIM} = I_{DIM} \cdot (R_{DIM1} + R_{DIM2}) \cdot \frac{PA}{180^{\circ}} \quad (2)$$

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As a function of dimming reference modulation shown in Figure 18, output current is constantly regulated with constant $V_{REF}$ when $V_{DIM}$ is higher than 3 V and $V_{REF}$ is set lower than $V_{EAI}$ (TRUECURRENT® calculation result) when $V_{DIM}$ is lower than 2.25 V. Once $V_{DIM}$ is less than 2.25 V, the error amplifier always pulls down current in the output and FB voltage is clamped by MOD voltage so that open loop control starts for stable LED current control at low phase angle range.

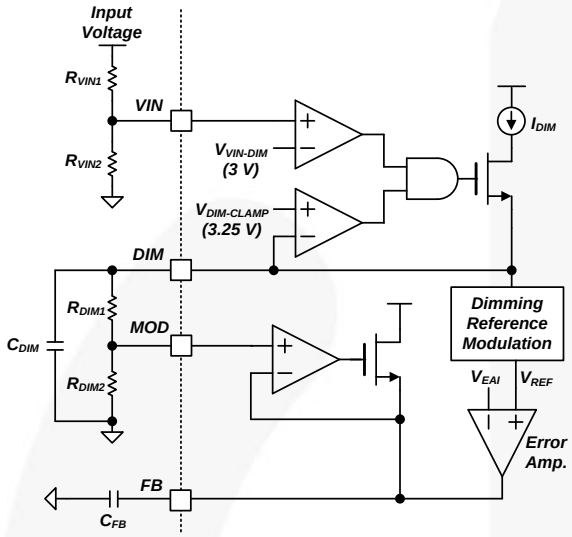


**Figure 18. Dimming Control**

High dimmer compatibility is implemented by bleeding current generated through BLD to RBLD and having the switching mode management by TCIC.

## PFC and THD

In a conventional boost converter, Boundary Conduction Mode (BCM) is generally used to keep input current in phase with input voltage for Power Factor (PF) and Total Harmonic Distortion (THD). However, BCM switching distorts input current in the single stage flyback / buck boost converter because power inductor current is not the same as input current. Moreover, it becomes more difficult to meet PF and THD once passive bleeder (resistor and capacitor in the driver input) is added for successful firing in the single stage TRIAC dimming system.

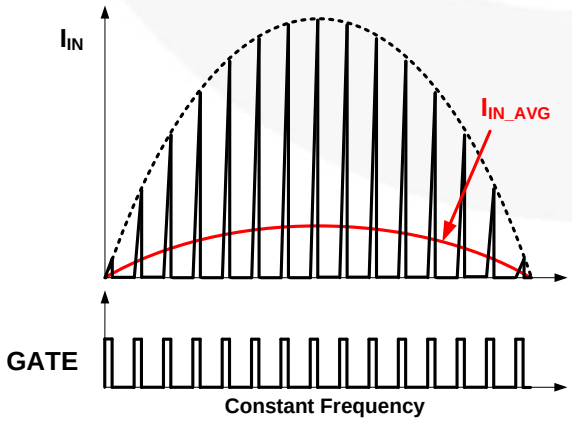


**Figure 19. PFC Control in DCM**

In order to optimize PF and THD in the single stage flyback topology, constant turn-on time and constant frequency in Discontinuous Conduction Mode (DCM) are the best method to make the input current proportional to the input voltage as shown in Figure 19. FL7734 basically adopts the DCM operation with constant turn-on and frequency in a half line cycle. Once dimmer absence is detected during startup sequence, FL7734 selects voltage mode in which constant turn-on time is maintained by an internal error amplifier and a large external capacitor (typically >1 µF) at the FB pin. Constant frequency and DCM operation are managed by linear frequency control.

## Linear Frequency Control

DCM should be guaranteed for high power factor in flyback topology. To maintain DCM in the wide range of output voltage, frequency is linearly adjusted by output voltage in linear frequency control. Output voltage is detected by auxiliary winding and resistive divider connected to the VS pin, as shown in Figure 20. When output voltage decreases, secondary diode conduction time is increased and the linear frequency control lengthens switching period, which retains DCM operation in the wide output voltage range. The frequency control lowers primary rms current for better power efficiency in full-load condition.

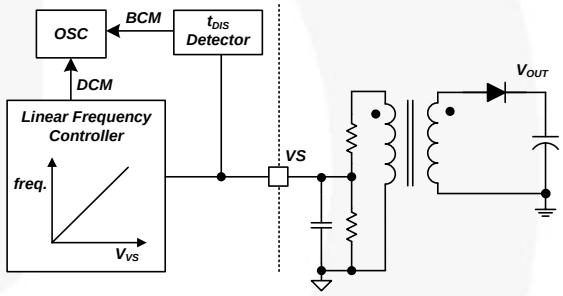


**Figure 20. Linear Frequency Control**

## BCM Control

The end of secondary diode conduction time ($t_{DIS}$) can be over a switching period set by linear frequency control. In this case, FL7734 doesn't allow CCM and operation mode changes from DCM to BCM. Therefore, magnetizing inductance can be largely designed to add BCM for better efficiency if PF and THD meet specification with enough margin.

## Short-LED Protection

In a short-LED condition, the switching MOSFET and secondary diode are usually stressed by the high powering current.

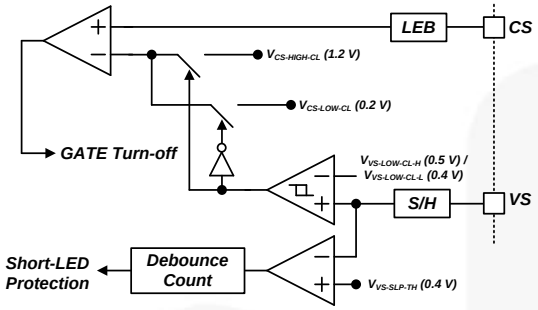


**Figure 21. Short LED Protection**

FL7734 changes the current-limit level in a short-LED condition. When sampled VS voltage is lower than $V_{VS-LOW-CL-L}$ (0.4 V), the current-limit level is reduced to 0.2 V from 1.2 V, as shown in Figure 21 so that powering is limited and external components' current stress is relieved. When the sampled VS voltage is continuously lower than $V_{VS-SLP-TH}$ (0.4 V) for 3 consecutive switching cycles, short-LED protection is triggered with gate shutdown. After all types of protection including short-LED protection is triggered, FL7734 internally counts 4 seconds for auto restart and begins startup sequence again.

## Open-LED Protection

When output load is open as high impedance, the output capacitor should be protected by limiting the capacitor voltage less than its maximum rating. FL7734 can detect the output over-voltage condition by sensing both VDD and VS voltages. When VDD voltage is higher than $V_{DD-OVP}$ (27 V typical) or sampled VS voltage is higher than $V_{VS-OVP}$ (3 V typical), protection is triggered. The protection mode is auto restart so normal operation resumes when the fault condition is removed.

## Sensing Resistor Short Protection

During SS3, the controller operates in current-mode control and the peak CS voltage is 0.2 V during switching mode. When a sensing resistor is short circuited, CS voltage cannot reach 0.2 V and turn on time is maximized with potential damage of switching MOSFET. In order to provide protection against the failure, FL7734 compares CS voltage with $V_{CS-SRSP}$ (0.1 V) during the initial two switching operation. When VCS doesn't reach 0.1 V for the two switching, Sensing Resistor Short Protection (SRSP) is triggered. In normal condition, input voltage corresponding to 1.5 V $V_{VIN}$ is high enough to make $V_{CS}$ higher than 0.1 V with turn-on time shorter than maximum turn-on time.

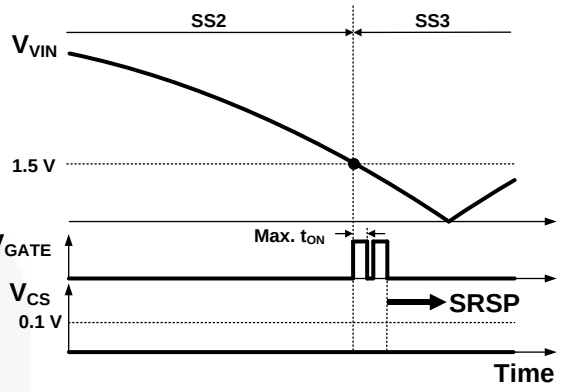


**Figure 22. Sensing Resistor Short Protection**

## Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 10.6 V and 7.75 V, respectively. During startup, the VDD capacitor must be charged higher than 10.6 V through the external bleeding MOSFET. The bleeding MOSFET supplies VDD operating current until power can be delivered from the auxiliary winding of the main transformer. Generally at small phase angle range, $V_{DD}$ supply time from auxiliary winding is short and $V_{DD}$ could reach to $V_{DD-OFF}$ (7.75 V). If $V_{DD}$ drops below $V_{DD-OFF}$, VDD hiccup occurs with a certain hiccup frequency determined by VDD capacitor value and VDD supply current from auxiliary winding. This hiccup mode could cause LED flicker. In order to remove the unstable mode of operation, external bleeding circuit never allows $V_{DD}$ voltage to fall down less than $V_{DD-OFF}$ (7.75 V) once input power is supplied.

## Over-Temperature Protection (OTP)

The built-in temperature-sensing circuit shuts down PWM output if the junction temperature exceeds 150°C. After Over-Temperature Protection (OTP) is triggered, FL7734 repeats auto-restart time counting until the junction temperature is lowered less than 140°C. Different from Short/Open-LED protection and SRSP, startup sequence doesn't appear every 4 seconds of auto-restart delay time because the temperature is detected by monitoring internally, not by checking external pin information. Normal startup sequence is started again when the junction temperature is out of the hysteresis temperature (140°C).

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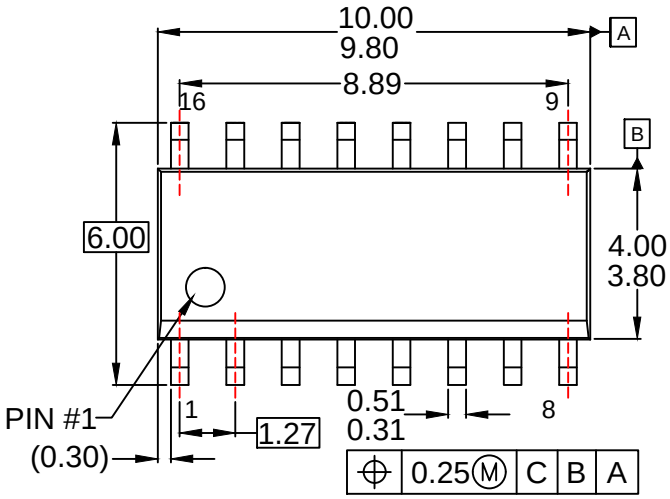
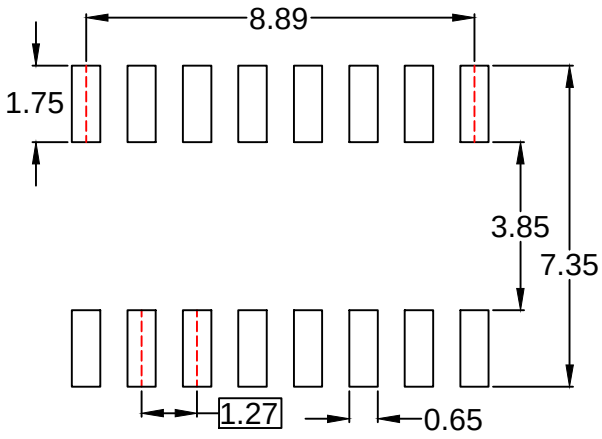
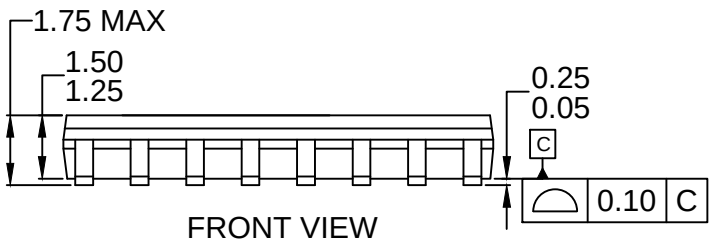


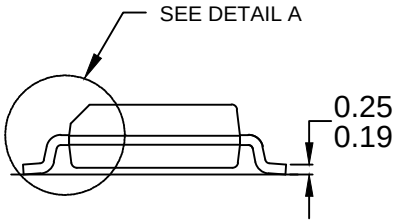

TOP VIEW

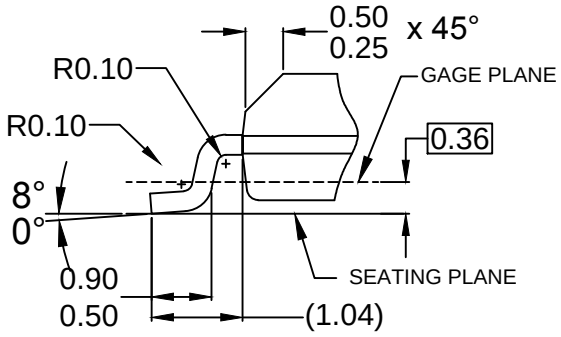



LAND PATTERN RECOMMENDATION




FRONT VIEW




DETAIL A

SCALE: 2:1

NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS

D) CONFORMS TO ASME Y14.5M-2009

E) LANDPATTERN STANDARD: SOIC127P600X175-16AM

F) DRAWING FILE NAME: M16AREV13.

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