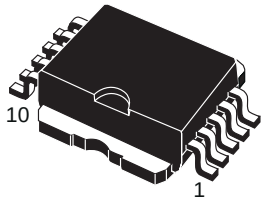
STV160NF03LA

N-CHANNEL 30V - 0.0021Ω - 160A PowerSO-10
STripFET™ POWER MOSFET

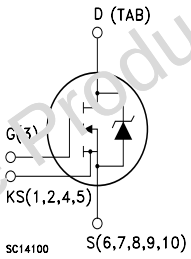
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STV160NF03LA	30 V	< 0.003 Ω	160 A

- TYPICAL $R_{DS}(on)$ = 0.0021 Ω
- LOW THRESHOLD DRIVE
- ULTRA LOW ON-RESISTANCE
- ULTRA FAST SWITCHING
- 100% AVALANCHE TESTED
- VERY LOW GATE CHARGE
- LOW PROFILE, VERY LOW PARASITIC INDUCTANCE PowerSO-10 PACKAGE

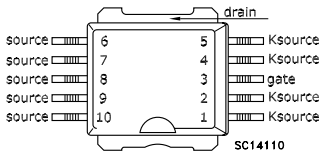


PowerSO-10

INTERNAL SCHEMATIC DIAGRAM



CONNECTION DIAGRAM (TOP VIEW)



DESCRIPTION

The **STV160NF03LA** represents the second generation of Application Specific STMicroelectronics well established STripFET™ process based on a very unique strip layout design. The resulting MOSFET shows unrivalled high packing density with ultra low on-resistance and superior switching charactestics. Process simplification also translates into improved manufacturing reproducibility. This device is particularly suitable for high current, low voltage switching application where efficiency is crucial

APPLICATIONS

- BUCK CONVERTERS IN HIGH PERFORMANCE TELECOM AND VRMs DC-DC CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	30	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	30	V
V_{GS}	Gate- source Voltage	± 15	V
I_D(**)	Drain Current (continuos) at T_C = 25°C	160	A
I_D	Drain Current (continuos) at T_C = 100°C	113	A
I_{DM} (●)	Drain Current (pulsed)	640	A
P_{TOT}	Total Dissipation at T_C = 25°C	210	W
	Derating Factor	1.4	W/°C
E_{AS} (1)	Single Pulse Avalanche Energy	330	mJ
T_{stg}	Storage Temperature	–65 to 175	°C
T_j	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area
Note: Marking will be STV160NF03AL

(1) V_{DD} = 35V, I_D = 45A, R_G = 22Ω , L = 330µH, Starting T_j=25°C
(**)Limited only maximum junction temperature allowed by PowerSO-10

Obsolete Product(s) - Obsolete Product(s)

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.71	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	50	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 15 V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V, I_D = 80 A		2.1	3	mΩ
		V_{GS} = 10 V, I_D = 45 A		2.05	3	mΩ
		V_{GS} = 8 V, I_D = 80 A		2.2	4	mΩ
		V_{GS} = 5 V, I_D = 40 A		4.2	7	mΩ
		V_{GS} = 10 V, I_D=80 A;T_j = 175 °C			6.6	mΩ
		V_{GS} = 8 V, I_D=80 A; T_j = 175 °C			8.8	mΩ
		V_{GS} = 5 V, I_D=40 A; T_j = 175 °C			15.4	mΩ
$I_{D(on)}$	On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, V_{GS} = 10V	160			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 80 A		210		S
R_g	Gate resistance	V_{DS} = 0 V, f = 1 MHz, V_{GS} = 0		1.1		Ω
C_{iss}	Input Capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		5350		pF
C_{oss}	Output Capacitance			1700		pF
C_{rss}	Reverse Transfer Capacitance			300		pF
C_{iss}	Input Capacitance	V_{DS} = 0 V, f = 1 MHz, V_{GS} = 0		8200		pF
C_{oss}	Output Capacitance			12400		pF
C_{rss}	Reverse Transfer Capacitance			5200		pF
L_S	Internal Source Inductance	From the Lead End (6mm from Package Body) to the Die Center		3		nH
L_D	Internal Drain Inductance		Not Available on Surface Mounting Package			

Obsolete Product(s) - Obsolete Product(s)

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 15 V, I_D = 80 A		30		ns
t_r	Rise Time	R_G = 4.7Ω V_{GS} = 10V (see test circuit, Figure 3)		380		ns
Q_g	Total Gate Charge	V_{DD} = 24 V, I_D = 160 A, V_{GS} = 10 V		123	160	nC
Q_{gs}	Gate-Source Charge			21		nC
Q_{gd}	Gate-Drain Charge			40		nC

SWITCHING OFF

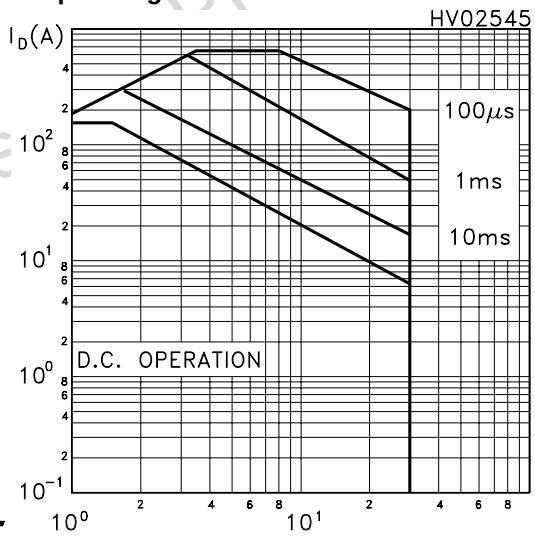
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	V_{DD} = 15 V, I_D = 80 A,		100		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 10 V (see test circuit, Figure 5)		150		ns
$t_{d(off)}$	Turn-off Delay Time	Vclamp = 24 V, I_D = 40 A		95		ns
$t_{r(Voff)}$	Off-voltage Rise Time	R_G = 4.7Ω, V_{GS} = 10V		35		ns
t_f	Fall Time			75		ns
t_c	Cross-over Time			110		ns

SOURCE DRAIN DIODE

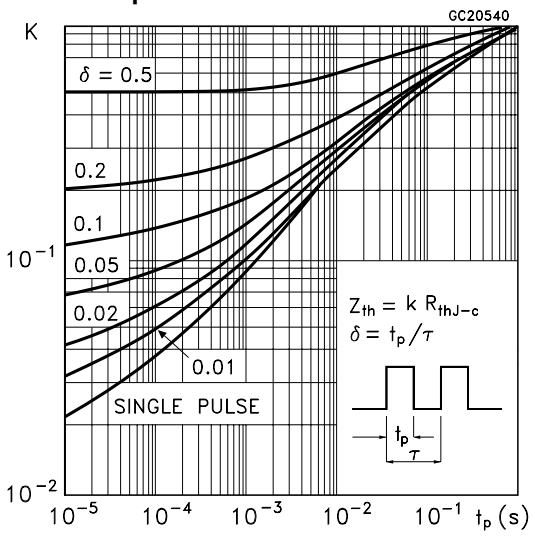
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				160	A
I_{SDM} (1)	Source-drain Current (pulsed)				640	A
V_{SD} (2)	Forward On Voltage	I_{SD} = 160 A, V_{GS} = 0			1.5	V
t_{rr}	Reverse Recovery Time	I_{SD} = 160A, di/dt = 100A/µs, V_{DD} = 15V, T_j = 25°C (see test circuit, Figure 5)		80		ns
Q_{rr}	Reverse Recovery Charge			180		nC
I_{RRM}	Reverse Recovery Current			4.5		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Safe Operating Area

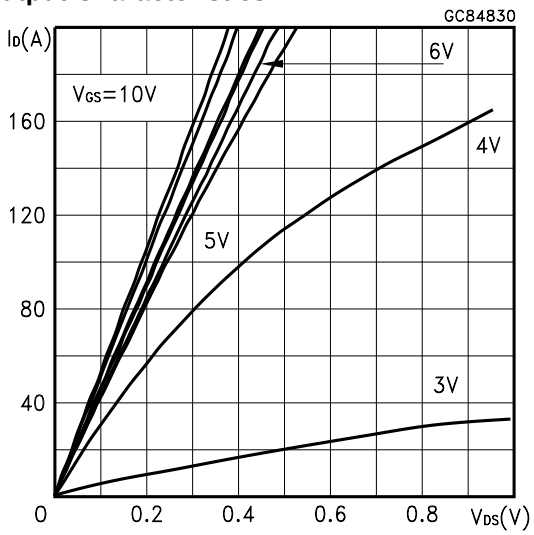


Thermal Impedance

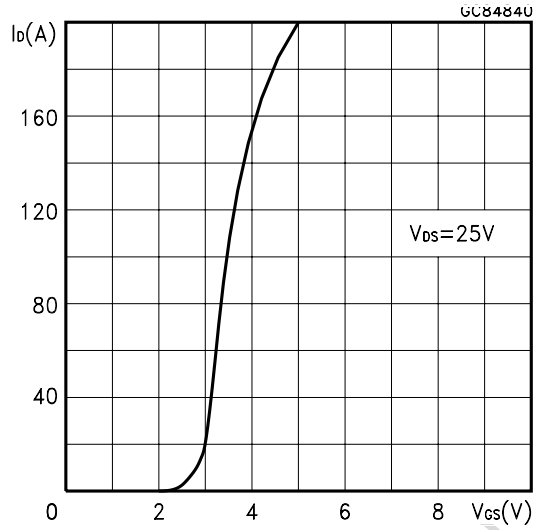


Obsolete Product(s) - Obsolete Product(s)

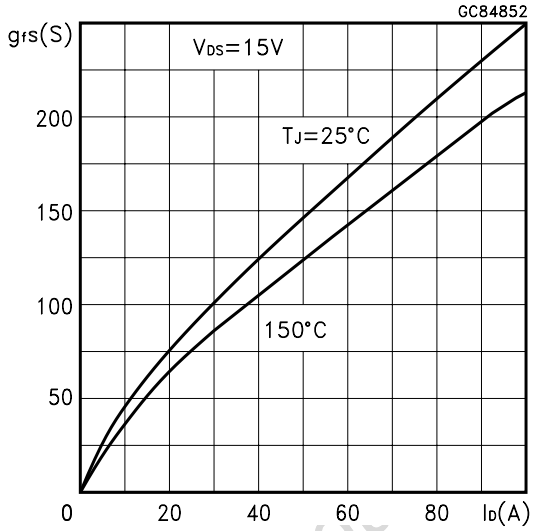
Output Characteristics



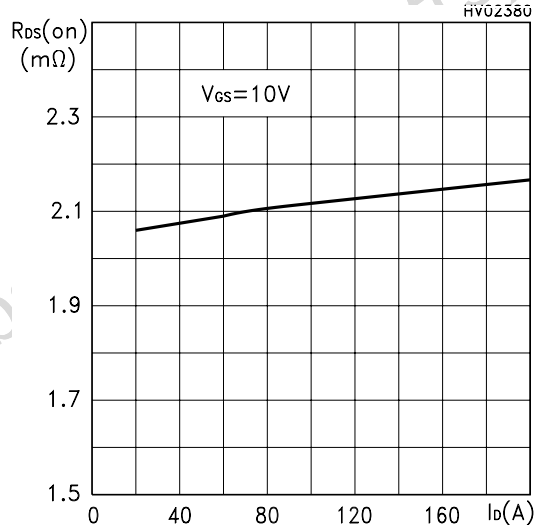
Tranfer Characteristics



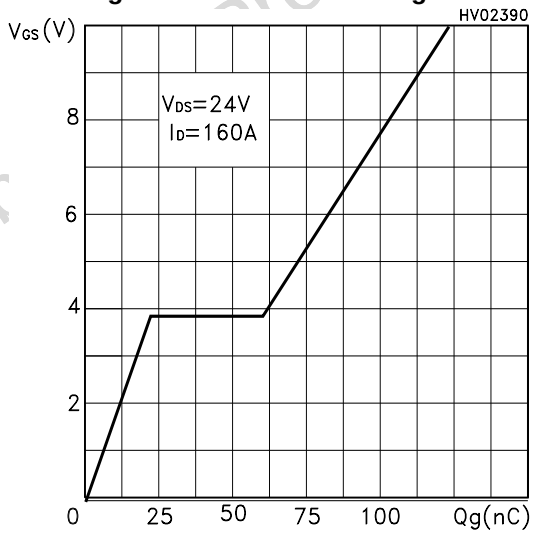
Tranconductance



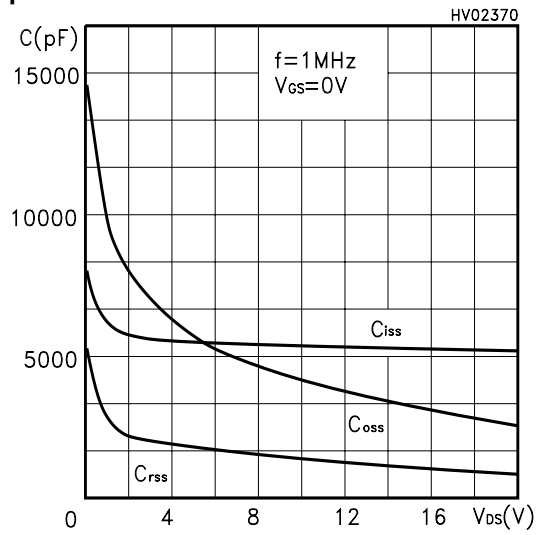
Static Drain-Source On Resistance



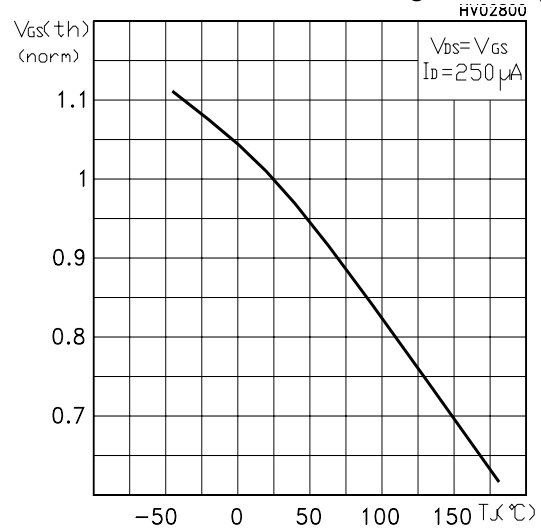
Gate Charge vs Gate-source Voltage



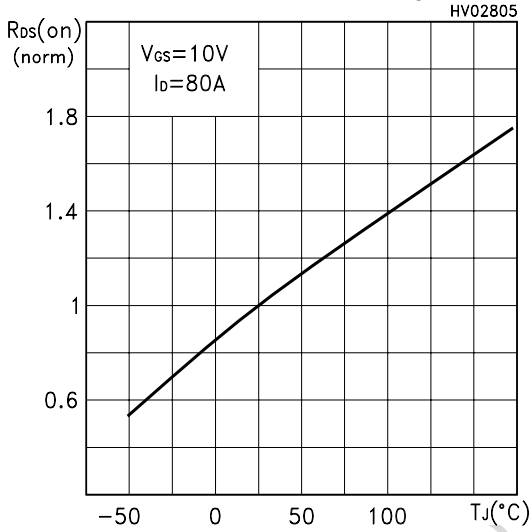
Capacitance Variations



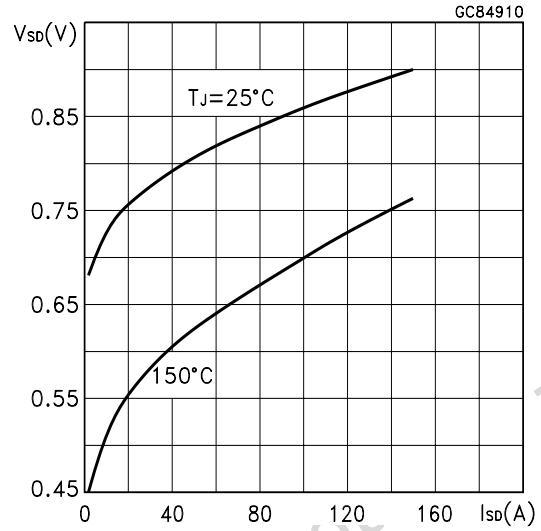
Normalized Gate Thereshold Voltage vs Temp.



Normalized On Resistance vs Temperature

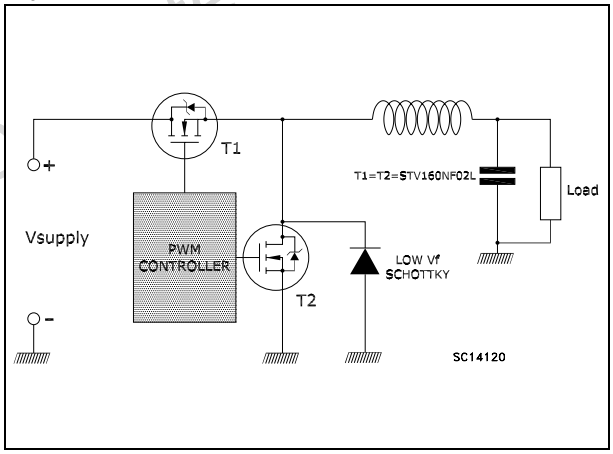


Source-drain Diode Forward Characteristics



Obsolete Product(s)

Basic Schematic For Motherboard VRM Whith Synchronous Rectification



Basic Schematic Mosfets Switch Used In Secondary Side Of a Froward Convert

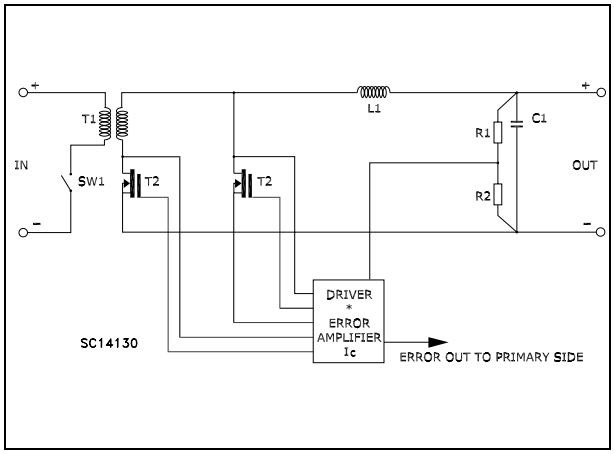


Fig. 1: Unclamped Inductive Load Test Circuit

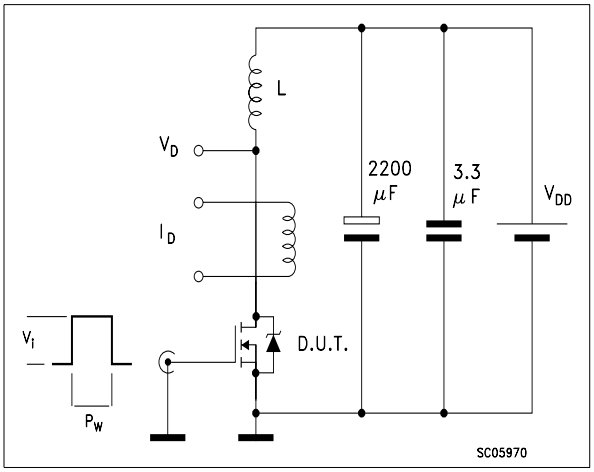


Fig. 2: Unclamped Inductive Waveform

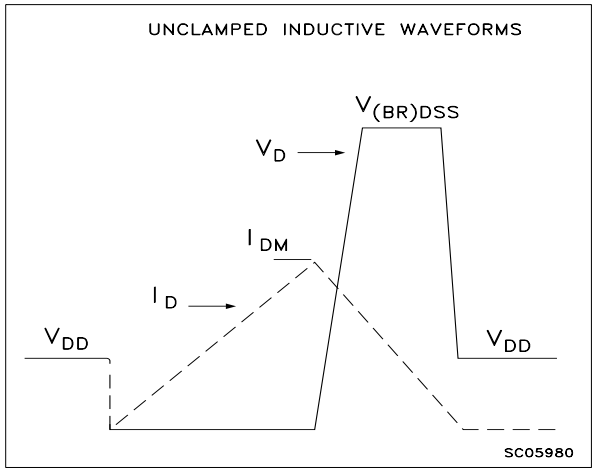


Fig. 3: Switching Times Test Circuit For Resistive Load

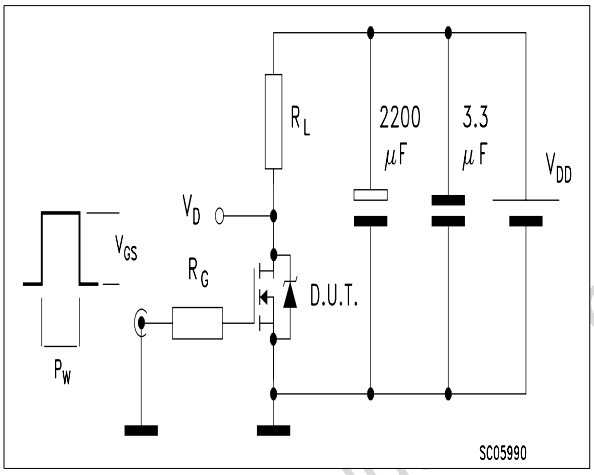


Fig. 4: Gate Charge test Circuit

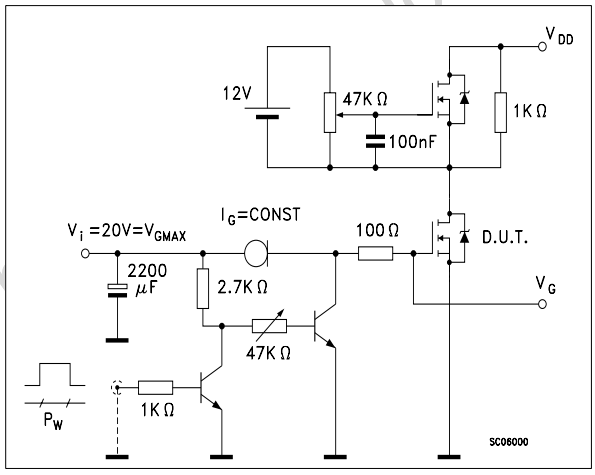
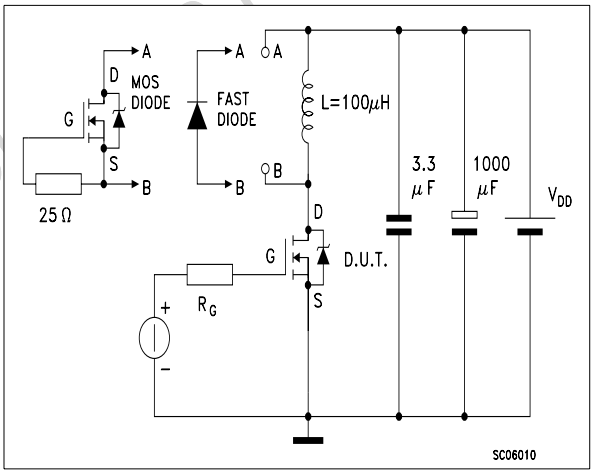
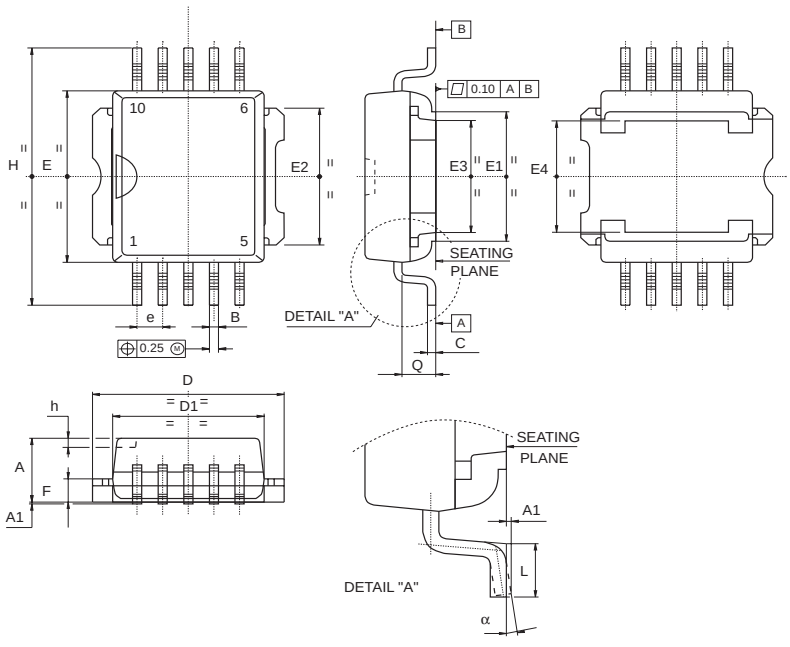


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



PowerSO-10 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
C	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
e		1.27			0.050	
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
F	1.25		1.35	0.049		0.053
h		0.50			0.002	
H	13.80		14.40	0.543		0.567
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
α	0°		8°			



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