# NSPM6201

# Surge and ESD Protection Diode

**Features**

- Protection for the following IEC Standards:
  IEC61000−4−2 Level 4: ±30 kV Contact Discharge
  IEC61000−4−5 (Lightning) 100 A (8/20 μs)
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

**MAXIMUM RATINGS**

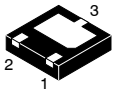
| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| IEC 61000−4−2 (ESD) | Contact<br>Air | | ±30<br>±30 | kV |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | −65 to +150 | °C |
| Maximum Peak Pulse Current 8/20 μs @ $T_A$ = 25°C | | $I_{PP}$ | 100 | A |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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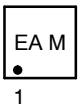
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**UDFN3**
**CASE 517DN**

**MARKING DIAGRAM**




EA = Specific Device Code
M = Date Code

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NSPM6201MUTBG | UDFN3<br>(Pb−Free) | 3000 / Tape & Reel |

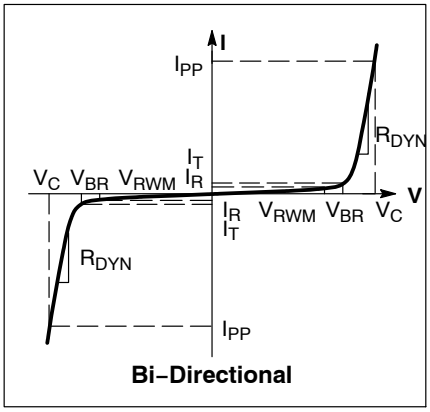
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## ELECTRICAL CHARACTERISTICS
($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter |
|---|---|
| $I_{PP}$ | Maximum Reverse Peak Pulse Current |
| $V_C$ | Clamping Voltage @ $I_{PP}$ |
| $V_{RWM}$ | Working Peak Reverse Voltage |
| $I_R$ | Maximum Reverse Leakage Current @ $V_{RWM}$ |
| $V_{BR}$ | Breakdown Voltage @ $I_T$ |
| $I_T$ | Test Current |

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Bi−Directional

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Reverse Working Voltage | $V_{RWM}$ | I/O Pin to Pin 3 | | | 20 | V |
| Breakdown Voltage | $V_{BR}$ | $I_T$ = 1 mA, I/O Pin to Pin 3 | 21 | 24 | 27 | V |
| Reverse Leakage Current | $I_R$ | $V_{RWM}$ = 20 V | | | 1.0 | μA |
| Clamping Voltage (Note 1) | $V_C$ | $I_{PP}$ = 50 A, $t_p$ = 8 x 20 μs | | | 34 | V |
| Clamping Voltage (Note 1) | $V_C$ | $I_{PP}$ = 100 A, $t_p$ = 8 x 20 μs | | 36 | 39 | V |
| Clamping Voltage TLP (Note 2) | $V_C$ | $I_{PP}$ = 8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±8 kV Air) | | 26.7 | | V |
| | | $I_{PP}$ = 16 A } IEC 61000−4−2 Level 4 equivalent (±8 kV Contact, ±16 kV Air) | | 27.1 | | |
| Dynamic Resistance | $R_{DYN}$ | 100 ns TLP Pulse | | 0.057 | | Ω |
| Junction Capacitance | $C_J$ | $V_R$ = 0 V, f = 1 MHz | | 320 | 400 | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Non−repetitive current pulse at $T_A$ = 25°C, per IEC61000−4−5 waveform.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: $Z_0$ = 50 Ω, $t_p$ = 100 ns, $t_r$ = 1 ns, averaging window; $t_1$ = 70 ns to $t_2$ = 90 ns.

## TYPICAL CHARACTERISTICS

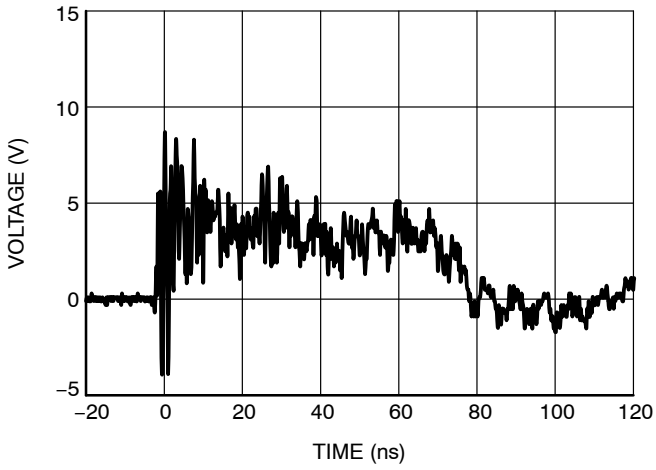



**Figure 1. ESD Clamping Voltage P1,2 to P3 – 8 kV Contact per IEC61000−4−2**

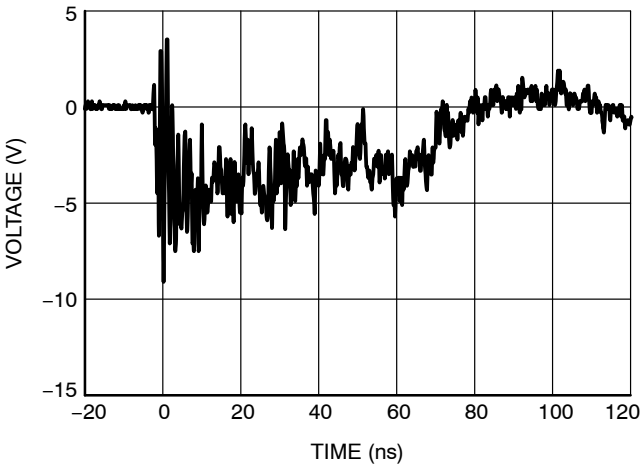



**Figure 2. ESD Clamping Voltage P3 to P1,2 – 8 kV Contact per IEC61000−4−2**

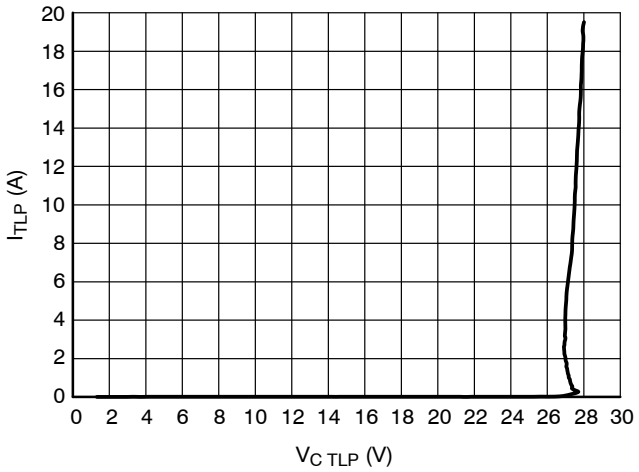



**Figure 3. 100 ns TLP I−V Curve, P1,2 to P3**

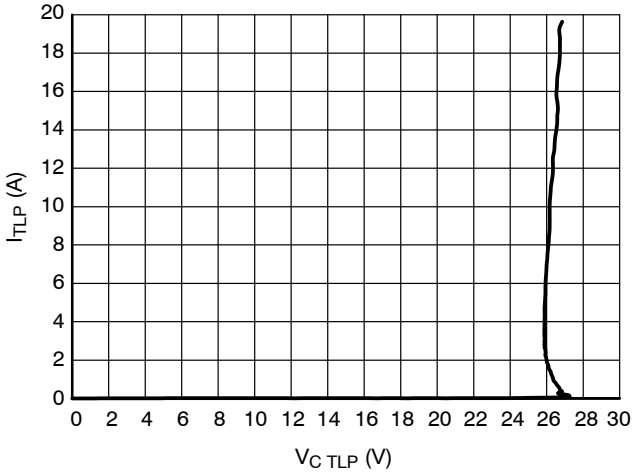



**Figure 4. 100 ns TLP I−V Curve, P3 to P1,2**

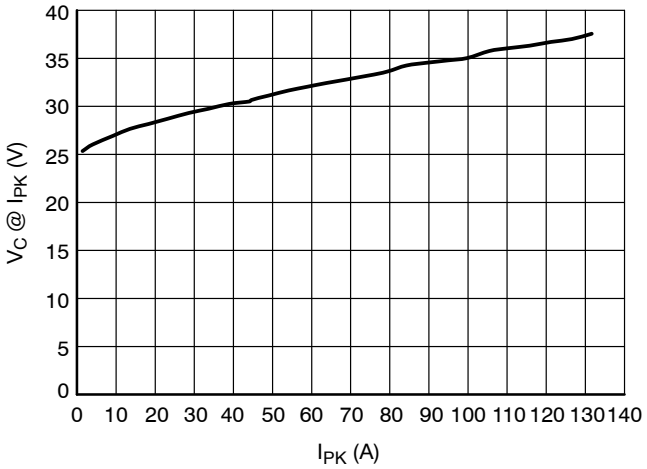



**Figure 5. Clamping Voltage vs. Peak Pulse Current ($t_p$ = 8/20 μs), P1,2 to P3**

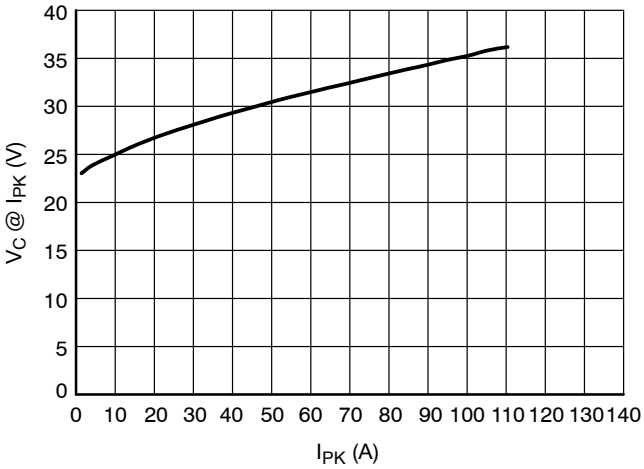



**Figure 6. Clamping Voltage vs. Peak Pulse Current ($t_p$ = 8/20 μs), P3 to P1,2**

### Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 7. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 8 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and how to interpret them please refer to AND9007/D.

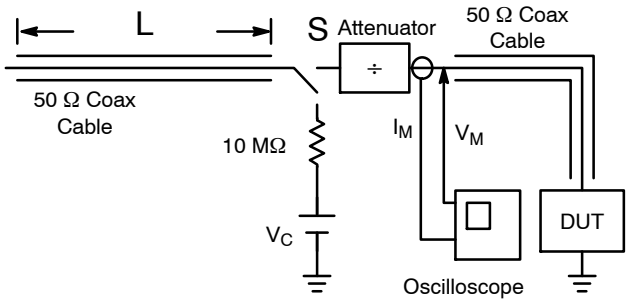



**Figure 7. Simplified Schematic of a Typical TLP System**

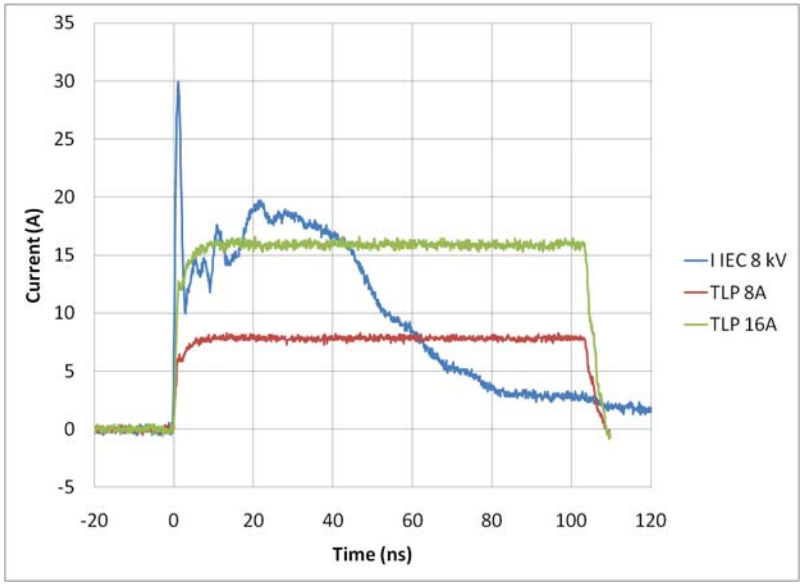



**Figure 8. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms**

**IEC 61000−4−2 Spec.**

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|---|---|---|---|---|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |

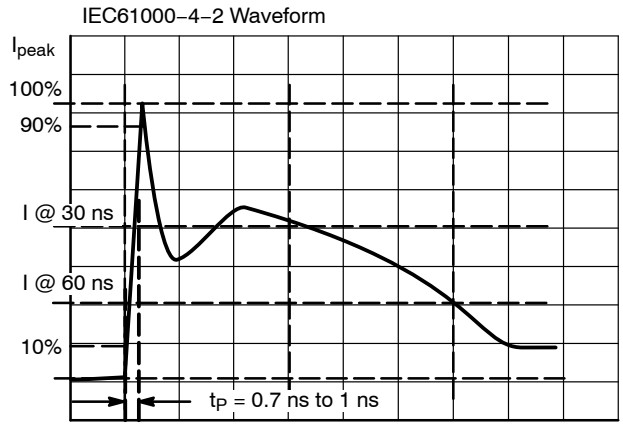



**Figure 9. IEC61000−4−2 Spec**

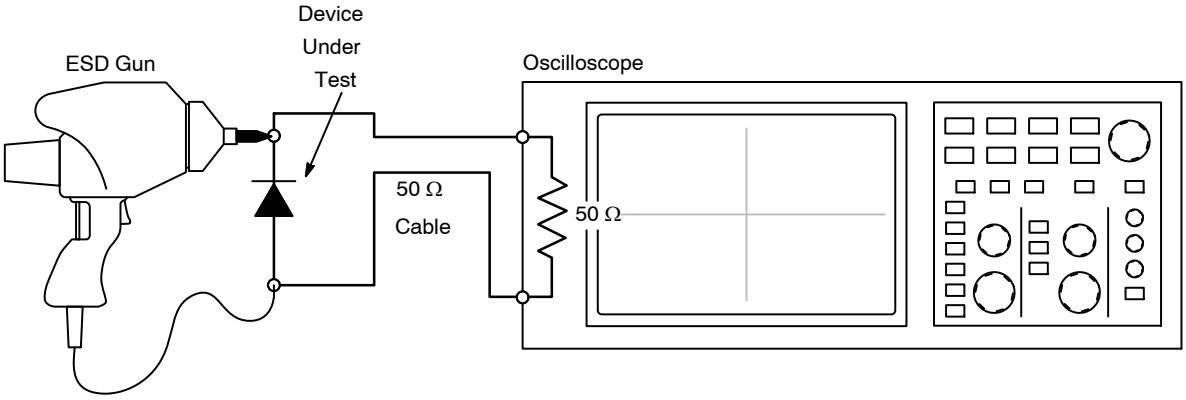



**Figure 10. Diagram of ESD Test Setup**

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

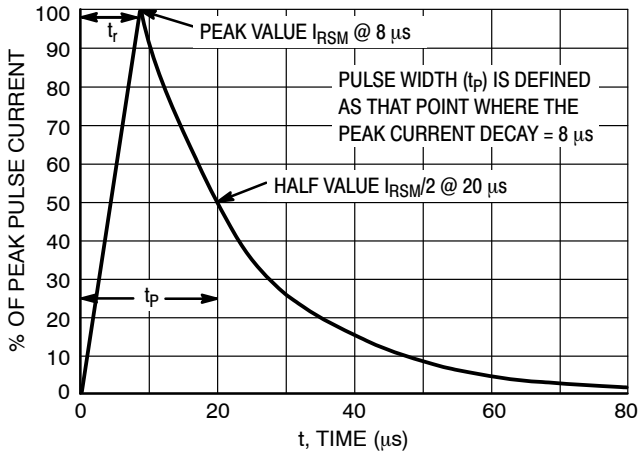
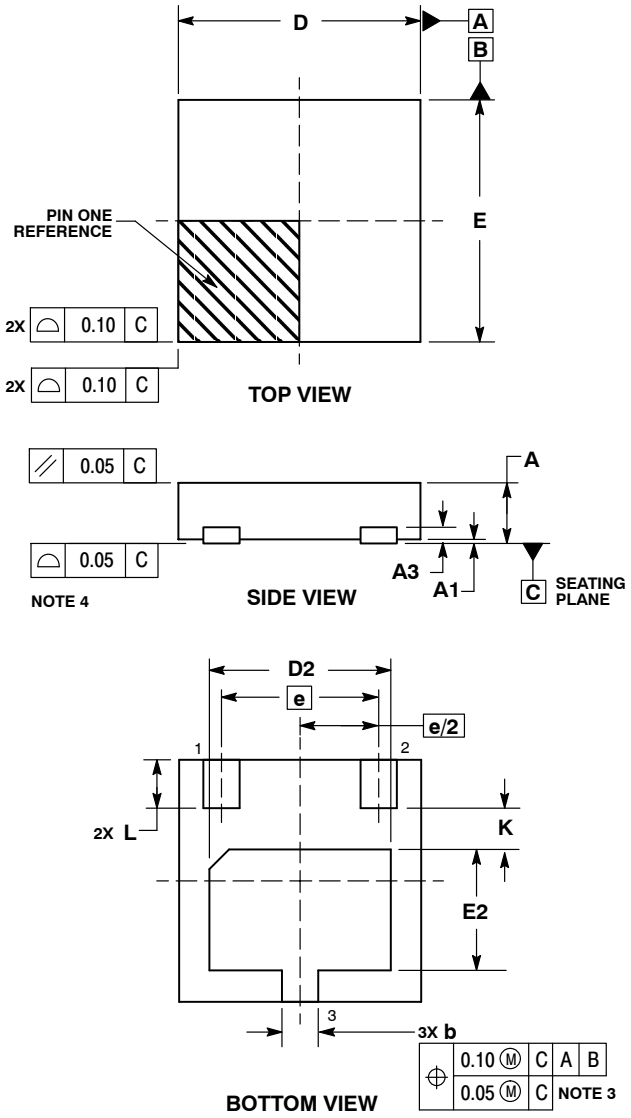



**Figure 11. 8 x 20 μs Pulse Waveform**

## PACKAGE DIMENSIONS

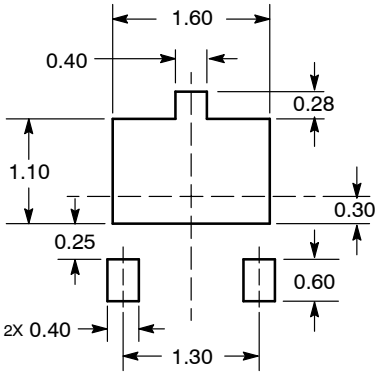
**UDFN3, 2x2, 1.3P**
CASE 517DN
ISSUE O




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.45 | 0.50 | 0.55 |
| A1 | 0.00 | --- | 0.05 |
| A3 | | 0.13 REF | |
| b | 0.25 | 0.30 | 0.35 |
| D | 1.90 | 2.00 | 2.10 |
| D2 | 1.40 | 1.50 | 1.60 |
| E | 1.90 | 2.00 | 2.10 |
| E2 | 0.90 | 1.00 | 1.10 |
| e | | 1.30 BSC | |
| K | | 0.35 REF | |
| L | 0.35 | 0.40 | 0.45 |

### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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